**Date:**  January 22nd

**From:** Hakeem Buchanan

**To:** Dr. Kaputa

**Subject:** VHDL PWM

# Introduction

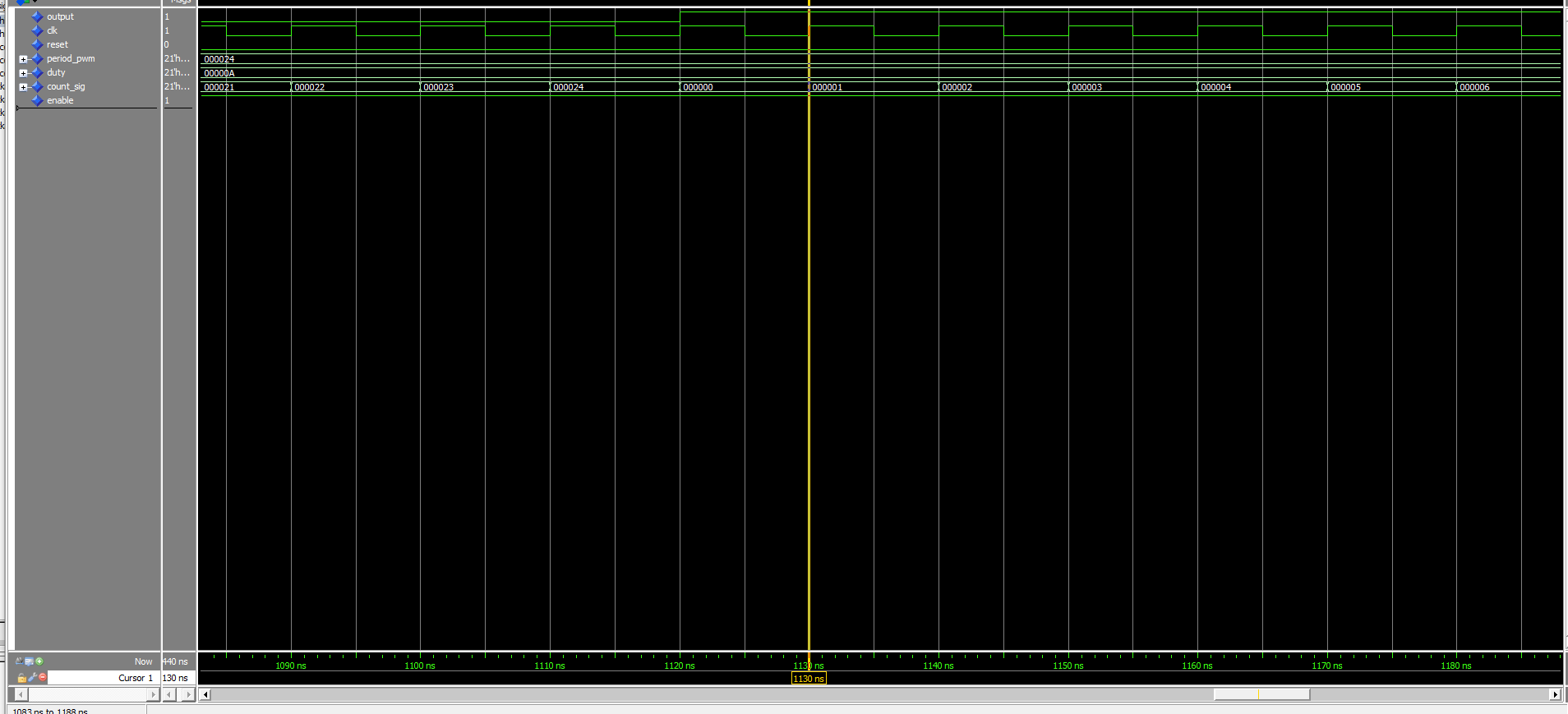
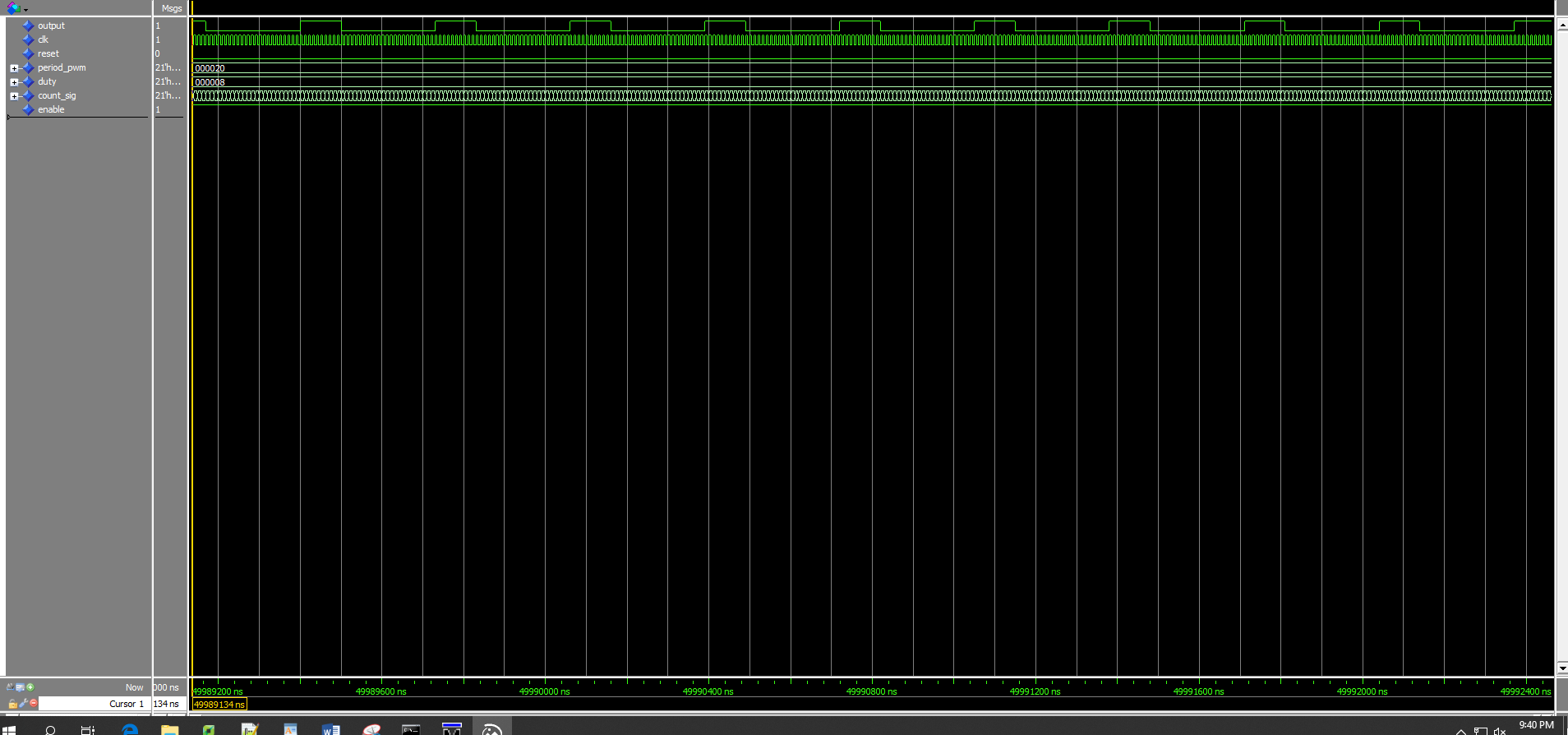
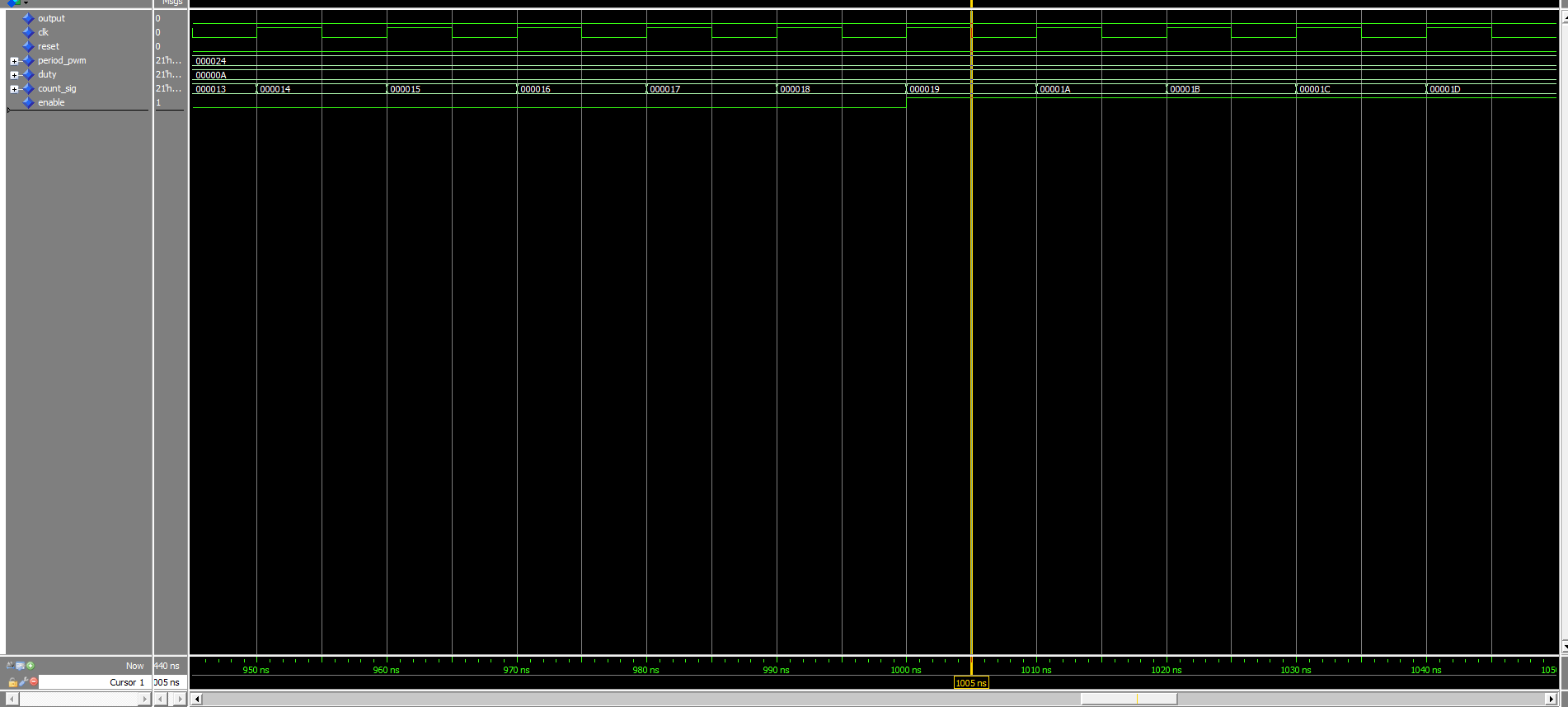
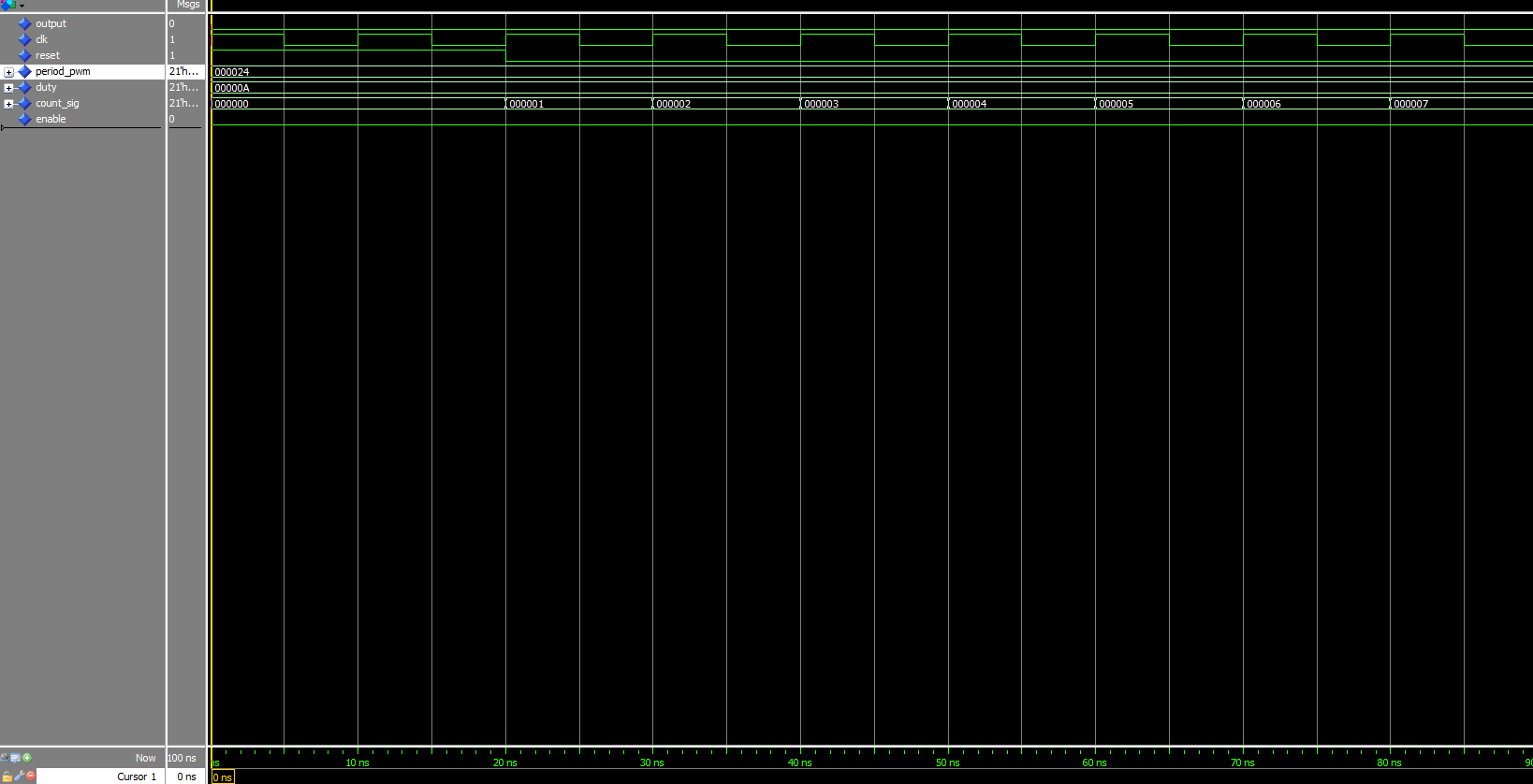
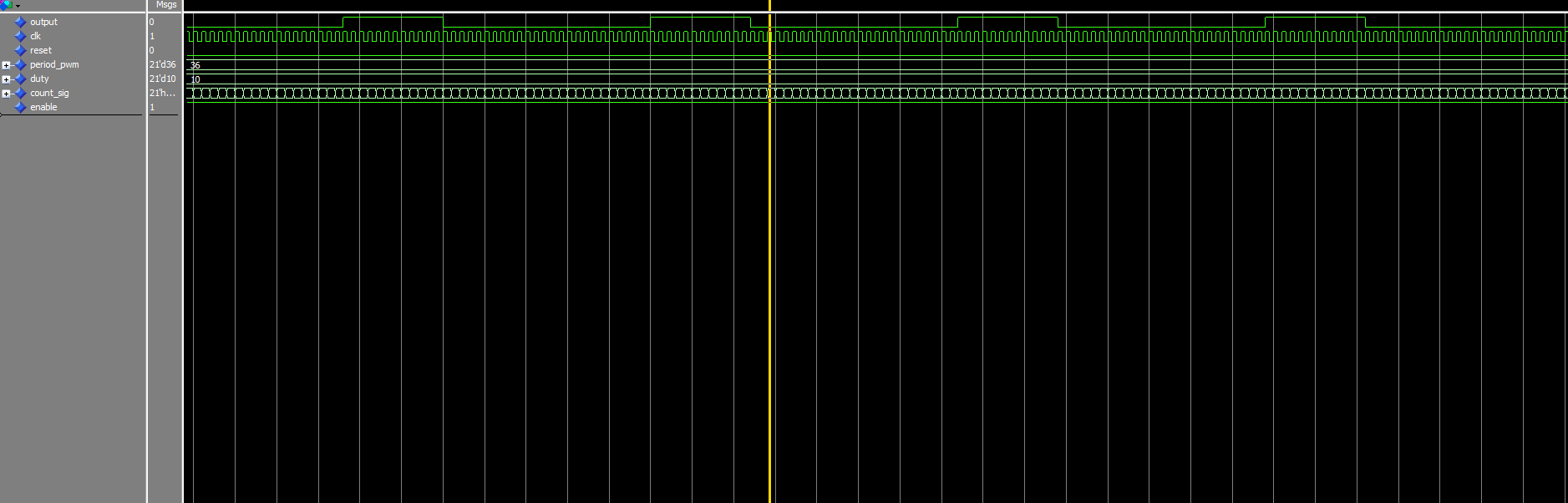
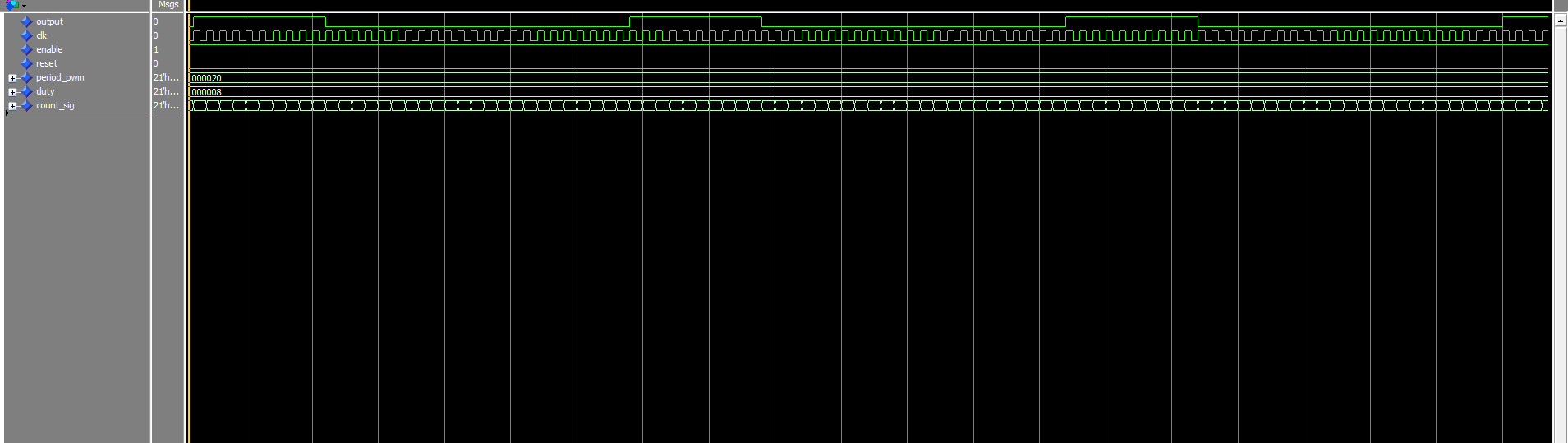
*For Lab 2 students were tasked with creating a PWM module using VHDL and Modelsim to test. Students were expected not to use generics, create an enable signal and be able to change the duty cycle and period at will. This memo serves to show the objectives have been achieved and will be useful in moving the final drone project.*

# Analysis

Using the counter provided a PWM module was created. A pulse width modulator signal has a variety of uses with control valves and pumps to DC motors and even hydraulics. The PWM module created includes an enable signal that would determine if the output would even be displayed. A PWM signal consists of two main components : a duty cycle and a frequency. The Frequency of the clock for this lab was assumed to be around 50MHz.

The system clock divided by the PWM frequency equals the number of clock pulses in one PWM period. The duty cycle determines the points during the period when the PWM’s rising and falling edges occur.

The pictures provided show varying cases of use. To test these cases, the duty cycle and period were changed to different values, the enable was shut off the and the reset value was set to 1. This shows the varying conditions for a working PWM signal and if the other parameters work as well.



# Conclusion

* *The PWM module is operational.*
* *The enable pulse does control the output.*
* *The rest value was set and did in fact reset the signals as needed.*
* *PWM’s can be useful in moving the drone project and for a large list of other uses.*