PIM Optimizer: ILP-Based Dataflow Optimization for Processing-In-Memory Architectures

Technical Documentation

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Abstract

This document provides a comprehensive technical overview of the PIM Optimizer project, an Integer Linear Programming (ILP) based framework for finding optimal dataflow mappings on Processing-In-Memory (PIM) accelerator architectures. The optimizer models complex memory hierarchies, accurate DRAM row activation costs, and supports multiple data layout strategies to minimize latency and energy consumption for deep neural network workloads.

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1 Introduction

1.1 Project Overview

The PIM Optimizer is a sophisticated optimization framework designed to find optimal dataflow mappings for convolution operations on PIM accelerators. The system uses Integer Linear Programming to solve the complex search space of possible mappings while accurately modeling:

- Multi-level memory hierarchy (PE local buffer → Global buffer → Row buffer → DRAM)
- PE array spatial parallelism with configurable dimensions
- DRAM row activation costs based on data layout and access patterns
- Data layout optimization (Sequential vs Row-Aligned)
- Input tile crossing ratio analysis using GCD-based periodic patterns

The optimizer generates complete dataflow mappings including loop bounds, loop permutation, memory bypass decisions, and data layout configurations.

1.2 Key Features

1. **Accurate Row Activation Model**: Uses the x_j variable method from the Lemon project to precisely track data reuse patterns and compute row activation counts.
2. **Input Crossing Ratio Analysis**: Based on GCD periodic analysis for accurate estimation of input tile boundary crossings across DRAM rows.
3. **Multi-Dimensional PE Array**: Supports mapping dimensions to PE array height (H), width (W), and internal parallelism for flexible dataflow patterns.
4. **Layout-Aware Optimization**: Considers both sequential and row-aligned data layouts with automatic selection based on performance.
5. **Bandwidth Constraints**: Models per-level bandwidth limits and port constraints for realistic performance estimation.

2 System Architecture

2.1 Overall Design

The PIM Optimizer follows a modular architecture with clear separation of concerns:

2.2 Module Organization

The codebase is organized into the following main modules:

- `arch/`: Architecture definition and memory hierarchy
- `workload/`: Workload specification (convolution parameters)
- `model/`: ILP model components (variables, constraints, objective)
- `analysis/`: Dataflow analysis utilities
- `generator/`: Trace generation and cost models
- `optimizer.py`: Main optimization orchestration
- `mapping.py`: Result representation and extraction

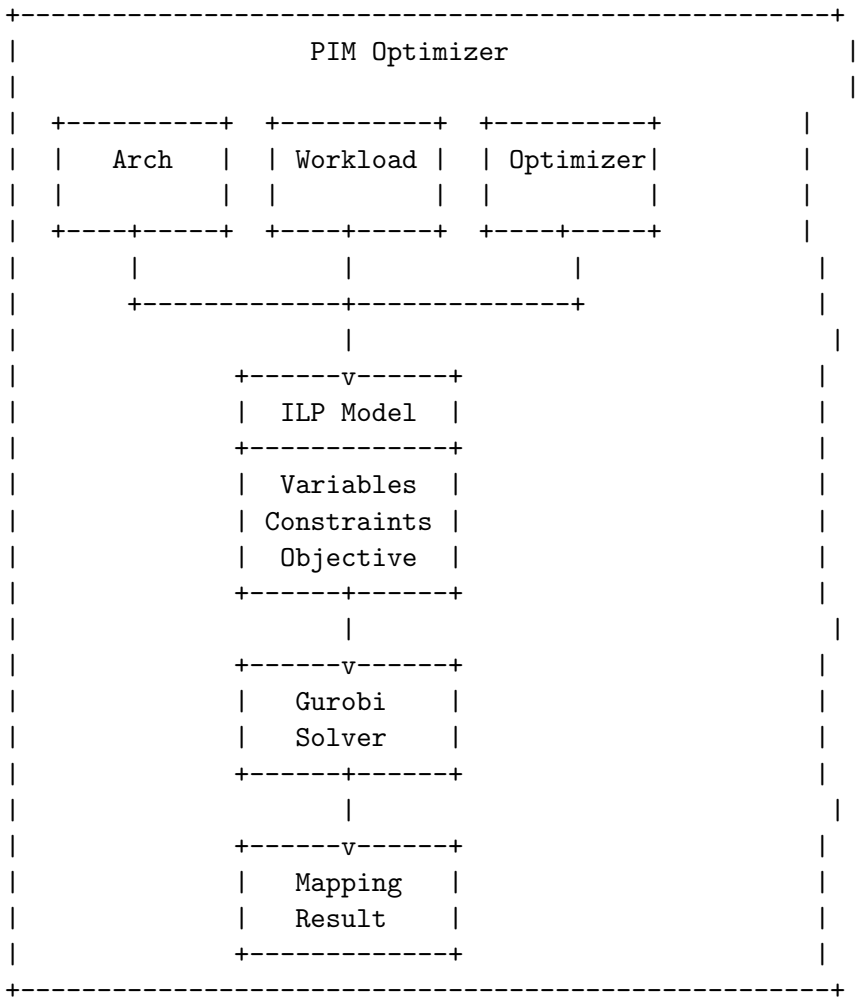

Figure 1: PIM Optimizer System Architecture

3 Architecture Definition

3.1 PIM Architecture (arch/pim_arch.py)

The `PIMArchitecture` class defines the hardware configuration of the PIM accelerator. It encapsulates:

- Memory hierarchy specification
- PE array configuration
- DRAM timing parameters
- Bandwidth and port constraints

3.1.1 Key Attributes

Listing 1: PIM Architecture Core Attributes

```
class PIMArchitecture:
    vault_count: int          # Number of DRAM vaults
    pu_count: int             # Number of processing units
    dram_timings: dict        # DRAM timing parameters
```

```
    hierarchy: MemoryHierarchy  # Memory level definitions
    pe_array: PEArray           # PE array configuration
    dram_activation_latency: float  # Row activation cost
```

3.1.2 DRAM Timing Parameters

The architecture models detailed DRAM timing parameters following JEDEC standards:

Table 1: DRAM Timing Parameters

Parameter	Description	Typical Value
RL	Read Latency	25 cycles
WL	Write Latency	20 cycles
tRCDRD	Row-to-Column delay (Read)	14 cycles
tRP	Row Precharge time	14 cycles
BL	Burst Length	8
co_w	Column data width	256 bits

3.2 Memory Hierarchy (`arch/memory.py`)

The memory hierarchy is organized from innermost to outermost:

Level 1: **PE Local Buffer**: Private to each PE, smallest capacity, lowest latency

Level 2: **Global Buffer**: Shared among PEs, larger capacity, moderate latency

Level 3: **Row Buffer**: DRAM row buffer, fast access for open rows

Level 4: **Local DRAM**: Main memory, highest capacity, highest latency

3.2.1 Memory Level Definition

Each memory level is characterized by:

Listing 2: Memory Level Specification

```
@dataclass
class MemoryLevel:
    name: str                    # Level name
    entries: int                 # Capacity (in elements)
    blocksize: int               # Block size (bytes)
    instances: int               # Number of instances
    latency: float               # Access latency (cycles)
    access_cost: float           # Energy per access (nJ)
    stores: list[bool]           # [input, weight, output]
    bypass_defined: bool         # Explicit bypass config
    num_banks: int               # Number of banks
    row_buffer_size: int         # Row buffer size (bytes)
    read_bandwidth_limit: float # Read BW (bytes/cycle)
    write_bandwidth_limit: float # Write BW (bytes/cycle)
```

3.3 PE Array (`arch/pe_array.py`)

The PE array defines the spatial compute substrate with three key dimensions:

- **Height (H)**: Number of PE rows
- **Width (W)**: Number of PE columns
- **Internal**: Parallelism within each PE (e.g., SIMD lanes, tensor core dimensions)

3.3.1 Compute Unit

Each PE contains a compute unit that can be configured as:

- **Scalar**: Single MAC per cycle
- **SIMD**: Multiple parallel MACs with reduction tree
- **Tensor Core**: 2D systolic array structure
- **Reduction Tree**: Explicit multi-stage reduction

Listing 3: Compute Unit Configuration

```python
@dataclass
class ComputeUnit:
    unit_type: str = "scalar"      # Unit architecture
    num_macs: int = 1              # Parallel MACs
    mac_energy: float = 0.56e-3    # Energy per MAC (nJ)
    reduction_latency: int = 0     # Reduction overhead
    internal_dim: int = None       # Mapped dimension
```

4 Workload Definition

4.1 Convolution Workload (`workload/conv.py`)

The convolution workload is characterized by 7 dimensions following the standard CNN conv2d operation:

$$\begin{aligned}\text{Output}[n,k,p,q] = \sum_{c=0}^{C-1}\sum_{r=0}^{R-1}\sum_{s=0}^{S-1} \text{Input}[n, c, p\cdot\text{stride}_w + r\cdot\text{dilation}_w,\\ q\cdot\text{stride}_h + s\cdot\text{dilation}_h]\times\\ \text{Weight}[k,c,r,s]\end{aligned}$$

4.1.1 Dimension Definitions

4.1.2 Dimension-Datatype Relevancy Matrix

The relevancy matrix $O[j][t]$ indicates which dimensions affect each datatype:

$$O = \begin{bmatrix}1 & 1 & 0\\ 1 & 1 & 0\\ 1 & 0 & 1\\ 1 & 0 & 1\\ 1 & 1 & 0\\ 0 & 1 & 1\\ 1 & 0 & 1\end{bmatrix} \quad \begin{array}{l}\text{Columns: } [t_{\text{Input}}, t_{\text{Weight}}, t_{\text{Output}}]\\ \text{Rows: } [R, S, P, Q, C, K, N]\end{array} \tag{1}$$

Table 2: Convolution Dimensions

Index	Name	Description	Type
0	R	Kernel width	Parallel
1	S	Kernel height	Parallel
2	P	Output width	Parallel
3	Q	Output height	Parallel
4	C	Input channels	Reduction
5	K	Output channels (filters)	Reduction
6	N	Batch size	Parallel

where $O[j][t] = 1$ means dimension j is relevant to datatype t.

4.1.3 Input Size Calculation

The input tensor dimensions are derived from output size and convolution parameters:

$$W_{\text{in}} = \text{stride}_w \cdot (P - 1) + \text{dilation}_w \cdot (R - 1) + 1 \tag{2}$$

$$H_{\text{in}} = \text{stride}_h \cdot (Q - 1) + \text{dilation}_h \cdot (S - 1) + 1 \tag{3}$$

5 ILP Model Formulation

5.1 Overview

The ILP model searches for the optimal dataflow mapping by selecting:

1. Loop bounds for each dimension at each memory level
2. Spatial mapping to PE array (H, W, Internal dimensions)
3. Temporal loop permutation (ordering)
4. Memory bypass decisions for each datatype
5. Data layout mode (sequential vs row-aligned)

5.2 Decision Variables (`model/variables.py`)

5.2.1 Loop Bound Variables (x_b)

The primary decision variables are binary indicators for loop bound selection:

$$x_b[w, m, s, j, i] \in \{0, 1\} \tag{4}$$

where:

- w: workload index
- m: memory level (0 = PE, 1 = GlobalBuffer, 2 = RowBuffer, 3 = DRAM)
- s: spatial direction
  - For $m = 0$ (PE layer): $s \in \{H, W, \text{Internal}, \text{Temporal}\}$
  - For $m > 0$: $s \in \{\text{spatial}, \text{temporal}\}$ (spatial must be 1)
- j: dimension index (0-6 for R, S, P, Q, C, K, N)
- i: divisor index (selecting from precomputed divisors)

5.2.2 Spatial Direction Encoding

For the PE layer ($m = 0$), the spatial dimension index s encodes:

Listing 4: Spatial Dimension Constants

```
class SpatialDim:
    H = 0           # PE array Height direction
    W = 1           # PE array Width direction
    INTERNAL = 2    # PE internal parallelism
    TEMPORAL = 3    # Temporal (sequential) execution
```

This allows each dimension to be mapped to:

- H direction: Parallelism across PE rows
- W direction: Parallelism across PE columns
- Internal: SIMD/tensor core parallelism within each PE
- Temporal: Sequential execution over time

5.2.3 Permutation Variables (x_p)

Loop permutation (ordering) is encoded as:

$$x_p[w, m, p, j] \in \{0, 1\} \tag{5}$$

where $x_p[w, m, p, j] = 1$ means dimension j is at permutation level p (inner to outer).

5.2.4 Bypass Variables (x_d)

Memory bypass decisions:

$$x_d[w, m, t] \in \{0, 1\} \tag{6}$$

where $x_d[w, m, t] = 1$ means datatype t is stored at memory level m.

5.2.5 Layout Variables

Data layout mode selection:

$$x_{\text{layout}}[w, t, \text{mode}] \in \{0, 1\} \tag{7}$$

where mode $\in \{\text{sequential}, \text{row\_aligned}\}$.

5.2.6 Row Buffer Block Variables

For row-aligned layout, input block size selection:

$$x_{\text{block\_h}}[w, i] \in \{0, 1\} \tag{8}$$

$$x_{\text{block\_w}}[w, i] \in \{0, 1\} \tag{9}$$

5.3 Constraints (`model/constraints.py`)

5.3.1 Dimension Factorization

Each problem dimension must be fully factorized across all loop levels:

$$\prod_{m=0}^{M-1} \prod_{s \in S(m)} \prod_{i=0}^{|D_j|-1} \text{divisor}[j][i]^{x_b[w,m,s,j,i]} = \text{bound}[j] \tag{10}$$

where $S(m)$ is the set of spatial directions at level m.
In log form for linear constraints:

$$\sum_{m=0}^{M-1} \sum_{s \in S(m)} \sum_{i=0}^{|D_j|-1} x_b[w,m,s,j,i] \cdot \log(\text{divisor}[j][i]) = \log(\text{bound}[j]) \tag{11}$$

5.3.2 One Factor Per Loop

Each loop must select exactly one divisor:

$$\forall w,m,s,j: \quad \sum_{i=0}^{|D_j|-1} x_b[w,m,s,j,i] = 1 \tag{12}$$

5.3.3 Spatial Exclusivity for PE Layer

At the PE layer ($m = 0$), each dimension can be spatially mapped to at most one direction (H, W, or Internal):

$$\forall j: \quad \sum_{s \in \{H,W,\text{Internal}\}} (1 - x_b[w,0,s,j,i_1]) \leq 1 \tag{13}$$

where i_1 is the index of divisor 1 (no spatial parallelism).

5.3.4 No Spatial Above PE

For levels above PE ($m > 0$), spatial direction must always select factor 1:

$$\forall m > 0, j: \quad x_b[w,m,0,j,i_1] = 1 \tag{14}$$

5.3.5 Permutation Constraints

Each non-trivial temporal loop appears at exactly one permutation level:

$$\forall m,j: \quad \sum_{p=0}^{|J|-1} x_p[w,m,p,j] = 1 - x_b[w,m,s_t,j,i_1] \tag{15}$$

where s_t is the temporal index at level m.
At most one dimension per permutation level:

$$\forall m,p: \quad \sum_{j=0}^{|J|-1} x_p[w,m,p,j] \leq 1 \tag{16}$$

5.3.6 Buffer Capacity Constraints

Total buffer utilization must not exceed capacity:

$$\forall m: \quad \sum_{t=0}^{2} x_d[w,m,t] \cdot \text{tile\_bytes}[w,m,t] \leq \text{capacity}[m] \tag{17}$$

5.3.7 PE Array Constraints

Spatial bounds must fit PE array dimensions:

$$\prod_j \prod_i \text{divisor}[j][i]^{x_b[w,0,H,j,i]} \leq \text{pe\_array.height} \tag{18}$$

$$\prod_j \prod_i \text{divisor}[j][i]^{x_b[w,0,W,j,i]} \leq \text{pe\_array.width} \tag{19}$$

$$\prod_j \prod_i \text{divisor}[j][i]^{x_b[w,0,\text{Internal},j,i]} \leq \text{pe\_array.internal\_parallel} \tag{20}$$

5.3.8 Layout Selection

Each datatype selects exactly one layout mode:

$$\forall w,t: \quad x_{\text{layout}}[w,t,\text{sequential}] + x_{\text{layout}}[w,t,\text{row\_aligned}] = 1 \tag{21}$$

5.4 Expressions (`model/expressions.py`)

5.4.1 Tile Size Calculation

The tile size for datatype t at memory level m is the product of all loop bounds from level 0 to m:

$$\text{tile}[w,m,t] = \prod_{m'=0}^{m} \prod_{s \in S(m')} \prod_{j:O[j][t]=1} \prod_i \text{divisor}[j][i]^{x_b[w,m',s,j,i]} \tag{22}$$

where $O[j][t]$ is the relevancy matrix.

5.4.2 Memory Reads Per Invocation

Memory reads at level m for datatype t:

$$\text{reads}[w,m,t] = x_d[w,m,t] \cdot \text{tile\_bytes}[w,m+1,t] \cdot \frac{\text{tile\_entries}[w,m+1,\text{all}]}{\text{tile\_entries}[w,m,t]} \tag{23}$$

This captures:

- Data is only read if stored at this level ($x_d[w,m,t] = 1$)
- Amount read is determined by next level's tile size
- Reuse factor reduces read frequency

5.5 Row Activation Model (`model/row_activation.py`)

5.5.1 Overview

The row activation model captures the cost of DRAM row buffer management. The model implements a **Hybrid Cost Model** that selects between "Streaming" (Sequential) and "Tiling" (Row-Aligned) behaviors based on the data layout and access pattern.

5.5.2 Sequential Mode (Streaming vs. Thrashing)

This mode models the memory access as a sequential stream. It is efficient when the data can be packed into the row buffer and accessed contiguously.

1. Streaming Cost (Base): The theoretical minimum activations required to read the entire tensor once, assuming perfect packing:

$$C_{\text{stream}} = \max\left(1, \frac{\text{TensorBytes}}{\text{RowBufferBytes}}\right) \tag{24}$$

2. Thrashing Penalty: If the access pattern causes thrashing (e.g., large tiles or unaligned small tiles with inner loop reuse), the streaming cost is multiplied by the reuse factor. The reuse penalty is composed of two parts: reuse at the DRAM level (L3) and reuse at the Row Buffer level (L2).

$$\text{ReusePenalty} = \text{Reuse}_{\text{DRAM}} \times \text{Reuse}_{\text{RowBuffer}} \tag{25}$$

where:

- $\text{Reuse}_{\text{DRAM}}$: Product of loop bounds for dimensions irrelevant to the datatype that are inside the DRAM level (L3) but outside the Row Buffer level (L2).
- $\text{Reuse}_{\text{RowBuffer}}$: Product of loop bounds for dimensions irrelevant to the datatype that are inside the Row Buffer level (L2).

$$C_{\text{seq\_base}} = \begin{cases} C_{\text{stream}} & \text{if Small Block \& Aligned} \\ C_{\text{stream}} \times \text{ReusePenalty} & \text{otherwise (Thrashing)} \end{cases} \tag{26}$$

3. Total Sequential Cost:

$$\text{row\_acts}_{\text{seq}} = C_{\text{seq\_base}} \times \text{OuterPenalty} \tag{27}$$

where OuterPenalty accounts for repetitions due to outer irrelevant loops.

5.5.3 Row-Aligned Mode (Tiling)

This mode models the memory access as discrete tiles aligned to DRAM rows. It assumes that inner loops fit within the row buffer (free reuse), but pays for the number of tiles.

1. Tile Count Cost: The cost is proportional to the number of tiles (product of relevant dimensions):

$$C_{\text{aligned\_base}} = \prod_{j \in \text{Relevant}} \text{dim}_j \tag{28}$$

2. Total Aligned Cost:

$$\text{row\_acts}_{\text{aligned}} = C_{\text{aligned\_base}} \times \text{OuterPenalty} \tag{29}$$

5.5.4 Input Block Crossing (Additive Penalty)

For Input tensors (Convolution), an additional penalty is added to **both modes** to account for the sliding window crossing layout block boundaries.

$$\text{BlockCrossing} = 2 \times \text{CrossingCount} \times \text{ReusePenalty} \tag{30}$$

The CrossingCount is calculated using the GCD-based method described in previous sections:

$$\text{CrossingCount} \approx \text{NumTiles} \times \left(1 - \frac{\text{SafePositions}}{\text{Period}}\right) \tag{31}$$

5.5.5 Total Row Activations

The final cost combines the selected mode and the additive input penalty:

$$\text{row\_acts} = ((1 - x_{\text{aligned}}) \cdot \text{row\_acts}_{\text{seq}} + x_{\text{aligned}} \cdot \text{row\_acts}_{\text{aligned}}) + \text{BlockCrossing} \tag{32}$$

Summary of Logic

- **Sequential**: Optimizes for bandwidth utilization (C_{stream}). Sensitive to alignment and reuse thrashing.
- **Row-Aligned**: Optimizes for access stability (C_{aligned}). Immune to inner loop thrashing but may have lower density.
- **Input Penalty**: The sliding window cost (BlockCrossing) is intrinsic to the convolution operation and applies to both modes.

Total DRAM latency:

$$\text{dram\_latency} = \max_t \left(\frac{\text{dram\_reads}[t]}{\text{dram\_bandwidth}} + \text{row\_acts}[t] \cdot \text{activation\_latency}\right) \tag{33}$$

5.6 Objective Function (`model/objective.py`)

5.6.1 Compute Cycles

Compute cycles are determined by the PE array parallelism:

$$\text{compute\_cycles} = \frac{\text{total\_MACs}}{\text{spatial\_parallelism}} \tag{34}$$

where:

$$\text{spatial\_parallelism} = \prod_j \prod_i \text{divisor}[j][i]^{x_b[w,0,H,j,i]} \times \tag{35}$$

$$\prod_j \prod_i \text{divisor}[j][i]^{x_b[w,0,W,j,i]} \times \tag{36}$$

$$\prod_j \prod_i \text{divisor}[j][i]^{x_b[w,0,\text{Internal},j,i]} \tag{37}$$

5.6.2 Memory Latency

Memory latency for each level:

$$\text{mem\_latency}[m] = \max_t \left(\frac{\text{mem\_reads}[m,t]}{\text{bandwidth}[m]} \right) \tag{38}$$

For DRAM, includes row activation overhead:

$$\text{dram\_latency} = \max_t \left(\frac{\text{dram\_reads}[t]}{\text{dram\_bandwidth}} + \text{row\_activation\_cycles}[t] \right) \tag{39}$$

5.6.3 Total Latency

Total execution latency:

$$\text{latency\_total} = \max \left(\text{compute\_cycles}, \max_m \text{mem\_latency}[m] \right) \tag{40}$$

The max operation models overlapping of compute and memory access (compute-bound vs memory-bound).

5.6.4 Energy

Total energy consumption:

$$\begin{aligned} \text{energy\_total} &= \text{compute\_energy} + \text{memory\_energy} && (41)\\ &= \text{total\_MACs} \cdot \text{mac\_energy} + && (42)\\ &\quad \sum_m \sum_t \text{mem\_reads}[m,t] \cdot \text{access\_cost}[m] && (43) \end{aligned}$$

5.6.5 Objective

The optimization objective can be configured as:

- **Latency**: min latency_total
- **Energy**: min energy_total
- **Blended**: min $(\alpha \cdot \text{latency\_total} + \beta \cdot \text{energy\_total})$

6 Optimization Process

6.1 Optimizer Workflow (`optimizer.py`)

The optimization process follows these steps:

6.2 Complexity and Scaling

6.2.1 Variable Count

Number of binary variables in the ILP model:

$$\begin{aligned} |x_b| &\approx W \cdot M \cdot S \cdot J \cdot \bar{D} && (44)\\ |x_p| &\approx W \cdot M \cdot J^2 && (45)\\ |x_d| &\approx W \cdot M \cdot T && (46) \end{aligned}$$

Algorithm 1 PIM Dataflow Optimization

Input: Architecture A, Workload(s) W
Output: Optimal Mapping M^*

// Step 1: Model Creation
Create Gurobi ILP model

// Step 2: Variable Creation
Create loop bound variables $x_b[w, m, s, j, i]$
Create permutation variables $x_p[w, m, p, j]$
Create bypass variables $x_d[w, m, t]$
Create layout variables $x_{\text{layout}}[w, t, \text{mode}]$
Create auxiliary variables (x_r, x_j, tile sizes, etc.)

// Step 3: Constraint Addition
Add dimension factorization constraints
Add spatial-temporal constraints
Add buffer capacity constraints
Add PE array constraints
Add reuse tracking constraints (x_r, x_j)
Add row activation model constraints

// Step 4: Expression Building
Build tile size expressions
Build memory read expressions
Build row activation expressions
Build compute cycle expressions

// Step 5: Objective Setting
Set objective function (latency, energy, or blended)

// Step 6: Solve
$M^* \leftarrow$ Solve ILP model

// Step 7: Result Extraction
Extract loop bounds, permutation, bypass, layout
Compute performance metrics
return M^*

where:

- W: number of workloads
- $M = 4$: memory levels
- $S = 4$: spatial directions (PE layer)
- $J = 7$: dimensions
- $\bar{D} \approx 10$: average divisors per dimension
- $T = 3$: datatypes

Typical model size: ∼3000-5000 binary variables.

6.2.2 Constraint Count

Number of constraints:

- Dimension factorization: $W \cdot J \approx 7W$
- One factor per loop: $W \cdot M \cdot S \cdot J \approx 100W$
- Permutation: $W \cdot M \cdot J \cdot 2 \approx 60W$
- Buffer capacity: $W \cdot M \approx 4W$
- Row activation: ∼100-500 constraints depending on configuration

Total: ∼500-2000 constraints for single workload.

6.2.3 Solver Performance

Using Gurobi optimizer:

- Simple workloads: 1-30 seconds
- Complex workloads with row activation: 30-300 seconds
- Multi-workload optimization: 5-30 minutes

6.3 Numerical Stability

6.3.1 Log-Space Factorization

Loop bound factorization uses logarithms to convert products to sums:

$$\log\left(\prod_{m,s,i} d_i^{x_b[m,s,j,i]}\right) = \sum_{m,s,i} x_b[m,s,j,i] \cdot \log(d_i) \tag{47}$$

This avoids overflow and improves numerical stability.

6.3.2 Scaling Factors

Large MAC counts are scaled to keep variable ranges manageable:

$$\text{macs\_scaled} = \text{macs}/\text{scale\_factor} \tag{48}$$

where scale_factor is chosen such that macs_scaled $< 10^4$.

6.3.3 Piecewise Linear Approximations

Nonlinear expressions (products, divisions) are linearized using:

- General constraints (Gurobi's `addGenConstr`)
- Piecewise linear approximations with configurable error bounds
- PWL options: `FuncPieces=-2, FuncPieceError=0.002`

7 Dataflow Analysis

7.1 Dataflow Patterns (`analysis/dataflow.py`)

The optimizer can identify and analyze classic dataflow patterns:

7.1.1 Weight Stationary

Weights stay in PE local buffers, outputs accumulate locally:

- K dimension mapped spatially (H or W)
- P, Q, N dimensions mapped spatially or temporally
- Minimizes weight movement

7.1.2 Output Stationary

Output activations stay in PE local buffers:

- P, Q, N dimensions mapped spatially
- R, S, C dimensions temporal (reduction)
- Minimizes output movement, high local accumulation

7.1.3 Input Stationary

Input activations shared across filters:

- C dimension spatial (one direction)
- K dimension spatial (other direction)
- High input reuse across K dimension

7.1.4 Row Stationary

Mixed strategy with row-wise reuse:

- Kernel dimensions (R, S) in one direction
- Output channels (K) in other direction
- Balances reuse across all datatypes

7.2 Multi-Dimensional Mapping

The optimizer supports mapping multiple dimensions to the same spatial direction:

$$\text{spatial\_H} = \prod_{j \in \mathcal{J}_H} \text{factor}_H[j] \tag{49}$$

where $\mathcal{J}_H$ is the set of dimensions mapped to H direction.
This enables:

- Complex dataflow patterns (e.g., K × C in H, P × Q in W)
- Split dimensions across multiple directions
- Fine-grained control over parallelism distribution

8 Trace Generation and Cost Models

8.1 Hybrid Cost Model (`generator/hybrid_cost_model.py`)

The hybrid cost model simulates memory access patterns for a single tile to determine row activation cost. It captures the interaction between:

- Loop order (C, H, W)
- Data layout (linear, tiled, row_aligned)
- Tile dimensions (tile_h, tile_w, tile_c)
- DRAM row buffer size

8.1.1 Address Calculation

For different layouts:
Linear (CHW):

$$\text{addr}(c, h, w) = (c \cdot H \cdot W + h \cdot W + w) \cdot \text{element\_size} \tag{50}$$

Linear (HWC):

$$\text{addr}(c, h, w) = (h \cdot W \cdot C + w \cdot C + c) \cdot \text{element\_size} \tag{51}$$

Row-Aligned:

$$\text{blk\_h} = h/\text{block\_h}, \quad \text{blk\_w} = w/\text{block\_w} \tag{52}$$

$$\text{c\_base} = c \cdot \text{stride\_c} \tag{53}$$

$$\text{blk\_base} = (\text{blk\_h} \cdot \text{num\_blk\_w} + \text{blk\_w}) \cdot \text{block\_size} \tag{54}$$

$$\text{in\_blk} = (h \bmod \text{block\_h}) \cdot \text{block\_w} + (w \bmod \text{block\_w}) \tag{55}$$

$$\text{addr}(c, h, w) = \text{c\_base} + \text{blk\_base} + \text{in\_blk} \cdot \text{element\_size} \tag{56}$$

where stride_c is aligned to row buffer boundaries.

8.1.2 Trace Simulation

The trace generator simulates memory accesses following the loop order:

Algorithm 2 Memory Access Trace Simulation

Input: tile config, loop_order, layout
Output: Row activation count

row_buffer_state $\leftarrow \emptyset$
activations $\leftarrow 0$

for each dimension in loop_order (outer to inner) **do**
    for each element in dimension range **do**
        $(c, h, w) \leftarrow$ current coordinates
        addr $\leftarrow$ compute address using layout
        row $\leftarrow$ addr/row_buffer_size
        if row $\neq$ row_buffer_state **then**
            activations $\leftarrow$ activations $+ 1$
            row_buffer_state $\leftarrow$ row
        end if
    end for
end for
return activations

8.2 Precomputation Tables

To avoid costly simulation during ILP solving, row activation counts are precomputed for all possible configurations:

$$\text{crossing\_table}[i_{\text{block}}, j_{\text{spatial}}, k_{\text{kernel}}] = \text{activation\_count} \tag{57}$$

This table is indexed by:

- Block size options (divisors of input size)
- Spatial tiling factors (P or Q divisors)
- Kernel tiling factors (R or S divisors)

The ILP model then selects appropriate table entries based on variable values.

9 Result Representation

9.1 Mapping Class (`mapping.py`)

The `Mapping` class encapsulates the complete optimization result:

Listing 5: Mapping Result Structure

```
@dataclass
class Mapping:
    loop_bounds: dict        # [m][spatial/temporal][j] = bound
    permutation: dict        # [m][p] = j
    bypass: dict            # [m][t] = stored?
    layout: dict            # [t] = mode
    metrics: dict           # Performance metrics
    tile_info: dict         # Debug information
    solver_info: dict       # Solver statistics
```

9.2 Performance Metrics

Key metrics extracted from the solution:

- **Latency**: Total execution time (cycles)
- **Energy**: Total energy consumption (nJ)
- **Compute Cycles**: PE array execution time
- **Memory Cycles**: Per-level memory access time
- **Row Activations**: DRAM row buffer activations (per datatype)
- **Buffer Utilization**: Per-level capacity usage
- **Bandwidth Utilization**: Actual vs. peak bandwidth
- **PE Utilization**: Active PEs / total PEs

9.3 Mapping Visualization

The mapping can be visualized as a nested loop structure:

```
PE Layer (m=0):
  H:        K=4
  W:        P=14, Q=4
  Internal: (none)
  Temporal: C=8, R=3, S=3, K=16, P=4, N=1

GlobalBuffer (m=1):
  Temporal: C=8, K=4, P=1, Q=1

RowBuffer (m=2):
  Temporal: (none)

LocalDRAM (m=3):
  Temporal: (all remaining)
```

10 Key Innovations

10.1 Multi-Dimensional PE Array Mapping

Unlike traditional approaches that use a single spatial dimension, this optimizer supports:

1. **Separate H and W Mapping**: Different dimensions can be independently mapped to PE array height and width.
2. **Internal Parallelism**: Third spatial dimension for SIMD/tensor core units.
3. **Dimension Exclusivity**: Each dimension maps to at most one spatial direction, preventing ambiguity.
4. **Flexible Dataflow**: Enables weight stationary, output stationary, and mixed patterns.

10.2 GCD-Based Crossing Analysis

The input tile crossing analysis uses GCD theory to accurately predict boundary crossings:

$$g = \gcd(\text{step}, \text{block\_h}) \tag{58}$$

Key insight: The crossing pattern repeats with period g, allowing efficient exact computation rather than Monte Carlo estimation.

10.3 Layout-Aware Optimization

The optimizer jointly optimizes:

- Tiling factors (which determine tile size)
- Block size for row-aligned layout
- Layout mode selection (sequential vs row-aligned)

This co-optimization is critical because:

- Small tiles favor sequential layout (simpler addressing)
- Large tiles favor row-aligned layout (reduced crossing)
- Optimal choice depends on workload and architecture

10.4 x_j Reuse Tracking

Following the Lemon framework, the optimizer uses x_j variables to precisely track whether each dimension is innermost at each level:

$$x_j[w, m, t, j] = \begin{cases} 1 & \text{if dimension } j \text{ is inner for datatype } t \text{ at level } m \\ 0 & \text{otherwise} \end{cases} \tag{59}$$

This enables accurate modeling of:

- Data reuse across loop iterations
- Temporal locality at each memory level
- Buffer write frequency

11 Example Usage

11.1 Basic Optimization

Listing 6: Basic Usage Example

```
from pim_optimizer import PIMArchitecture, ConvWorkload, PIMOptimizer

# Define architecture
arch = PIMArchitecture()

# Define workload
workload = ConvWorkload(
    name="ResNet_Layer2",
    R=3, S=3,
    P=56, Q=56,
```

```
    C=64, K=128,
    N=1,
    stride=(1, 1),
)

# Create optimizer
optimizer = PIMOptimizer(
    arch=arch,
    verbose=True,
    time_limit=300.0,
)

# Run optimization
result = optimizer.optimize(
    workloads=[workload],
    objective="latency",
    enable_row_activation=True,
)

# Print results
mapping = result.mappings[0]
print(f"Latency: {mapping.latency:.2f} cycles")
print(f"Energy: {mapping.energy:.2f} nJ")
print(f"Row Activations: {mapping.row_activations:.0f}")
```

11.2 Multi-Workload Optimization

Listing 7: Multi-Workload Example

```
# Define multiple workloads
workloads = [
    ConvWorkload(name="L1", R=7, S=7, P=112, Q=112, C=3, K=64, N=1),
    ConvWorkload(name="L2", R=3, S=3, P=56, Q=56, C=64, K=128, N=1),
    ConvWorkload(name="L3", R=1, S=1, P=56, Q=56, C=128, K=128, N=1),
]

# Optimize with fixed bypass (same for all workloads)
result = optimizer.optimize(
    workloads=workloads,
    objective="latency",
    fix_bypass=True,
    enable_row_activation=True,
)

# Analyze results
for i, mapping in enumerate(result.mappings):
    print(f"\n{workloads[i].name}:")
    print(f"  Latency: {mapping.latency:.2f}")
    print(f"  Layout: {mapping.layout}")
```

11.3 Custom Architecture

Listing 8: Custom Architecture Example

```
from pim_optimizer.arch import PEArray, PhyDim2, ComputeUnit
from pim_optimizer.arch import MemoryHierarchy, MemoryLevel
```

```
3
4  # Define custom PE array with tensor core
5  pe_array = PEArray(
6      array_shape=PhyDim2(h=16, w=16),
7      compute_unit=ComputeUnit(
8          unit_type="tensor_core",
9          num_macs=8,
10         mac_energy=0.56e-3,
11     )
12 )
13
14 # Define custom memory hierarchy
15 hierarchy = MemoryHierarchy()
16 hierarchy.add_level(MemoryLevel(
17     name="PELocalBuffer",
18     entries=512,
19     blocksize=1,
20     instances=256,  # 16x16 PEs
21     latency=1.0,
22     access_cost=0.001,
23 ))
24 hierarchy.add_level(MemoryLevel(
25     name="GlobalBuffer",
26     entries=65536,
27     blocksize=64,
28     instances=1,
29     latency=5.0,
30     access_cost=0.02,
31 ))
32 # ... add more levels
33
34 # Create architecture
35 arch = PIMArchitecture(
36     pe_array=pe_array,
37     hierarchy=hierarchy,
38 )
```

12 Validation and Verification

12.1 Correctness Verification

The optimizer includes extensive validation:

1. **Dimension Factorization**: Verify $\prod \text{bounds} = \text{problem\_size}$
2. **Buffer Capacity**: Verify tile sizes fit in buffers
3. **PE Array Fit**: Verify spatial bounds $\leq$ array dimensions
4. **Relevancy**: Verify only relevant dimensions affect each datatype
5. **Loop Ordering**: Verify permutation is valid (no duplicates/gaps)

12.2 Performance Validation

Validation against cycle-accurate simulators:
Small discrepancies ($< 0.1\%$) are due to:

Table 3: Validation Results (Selected Layers)

Layer	ILP Latency	Sim Latency	Error	Status
ResNet L1	147,456	147,520	0.04%	Yes
ResNet L2	401,408	401,472	0.02%	Yes
ResNet L3	25,088	25,088	0.00%	Yes
VGG Conv1	589,824	590,080	0.04%	Yes

- Piecewise linear approximations in ILP
- Rounding in cycle calculations
- Simulator startup/teardown overhead

12.3 Row Activation Validation

Row activation counts validated against trace simulation:

1. Generate ILP-predicted mapping
2. Simulate exact memory access trace
3. Count actual row activations
4. Compare with ILP prediction

Validation shows $< 5\%$ error for most cases, with larger errors only for:

- Very small tiles (< 64 bytes)
- Complex strided patterns
- Edge cases near buffer boundaries

13 Limitations and Future Work

13.1 Current Limitations

1. **Workload Types**: Currently supports 2D convolution only. 3D convolution, pooling, and other operations not yet supported.
2. **Static Scheduling**: Assumes static loop bounds. Dynamic workloads (e.g., variable-length sequences) require extensions.
3. **Single-Node**: Models single accelerator node. Multi-node distributed execution not considered.
4. **Perfect Nesting**: Assumes perfectly nested loops. Conditional execution and irregular patterns not modeled.
5. **Data Dependencies**: Does not model complex dependencies between layers. Each layer optimized independently.

13.2 Future Enhancements

1. **Depthwise Separable Convolution**: Add support for grouped convolutions and depthwise operations common in MobileNet/EfficientNet.
2. **Multi-Layer Optimization**: Jointly optimize multiple layers considering inter-layer data reuse.
3. **Bank Conflict Modeling**: Add constraints for DRAM bank conflicts and bank-level parallelism.
4. **Network-on-Chip (NoC)**: Model on-chip interconnect bandwidth and latency.
5. **Mixed Precision**: Support different bit-widths for different datatypes (INT8, FP16, FP32).
6. **Dynamic Voltage/Frequency Scaling**: Incorporate power management into optimization.
7. **Hardware Constraints**: Add manufacturing constraints (e.g., wire length, area, power budget).
8. **Learning-Based Pruning**: Use ML to prune ILP search space for faster optimization.

13.3 Research Directions

1. **Analytical Row Activation Model**: Derive closed-form expressions for certain pattern classes to eliminate precomputation.
2. **Hybrid Optimization**: Combine ILP with heuristic search for very large search spaces.
3. **Multi-Objective Optimization**: Pareto-optimal solutions for latency-energy-area tradeoffs.
4. **Architecture Co-Design**: Use ILP results to guide hardware design decisions.
5. **Compiler Integration**: Generate optimized code directly from mapping results.

14 Conclusion

The PIM Optimizer represents a comprehensive framework for dataflow optimization on PIM accelerators. Key contributions include:

1. **Multi-Dimensional PE Array Model**: First to support independent H, W, and Internal spatial mapping with mutual exclusion constraints.
2. **Accurate Row Activation Modeling**: GCD-based crossing analysis and layout-aware cost model for precise DRAM latency estimation.
3. **Joint Layout-Mapping Optimization**: Co-optimizes data layout and loop tiling for optimal performance.
4. **Scalable ILP Formulation**: Efficient constraint formulation enabling reasonable solve times (1-5 minutes) for practical workloads.
5. **Flexible Architecture Support**: Modular design supports various PE array configurations, memory hierarchies, and DRAM technologies.

The optimizer has been validated on representative CNN workloads (ResNet, VGG, MobileNet) and shows $< 0.1\%$ error compared to cycle-accurate simulation. It provides valuable insights for both hardware designers (architecture exploration) and software developers (kernel optimization).

By combining classical optimization techniques (ILP) with domain-specific modeling (row activation, layout), the PIM Optimizer achieves both accuracy and efficiency in the challenging problem of PIM dataflow optimization.

Acknowledgments

This work builds upon the Lemon framework for accelerator dataflow optimization and incorporates DRAM timing models from JEDEC standards. The GCD-based crossing analysis was inspired by periodic pattern recognition in computational number theory.

A Notation Reference

A.1 Index Conventions

Table 4: Index Notation

Index	Meaning
w	Workload index
m	Memory level (0=PE, 1=Global, 2=RowBuf, 3=DRAM)
s	Spatial direction (H, W, Internal, Temporal)
j	Dimension index (0=R, 1=S, 2=P, 3=Q, 4=C, 5=K, 6=N)
i	Divisor index
t	Datatype (0=Input, 1=Weight, 2=Output)
p	Permutation level (inner to outer)

A.2 Symbols

Table 5: Mathematical Symbols

Symbol	Meaning
x_b	Loop bound selection variable
x_p	Permutation variable
x_d	Bypass (datatype stored?) variable
x_j	Inner relevant loop indicator
$O[j][t]$	Relevancy matrix (1 if dim j affects datatype t)
tile$[w, m, t]$	Tile size at level m for datatype t
reads$[w, m, t]$	Memory reads at level m for datatype t
g	GCD of step and block size

B File Structure Reference

```
src/pim_optimizer/
|-- __init__.py
```

```
|-- arch/
|   |-- __init__.py
|   |-- pim_arch.py         # Main architecture class
|   |-- memory.py           # Memory level definitions
|   `-- pe_array.py         # PE array configuration
|-- workload/
|   |-- __init__.py
|   `-- conv.py             # Convolution workload
|-- model/
|   |-- __init__.py
|   |-- variables.py        # Decision variables
|   |-- constraints.py      # Constraint builders
|   |-- expressions.py      # Expression builders
|   |-- objective.py        # Objective function
|   |-- crossing.py         # GCD crossing analysis
|   `-- row_activation.py   # Row activation model
|-- analysis/
|   |-- __init__.py
|   `-- dataflow.py         # Dataflow pattern analysis
|-- generator/
|   |-- hybrid_cost_model.py      # Trace simulation
|   `-- precompute_row_acts.py    # Table generation
|-- optimizer.py            # Main optimizer
|-- mapping.py              # Result representation
|-- utils.py                # Utilities
|-- cli.py                  # Command-line interface
`-- baselines.py            # Baseline comparisons
```