

RTD2797P-CG

## **MULTI-FUNCTION DISPLAY CONTROLLER**

### **DATASHEET**

**Rev. 0.9** 

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#### **USING THIS DOCUMENT**

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

#### **REVISION HISTORY**

Revision	Release Date	Summary
0.9	2015/09/01	First release.



### **Table of Contents**

1.	GENERAL DESCRIPTION	1
2.	FEATURES	••••
3.	SYSTEM APPLICATIONS	
4.	BLOCK DIAGRAM	7
5.	PIN ASSIGNMENTS	8
6.	PIN ASSIGNMENTS TABLE	9
7.	REGISTER DESCRIPTION	
8.	ELECTRICAL SPECIFICATIONS	
8.1	. Recommended Operating Conditions	.28
8.2	Absolute Maximum Ratings	28
8.3	Reset Period	.28
8.4	Recommended Operating Conditions	.29
8.5	. Absolute Maximum Ratings	.29
8.6	Absolute Maximum Ratings	.29
9.	MECHANICAL SPECIFICATIONS	30
10.	ORDERING INFORMATION	32

## **List of Tables**

TABLE 1.	SIGNALS PIN ASSIGNMENT OF EDHS BGA	9
TABLE 2.	POWER / GROUND PIN ASSIGNMENT OF EDHS BGA	25
TABLE 3.	RECOMMENDED OPERATING CONDITIONS OF EDHS BGA	28
TABLE 4.	ABSOLUTE MAXIMUM RATINGS OF EDHS BGA	28
TABLE 5.	RESET PERIOD OF EDHS BGA	28
TABLE 6.	RECOMMENDED OPERATING CONDITIONS OF PBGA	29
Table 7.	ABSOLUTE MAXIMUM RATINGS OF PBGA	29
TABLE 8.	RESET PERIOD OF PBGA	29
TABLE 9.	ORDERING INFORMATION	32

## **List of Figures**

FIGURE 1.	Data Path	7
FIGURE 2.	BALL DIAGRAM OF EDHS BGA	8
FIGURE 3.	MECHANICAL SPECIFICATION OF EDHS BGA (1)	30
FIGURE 4.	MECHANICAL SPECIFICATION OF EDHS BGA (2)	31

### 1. General Description

The Realtek RTD2797P-CG monitor controller combines an analog RGB input interface, multiple HDMI 2.0 compliant digital input interfaces with HDCP1.4/HDCP2.2, multiple DP1.2 digital input interfaces with HDCP1.4, and multiple MHL2.2 digital input interfaces with HDCP1.4. The embedded MCU is based on an industrial standard 8051 core with external serial flash.

The RTD2797P-CG is suitable for multiple market segments and display applications, such as monitor, All in One PC, and embedded applications.

#### 2. Features

#### General

- RTD2797P-CG supports input format up to 4096x2160 @ 60Hz.
- RTD2797P-CG supports one analog RGB input and six multiple-digital-interface combo inputs
- Support multiple panel interfaces like, V-by-One, and eDP
- RTD2797P-CG supports PIP / PBP and 4P function
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency.

#### Crystal

■ Support 14.318MHz crystal type

#### **Analog RGB Input Interface**

- 1 Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC

- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL
- YPbPr support up to HDTV 1080p resolution

#### **Ultra-High Speed Combo Receiver**

- 4 ports of Ultra-High Speed Combo Receivers.
- Support two HDMI2.0 (6GHz), and two DisplayPort1.2 (5.4GHz, HBR2).
- In HDMI mode, the latest HDMI2.0 is supported
- In HDMI mode, data enable only mode is supported
- In HDMI mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In HDMI mode, High-Bandwidth Digital Content Protection (HDCP 1.4/HDCP2.2) is supported
- In HDMI mode, HDMI audio is allowed to transmit to I2S/SPDIF output
- In DisplayPort mode, the latest DisplayPort 1.2 is supported
- In DisplayPort mode, three link layer speed HBR2 (5.4GHz), HBR (2.7GHz), RBR (1.62GHz) are supported
- In DisplayPort mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported

- In DisplayPort mode, High-Bandwidth Digital Content Protection (HDCP 1.4) is supported
- In DisplayPort mode,DisplayPort audio is allowed to transmit to I2S/SPDIF output

#### **High Speed Combo Receiver**

- RTD2797P-CG supports 2 ports of High Speed Combo Receivers.
- Each port can be configured as HDMI1.4 (3GHz), MHL2.1 (3GHz), or DVI as desired
- In HDMI mode, HDMI1.4 is supported
- In HDMI mode, data enable only mode is supported
- In HDMI mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In HDMI mode, High-Bandwidth Digital Content Protection (HDCP 1.4) is supported
- In HDMI mode, HDMI audio is allowed to transmit to I2S/SPDIF output
- In MHL mode, MHL2.1 is supported
- In MHL mode, High-Bandwidth Digital Content Protection (HDCP 1.4) is supported
- In MHL mode, packet pixel mode is supported
- In DVI mode, Digital Content Protection (HDCP 1.4) is supported
- In DVI mode, two adjacent receivers to support dual-link DVI with HDCP

#### **Embedded MCU**

■ Industrial standard 8051 core with external serial flash

- Low speed ADC for various application
- I2C Master or Slave hardware supported

#### **Auto Detection / Auto Calibration**

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

#### Audio

- Output: IIS , SPDIF
- Embedded Audio DAC
- Embedded headphone amp

#### Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

#### **Color Processor**

- True 12-bit color processing engine
- Programmable 14-bit gamma support
- Programmable 12-bit 3D gamma support
- xvYCC supported

- Adobe/sRGB compliance
- Advanced dithering logic for the fewer panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Peaking/Coring function for video sharpness
- Support UltraVivid III function to enhance image quality with minimal artificial effect on productivity applications
- Panel Uniformity (Brightness and color uniformity)

#### $VividColor^{TM}$

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- 2nd generation of Precise color mapping (PCM)
- Content adaptive backlight control (CABC)
- Support ADC Noise Reduction

#### **Embedded DDR3 Controller**

- RTD2797P-CG support maximal 2 external 16-bit DDR3 DRAM
- Support DDR3 speed up to 1.6GHz
- Support 90 degree image rotation:
   Portrait-to-Landscape or Landscape-to-Portrait
- LiveShow<sup>TM</sup> Function, High-performance RTC (response time compensation).
- Frame Rate Control Function

■ RTD2797P-CG supports PIP / PBP and 4P function

#### **Output Interface**

- Support 8-bit / 10-bit output through either RTD2797P, V-by-1, or eDP
- RTD2797P-CG supports 8-lane V-by-One or 8-lane eDP (HBR) with the output format up to 4k2k (4096x2160 @ 60Hz).
- Support 4-lane eDP (HBR2) with the output format up to 4096x2160 @ 60Hz.
- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Fixed Last Line output for perfect panel capability

#### **Embedded OSD**

- Embedded 64K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 64 color palette
- Maximum 26 window with alpha-blending /
- gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow
- Rotate 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character

- OSD-made internal pattern generator for factory mode
- Support  $12x18 \sim 4x18$  proportional font
- Hardware decompression for OSD font
- Support OSD scrolling
- Support 2 independent font based OSD

#### **Power Supply**

 $\blacksquare$  3.3V / 1.5V / 1.1V power supply

## 3. System Applications

- Display System on Motherboard, Monitor
- Display System for All in One PCs and embedded applications

## 4. Block Diagram

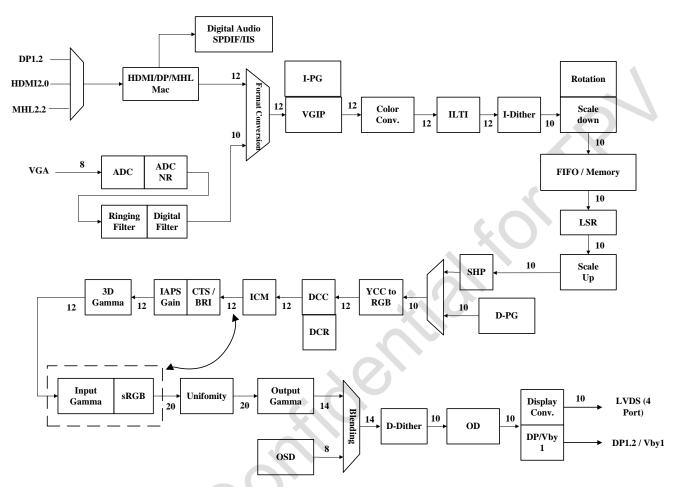
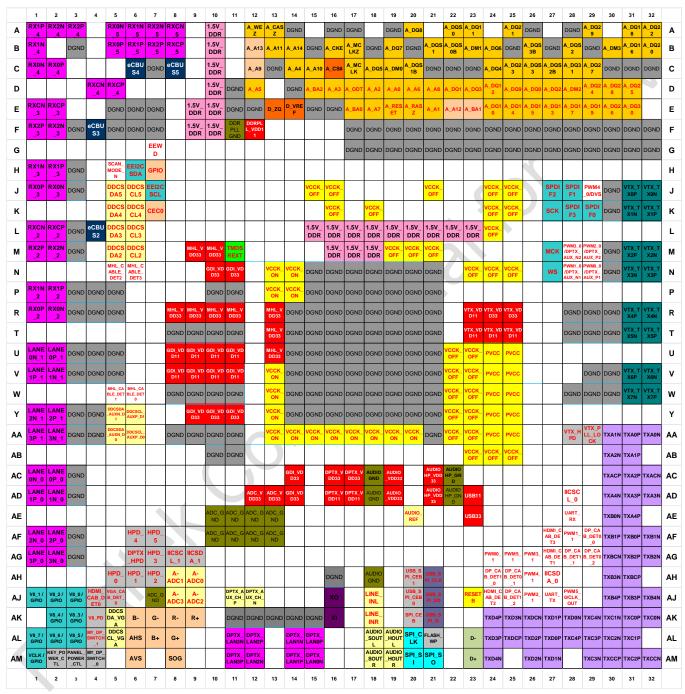


Figure 1. Data Path

### 5. Pin Assignments

#### 1024 Ball EDHS BGA



**Figure 2. Ball Diagram of EDHS BGA**Ball Diagram of RTD2797P-CG

## 6. Pin Assignments Table

#### **EDHS BGA Pin Table**

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Signals Total: 318 balls

Table 1. Signals Pin Assignment of EDHS BGA

Pin Name	I/O	Pin#	Description	Note
TMDS REXT	AI	M11	Impedance Match Reference Resistor For Scan mode,it should be pulled high	Ref value: 12 K ohm (Reference to GND)
eCBUS5	AIO	C8	MHL eCBUS 5 / Hot Plug Detect 5 / MCU GPIO	5V tolerance even when power-off
RXCP_5	Al	В8	TMDS Differential Signal Input	3.3V tolerance
RXCN_5	Al	A8	TMDS Differential Signal Input	3.3V tolerance
RX2P_5	Al	В7	TMDS Differential Signal Input	3.3V tolerance
RX2N_5	Al	A7	TMDS Differential Signal Input	3.3V tolerance
RX1P_5	Al	В6	TMDS Differential Signal Input	3.3V tolerance
RX1N_5	Al	A6	TMDS Differential Signal Input	3.3V tolerance
RX0P_5	Al	B5	TMDS Differential Signal Input	3.3V tolerance
RX0N_5	Al	A5	TMDS Differential Signal Input	3.3V tolerance
eCBUS4	AIO	C6	MHL eCBUS 4 / Hot Plug Detect 4 / MCU GPIO	5V tolerance even when power-off
RXCP_4	Al	D5	TMDS Differential Signal Input	3.3V tolerance
RXCN_4	Al	D4	TMDS Differential Signal Input	3.3V tolerance
RX2P_4	Al	A3	TMDS Differential Signal Input	3.3V tolerance
RX2N_4	Al	A2	TMDS Differential Signal Input	3.3V tolerance
RX1P_4	Al	A1	TMDS Differential Signal Input	3.3V tolerance
RX1N_4	Al	B1	TMDS Differential Signal Input	3.3V tolerance
RX0P_4	Al	C2	TMDS Differential Signal Input	3.3V tolerance
RX0N_4	Al	C1	TMDS Differential Signal Input	3.3V tolerance
eCBUS3	AIO	F4	MHL eCBUS 3 / Hot Plug Detect 3 / MCU GPIO	5V tolerance even when power-off

RXCP_3	Al	E2	TMDS Differential Signal Input	3.3V tolerance
RXCN_3	Al	E1	TMDS Differential Signal Input	3.3V tolerance
RX2P_3	Al	F1	TMDS Differential Signal Input	3.3V tolerance
RX2N_3	Al	F2	TMDS Differential Signal Input	3.3V tolerance
RX1P_3	Al	H2	TMDS Differential Signal Input	3.3V tolerance
RX1N_3	Al	H1	TMDS Differential Signal Input	3.3V tolerance
RX0P_3	Al	J1	TMDS Differential Signal Input	3.3V tolerance
RX0N_3	Al	J2	TMDS Differential Signal Input	3.3V tolerance
eCBUS2	AIO	L4	MHL eCBUS 2 / Hot Plug Detect 2 / MCU GPIO	5V tolerance even when power-off
RXCP_2	Al	L2	TMDS Differential Signal Input	3.3V tolerance
RXCN_2	Al	L1	TMDS Differential Signal Input	3.3V tolerance
RX2P_2	Al	M1	TMDS Differential Signal Input	3.3V tolerance
RX2N_2	Al	M2	TMDS Differential Signal Input	3.3V tolerance
RX1P_2	Al	P2	TMDS Differential Signal Input	3.3V tolerance
RX1N_2	Al	P1	TMDS Differential Signal Input	3.3V tolerance
RX0P_2	Al	R1	TMDS Differential Signal Input	3.3V tolerance
RX0N_2	Al	R2	TMDS Differential Signal Input	3.3V tolerance
LANE0P_1	Al	U2	DP Input : LANE0P / TMDS Differential Signal Input	3.3V tolerance
LANE0N_1	Al	U1	DP Input : LANE0N / TMDS Differential Signal Input	3.3V tolerance
LANE1P_1	Al	V1	DP Input : LANE1P / TMDS Differential Signal Input	3.3V tolerance
LANE1N_1	Al	V2	DP Input : LANE1N / TMDS Differential Signal Input	3.3V tolerance
LANE2P_1	Al	Y2	DP Input : LANE2P / TMDS Differential Signal Input	3.3V tolerance
LANE2N_1	Al	Y1	DP Input : LANE2N / TMDS Differential Signal Input	3.3V tolerance
LANE3P_1	Al	AA1	DP Input : LANE3P / TMDS Differential Signal Input	3.3V tolerance
LANE3N_1	Al	AA2	DP Input : LANE3N / TMDS Differential Signal Input	3.3V tolerance

				_
LANE0P_0	Al	AC2	DP Input : LANE0P / TMDS Differential Signal Input	3.3V tolerance
LANE0N_0	Al	AC1	DP Input : LANE0N / TMDS Differential Signal Input	3.3V tolerance
LANE1P_0	Al	AD1	DP Input : LANE1P / TMDS Differential Signal Input	3.3V tolerance
LANE1N_0	Al	AD2	DP Input : LANE1N / TMDS Differential Signal Input	3.3V tolerance
LANE2P_0	Al	AF2	DP Input : LANE2P / TMDS Differential Signal Input	3.3V tolerance
LANE2N_0	Al	AF1	DP Input : LANE2N / TMDS Differential Signal Input	3.3V tolerance
LANE3P_0	Al	AG1	DP Input : LANE3P / TMDS Differential Signal Input	3.3V tolerance
LANE3N_0	Al	AG2	DP Input : LANE3N / TMDS Differential Signal Input	3.3V tolerance
MHL_CABLE_DET1	Ю	W5	MHL Cable Detect 1 / MCU GPIO	5V tolerance even when power-off
MHL_CABLE_DET0	10	W6	MHL Cable Detect 0 / MCU GPIO	5V tolerance even when power-off
DDCSCL_AUXP_D1	Ю	Y6	AUX-CH 1 / DDC1 (Open drain I/O) / MCU GIPO	5V tolerance even when power-off
DDCSDA_AUXN_D1	Ю	Y5	AUX-CH 1 / DDC1 (Open drain I/O) / MCU GIPO	5V tolerance even when power-off
DDCSCL_AUXP_D0	Ю	AA6	AUX-CH 1 / DDC1 (Open drain I/O) / MCU GIPO	5V tolerance even when power-off
DDCSDA_AUXN_D0	Ю	AA5	AUX-CH 1 / DDC1 (Open drain I/O) / MCU GIPO	5V tolerance even when power-off
V8_0	Ю	AJ3	Video 8 input 0 / MCU GPIO	5V tolerance even when

				power-off
				5V tolerance
V8_1	Ю	AJ1	Video 8 input 1 / MCU GPIO	even when
VO_1	10	AJI	Video 8 input 17 ivico GF10	power-off
				5V tolerance
V0 2	Ю	AJ2	Video 9 input 2 / MCLL CRIC	even when
V8_2	10	AJZ	Video 8 input 2 / MCU GPIO	
				power-off
V0 2	10	A IZ 2	Video 9 input 2 / MCLL CRIC	5V tolerance
V8_3	Ю	AK3	Video 8 input 3 / MCU GPIO	even when
				power-off
\(\(\text{O}\) \(\text{A}\)	10	ALCO	Wide Oisset A / MOU ODIO	5V tolerance
V8_4	Ю	AK2	Video 8 input 4 / MCU GPIO	even when
				power-off
				5V tolerance
V8_5	Ю	AL3	Video 8 input 5 / MCU GPIO	even when
				power-off
				5V tolerance
V8_6	Ю	AL2	Video 8 input 6 / MCU GPIO	even when
				power-off
				5V tolerance
V8_7	Ю	AL1	Video 8 input 7 / MCU GPIO	even when
				power-off
		1		5V tolerance
VCLK	Ю	AM1	Video 8 Clock / MCU GPIO	even when
				power-off
				5V tolerance
AVS	I	AM6	ADC vertical sync input	even when
				power-off
~'0				5V tolerance
AHS	- 1	AL6	ADC horizontal sync input	even when
				power-off
B-	Al	AK6	Negatice Blue analog input (Pb-)	3.3V tolerance
B+	Al	AL7	Positive Blue analog input (Pb+)	3.3V tolerance
G-	Al	AK7	Negatice Green analog input (Y-)	3.3V tolerance
G+	Al	AL8	Positive Green analog input (Y+)	3.3V tolerance
SOG	Al	AM8	Sync-On-Green	3.3V tolerance
•			1	

		A 1 7 5	N ( DED ) ( )	0.01//
R-	Al	AK8	Negative RED analog input (Pr-)	3.3V tolerance
R+	Al	AK9	Positive RED analog input (Pr+)	3.3V tolerance
				5V tolerance
DDCSDA_VGA	Ю	AK5	DDC(Open drain I/O) / MCU GPIO	even when
				power-off
				5V tolerance
DDCSCL_VGA	Ю	AL5	DDC(Open drain I/O) / MCU GPIO	even when
				power-off
			My DP Switch 0 / PWM / TCON / MCU	5V tolerance
MY_DP_SWITCH_0	Ю	AM4	GPIO	even when
			GPIO	power-off
			Mar DD Conitate 4 / DIAMA / TOOM / MOUL	5V tolerance
MY_DP_SWITCH_1	Ю	AL4	My DP Switch 1 / PWM / TCON / MCU	even when
			GPIO	power-off
				5V tolerance
V8_PD	Ю	AK4	Video8 Power Down / PWM / TCON / INT / MCU GPIO	even when
_				power-off
	Ю	AJ5	VGA Cable Detect 0 / PWM / TCON / MCU GPIO	5V tolerance
VGA_CAB_DET_0				even when
				power-off
	Ю	AM3	Panel Power Control / PWM / TCON / MCU GPIO	5V tolerance
PANEL_POWER_CTL				even when
				power-off
				5V tolerance
KEY_POWER_CTL	Ю	AM2	Key Power Control / PWM / TCON / MCU GPIO	even when
				power-off
, x O				5V tolerance
IICSDA_1	Ю	AG9	IIC BUS / PWM / TCON / MCU GPIO	even when
			INC BOOT WINT TOOM, MOO CITIC	power-off
				5V tolerance
IICSCL_1	Ю	AG8	IIC BUS / PWM / TCON / MCU GPIO	even when
	'0	7,00	THE BOOT I WINT TOOM TINOU OF TO	power-off
				5V tolerance
DP_HOT_PLUG_0	Ю	AH5	Hot Plug Detect 0 / MCU GPIO	even when
DF_NO1_FLUG_U		Ailo	That I may beleet of Moo Grio	power-off
DP_HOT_PLUG_1	IO	AH6	Hot Plug Detect 1 / MCU GPIO	5V tolerance
Di _1101_FL06_1	)	\(\)10	TIOLITING DELECT 1/ MICO GFIO	JV LOIGIAILLE

				even when
				power-off
				5V tolerance
MHL_SEL_2	Ю	AH7	HDMI_MHL_SEL_2 / MCU GPIO	even when
				power-off
				5V tolerance
MHL_SEL_3	Ю	AG7	HDMI_MHL_SEL_3 / MCU GPIO	even when
				power-off
				5V tolerance
MHL_SEL_4	Ю	AF6	HDMI_MHL_SEL_4 / MCU GPIO	even when
				power-off
			XC	5V tolerance
MHL_SEL_5	Ю	AF7	HDMI_MHL_SEL_5 / MCU GPIO	even when
			. (2)	power-off
			7/0	5V tolerance
HDMI_CAB_DET0	Ю	AJ4	HDMI Cable Detect 0 / MCU GPIO	even when
				power-off
			70	5V tolerance
DPTX_HPD	Ю	AG6	DP Hot Plug Detect / MCU GPIO	even when
				power-off
				5V tolerance
A-ADC0	Ю	AH9	8-bit MCU ADC Input / INT /MCU GPIO	even when
				power-on
				5V tolerance
A-ADC1	Ю	AH8	8-bit MCU ADC Input / INT /MCU GPIO	even when
				power-on
(XO				5V tolerance
A-ADC2	Ю	AJ9	8-bit MCU ADC Input / MCU GPIO	even when
				power-on
				5V tolerance
A-ADC3	Ю	AJ8	8-bit MCU ADC Input / MCU GPIO	even when
				power-on
XI	Al	AK16	Crystal Input	3.3V tolerance
XO	AO	AJ16	Crystal Output	3.3V tolerance
LINE_INL	Al	AJ18	LINE-IN / IIS-WS / MCU GPIO	3.3V tolerance
LINE_INR	Al	AK18	LINE-IN / IIS-SCK / MCU GPIO	3.3V tolerance

AUDIO_REF	I	AE20	Audio Reference Resustance / IIS-MCK / MCU GPIO	3.3V tolerance
AUDIO_SOUTL	AO	AL18	Audio Speaker Output / IIS-SD0 / SPDIF 0 / MCU GPIO	3.3V tolerance
AUDIO_SOUTR	АО	AM18	Audio Speaker Output / IIS-SD1 / SPDIF 1 / MCU GPIO	3.3V tolerance
AUDIO_HOUTL	AO	AL19	Audio Headphone Output / IIS-SD2 / SPDIF 2 / MCU GPIO	3.3V tolerance
AUDIO_HOUTR	AO	AM19	Audio Headphone Output / IIS-SD3 / SPDIF 3 / MCU GPIO	3.3V tolerance
SPI_SI	Ю	AM20	SPI flash serial data input	3.3V tolerance
SPI_CLK	Ю	AL20	SPI flash serial clock	3.3V tolerance
SPI_CEB	Ю	AK20	SPI flash chip enable bar	3.3V tolerance
SPI_SO	Ю	AM21	SPI flash serial data output	3.3V tolerance
USB_SPI_CLK	Ю	AH21	Serial clock / CLKO /MCU GPIO	5V tolerance even when power-off
FLASH_WP	Ю	AL21	FLASH Write Protect / MCU GPIO	3.3V tolerance
USB_SPI_SO	Ю	AJ21	Serial data output / INT /MCU GPIO	5V tolerance even when power-off
USB_SPI_SI	Ю	AK21	Serial data input / INT / MCU GPIO	5V tolerance even when power-off
USB_SPI_CEB1	Ю	AH20	SPI chip enable bar 1 /T2EX/ MCU GPIO	5V tolerance even when power-off
USB_SPI_CEB0	Ю	AJ20	SPI chip enable bar 0 /IRQB / MCU GPIO	5V tolerance even when power-off
RESETB	I	AJ23	Chip reset bar	3.3V tolerance
HDMI_CAB_DET2	Ю	AJ24	HDMI Cable Detect 2/ IIS-SCK / MCU GPIO	5V tolerance even when power-off
HDMI_CAB_DET1	Ю	AG27	HDMI Cable Detect 1 / IIS-WS / MCU	5V tolerance

power-off 5V toleran	
5V toleran	
DD Calla Data at 4 O/TOON / MOU	nce
DP_CAB_DET1_0 IO AH24 DP Cable Detect 1_0/ TCON / MCU even when	n
GPIO power-off	
JUDAN Cable Datest 3/ US MCK / MCH 5V toleran	nce
HDMI_CAB_DET3 IO AF27 HDMI Cable Detect 3/ IIS-MCK / MCU even when	n
GPIO power-off	
5V toleran	nce
DP_CAB_DET1_2 IO AJ25 DP Cable Detect 1_2 / IIS-SD1 / even when	n
SPDIF1 / TCON / MCU GPIO power-off	
5V toleran	nce
DP_CAB_DET1_1 IO AG28 DP Cable Detect 1_1 / IIS-SD0 / even when	n
SPDIF0 / TCON / MCU GPIO power-off	
5V tolerar	nce
DP_CAB_DET0_1 IO AH25 DP_CAB_DET0_1/SD3/SPDIF3/ even when	n
TCON / MCU GPIO power-off	
5V toleran	nce
DP_CAB_DET0_0 IO AF29 DP_CAB_DET0_0 / SD2 / SPDIF2 / even when	n
TCON / MCU GPIO power-off	
5V tolerar	nce
UART_TX IO AJ27 UART TX / TCON / MCU GPIO even when	n
power-off	
5V toleran	nce
DP_CAB_DET0_2 IO AG29 DP_CAB_DET0_2/ TCON / MCU GPIO even when	n
/ Test4b power-off	
5V toleran	nce
PWM0_1 IO AG24 PWM / TCON / MCU GPIO / PCB even when	n
Power Down power-off	
5V tolerar	nce
UART_RX IO AE28 UART RX / TCON/ MCU GPIO even when	n
power-off	
5V toleran	nce
PWM2_1 IO AJ26 PWM / TCON / IR Receiver / MCU even when	n
GPIO power-off	
PWM1_1 IO AF28 PWM / TCON / MCU GPIO 5V tolerar	nce

				even when
				power-off
				5V tolerance
PWM4_1	Ю	AH26	PWM / TCON / T1 / MCU GPIO	even when
				power-off
				5V tolerance
PWM3_1	Ю	AG26	PWM / TCON / T2/ MCU GPIO	even when
				power-off
			PWM / XTAL_CLK_OUT / TCON / MCU	5V tolerance
PWM5_0	Ю	AJ28	GPIO	even when
			GIIO	power-off
			XC	5V tolerance
PWM5_1	Ю	AG25	PWM / TCON / T0 / MCU GPIO	even when
			. (2)	power-off
			*/0,	5V tolerance
IICSDA_0	Ю	AH27	IIC BUS / TCON / MCU GPIO	even when
				power-off
			70	5V tolerance
IICSCL_0	Ю	AD28	IIC BUS / TCON / MCU GPIO	even when
				power-off
			Why One Het Dive Detect / DDTV Het	5V tolerance
VTX_HPD	Ю	AA28	V-by-One Hot Plug Detect / DPTX Hot Plug Detect 1 / MCU GPIO	even when
			Plug Detect 17 MCO GPIO	power-off
			Why One DLL Leek / DDTV Het Dlug	5V tolerance
VTX_PLL_LOCK	Ю	AA29	V-by-One PLL Lock / DPTX Hot Plug	even when
			Detect 2 / MCU GPIO	power-off
USB_D-	Ю	AL23	USB Data-	3.3V tolerance
USB_D+	Ю	AM23	USB Data+	3.3V tolerance
TXD4P	Ю	AK24	NC	3.3V tolerance
TXD4N	Ю	AM24	NC	3.3V tolerance
TXD3P	Ю	AL24	NC	3.3V tolerance
TXD3N	Ю	AK25	NC	3.3V tolerance
TXDCP	Ю	AL25	NC	3.3V tolerance
TXDCN	Ю	AK26	NC	3.3V tolerance
TXD2P	Ю	AL26	NC	3.3V tolerance
	L	I	<u>L</u>	L

TXD2N	Ю	AM26	NC	3.3V tolerance
TXD1P	Ю	AK27	NC	3.3V tolerance
TXD1N	Ю	AM27	NC	3.3V tolerance
TXD0P	Ю	AL27	NC	3.3V tolerance
TXD0N	Ю	AK28	NC	3.3V tolerance
TXC4P	Ю	AL28	NC	3.3V tolerance
TXC4N	Ю	AK29	NC	3.3V tolerance
TXC3P	Ю	AL29	NC	3.3V tolerance
TXC3N	Ю	AM29	NC	3.3V tolerance
TXCCP	Ю	AM30	NC	3.3V tolerance
TXCCN	Ю	AM32	NC	3.3V tolerance
TXC2P	Ю	AM31	NC	3.3V tolerance
TXC2N	Ю	AL30	NC	3.3V tolerance
TXC1P	Ю	AL31	NC	3.3V tolerance
TXC1N	Ю	AK30	NC	3.3V tolerance
TXC0P	Ю	AK31	NC	3.3V tolerance
TXC0N	Ю	AK32	NC	3.3V tolerance
TXB4P	Ю	AJ30	NC	3.3V tolerance
TXB4N	Ю	AJ32	NC	3.3V tolerance
TXB3P	Ю	AJ31	NC	3.3V tolerance
TXB3N	Ю	AH30	NC	3.3V tolerance
TXBCP	Ю	AH31	NC	3.3V tolerance
TXBCN	Ю	AG30	NC	3.3V tolerance
TXB2P	Ю	AG31	NC	3.3V tolerance
TXB2N	10	AG32	NC	3.3V tolerance
TXB1P	Ю	AF30	NC	3.3V tolerance
TXB1N	Ю	AF32	NC	3.3V tolerance
TXB0P	Ю	AF31	NC	3.3V tolerance
TXB0N	Ю	AE30	NC	3.3V tolerance
TXA4P	Ю	AE31	NC	3.3V tolerance
TXA4N	Ю	AD30	NC	3.3V tolerance
TXA3P	Ю	AD31	NC	3.3V tolerance
TXA3N	Ю	AD32	NC	3.3V tolerance
TXACP	Ю	AC30	NC	3.3V tolerance
TXACN	Ю	AC32	NC	3.3V tolerance
·		_		

	1	1		,
TXA2P	Ю	AC31	NC	3.3V tolerance
TXA2N	Ю	AB30	NC	3.3V tolerance
TXA1P	Ю	AB31	NC	3.3V tolerance
TXA1N	Ю	AA30	NC	3.3V tolerance
TXA0P	Ю	AA31	NC	3.3V tolerance
TXA0N	Ю	AA32	NC	3.3V tolerance
\		34/04	V-by-One Output : 7N / DP	200
VTX_TX7N	AO	W31	Output :LANE3N	3.3V tolerance
			V-by-One Output : 7P / DP	
VTX_TX7P	AO	W32	Output :LANE3P	3.3V tolerance
			V-by-One Output : 6N / DP	
VTX_TX6N	AO	V32	Output :LANE2N	3.3V tolerance
			V-by-One Output : 6P / DP	
VTX_TX6P	AO	V31	Output :LANE2P	3.3V tolerance
			V-by-One Output : 5N / DP	
VTX_TX5N	AO	T31	Output :LANE1N	3.3V tolerance
			V-by-One Output : 5P / DP	
VTX_TX5P	AO	T32	Output :LANE1P	3.3V tolerance
			V-by-One Output : 4N / DP	
VTX_TX4N	AO	R32	Output :LANE0N	3.3V tolerance
			V-by-One Output : 4P / DP	
VTX_TX4P	AO	R31	Output :LANE0P	3.3V tolerance
			V-by-One Output : 3N / DP	
VTX_TX3N	AO	N31	Output :LANE3N	3.3V tolerance
			V-by-One Output : 3P / DP	
VTX_TX3P	AO	N32	Output :LANE3P	3.3V tolerance
110			V-by-One Output : 2N / DP	
VTX_TX2N	AO	M32	Output :LANE2N	3.3V tolerance
<b>70</b>			V-by-One Output : 2P / DP	
VTX_TX2P	AO	M31	Output :LANE2P	3.3V tolerance
			V-by-One Output : 1N / DP	
VTX_TX1N	AO	K31	Output :LANE1N	3.3V tolerance
			V-by-One Output : 1P / DP	
VTX_TX1P	AO	K32	Output :LANE1P	3.3V tolerance
VTX_TX0N	AO	J32	V-by-One Output : 0N / DP	3.3V tolerance
			.,,,	

			Output :LANE0N	
\(\pi\) \(\pi\)		10.4	V-by-One Output : 0P / DP	0.0077
VTX_TX0P	AO	J31	Output :LANE0P	3.3V tolerance
			IIS-WS / TCON / MCU GPIO	5V tolerance
WS	Ю	N27	(This pin can not work when power	even when
			saving & power Down.)	power-off
			IIS-SCK / TCON / MCU GPIO	5V tolerance
SCK	Ю	K27	(This pin can not work when power	even when
			saving & power Down.)	power-off
			IIS-MCK / MCU GPIO	5V tolerance
MCK	Ю	M27	(This pin can not work when power	even when
			saving & power Down.)	power-off
			SPDIF0 / IIS-SD0 / MCU GPIO	5V tolerance
SPDIF0	Ю	K29	(This pin can not work when power	even when
			saving & power Down.)	power-off
			SPDIF1 / IIS-SD1 / MCU GPIO	5V tolerance
SPDIF1	Ю	J28	(This pin can not work when power	even when
			saving & power Down.)	power-off
			SPDIF2 / IIS-SD2 / MCU GPIO	5V tolerance
SPDIF2	Ю	J27	(This pin can not work when power	even when
			saving & power Down.)	power-off
			SPDIF3 / IIS-SD2 / MCU GPIO	5V tolerance
SPDIF3	Ю	K28	(This pin can not work when power	even when
			saving & power Down.)	power-off
			PWM / DVS / TCON / MCU GPIO	5V tolerance
PWM4_0	IO	J29	(This pin can not work when power	even when
VXV			saving & power Down.)	power-off
			PWM / DPTX AUX-CH / TCON / MCU	E)/tolorene
DIAMAG	10	NICO	GPIO	5V tolerance
PWM0_0	Ю	N29	(This pin can not work when power	even when
			saving & power Down.)	power-off
			PWM / DPTX AUX-CH / TCON / MCU	EV/tolorense
D\\/\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	10	NOO	GPIO	5V tolerance
PWM1_0	Ю	N28	(This pin can not work when power	even when
			saving & power Down.)	power-off
PWM2_0	Ю	M29	PWM / DPTX AUX-CH / TCON / MCU	5V tolerance

			GPIO	even when
			(This pin can not work when power	power-off
			saving & power Down.)	
PWM3_0	Ю	M28	PWM / DPTX AUX-CH / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
D_VREF	I	E14	Reference Voltage	
A_BA0	Ю	E17	Bank Address Input	
A_BA1	Ю	E23	Bank Address Input	
A_BA2	O	D15	Bank Address Input	
A_A0	O	D19	Address Input	
A_A1	O	E21	Address Input	
A_A2	Ю	D18	Address Input	
A_A3	OI	D16	Address Input	
A_A4	O	C14	Address Input	
A_A5	OI	D12	Address Input	
A_A6	O	D20	Address Input	
A_A7	O	E18	Address Input	
A_A8	O	D21	Address Input	
A_A9	O	C12	Address Input	
A_A10	Ю	C15	Address Input	
A_A11	Ю	B13	Address Input	
A_A12	0	E22	Address Input	
A_A13	0	B12	Address Input	
A_A14	10	B14	Address Input	
A_DM0	Ю	C19	Input Data Mask	
A_DM1	O	B23	Input Data Mask	
A_DM2	Ю	D28	Input Data Mask	
A_DM3	Ю	B30	Input Data Mask	
A_DQ0	Ю	D26	Data Input / Output	
A_DQ1	Ю	D22	Data Input / Output	
A_DQ2	Ю	D27	Data Input / Output	
A_DQ3	Ю	D23	Data Input / Output	
A_DQ4	Ю	C24	Data Input / Output	

A_DQ5	Ю	C18	Data Input / Output	
A_DQ6	Ю	B24	Data Input / Output	
A_DQ7	Ю	B19	Data Input / Output	
A_DQ8	Ю	A20	Data Input / Output	
A_DQ9	Ю	D25	Data Input / Output	
A_DQ10	Ю	E24	Data Input / Output	
A_DQ11	Ю	A23	Data Input / Output	
A_DQ12	Ю	D24	Data Input / Output	
A_DQ13	Ю	E27	Data Input / Output	
A_DQ14	Ю	E25	Data Input / Output	
A_DQ15	Ю	E26	Data Input / Output	
A_DQ16	Ю	B31	Data Input / Output	
A_DQ17	Ю	E28	Data Input / Output	
A_DQ18	Ю	A31	Data Input / Output	
A_DQ19	Ю	E29	Data Input / Output	
A_DQ20	Ю	B32	Data Input / Output	
A_DQ21	Ю	A25	Data Input / Output	
A_DQ22	Ю	A32	Data Input / Output	
A_DQ23	Ю	C25	Data Input / Output	
A_DQ24	Ю	D29	Data Input / Output	
A_DQ25	Ю	D31	Data Input / Output	
A_DQ26	Ю	E30	Data Input / Output	
A_DQ27	Ю	C29	Data Input / Output	
A_DQ28	Ю	D30	Data Input / Output	
A_DQ29	10	A29	Data Input / Output	
A_DQ30	Ю	E31	Data Input / Output	
A_DQ31	Ю	C28	Data Input / Output	
			Data strobe : Output with read data.	
A_DQS0	Ю	A22	Edge-aligned with read data. Input with	
			write data. Center-aligned to write data	
			Data strobe : Output with read data.	
A_DQS0B	Ю	B22	Edge-aligned with read data. Input with	
			write data. Center-aligned to write data	
A_DQS1	Ю	B21	Data strobe : Output with read data.	
, <u>, _ D &amp;</u> O I	.0	טב ו	Edge-aligned with read data. Input with	

		write data. Center-aligned to write data	
		Data strobe : Output with read data.	
Ю	C20	Edge-aligned with read data. Input with	
		write data. Center-aligned to write data	
		Data strobe : Output with read data.	
Ю	B28	Edge-aligned with read data. Input with	
		write data. Center-aligned to write data	
		Data strobe : Output with read data.	
Ю	C27	Edge-aligned with read data. Input with	
		write data. Center-aligned to write data	
		Data strobe : Output with read data.	
Ю	C26	Edge-aligned with read data. Input with	
		write data. Center-aligned to write data	
		Data strobe : Output with read data.	
Ю	B26	Edge-aligned with read data. Input with	
		write data. Center-aligned to write data	
		Command inputs : A_RASZ, A_CASZ,	
		and A_WEZ (along with A_CS#) define	
Ю	A13	the command	
		being entered and are referenced to	
		VREFCA.	
Ю	B16	Clock enable	
Ю	C16	Chip select	
	)	Clock : A_ MCLK and A_ MCLKZ are	
		differential clock inputs. All address and	
		control input signals are sampled on the	
10	C17	crossing of the positive edge of	
		A_MCLK and negative edge of	
		A_MCLKZ.	
		Clock : A_ MCLK and A_ MCLKZ are	
		differential clock inputs. All address and	
		control input signals are sampled on the	
Ю	B17	crossing of the positive edge of	
		A_MCLK and negative edge of	
		A_MCLKZ.	
Ю	D17	On-die termination : ODT enables	
	10 10 10 10 10 10 10 10 10 10 10 10 10 1	IO B28  IO C27  IO C26  IO B26  IO B16  IO C16  IO C17	Data strobe: Output with read data.  Edge-aligned with read data. Input with write data. Center-aligned to write data  Data strobe: Output with read data.  Edge-aligned with read data. Input with write data. Center-aligned to write data  Data strobe: Output with read data.  Data strobe: Output with read data.  Edge-aligned with read data. Input with write data. Center-aligned to write data  Data strobe: Output with read data.  Edge-aligned with read data. Input with write data. Center-aligned to write data  Data strobe: Output with read data.  Edge-aligned with read data. Input with write data. Center-aligned to write data  Command inputs: A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define the command being entered and are referenced to VREFCA.  IO B16 Clock enable  IO C16 Chip select  Clock: A_MCLK and A_MCLKZ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of A_MCLKZ.  Clock: A_MCLK and A_MCLKZ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of A_MCLKZ.  Clock: A_MCLK and A_MCLKZ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of A_MCLKZ.

(registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM.  Command inputs : A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define the command being entered and are referenced to	
termination resistance internal to the DDR3 SDRAM.  Command inputs : A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define the command being entered and are referenced to	
DDR3 SDRAM.  Command inputs : A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define  the command being entered and are referenced to	
Command inputs : A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define  A_RASZ  IO  E20  the command being entered and are referenced to	
A_RASZ IO E20 and A_WEZ (along with A_CS#) define the command being entered and are referenced to	
A_RASZ IO E20 the command being entered and are referenced to	
being entered and are referenced to	
VREFCA.	
Reset : A_RESET is an active LOW	
A_RESET IO E19 CMOS input referenced to VSS.	
Command inputs : A_RASZ, A_CASZ,	
and A_WEZ (along with A_CS#) define	
A_WEZ IO A12 the command	
being entered and are referenced to	
VREFCA.	
External reference ball for output drive	
calibration: This ball is tied to an	
D_ZQ I E13 external 240Ω resistor (1%), which is	
tied to VSSQ.	
5V tolerand	;e
GPIO IO H7 MCU GPIO even when	
power-off	
5V tolerand	;e
CEC0 IO K7 CEC 0 / MCU GPIO even when	
power-off	
EEWD IO G7 EEWD / PWM / Tcon / MCU GPIO 3.3V toleral	nce
EEI2CSCL IO J7 EEI2CSCL / PWM / TCON / MCU GPIO 3.3V toleral	nce
EEI2CSDA / PWM / TCON / MCU	
EEI2CSDA IO H6 GPIO 3.3V toleral	nce
When AC power is turned on, this ball	
SCAN_MODE_N IO H5 must be pull "High". 3.3V toleral	nce
5V tolerand	;e
DDCSCL5 IO J6 DDC5(Open drain I/O) / MCU GPIO even when	ſ
power-off	ſ
DDCSDA5 IO J5 DDC5(Open drain I/O) / MCU GPIO 5V tolerand	<del></del>

	•		T	
				even when
				power-off
				5V tolerance
DDCSCL4	Ю	K6	DDC4(Open drain I/O) / MCU GPIO	even when
				power-off
				5V tolerance
DDCSDA4	Ю	K5	DDC4(Open drain I/O) / MCU GPIO	even when
				power-off
				5V tolerance
DDCSCL3	Ю	L6	DDC4(Open drain I/O) / MCU GPIO	even when
			4.0	power-off
			XC	5V tolerance
DDCSDA3	Ю	L5	DDC4(Open drain I/O) / MCU GPIO	even when
			. (2)	power-off
			7/0	5V tolerance
DDCSCL2	Ю	M6	DDC4(Open drain I/O) / MCU GPIO	even when
				power-off
			70	5V tolerance
DDCSDA2	Ю	M5	DDC4(Open drain I/O) / MCU GPIO	even when
				power-off
				5V tolerance
MHL_CABLE_DET2	Ю	N5	MHL Cable Detect 2 / MCU GPIO	even when
				power-off
				5V tolerance
MHL_CABLE_DET3	Ю	N6	MHL Cable Detect 3 / MCU GPIO	even when
				power-off

### Power / Ground Pin Assigment

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Total: 322 balls

Table 2. Power / Ground Pin Assignment of EDHS BGA

P/G Pin Name	I/O	Pin #	Description	Note
GDI_VDD33	AP	N10, N11, Y9, Y10, Y11, AC14, AD14	3.3V Analog Power	7 balls
GDI_VDD11	AP	U8, U9, U10, U11, V8, V9, V10, V11		8 balls
MHL_VDD33	AP	R8, R9, R10, R11, T13, U13, M9, M10, R13	3.3V Analog Power	9 balls

ADC_VDD33	AP	AD12, AD13	3.3V ADC Power	2 balls
ADC_GND	AG	AJ7, AE11, AF11, AE10, AF10, AE12, AF12, AE13, AF13	ADC Gound	9 balls
DPTX_VDD11	AP	AD16, AD17	1.1V DPTx Power	2 balls
DPTX_VDD33	AG	AC16, AC17	3.3V DPTx Power	2 balls
AUDIO_VDD33	AP	AC19, AD19	3.3V Audio Power	2 balls
AUDIO_GND	AG	AC18, AD18, AH18	Audio Gound	3 balls
AUDIO HP	AP	AC21, AD21	3.3V Audio HP	2 balls
_VDD33			Power	
AUDIO	AG	AC22, AD22	Audio HP Ground	2 balls
HP_GND				
USB11	AP	AD23	USB 1.1V	1 ball
USB33	AP	AE23	USB 3.3V	1 ball
VTX_VDD11	AP	R23, T23, T24, T25	1.1V Analog Power	4 balls
VTX_VDD33	AP	R24, R25	3.3V Analog Power	2 balls
PVCC	Р	U25, V24, V25, W24, U24, W25, Y24, Y25, AA24, AA25	Pad Power	10 balls
1.5V_DDR	Р	A10, B10, C10, D10, E9, E10, F9, F10, L15, L16, L17, L18, L19, L20, M16, M17, M18, L21, L22, L23	1.5V DDR3 Power	20 balls
VCCK_ON	Р	AA18, AA17, AA16, AA13, Y13, W13, P13, N14, N13, P14, V13, AA14, AA15, AA19, AA20	1.1V Core Power	15 balls
VCCK_OFF	Р	L24, M21, M19, M20, K24, K25, K16, K18, J15, J16, J21, J24, J25, N23, N24, N25, U22, U23, V22, V23, W22, W23, Y22, Y23, AA22, AA23, AB23, AB24, AB25	1.1V Core Power	29 balls
DDRPLL_VDD1	Р	F12	1.1V DDR PLL	1 ball
1			Power	
DDR PLL GND	G	F11	DDR PLL Ground	1 ball
DGND	O	A14, A16, A17, A19, A26, A28, B15, B18, B20, B25, B27, B29, C13, C21, C22, C23, C30, C31, C32, D11, D14, E11, E12, E15, E16, F17, F18, F19, F20, F21, F22, F23, F25, F26, F27, F28, G17, G18, G20, G21, G22, G23, G24, G25, G26, G27, G28, H3, J3, J30, T8, T9, T10, T11, U3, U4, U5, V14, V15, V16, V17, V18, V19, V20, V21, W14, W15, W16, W17, W18, W19, W20, W21, W28, W29, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, AA3, AA4,	Digital Ground	190 balls

AA8, AA9, AA10, AA11, AA21,	
N20, P3, P4, P5, P10, P11, P15,	
P16, P17, P18, P20, P21, R3, R4,	
R14, R15, P19, R5, R16, B3, C7,	
E5, E6, E7, F3, F5, F6, F7, F24,	
F29, F30, F31, F32, G19, G29,	
G30, G31, G32, K30, L3, M3,	
M30, N15, N16, N17, N18, N19,	
N30, R17, R18, R19, R20, R21,	
R28, R29, R30, T14, T15, T16,	
T17, T18, T19, T20, T21, T28,	
T29, T30, U14, U15, U16, U17,	
U18, U19, U20, U21, V3, V4, V5,	
V29, V30, W8, W9, W10, W11,	
W30, Y3, Y4, AB10, AB11, AC3,	
AD3, AF3, AG3, AH16, AK11,	
AK12, AK13, AK14, AK15, N21	

### 7. Electrical Specifications

**EDHS BGA DC Characteristics** 

### 7.1. Recommended Operating Conditions

Table 3. Recommended Operating Conditions of EDHS BGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerance)	$V_{IN}$	-1		5	V
Supply Voltage	PVCC	3.14	3.30	3.47	V
DDR Voltage	1.5V_DDR	1.43	1.5	1.57	V
Core Power On Voltage	VCCK_ON	1.05	1.1	1.15	V
Core Power Off Voltage	VCCK_OFF	1.05	1.1	1.15	V
Electrostatic Discharge	$V_{ESD}$			±2.5	kV
Latch-Up	I <sub>LA</sub>			±100	mA
Ambient Operating Temperature	T <sub>A</sub>	0		70	°C
Storage Temperature (plastic)	T <sub>STG</sub>	-55		110	٥C
Thermal Resistance (Junction to Air)	$\theta_{JA}$		13.85		°C/W
Thermal Resistance (Junction to Case)	$\theta_{JC}$		5.07		°C/W
Junction Acceptable Temperature	T <sub>i</sub>			125	°C

### 7.2. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings of EDHS BGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	PVCC			3.6	V
Storage Temperature (plastic)	$T_{STG}$			150	∘C
Junction Acceptable Temperature	$T_{\rm j}$			125	٥C

Note: Operation under the absolute maximum ratings does not imply well-functioning. Long-term stress to the absolute maximum ratings would probably affect the device reliability or further cause permanent damage.

## 7.3. Reset Period

Table 5. Reset Period of EDHS BGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset Pulse Period	Trst-en <sup>1</sup>	1120			ns
Power-on-Reset Period	Tpor-rst <sup>2</sup>	145	146.5	148	ms

<sup>1. 16 \*</sup> Xtal\_cycle(1/14.3Mhz)

<sup>2. 65536\*16\*2\*</sup>Xtal\_cycle(1/14.3Mhz)

### 7.4. Recommended Operating Conditions

Table 6. Recommended Operating Conditions of PBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerance)	V <sub>IN</sub>	-1		5	V
Supply Voltage	PVCC	3.14	3.30	3.47	V
DDR Voltage	1.5V_DDR	1.43	1.5	1.57	V
Core Power On Voltage	VCCK_ON	1.05	1.1	1.15	V
Core Power Off Voltage	VCCK_OFF	1.05	1.1	1.15	V
Electrostatic Discharge	$V_{ESD}$			±2.5	kV
Latch-Up	I <sub>LA</sub>			±100	mA
Ambient Operating Temperature	T <sub>A</sub>	0		70	°C
Storage Temperature (plastic)	T <sub>STG</sub>	-55		110	٥C
Thermal Resistance (Junction to Air)	$\theta_{JA}$		16.32		°C/W
Thermal Resistance (Junction to Case)	$\theta_{JC}$		5.52		°C/W
Junction Acceptable Temperature	T <sub>i</sub>			125	٥C

### 7.5. Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings of PBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	PVCC			3.6	V
Storage Temperature (plastic)	$T_{STG}$			150	٥C
Junction Acceptable Temperature	$T_i$			125	۰C

Note: Operation under the absolute maximum ratings does not imply well-functioning. Long-term stress to the absolute maximum ratings would probably affect the device reliability or further cause permanent damage.

## 7.6. Reset Period

Table 8. Reset Period of PBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset Pulse Period	Trst-en <sup>1</sup>	1120			ns
Power-on-Reset Period	Tpor-rst <sup>2</sup>	145	146.5	148	ms

<sup>1. 16 \*</sup> Xtal\_cycle(1/14.3Mhz)

<sup>2. 65536\*16\*2\*</sup>Xtal\_cycle(1/14.3Mhz)

## 8. Mechanical Specifications

EDHS BGA

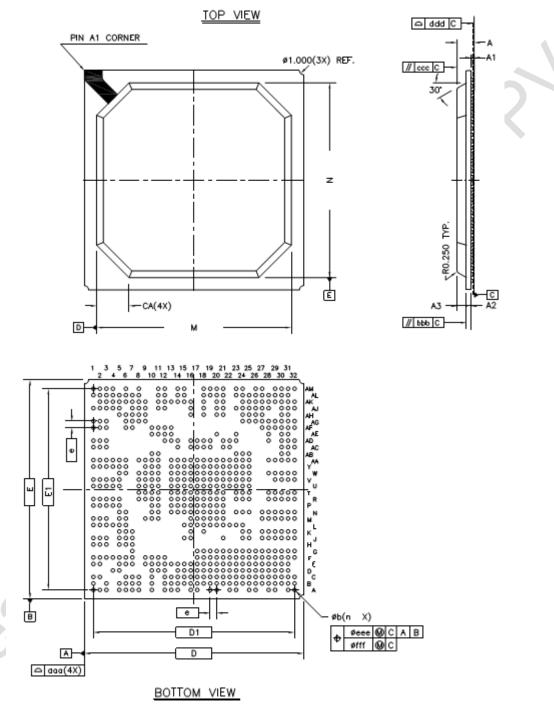


Figure 3. Mechanical Specification of EDHS BGA (1)

			Commo	on Dimer	nsions		
		Symbol	MIN.	NOM.	MAX.		
Package :			HS FBGA				
Body Size:	X Y	D E	27.000 27.000				
Ball Pitch :	6	0.800					
Total Thickness :	A	1.982 2.100 2.21					
Mold Thickness :	A3	1.1	70 I	Ref.			
Substrate Thickness :	A2	0.5	60 F	Ref.			
Ball Diameter :		O	.450				
Stand Off:	A1	0.320	-	0.420			
Ball Width :	ь	0.375		0.525			
Mold Area :	M	24.000 24.000					
H/S Exposed Size:	P	19 ~ 20					
H/S Flatness		Q	0.100				
H/S Shift With Substrate Edge:		R	0.300				
H/S Shift With Mold Area:		s	0.500				
Chamfer		CA	4.000 Ref.				
Package Edge Tolerance :		aaa	0.150				
Substrate Parallelism :		bbb	0.100				
Mold Parallelism :		ccc	0.200				
Coplanarity:	ddd	0.150					
Ball Offset (Package) :		eee	0.150				
Ball Offset (Ball) :	fff	0.080					
Ball Count :		n	640				
Edge Ball Center to Center :	D1 E1		24.80 24.80				

Figure 4. Mechanical Specification of EDHS BGA (2)

## 9. Ordering Information

Table 9. Ordering Information

Part No.	Max. Resolution / Timing	Input: VGA	Input: HDMI2.0	Input DP1.2 HBR2	Input: DHMI1.4/ MHL2/DVI	Output: Vx1/eDP HBR/eDP HBR2/LVD S	•	4P	FRC	OD	Max number of DDR3 support	Package
RTD2797P -CG	4096x2160 @60Hz	•	2 Port	2 Port	2 Port	•	•	•	•	•	2	640-ball PBGA

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