Outline

I. HDMI Introduction

i. Overview

ii. Data Path

iii. Signal Flow

II. Firmware Flow

i. Switch

ii. Pre-detect

iii. Scan

iv. Measure

Outline

I. HDMI Introduction

i. Overview

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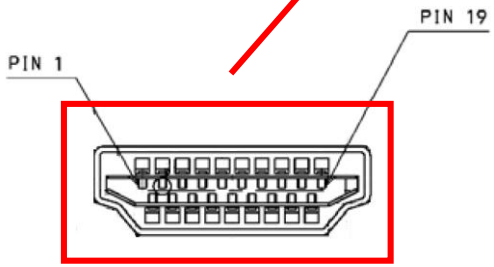
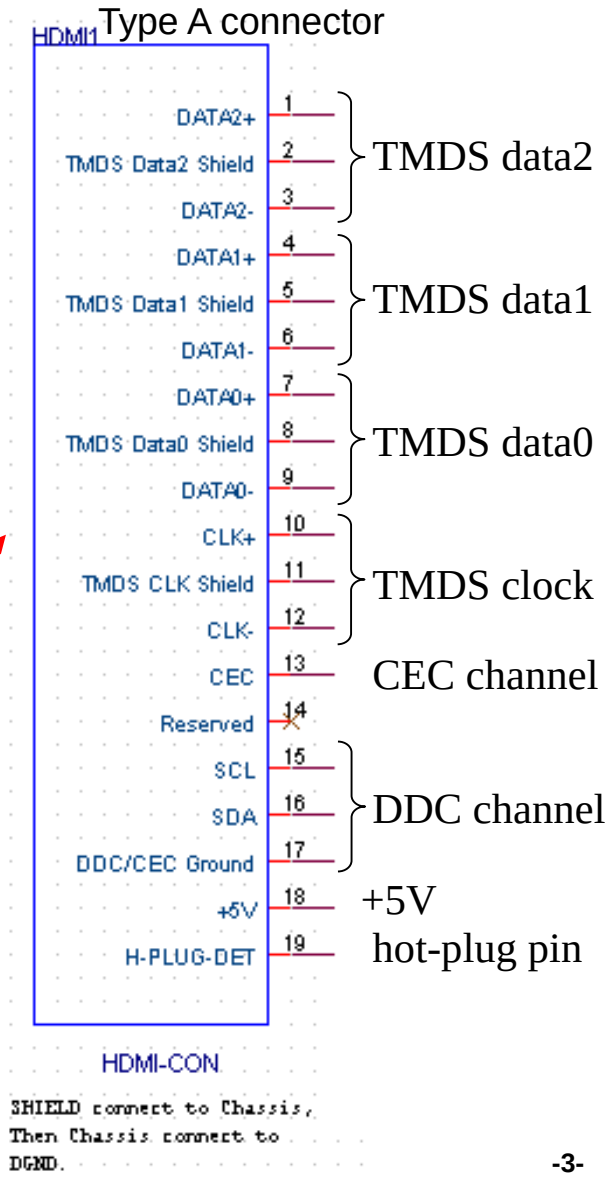
II. Firmware Flow

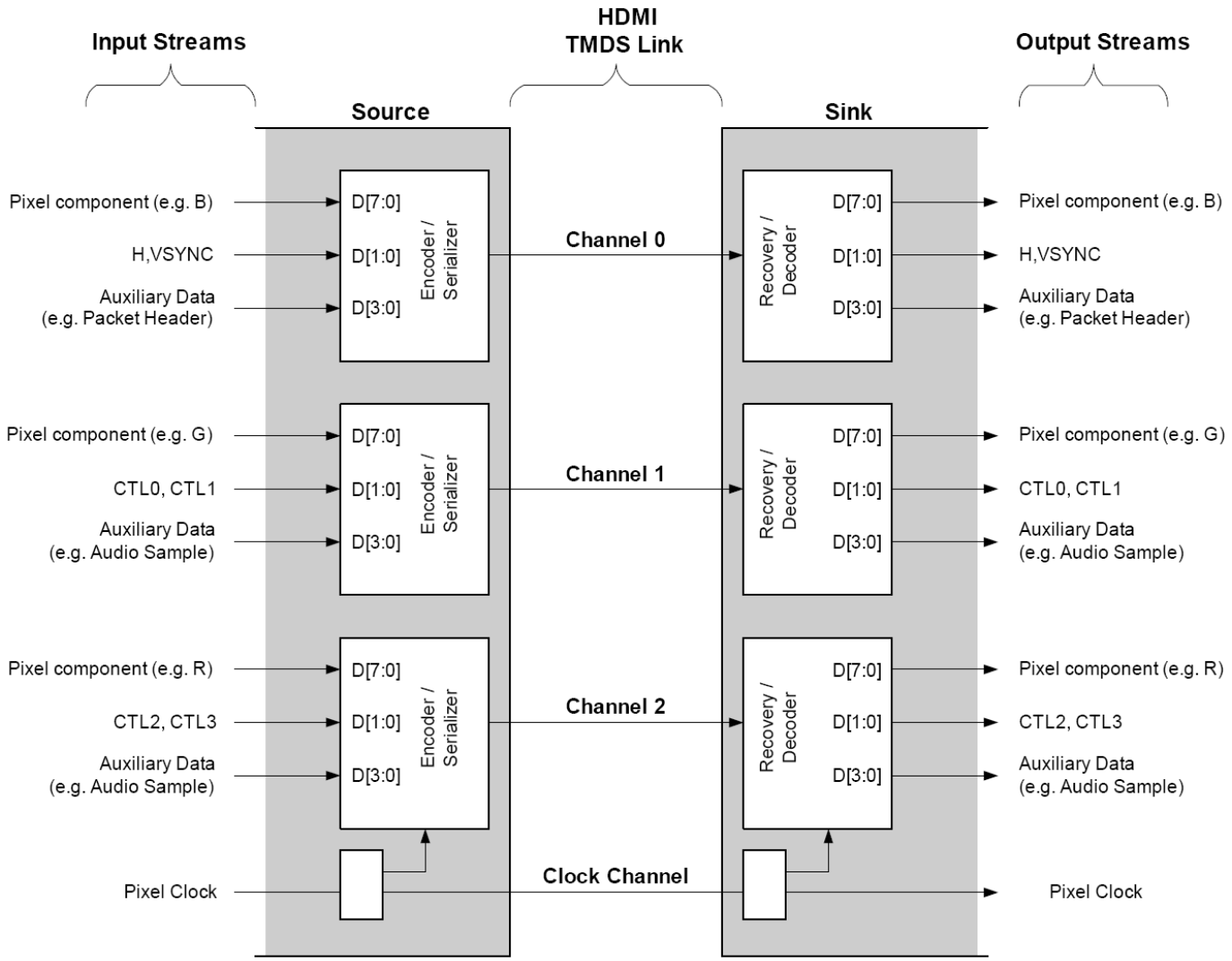
HDMI Connector

- 4 TMDS Links
  - 3 data channels
  - 1 clock channel
- DDC channel
  - to EEPROM
  - to IC
- CEC channel
- Hot-plug pin

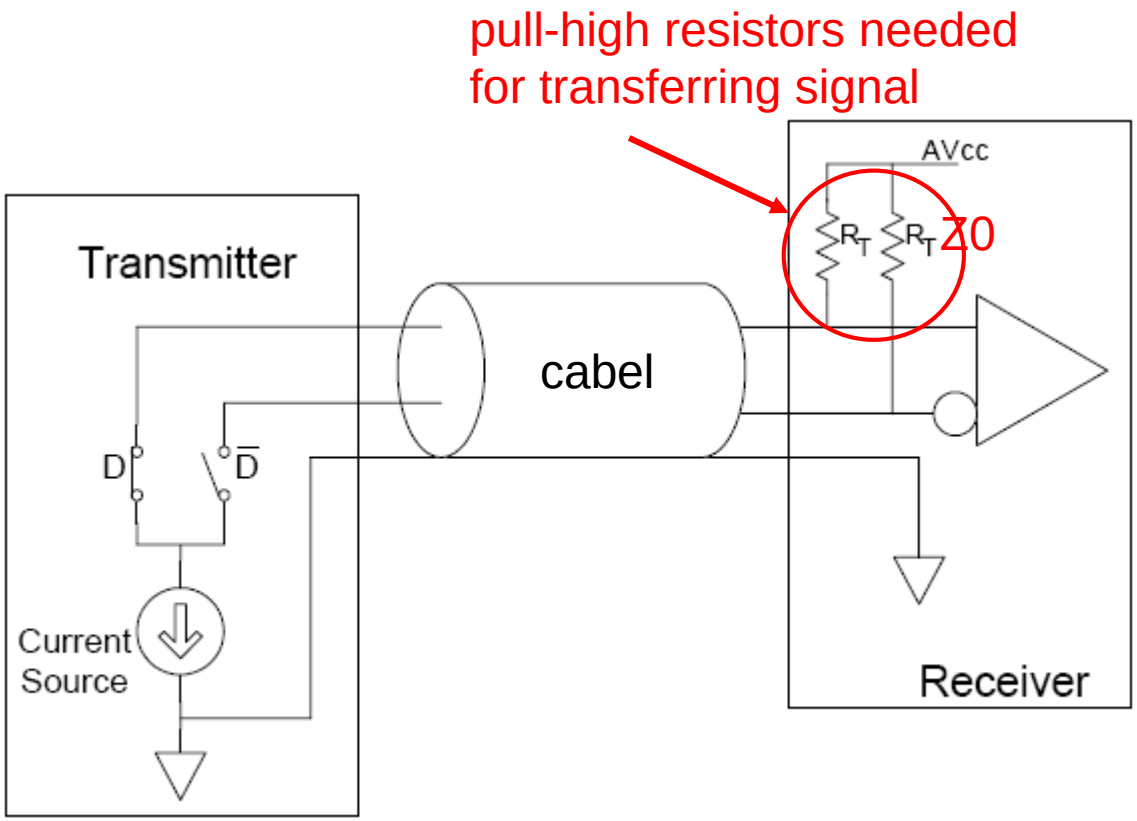


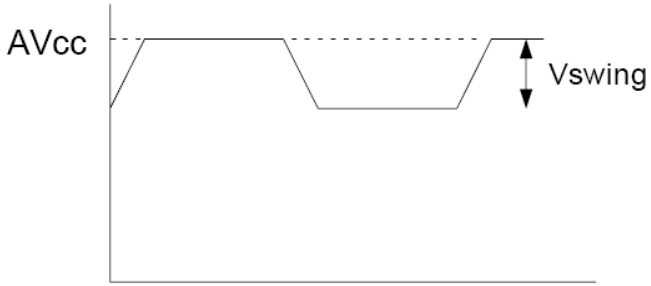


TMDS Link (1/3)

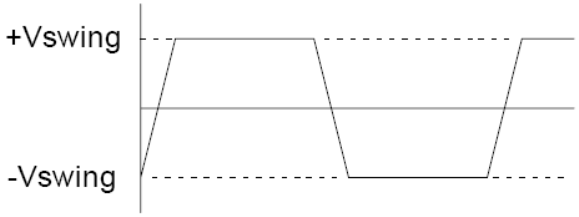

Input Streams
HDMI
TMDS Link
Output Streams
Source
Sink
Pixel component (e.g. B)
H,VSYNC
Auxiliary Data
(e.g. Packet Header)
D[7:0]
D[1:0]
D[3:0]
Encoder / Serializer
Channel 0
Recovery / Decoder
Pixel component (e.g. B)
H,VSYNC
Auxiliary Data
(e.g. Packet Header)
Pixel component (e.g. G)
CTL0, CTL1
Auxiliary Data
(e.g. Audio Sample)
Channel 1
Pixel component (e.g. G)
CTL0, CTL1
Auxiliary Data
(e.g. Audio Sample)
Pixel component (e.g. R)
CTL2, CTL3
Auxiliary Data
(e.g. Audio Sample)
Channel 2
Pixel component (e.g. R)
CTL2, CTL3
Auxiliary Data
(e.g. Audio Sample)
Pixel Clock
Clock Channel
Pixel Clock

TMDS Link (2/3)





Single-ended Differential Signal



Differential Signal

TMDS Link (3/3)

Data Channel

- transfer 10 bits per TMDS clock
  - 10-bit encoding
  - 3 data transferring period

Clock Channel

- pixel clock: 25M~340M (Hz)
- change with color depth

TMDS Encoding

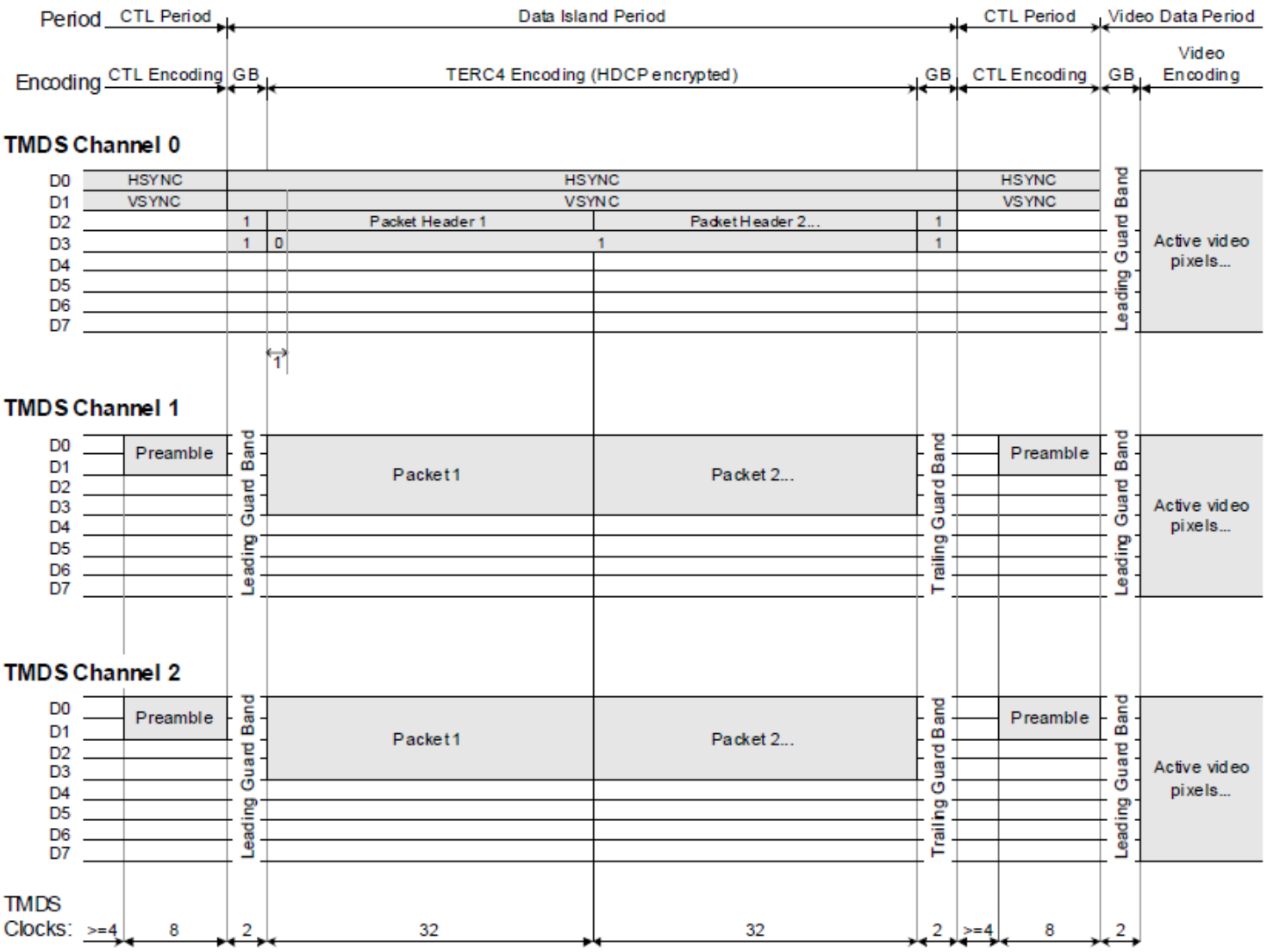
Transition-**M**inimized **D**ifferential **S**ignaling:

- transition minimized: fewer 0->1 & 1->0
- DC balanced: equal 0s & 1s

Encoding

- video data: 8b/10b
- packet data: 4b/10b
- control data: 2b/10b (transition maximized)

HDMI: Signal Format(1/3)

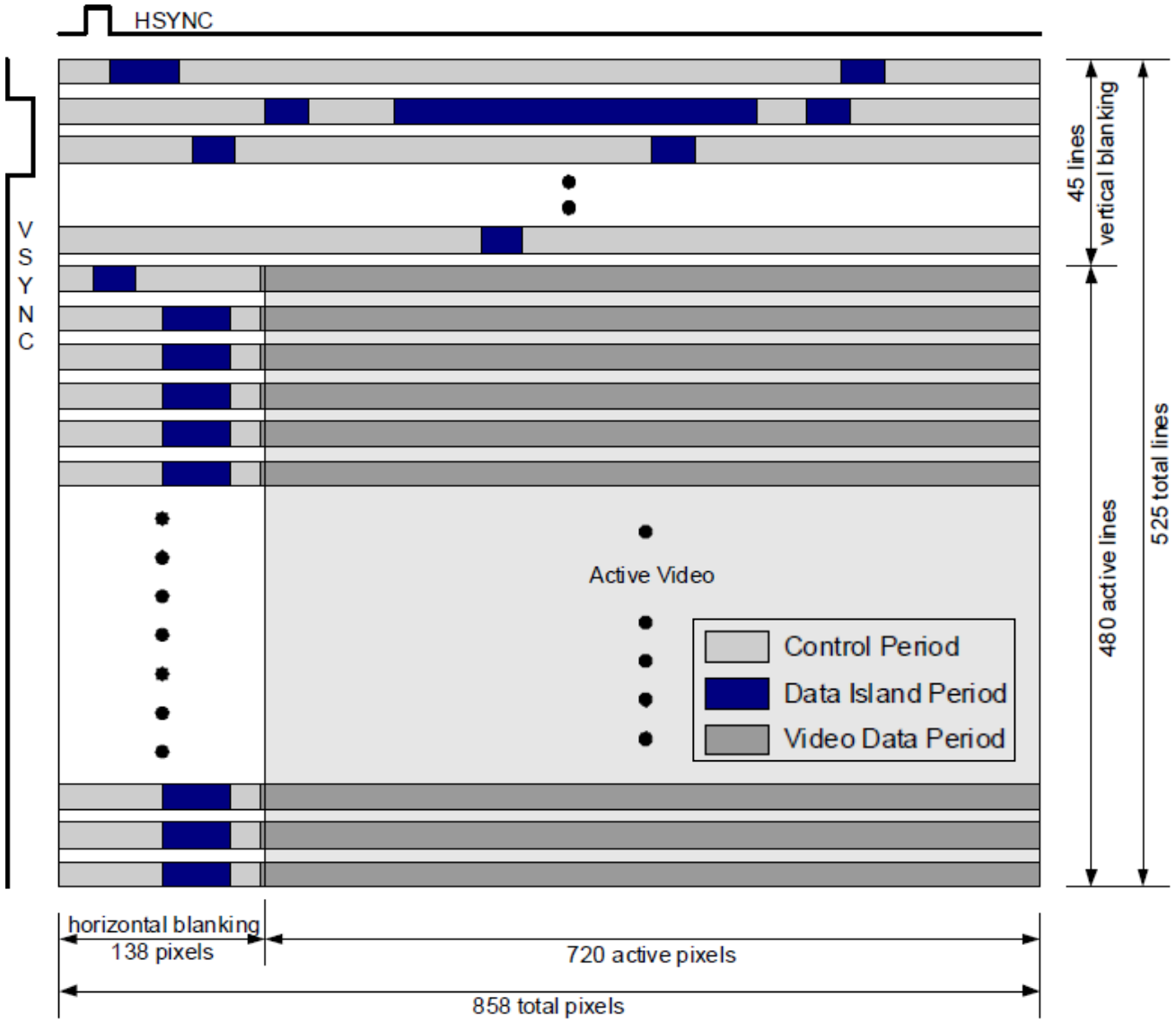


HDMI: Signal Format(2/3)

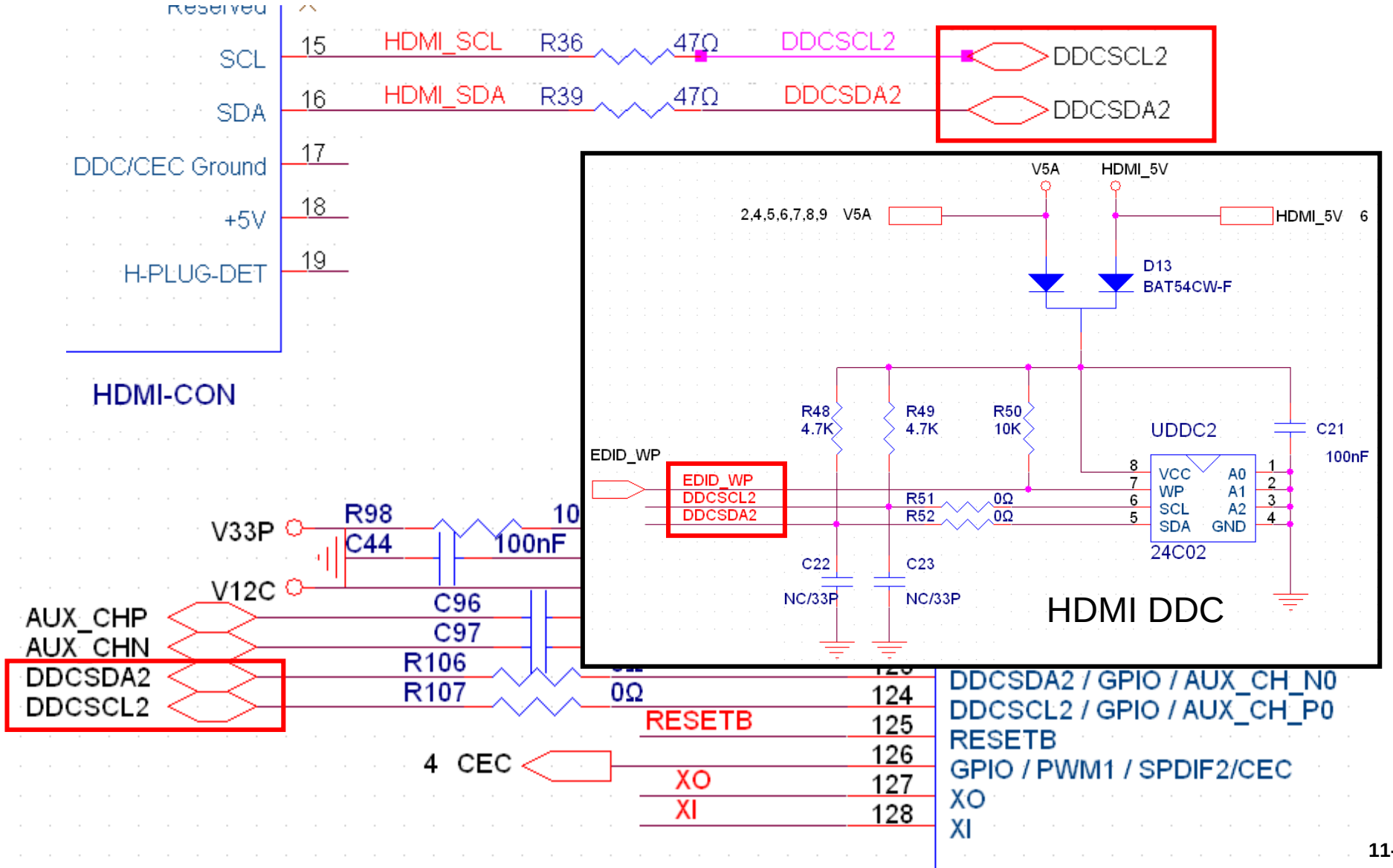
1. **video data period**
   - pixel data
2. **data island period**
   - packet data (ex: audio, auxiliary data)
   - associated error correction codes (BCH)
3. **control period**
   - preamble
   - HS/VS & CTLx

HDMI: Signal Format(3/3)

EX:
720x480p video frame



HDMI DDC Channel



HDMI Video Format

pixel encoding:

- RGB
- YCbCr 444/422

color depth

- 24 bits
- 30, 36, and 48 bits per pixel

Pixel Packing

24 bit mode: P (pixels/group) = 1 pixel; L (fragments/group) = 1 fragment (1 TMDS character). Standard HDMI format.

Fragment	Phase	Pixels	8 bit HDMI pixel data code (to encoder)							
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
8P0	0	A	A0	A1	A2	A3	A4	A5	A6	A7

30 bit mode: P = 4 pixels; L = 5 fragments

Fragment	Phase	Pixels	8 bit HDMI pixel data code (to encoder)							
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
10P0	0	A	A0	A1	A2	A3	A4	A5	A6	A7
10P1	1	A+B	A8	A9	B0	B1	B2	B3	B4	B5
10P2	2	B+C	B6	B7	B8	B9	C0	C1	C2	C3
10P3	3	C+D	C4	C5	C6	C7	C8	C9	D0	D1
10P4	4	D	D2	D3	D4	D5	D6	D7	D8	D9

36 bit mode: P = 2 pixels; L = 3 fragments

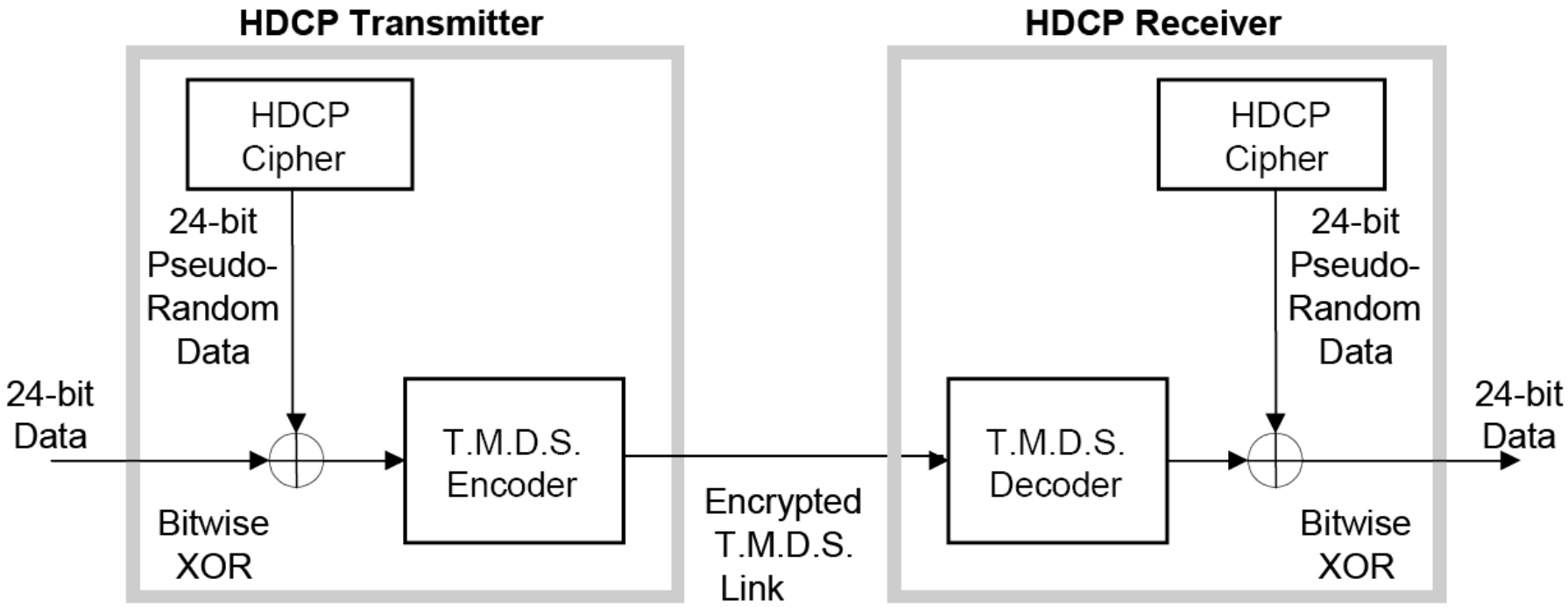
Fragment	Phase	Pixels	8 bit HDMI pixel data code (to encoder)							
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
12P0	0	A	A0	A1	A2	A3	A4	A5	A6	A7
12P1	1	A+B	A8	A9	A10	A11	B0	B1	B2	B3
12P2	2	B	B4	B5	B6	B7	B8	B9	B10	B11

48 bit mode: P = 1 pixel; L = 2 fragments

Fragment	Phase	Pixels	8 bit HDMI pixel data code (to encoder)							
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
16P0	0	A	A0	A1	A2	A3	A4	A5	A6	A7
16P1	1	A	A8	A9	A10	A11	A12	A13	A14	A15

HDCP Encryption

HDCP cipher generates a new 24bit data for every pixel of HDCP content to be encrypted.



Outline

I. HDMI Introduction

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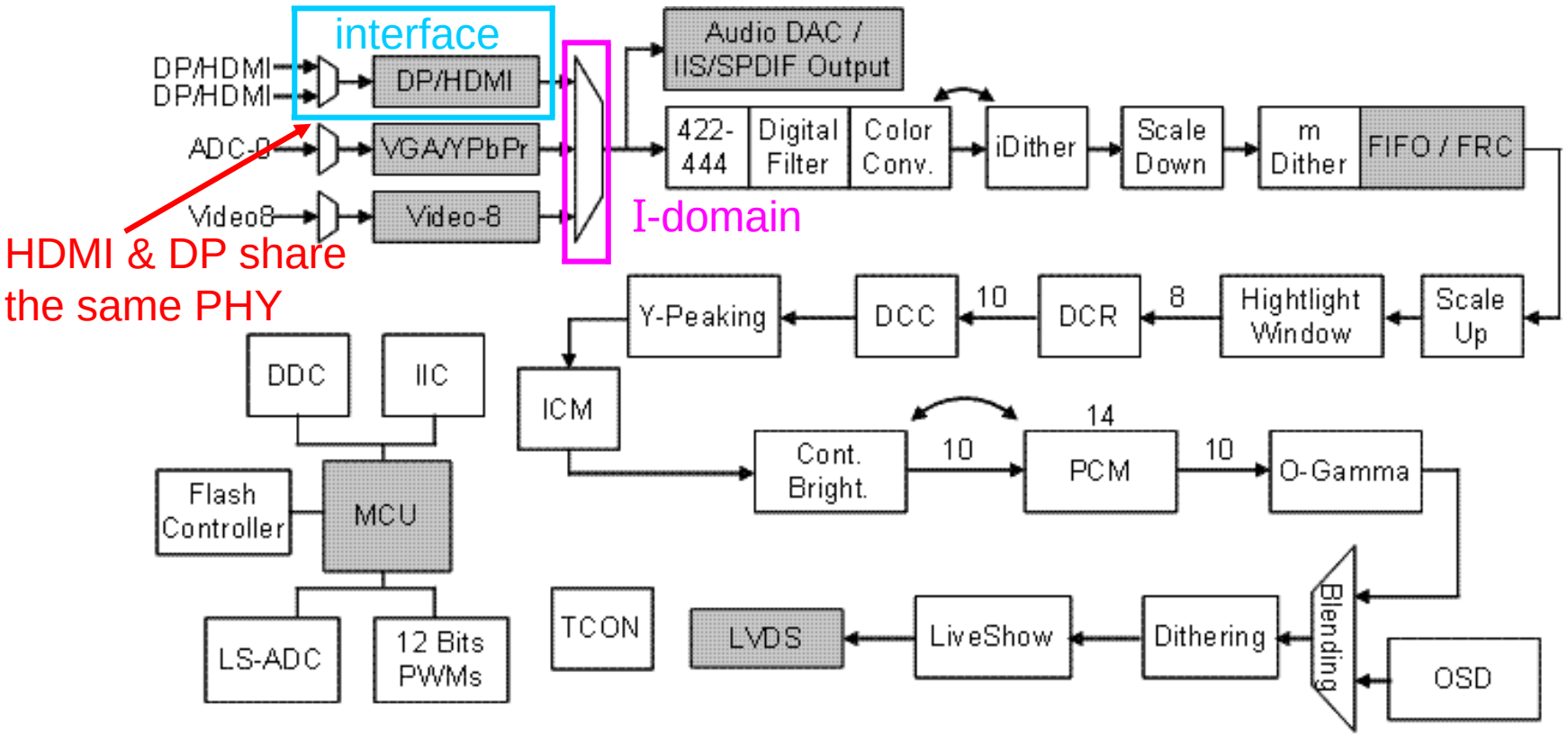
II. Firmware Flow

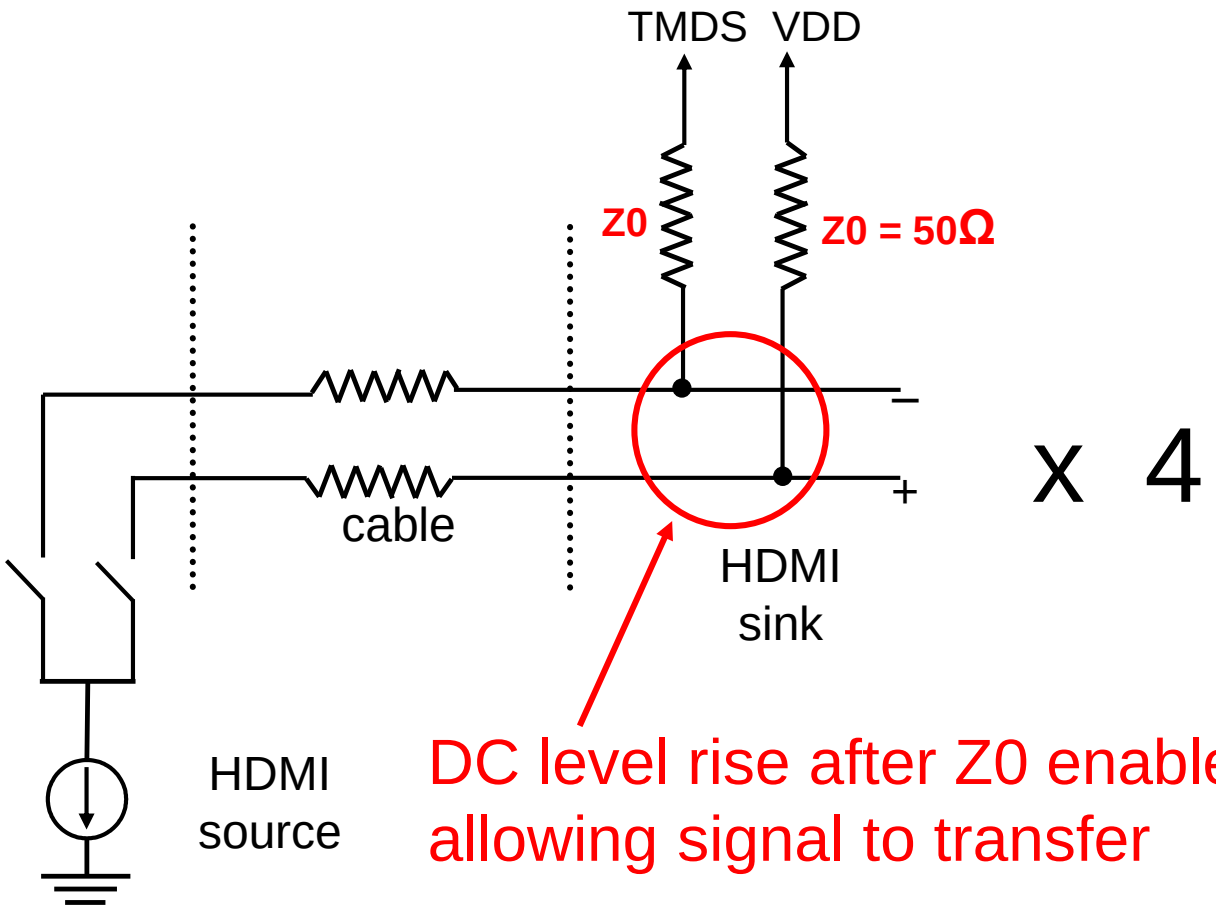
Scaler Data Path



RTD2486 Chip Data Path Block Diagram

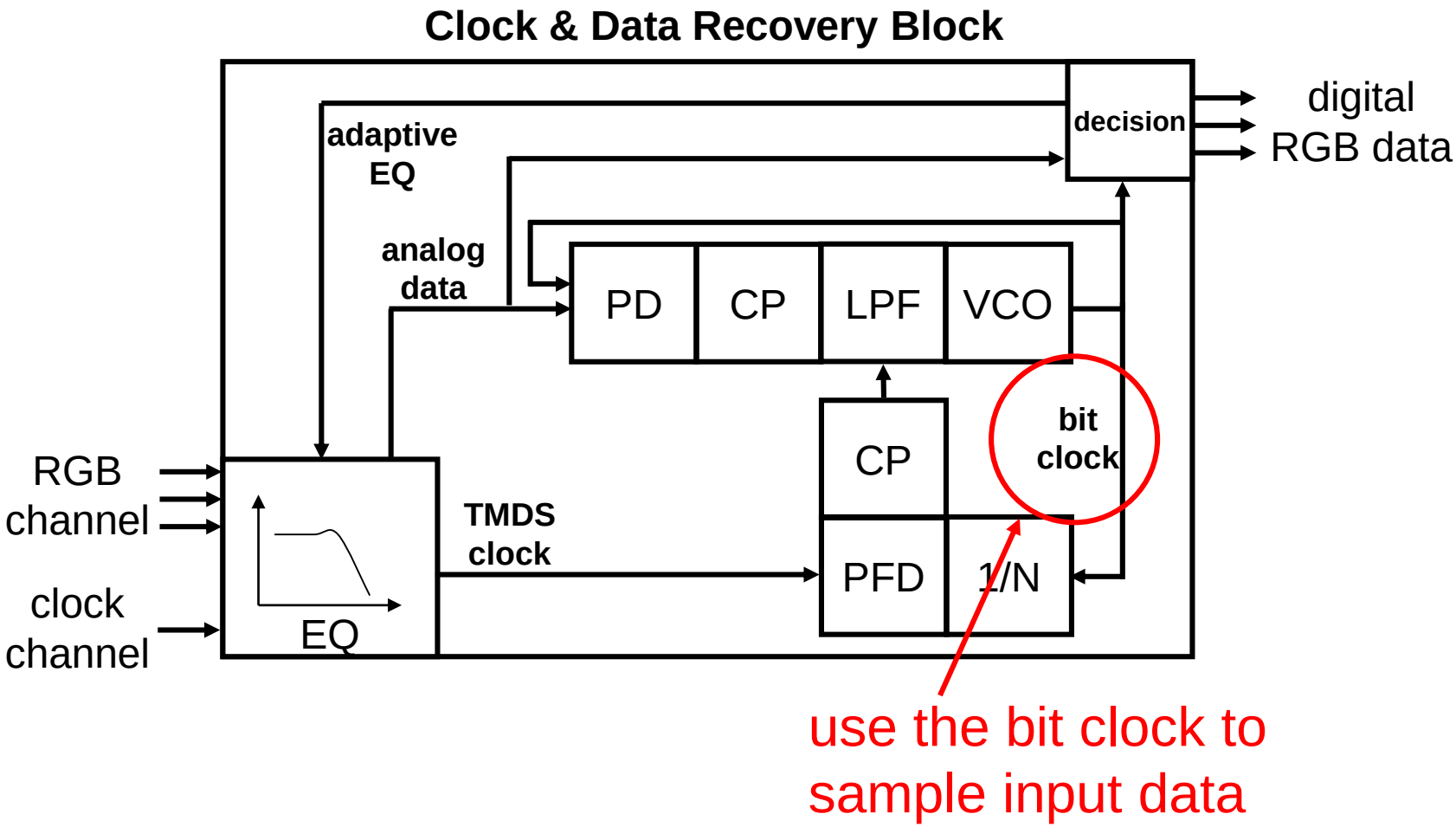
Z0

For each digital port:

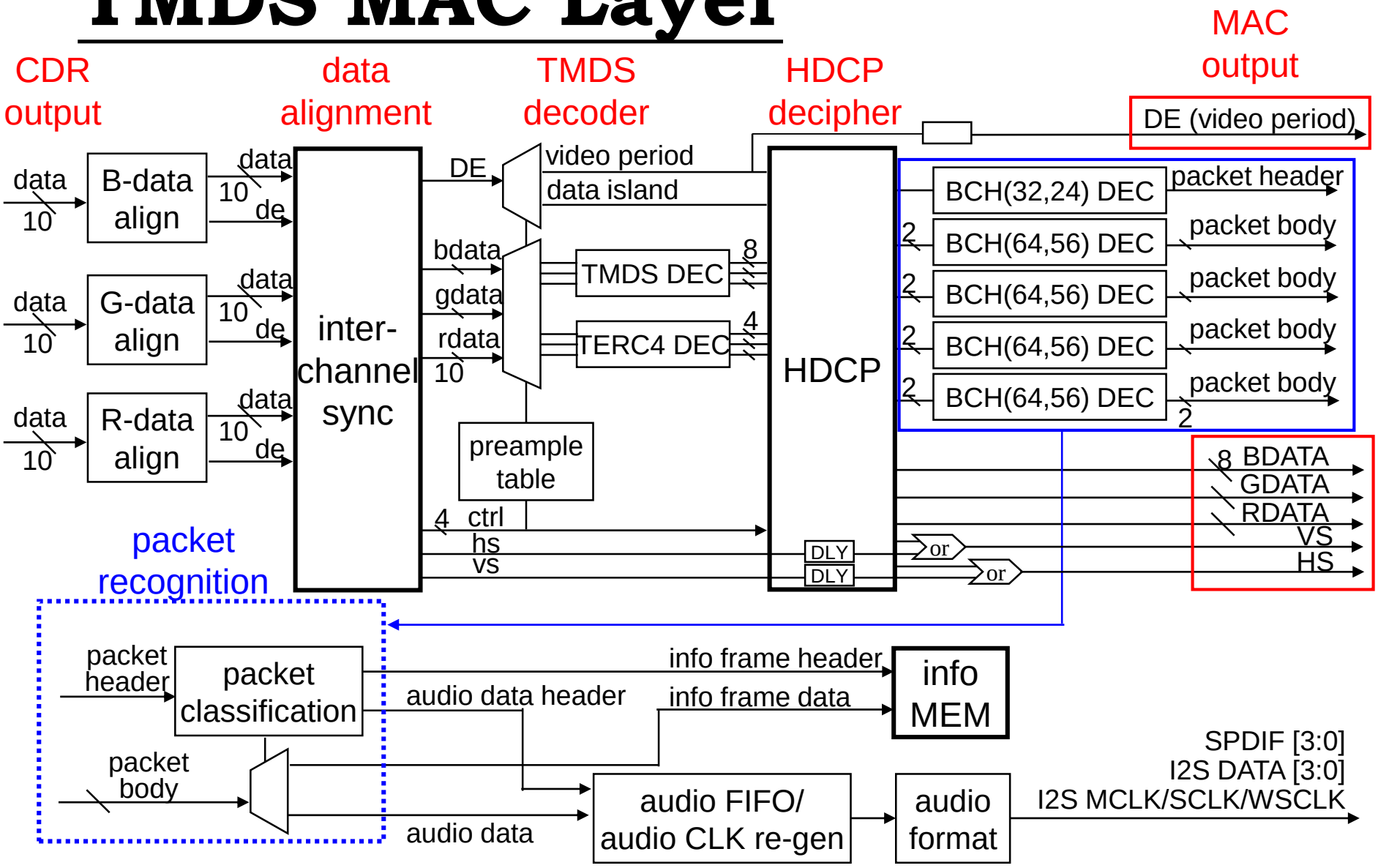


x 4

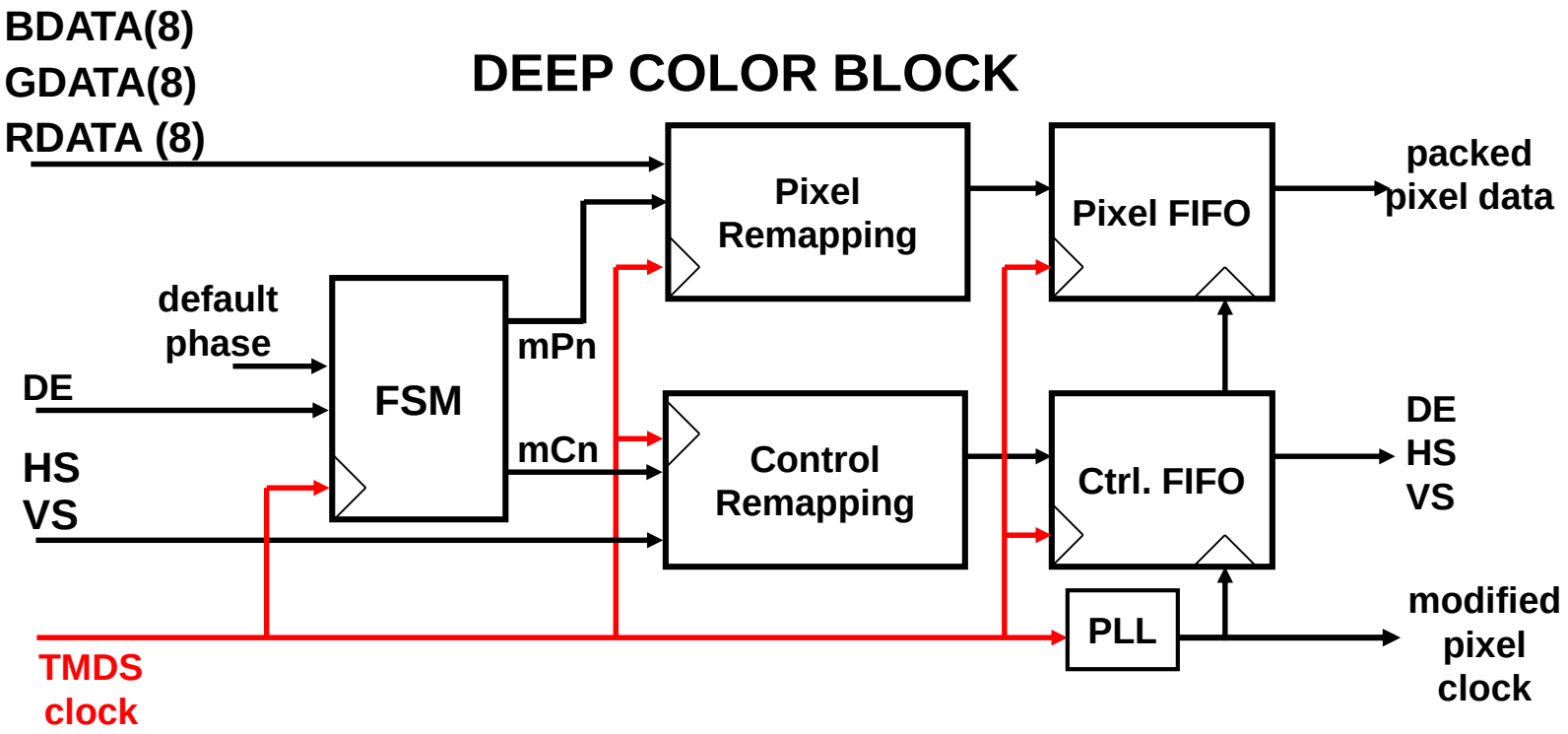
TMDS Physical Layer



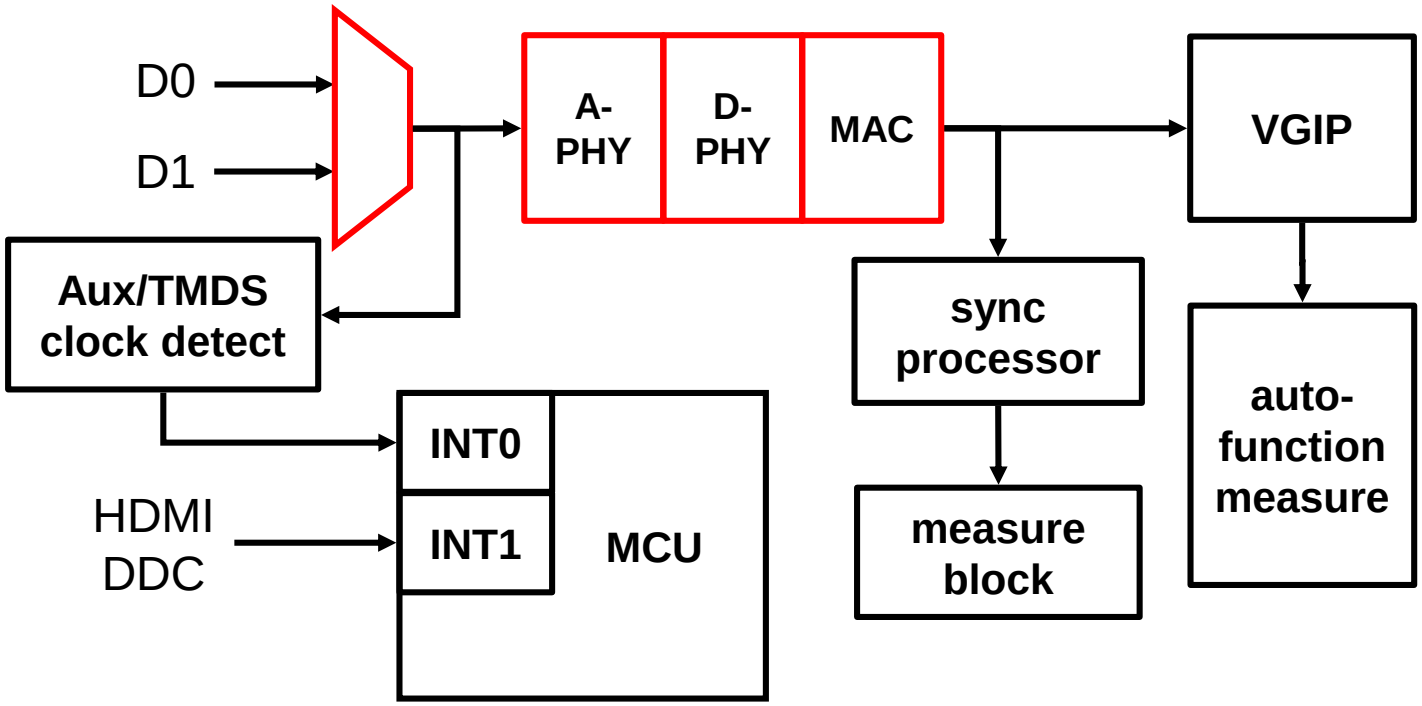
TMDS MAC Layer



Pixel Packing



Detect & Measure Blocks



Outline

I. HDMI Introduction

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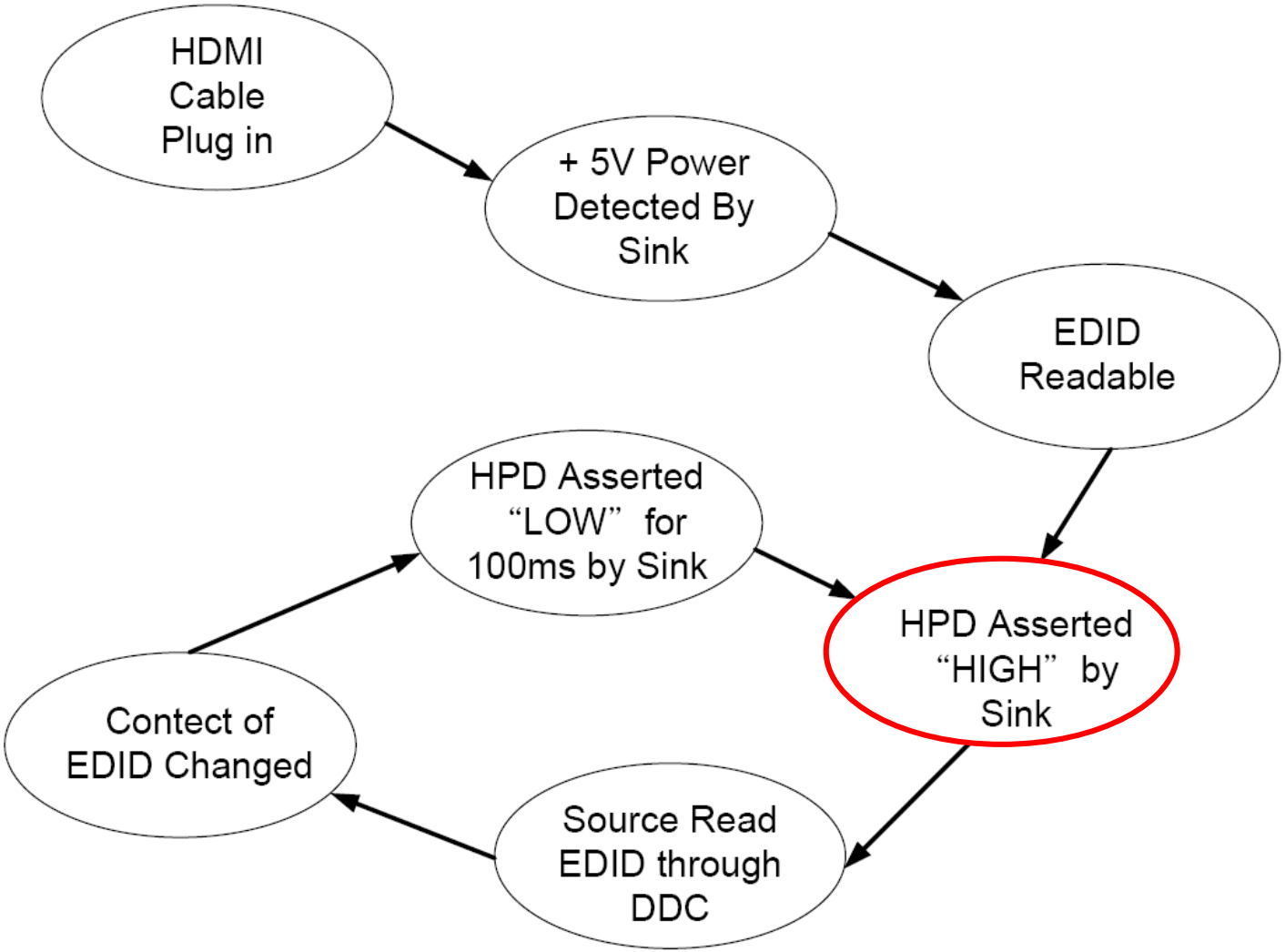
HDMI Signal Flow

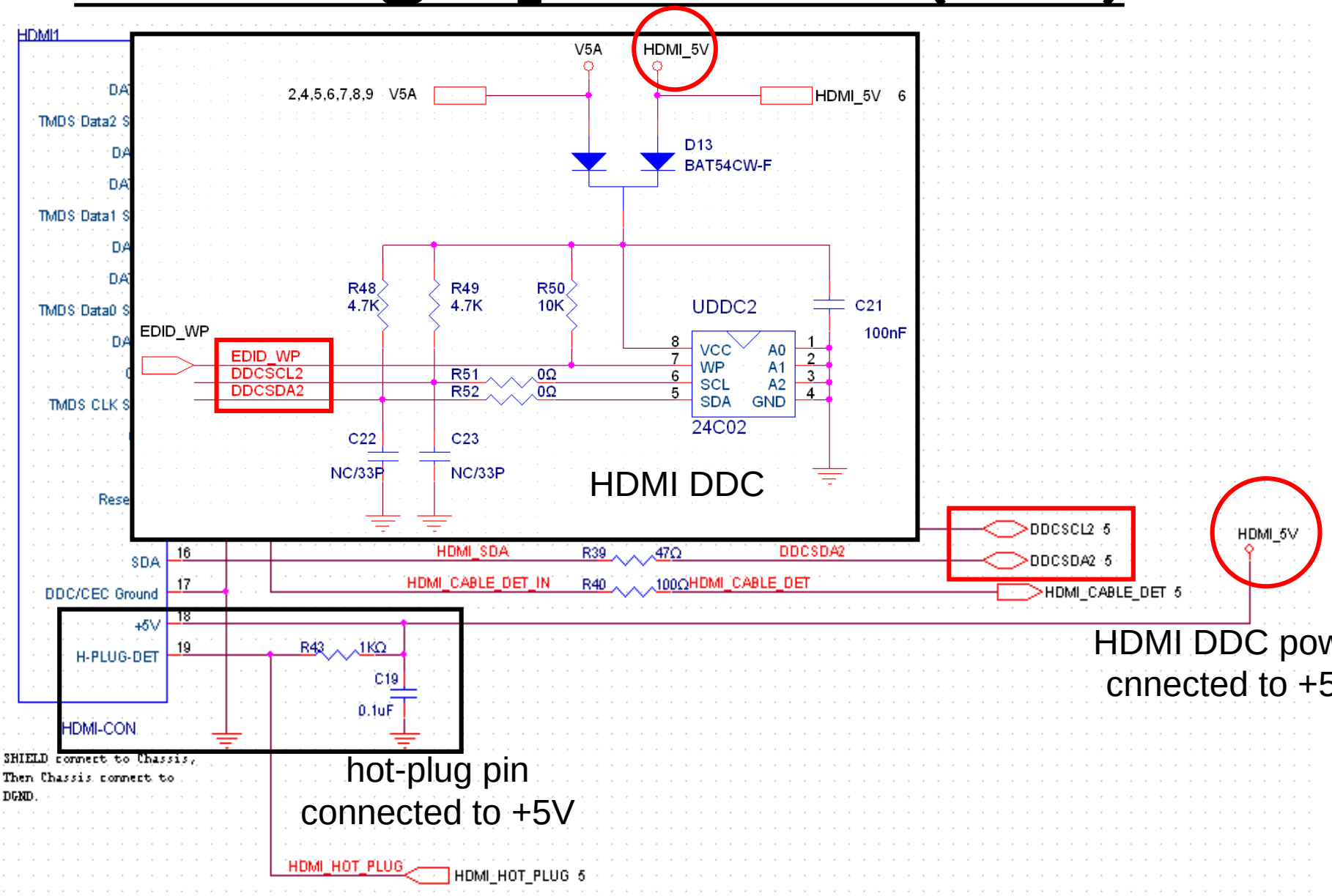
Things need to be done before detecting / measuring:

1. Hot-plug detect → notify HDMI source
2. enable Z0 → allow TMDS signal in
3. HDCP handshaking → for MAC

Hot-Plug Operations (1/2)



Hot-Plug Operations (2/2)



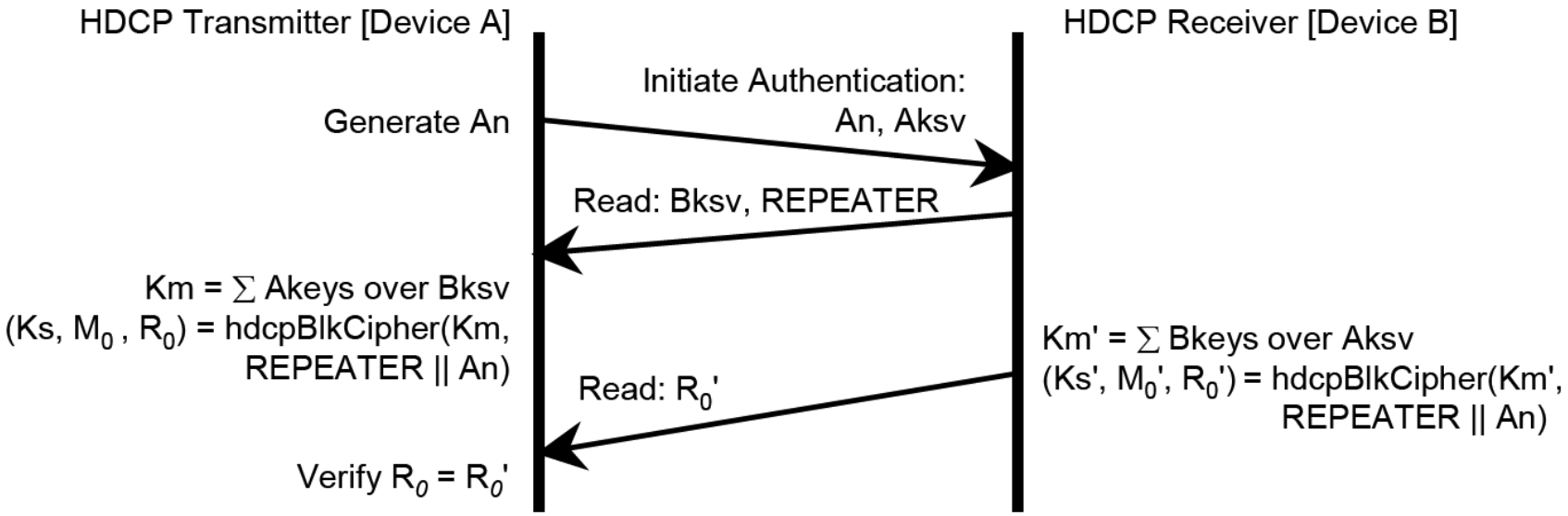
HDMI DDC power cnnected to +5V

hot-plug pin connected to +5V

Enabling ZO


2s 0.0000s Roll Stop 1/ 1 98%
CH1
Coupling
DC1MΩ
Bandwidth
Full
Probe
Auto
Invert
Off On
Next
(1/2)
A: 1 Frequency **********
B: 1 Duty Cycle **********
C: 1 Mean 2.46V
D: Off
Δt=19.2s 1/Δt=52.0mHz Edge 3 DC 1.84V
1: 2.00V DC1MΩ ofs 0.00V
2: 2.00V BW DC1MΩ ofs -4.00V
3: 2.00V DC1MΩ Empty
4: 500mV DC1MΩ Empty
LeCroy f:0.00000Hz 25kS 500k points RTC:2010/12/17 20:56:27

HDCP Handshaking



- An, Aksv would be send anytime
- data needed during handshaking:
  - Bksv (will be reset after power isolation)
  - R0 (100ms after An, Aksv received)

Outline

I. HDMI Introduction

II. **Firmware Flow**

- i. Switch
- ii. Pre-detect
- iii. Scan
- iv. Measure

Signal to Timing: Steps

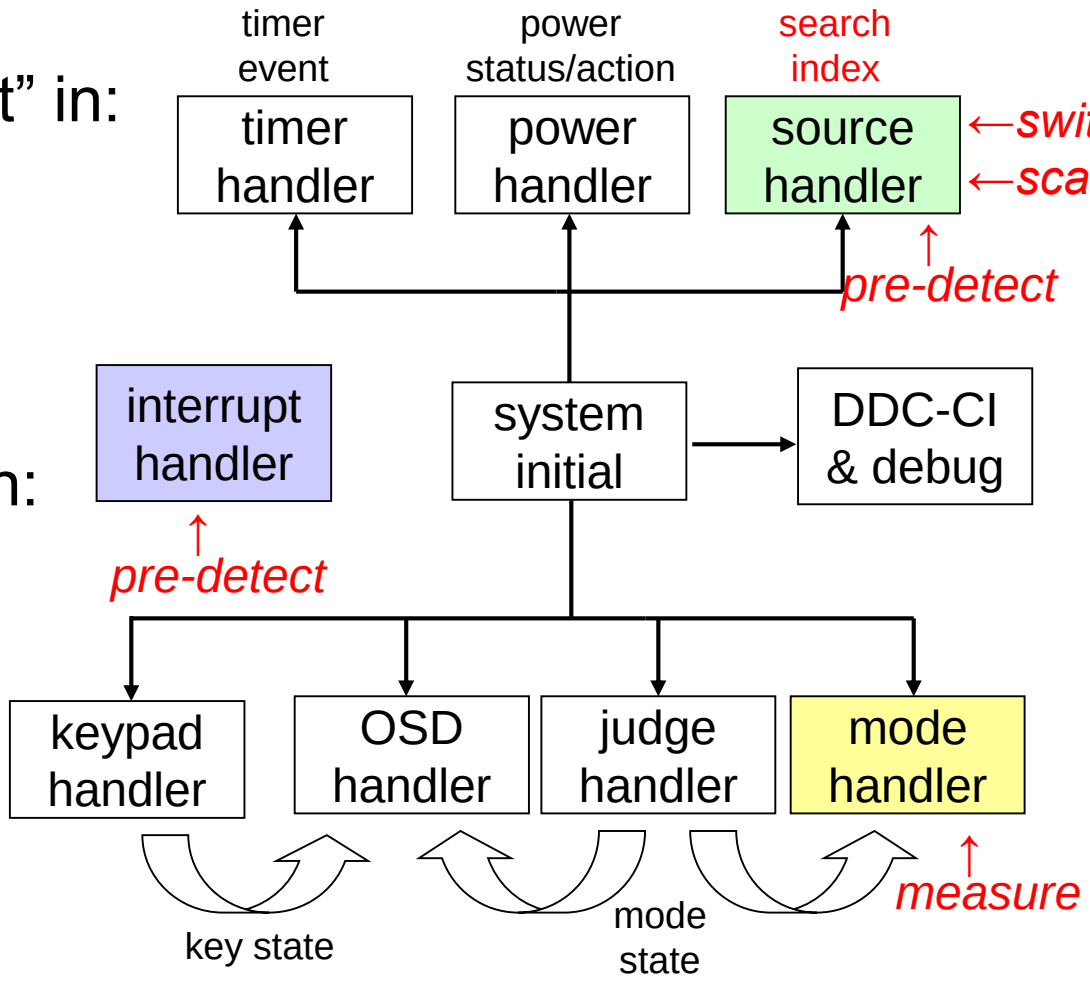
1. **Port switching**
   - switch to a specific digital port
2. **Source pre-detection**
   - detect the signal status by interrupts
3. **Input port scan**
   - get & set the input video formats
4. **Timing measurement**
   - measure HS, VS & DE

System Layer: Handlers

MODE STATUS

1. “switch / pre-detect” in:
   - power saving
   - no signal
   - no support

2. “scan / measure” in:
   - search



Outline

I. HDMI Introduction

II. Firmware Flow

i. Switch

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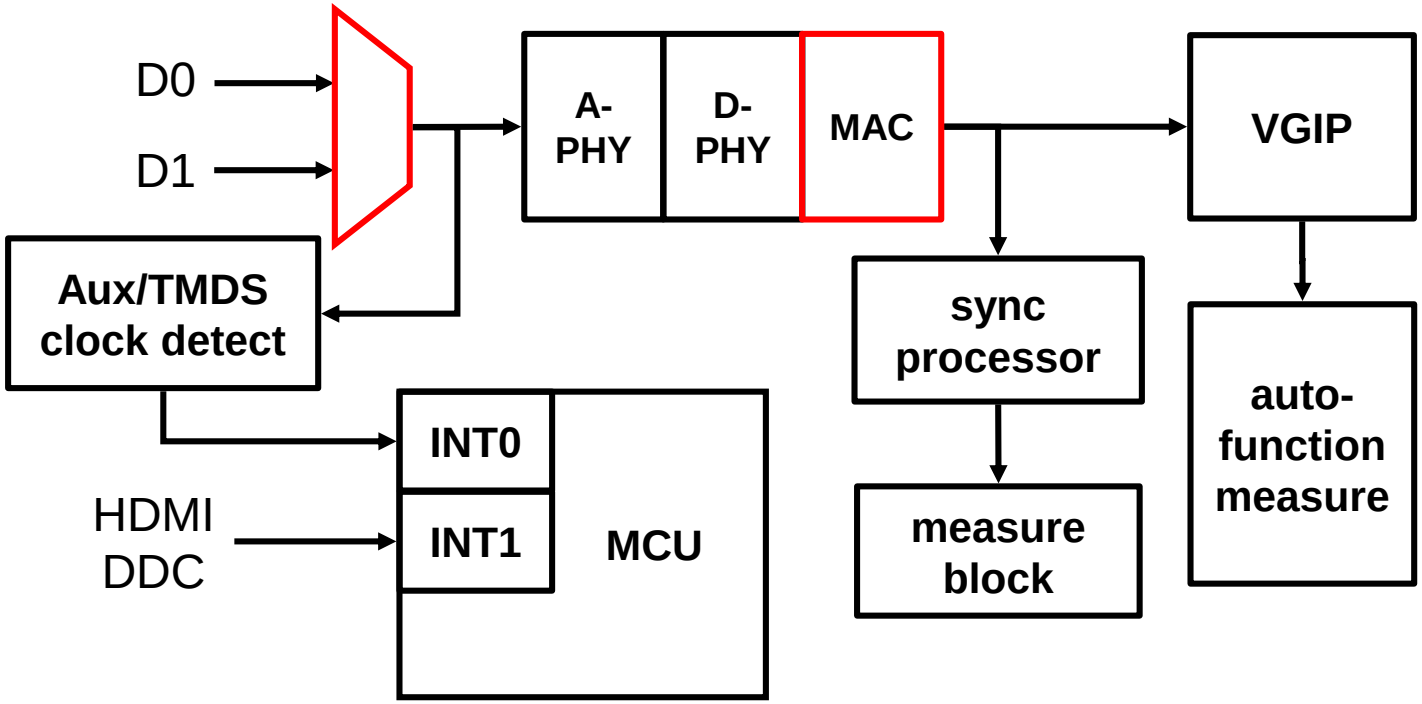
Port Switch

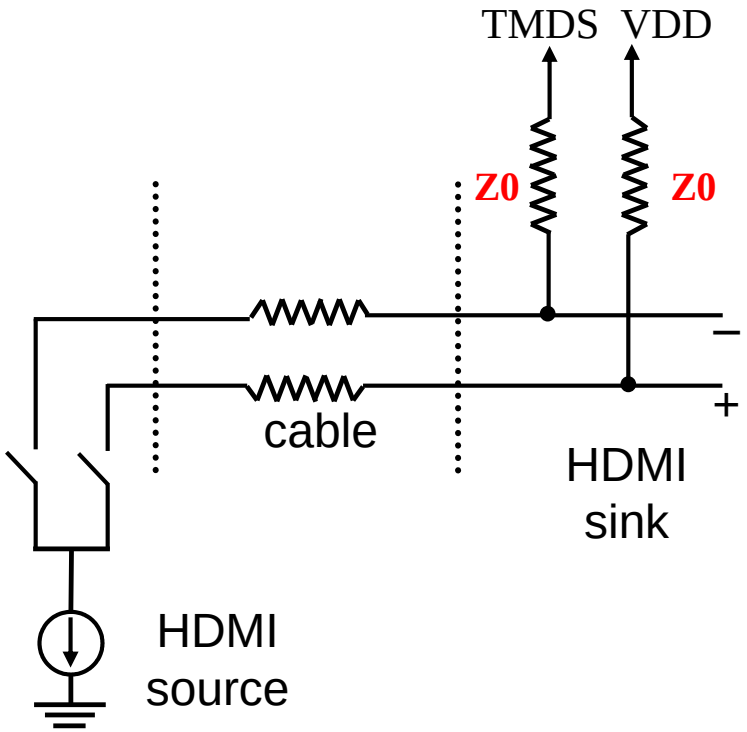
1. switch digital ports by "*search index*"
   - updated by the source handler
2. initialize TMDS for HDMI



Port Switch: To Digital Ports

Enable digital port

1. switch digital PHY to HDMI (PB, E0[4])
2. enable TMDS clock Rx (PB, B4[3])
3. enable Z0
4. 2D switch (PB, B5[2])



Disable analog port

– disable ADC/APLL

Port Switch: MAC Initial

1. disable TMDS output
2. Set DE-only mode HS/VS
3. set deep color auto-detect
4. enable BCH detection
5. enable packet variation detect
6. HDCP setting
   - select DDC channel
   - set HDCP feature
7. switch to HDMI
8. enable R, G, B, and clock input
9. swap ADC channel if needed
10. switch to DVI mode if no signal detected
11. Set DVI / HDMI detect conditions
12. enable error correction

Port Switch: Interrupt Setting

INT1

– enabled with Z0

INT0

– enabled while initializing TMDS

– starts with “stable IRQ”

– measure the TMDS clock

Outline

I. HDMI Introduction

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i. Switch

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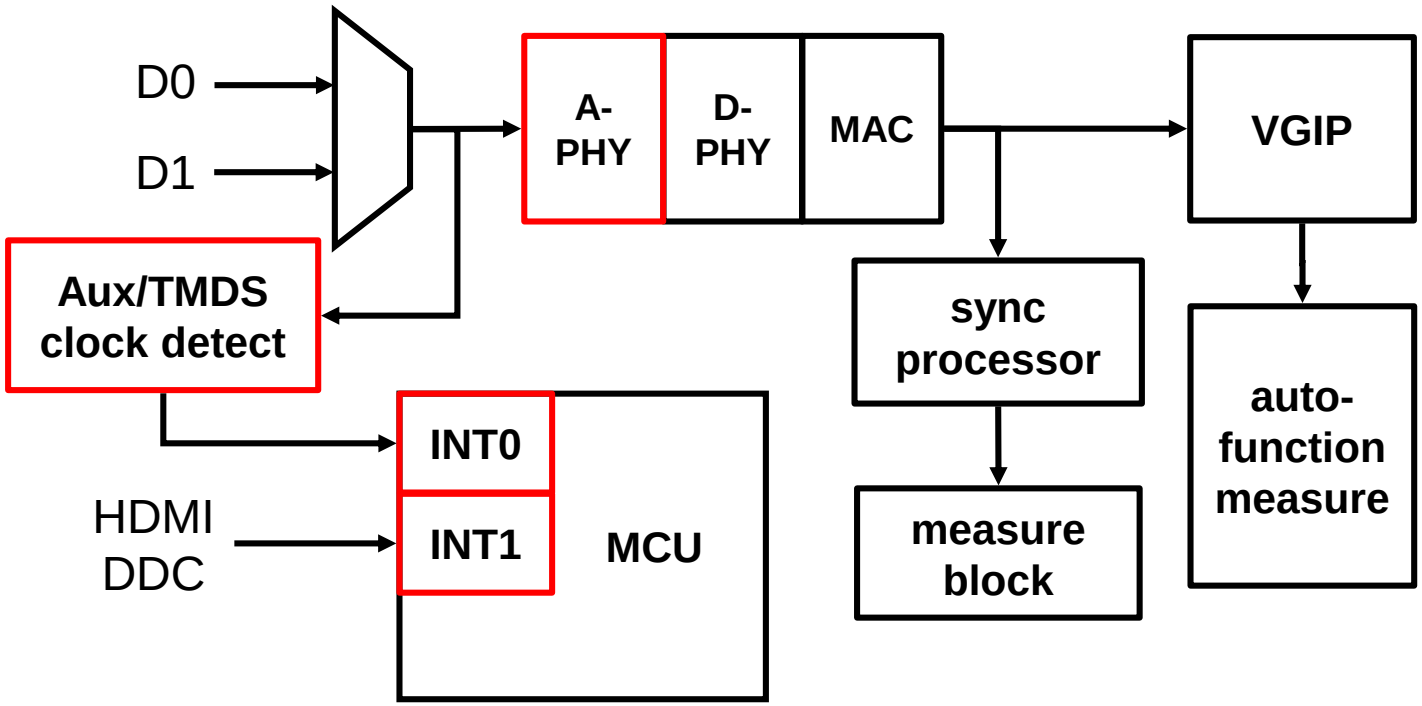
iv. Measure

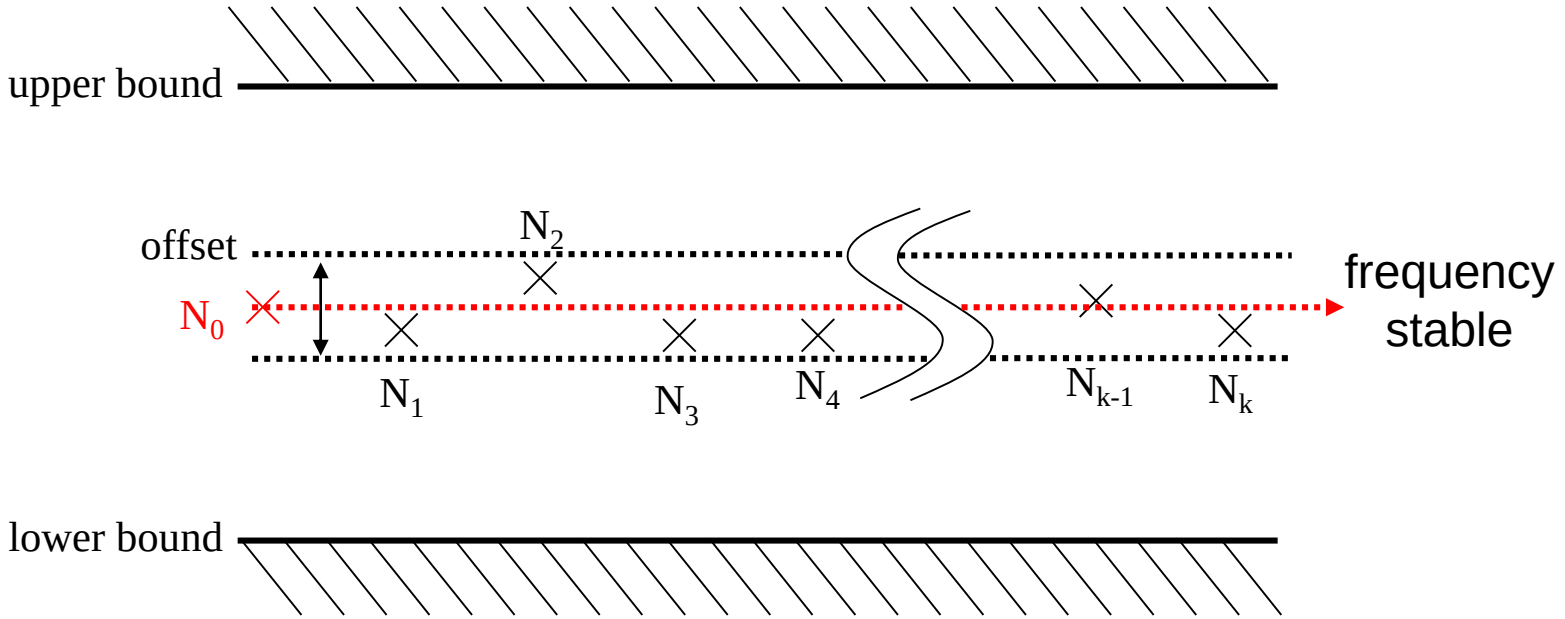
Pre-Detect

1. monitor TMDS clock stability (INT0)
2. monitor DDC channel behaviors (INT1)



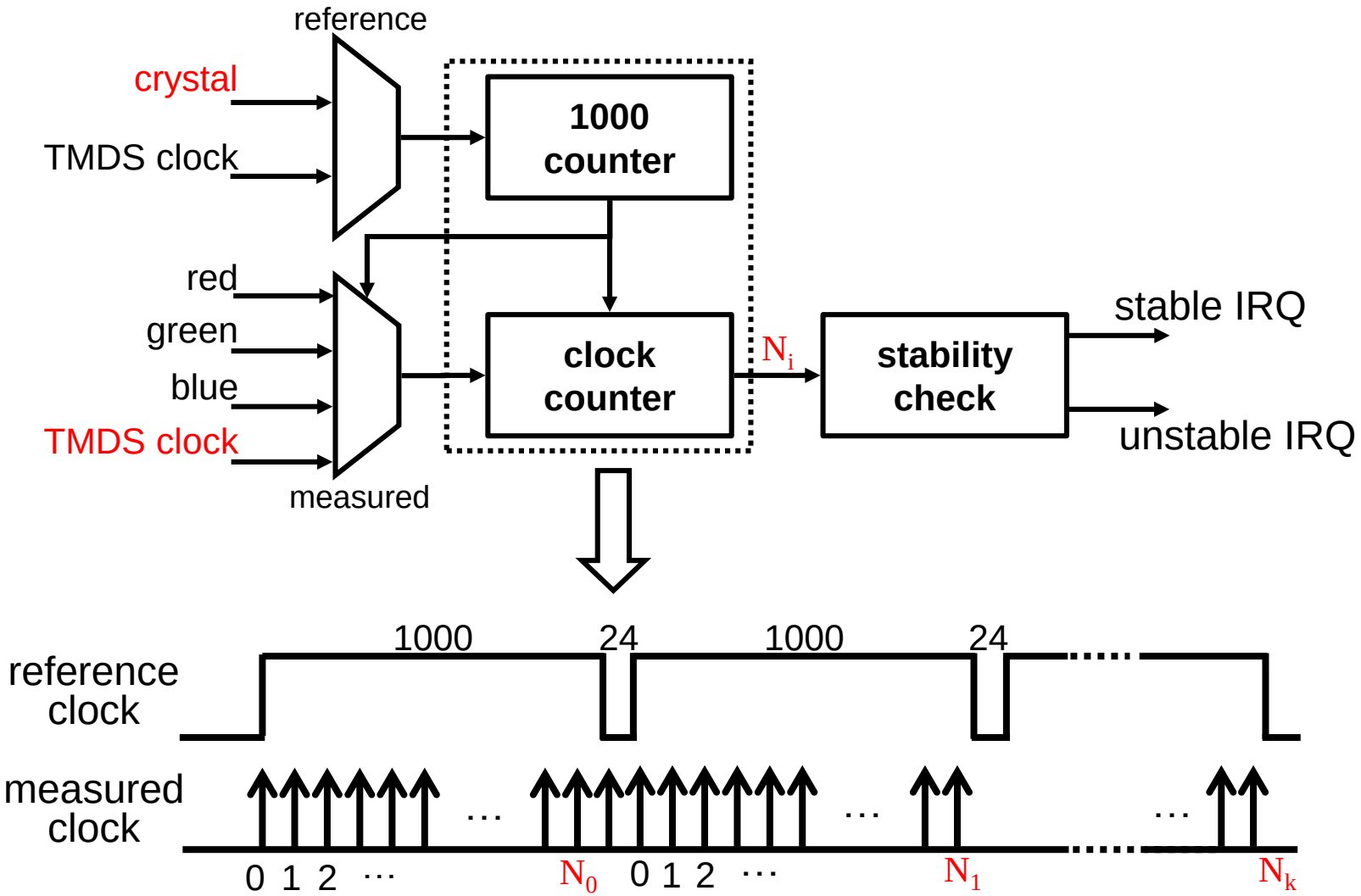
Clock Detect: Stable or Not?

N_i = TMDS clock frequency, measure(i)



Frequency unstable, if not stable.

Clock Detect: Blocks



Clock Detect: Stability Check

- **the measured clock is stable if:**

$$\forall i \in [1, \text{stabletimes}], N_i \in [\text{threshold}] \bigcap [N_0 \pm \text{var}]$$

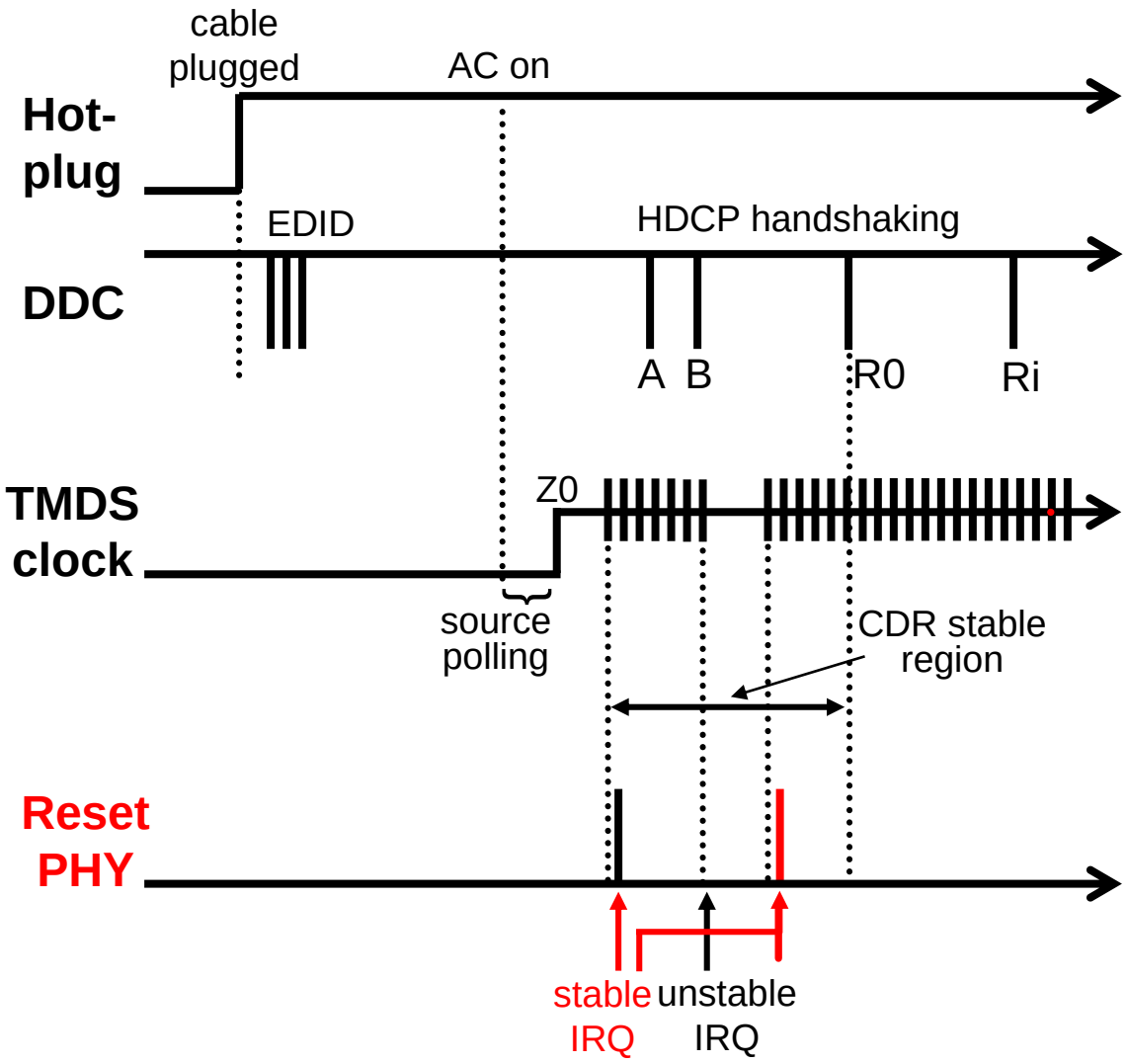
parameter	description	default setting
upper bound	N_i threshold	$1000 \times \frac{340\text{M}}{f_{\text{Xtal}}} \frac{1+4\%}{1-10\%}$
lower bound		$1000 \times \frac{25\text{M}}{f_{\text{Xtal}}} \frac{1-4\%}{1+10\%}$
offset	N_i variation	$\pm 127 \times \frac{f_{\text{Xtal}}}{1000}(\text{Hz})$
stable times	duration before stable	$127 \times 1024 \times (f_{\text{Xtal}})^{-1} \approx 5\text{ms}$

- **interrupt quest types (bind to INT0)**
  - –stable IRQ (default) (enabled in P2, 0xEF[7])
  - –unstable IRQ (enabled in P2, 0xE6[1])

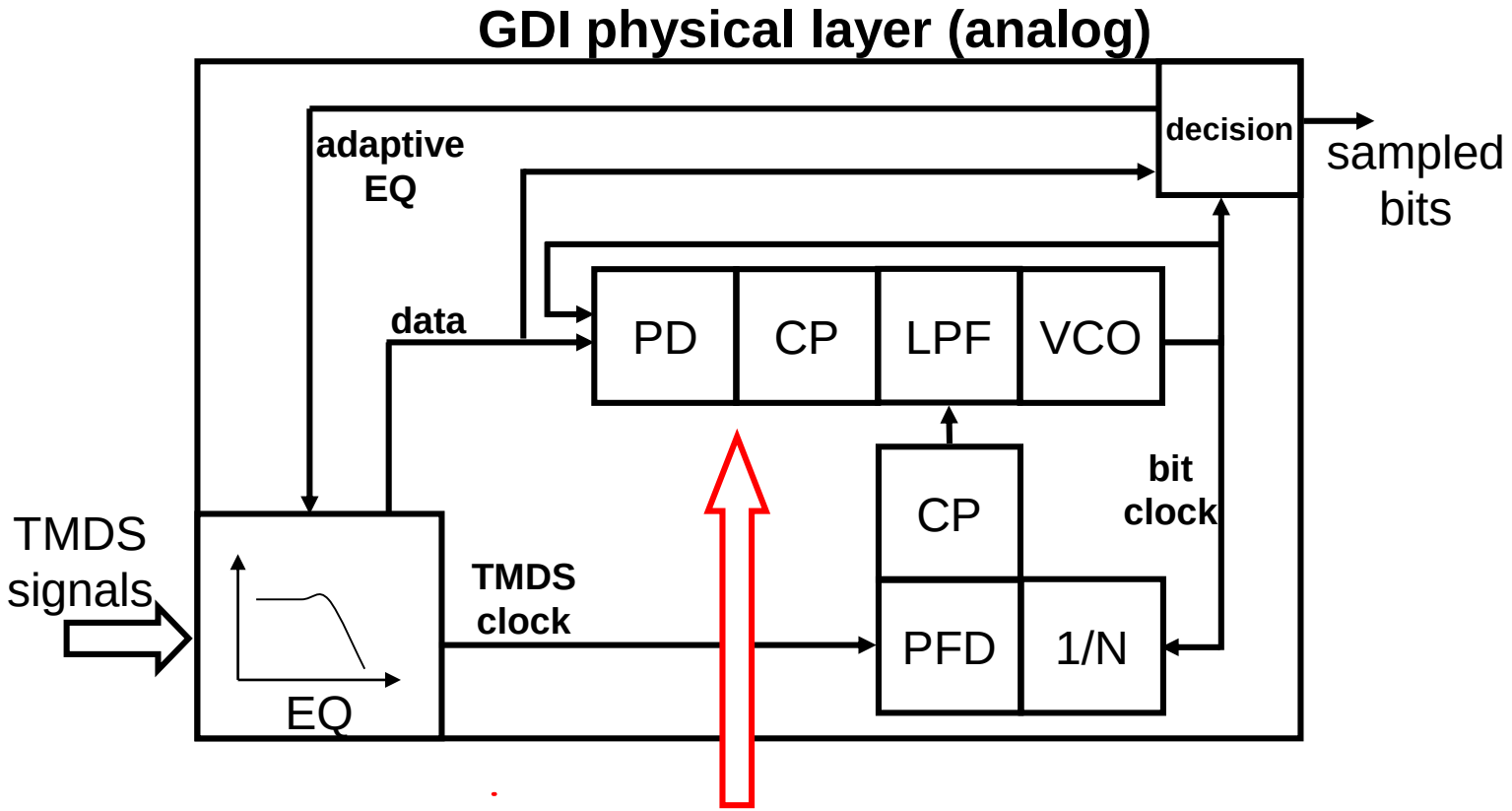
Clock Detect: What For?

- If the TMDS clock is stable:
  - a valid input signal present
  - adjust CDR accordingly, if necessary
- If the TMDS clock is unstable:
  - no valid input signal
  - pre-detection & port scan fail
- stable/unstable IRQ happens alternatively

Pre-Detect: INT0 Timing



TMDS Analog PHY (1/2)



	AEQ	PD	CP	LPF	VCO
lower speed	weak	linear full rate	current↓	R↑	divider ↑
higher speed	strong	binary half rate	current↑	R↓	divider ↓

TMDS Analog PHY (2/2)

RESET PHY

1. measure current TMDS clock
   - reference clock: M2PLL/10 or IOSC
2. set pixel clock rate (unit: 0.1M Hz)
3. set EQ & CDR
   - according to pixel clock rate
4. reset PHY

INT0: TMDS Handler (1/2)

STABLE IRQ

If CDR clock unstable, set PHY.

STEPS

1. switch to “unstable IRQ”
2. if CDR clock unstable:
   - set PHY parameters
   - narrow the clock detect threshold(±1.5%)
3. flag “TMDS_PHY_SET”

INT0: TMDS Handler (2/2)

UNSTABLE IRQ

If TMDS clock unstable, reset the “clock detect” block.

STEPS

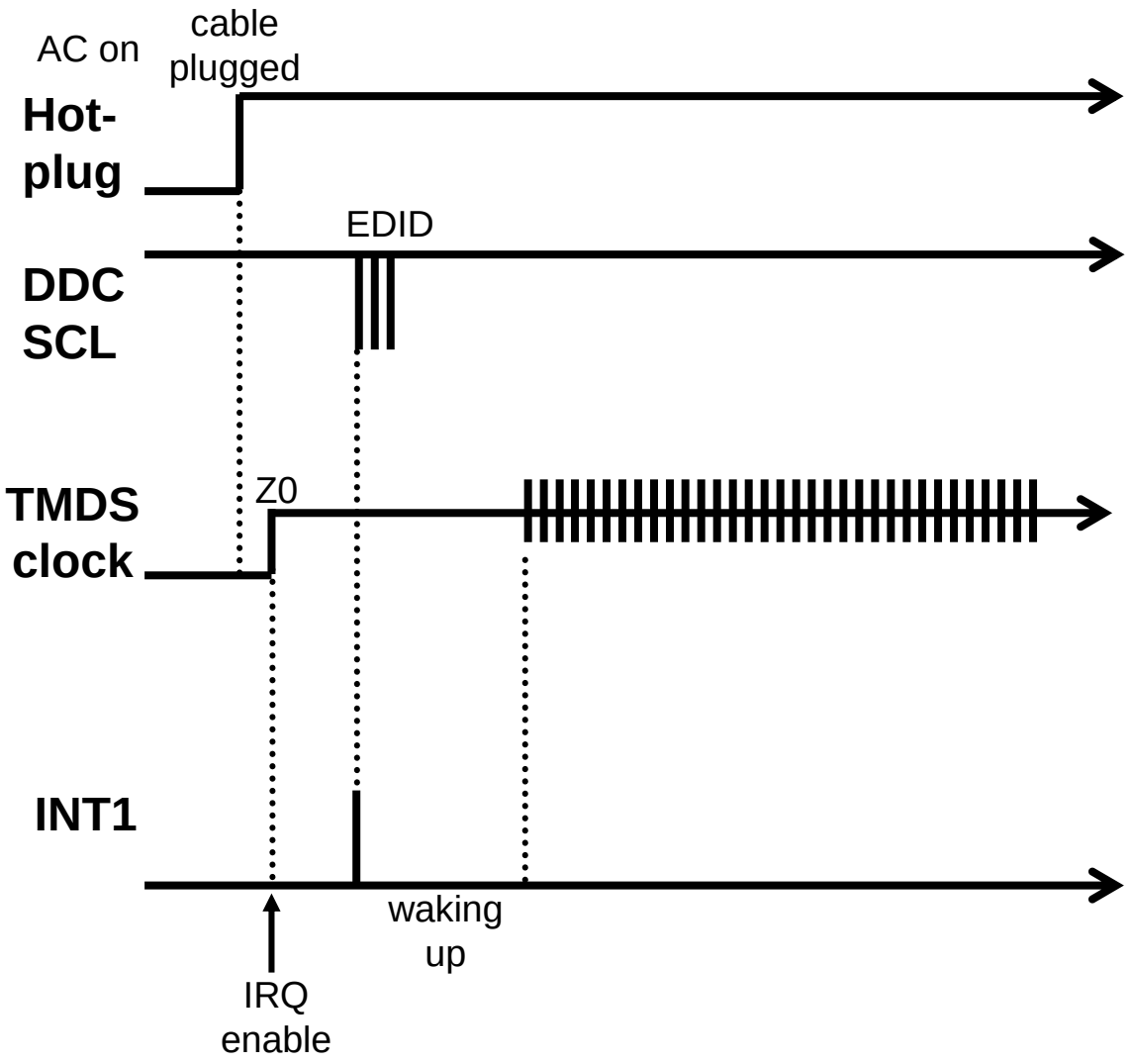
1. switch to “stable IRQ”
2. enlarge the clock detection range
3. clear “TMDS_PHY_SET” flag

Pre-Detect: DDC Interrupt

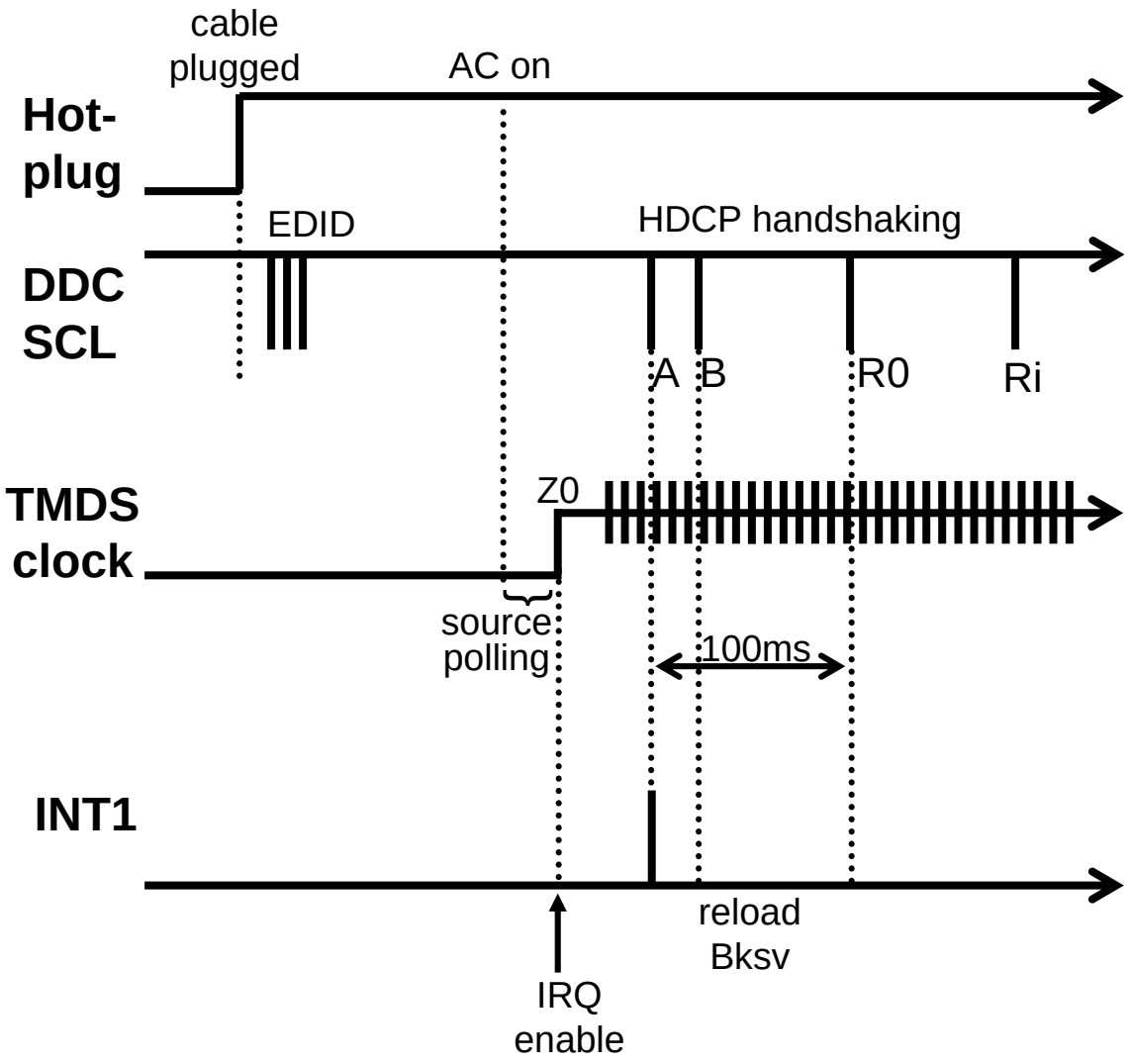
- trigger the “HDMI DDC IRQ”
  - 0xFFE5[3:2], bind to INT1
  - enable -> with Z0 enable
  - disable -> inside INT1 handler

- **WHAT FOR?**
  - catch the EDID read action
  - recover the HDCP key

Pre-Detect: INT1 Timing (1/2)



Pre-Detect: INT1 Timing (2/2)



INT1: Bksv Recovery

TO DO

- reload Bksv for HDCP handshaking
- the faster, the better

STEPS

- reset MCU & Flash clock dividers to 1
- GDI isolation OFF
- reload Bksv from memory
- set HDCP features

Outline

I. HDMI Introduction

II. Firmware Flow

i. Switch

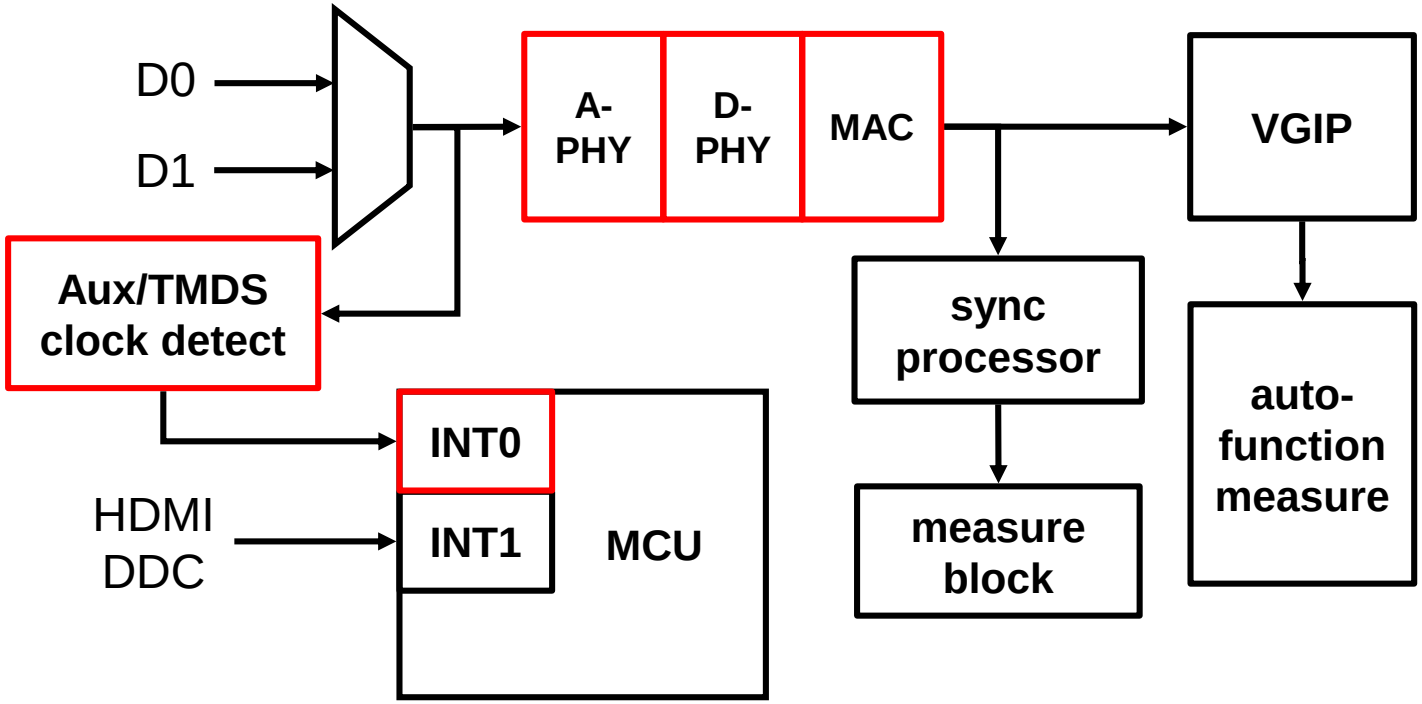
ii. Pre-detect

iii. Scan

iv. Measure

Port Scan

1. check clock stability (PHY)
2. decode pixel & packet data (MAC)



Port Scan: PHY Layer

1. check TMDS clock stability
   - scan fails if unstable

2. check CDR stability
   - if unstable:
     - scan fails
     - reset the clock detect configurations
     - switch to “stable IRQ”

Port Scan: MAC Layer

SCAN STEPS

1. detect signal format
   - HDMI or DVI
2. detect sync. format
   - RGBHV or DE-only
3. detect packet
   - check BCH error
   - video setting
   - deep color setting

AFTERWARDS

1. enable video output
2. enable RGB clock output

HDMI: AVI Info-frame (1/3)

VIDEO FORMAT

- quantization ranges
- aspect
- pixel repetition

COLOR FORMAT

- color space (RGB or YCbCr)
- pixel encoding / packing
- colorimetry

HDMI: AVI Info-frame (2/3)

Packet Byte #	EIA/CEA-861B Byte #	7	6	5	4	3	2	1	0
PB0	N. A.	Checksum							
PB1	Data Byte 1	Rsvd (0)	Y1	Y0	A0	B1	B0	S1	S0
PB2	Data Byte 2	C1	C0	M1	M0	R3	R2	R1	R0
PB3	Data Byte 3	Reserved (0)						SC1	SC0
PB4	Data Byte 4	Rsvd (0)	VIC6	VIC5	VIC4	VIC3	VIC2	VIC1	VIC0
PB5	Data Byte 5	Reserved (0)				PR3	PR2	PR1	PR0
PB6	Data Byte 6	Line Number of End of Top Bar (lower 8 bits)							
PB7	Data Byte 7	Line Number of End of Top Bar (upper 8 bits)							
PB8	Data Byte 8	Line Number of start of Bottom Bar (lower 8 bits)							
PB9	Data Byte 9	Line Number of start of Bottom Bar (upper 8 bits)							
PB10	Data Byte 10	Pixel Number of End of Left Bar (lower 8 bits)							
PB11	Data Byte 11	Pixel Number of End of Left Bar (upper 8 bits)							
PB12	Data Byte 12	Pixel Number of End of Right Bar (lower 8 bits)							
PB13	Data Byte 13	Pixel Number of End of Right Bar (upper 8 bits)							
PB14-PB27	Data Bytes 14-27	Reserved (0)							

HDMI: AVI Info-frame (3/3)

- Y0, Y1 — RGB or YC_BC_R indicator. See EIA/CEA-861B table 8 for details.
- A0 — Active Information Present. See EIA/CEA-861B table 8 for details.
- B0, B1 — Bar Info data valid. See EIA/CEA-861B table 8 for details.
- S0, S1 — Scan Information (i.e. overscan, underscan). See EIA/CEA-861B table 8 for details.
- C0, C1 — Colorimetry (ITU BT.601, BT.709 etc.). See EIA/CEA-861B table 9 for details.
- M0, M1 — Picture Aspect Ratio (4:3, 16:9). See EIA/CEA-861B table 9 for details.
- R0…R3 — Active Format Aspect Ratio. See EIA/CEA-861B table 10 and Annex H for details.
- VIC0…VIC6 — Video Format Identification Code. See EIA/CEA-861B table 13 for details.
- PR0…PR3 — Pixel Repetition factor. See EIA/CEA-861B table 14 for details.
- SC1, SC0 — Non-uniform Picture Scaling. See EIA/CEA-861B table 11 and paragraph on page 58.

Port Scan: Video Setting

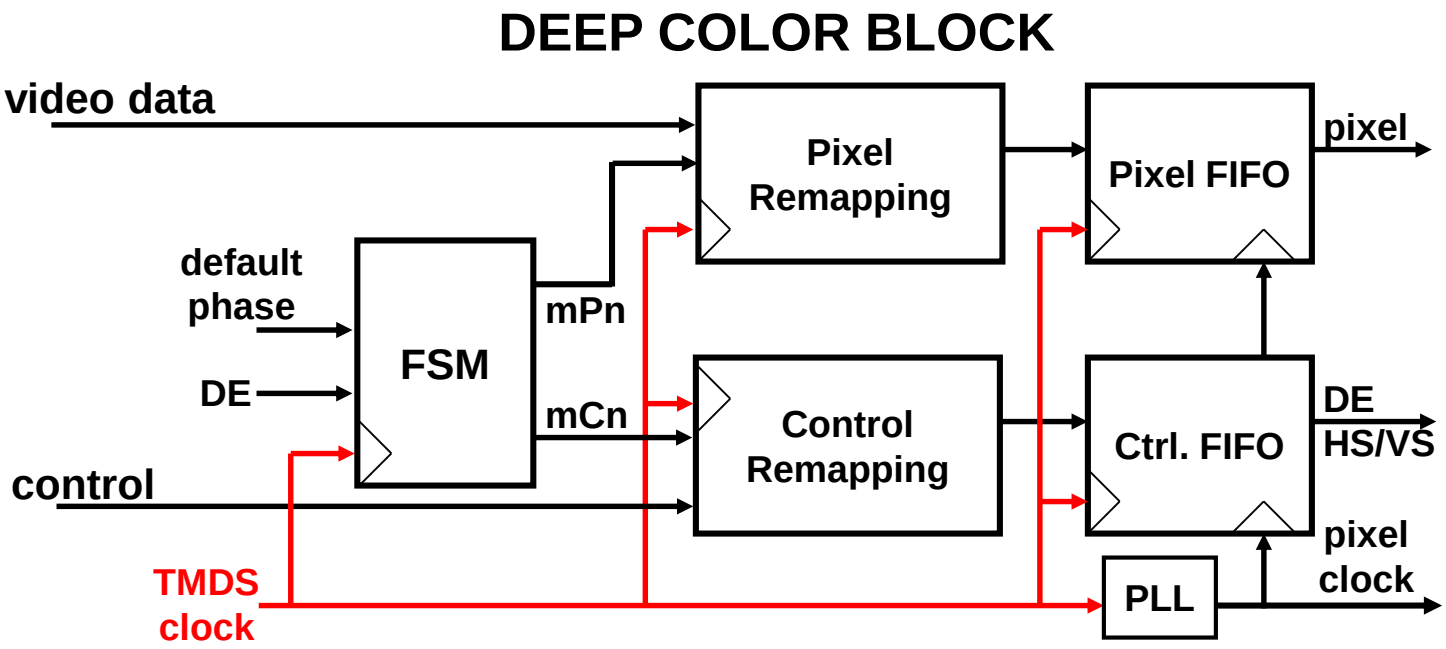
1. set “pixel repetition auto” mode
2. set “color space auto” mode
3. extract from received packet:
   - set color space
   - set extended colorimetry
4. set background color

HDMI: General Control Packet

Byte \ Bit #	7	6	5	4	3	2	1	0
SB0	0	0	0	Clear_AVMUTE	0	0	0	Set_AVMUTE
SB1	PP3	PP2	PP1	PP0	CD3	CD2	CD1	CD0
SB2	0	0	0	0	0	0	0	Default_Phase
SB3	0	0	0	0	0	0	0	0
SB4	0	0	0	0	0	0	0	0
SB5	0	0	0	0	0	0	0	0
SB6	0	0	0	0	0	0	0	0

- Set_AVMUTE [1 bit] Set the AVMUTE flag. (See description below).
- Clear_AVMUTE [1bit] Clear the AVMUTE flag. (See description below).
- PP [4 bits] Pixel Packing Phase. (See description in section 6.5.3.)
- CD [4 bits] Color Depth. (See description in section 6.5.3.)
- Default_Phase [1 bit] Default Phase. (See description in section 6.5.3.)

Deep Color: Setting



1. set color depth & pixel clock rate
2. enable deep color PLL block
3. enable deep color block (P2, B5[7])

Port Scan: Finish

1. set source type to “_SOURCE_HDMI”.
2. Measure input timing info in the Mode Handler.

Outline

I. HDMI Introduction

II. Firmware Flow

i. Switch

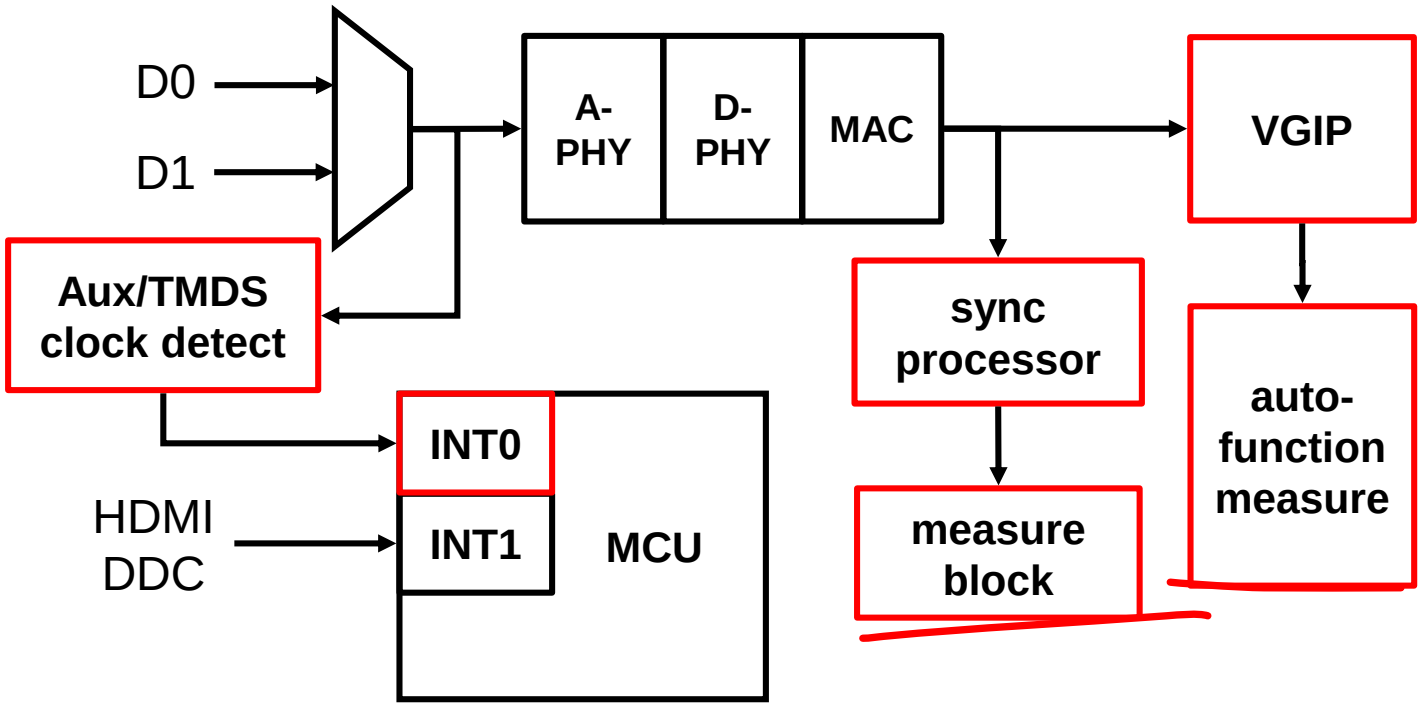
ii. Pre-detect

iii. Scan

iv. Measure

Timing Measurement

1. sync processor measure (HS/VS)
2. auto-function measure (active region)



Timing: Measure Initial

From the “Mode handler”:

1. initial VGIP input by-pass
2. enable on-line sync processor
   - VS timeout: $4096 \times 512 \times (\mathrm{Xtal})^{-1}$
   - from capture window
3. disable VS invert
4. measure source set to TMDS (0x49)

HS/VS Measure: Types

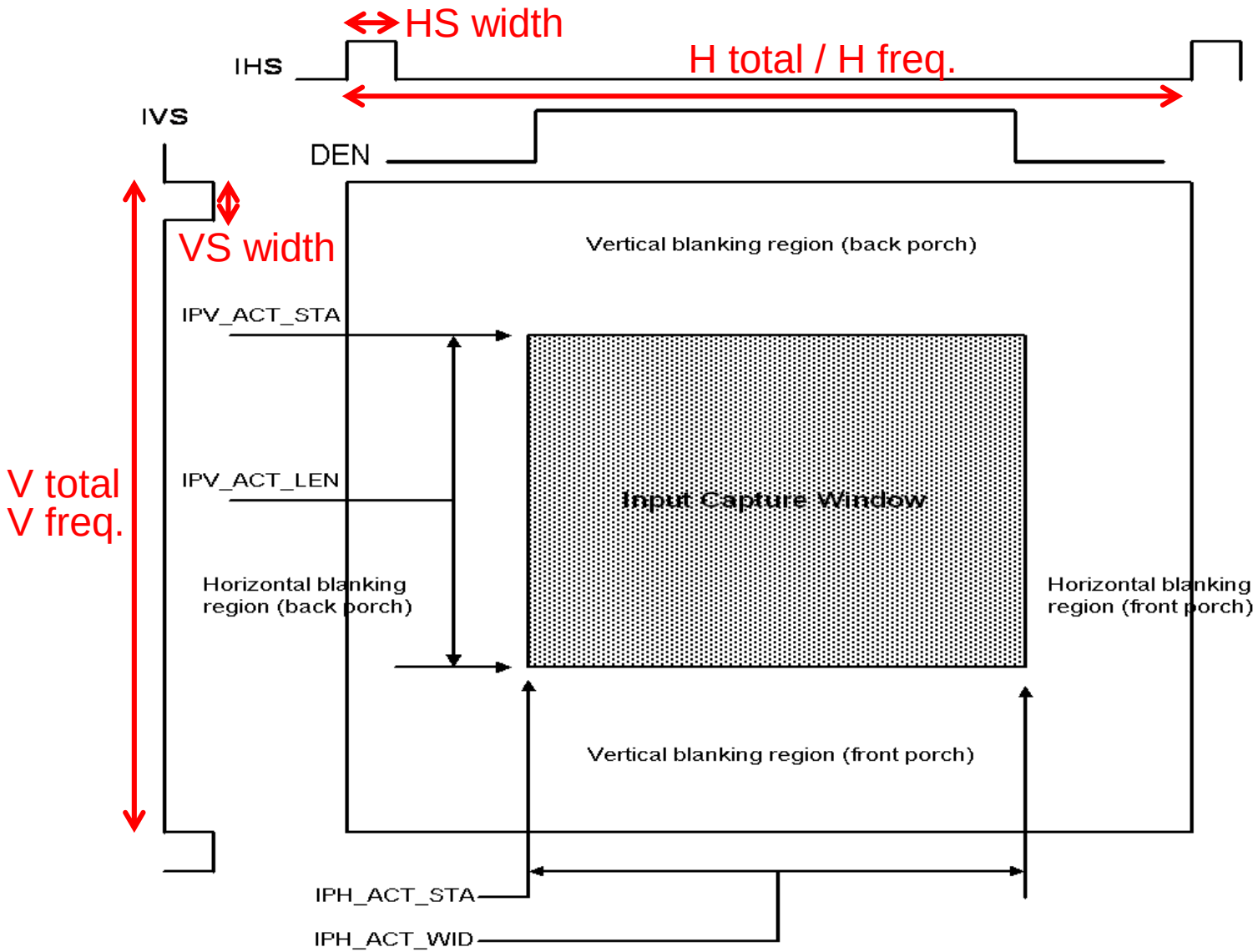
MEASURE LIST

- from analog:
  - HS/VS polarity
  - HS/VS width
  - H/V frequency
  - V total
- from digital:
  - H total

MODE

- analog
  - HS: by crystal clock
  - VS: by HS
- digital
  - HS: by pixel clock
  - VS: by DE

Input Timing: HS & VS



HS/VS Measure: Steps

1. enable on-line measure (0x52[7])
2. measure fails if:
   i. measuring one-frame timeout (0x50[7])
   ii. HS period measure overflow (0x52[4])
   iii. VS period measure overflow or timeout (0x54[5:4])
3. pop-out results (0x52[6])

Active Region Measure

MEASURE LIST

- H/V start
- H width
- V height

STEPS

1. set H / V boundary
   - 0x0002 to H/V total
2. start auto-function measure (0x7D)
   - digital mode
3. return measured data

Input Timing: Active Region