The **most prominent Key Language Uses** in grades 9-12 are the basis for its **Language Expectations.** They are marked with a filled-in circle (●) in the boxes of the table below. The half-filled circle and the open circle indicate lesser degrees of prominence of each Key Language Use; see the legend underneath the table.

Distribution of Key Language Uses in Grades 9-12				
WIDA ELD Standard	**Narrate**	**Inform**	**Explain**	**Argue**
1. Language for Social and Instructional Purposes	●	●	●	●
2. Language for Language Arts	●	●	◐	●
3. Language for Mathematics	○	◐	●	●
4. Language for Science	○	◐	●	●
5. Language for Social Studies	◐	○	●	●

● Most Prominent ◐ Prominent ○ Present

Class 1

The resurgence of chipmaking in Silicon Valley is being driven by the rapid rise of artificial AI and the growing demand for computational power. Rooted in the early innovations of semiconductors, such as transistors and integrated circuits, the chip industry has revolutionized modern computing. However, the exponential growth predicted by Moore's and Dennard's laws has encountered physical and technological limits, necessitating innovative approaches to sustain performance improvements and meet increasing demands.

At the heart of chipmaking are transistors, whose logic gates play an essential role in computation. According to Moore's and Dennard's laws, smaller transistors not only reduce unit costs but also improve performance. Yet, the industry faces a "power wall," where leakage currents impose limitations on the speed and efficiency of smaller transistors. To overcome this barrier, researchers are exploring alternatives, including abandoning traditional transistor structures and adopting new materials for chip fabrication.

As chips become smaller and more intricate, packaging has emerged as a critical technology for enhancing energy efficiency and computing power. Innovations such as placing power lines below transistors or packaging smaller chiplets together have pushed design and engineering boundaries. Additional technologies, such as organic components, 3D packaging, and light cables, aim to further increase efficiency. The ultimate goal is to create layered chips, akin to skyscrapers, capable of maximizing performance while minimizing energy consumption. These advances in packaging and materials are pivotal in meeting the computational demands of AI technologies.

The training of AI models, particularly large-scale neural networks, has highlighted the need for powerful and efficient chips. Traditional CPUs are often inefficient, as significant time is wasted shuttling data between cores and memory during matrix multiplication—the core operation in deep learning. GPUs, originally designed for image processing, have proven superior due to their ability to parallelize thousands of cores. Building on this concept, specialized chips like TPUs (Tensor Processing Units) have been developed explicitly for deep learning tasks. Companies are also exploring solutions such as 16-bit data usage and algorithmic optimization to further enhance efficiency. This trend toward custom chips for AI tasks underscores the growing intersection of hardware and software development.

Traditional computing methods are increasingly energy-intensive, particularly for AI applications. This has led to the emergence of alternative designs inspired by the structure of the human brain. Analog computing, which activates memory only when high current or voltage is needed, significantly reduces energy consumption and speeds up processing. Optical computing, based on Mach-Zehnder Interferometers (MZIs), offers promising capabilities for running neural networks efficiently. While these technologies still require integration with digital systems, their potential to dominate in an AI-driven era, where speed often outweighs precision, is becoming evident.

Over the past five decades, the chipmaking industry has achieved remarkable progress under Moore's law. However, as the law reaches its physical limits, the industry is adapting to sustain exponential gains in performance. The decline of traditional CPUs and the rise of specialized chips designed for specific software tasks mark a significant shift. As companies increasingly integrate control over both hardware and software, the future promises a far more powerful and efficient ecosystem than the legacy Wintel world.

Class 2

In the 1950s and 1960s, silicon-based chips emerged, replacing transistors as the core of computers and continuing to develop according to Moore's Law. However, in the 1980s, the spotlight shifted to software engineering, which gained significant attention, leading to a decline in the perceived importance of silicon-based chips. With the bursting of the Internet bubble and the rapid development of AI, silicon-based chips regained attention and returned to the forefront of the computer field. Despite these shifts, the primary concern of the chip industry has remained constant: ensuring exponential growth in chip performance.

Machines operating in extreme environments are used in chip manufacturing, highlighting the dynamic nature of the semiconductor industry. Electronic components in chips are becoming smaller, while the facilities producing them are becoming larger and more expensive. In the 19th century, it was discovered that smaller transistors contributed to lower unit costs and better performance. However, as chip sizes reached 90nm, quantum effects began to appear, requiring higher power to avoid them. To prevent current leakage, a new transistor structure known as "finFETs" was adopted. Despite these advancements, the need for further miniaturization persists. New 2D materials, such as transition metal chalcogenides (TMDs) and carbon nanotubes (CNTs), have shown potential to replace silicon.

Generally speaking, increasing the number of transistors on a chip is the most direct solution to improving chip performance. However, the size of transistors can no longer be reduced, and the volume of chips is also difficult to increase. As a result, packaging has become increasingly important. To more efficiently utilize chip area, backside power delivery and chiplets are used and assembled together during packaging. Achieving Moore's Law's goal of chips with one trillion transistors by the 2030s will require smarter and more sophisticated designs.

To meet the high demand for AI, specialized chips like GPUs and TPUs have been designed, offering better performance than CPUs by focusing on specific tasks. Both large firms and startups are increasingly investing in this technology. Efficiency can also be improved through algorithm optimization, such as using lower-precision numbers without sacrificing accuracy and removing irrelevant zeros from neural networks. However, this can pose challenges for chip designers, as hardware updates occur much slower than software updates.

Researchers are exploring alternative computing architectures to address the "von Neumann bottleneck," where processor performance outpaces memory access speed, particularly for AI applications. Neuromorphic computing, inspired by the human brain's parallel processing and energy efficiency, aims to create hardware that mimics brain-like structures, potentially reducing energy consumption and increasing efficiency. In-memory computing using memristors, which store values on a continuum rather than binary, allows for more energy-efficient matrix multiplications in machine learning. Optical accelerators, which use light instead of electricity, offer faster processing speeds and lower energy usage but are currently limited by the need for efficient signal conversion between analogue and digital systems. The potential for energy-efficient analogue computing in AI inference, where speed is prioritized over precision, could lead to broader adoption of these new computing paradigms.

Decades of rapid development have not erased concerns about the potential failure of Moore's Law. In fact, to maintain Moore's Law, computer chips are already undergoing significant changes. Under the influence of AI, the barriers that used to exist between software and hardware are being broken down. It can be foreseen that the future chip industry will become more colorful under the pressure of Moore's Law.

Class 4

Looking back, all major breakthroughs in computing can be traced to transistors getting smaller, faster and more affordable over the past decades in accord with Moore's law by and large. In this post-Moore era, however, it seems that chipmaking industry has encountered a bottleneck, especially in technology, which in turn pushes scientists and researchers to come up with new ways to maintain performance growth. These mainly include innovative chip designs, new materials, better packaging and silicon smartness.

Firstly, innovative chip designs can be divided into two parts. The first one is mainly about transistors' new structures such as FinFET, GAA and CFET framework to deal with the leakage current caused by quantum effects. The other one focuses on bespoke chips tailored to different use. For example, GPU or TPU for AI and firms designing their own chips for their own software. This can be seen as a measure to address the soaring demand for mounting data and energy to train AI models.

Secondly, new materials like TMDs and CNT have come to the spotlight in order to better address the need to squeeze once a transistor's gate length approaches 10nm with even more pronounced current leakages, with their own limits to be overcome by scientists and researchers.

Thirdly, Advanced packaging methods, including backside power delivery and chiplet technology, are revolutionizing chipmaking by improving efficiency and packing density.

Lastly, for smart silicon, two strategies have been proposed to handle the high time-and-energy consumption in the data transportation between the processor and memory. The idea to build hardware that mirrors the structure of human brain is valuable, and using light instead of electricity in accelerators seems promising.

Looking ahead, it is predictable that continuous innovation shall never stop in chipmaking industry, promising a booming and fierce future.

Software designing was once more important than chipmaking, but AI’s high demands on computing power have made chipmaking important again. Now chipmaking is the most important global technology issue and attracts great attention. However, the development of chipmaking is now facing a bottleneck and can no longer grow exponentially without new designs.

The first way is to experiment with new structures and materials of transistors. Transistors are the structural foundation of chips, which act as the circuit switches to control the on and off state of the current. Over the past century, technological advances have easily made transistors smaller, thus improving performance while reducing costs. However, continuing to reduce transistor size at current levels will lead to increased energy consumption and heat emissions, which means we have to find other ways out. Chip-making companies designed new structures and arrangements of transistors such as finFETs, GAA, and 3D stacking. Another way to break through the bottleneck is to replace silicon with other new materials, such as TMDs and CNT.

The second way is to change the way chips are packed. A strategy is to move the thick power lines to a layer below the transistors, called the “backside power strategy”. Another tactic is to de-integrate the functionality of the chips, which means breaking a chip into smaller blocks and packaging them together. Vertical chips may also be an answer, as they pack even denser connections between different parts of the chip. Besides, optical communication also has the potential to speed things up.

The third way is the specialized chip design. As AI is demanding higher processing power, software companies are making their own AI-chips. Based on the principle of AI calculation, AI-chips are designed to split tasks into multiple parallel threads that run simultaneously. Companies also tried to design TPU to reduce the need to access the of-chip memory so time won’t be wasted. Besides shifting the design of hardware, using less precise numbers and pruning the network to remove irrelevant cruft can also help improve the chip’s performance. Redesigning the chip to fit software can quickly become obsolete because software changes much faster than hardware.

As transporting data between processor and memory consumes a lot of time and energy, the fourth way to break through is to establish a new architecture. One way to build a new architecture is to mirror the structure of the brain to improve efficiency, and this architecture might be realized by a memristor. Another alternative is to use light to compute, which has a promising future in machine learning.

Many people believe Moore’s law has ended, and chipmaking is facing a bottleneck, especially for its high energy consumption. In search of a breakthrough, the chipmaking industry is now making chips specialized for specific software, and this trend leads to the rise of firms that control both hardware and software. Ultimately, we all believe that the bottleneck will be overcome by our persistent innovation from all directions.