

Electrical Rules Check Report

Class	Document	Message
Warning	BSU_Connector.SchDoc	Floating Power Object +5V at (10700mil,5800mil)
Warning	BSU_Connector.SchDoc	Floating Power Object GND at (7800mil,4700mil)
Warning	BSU_Connector.SchDoc	Floating Power Object GND at (10700mil,4700mil)
Warning	BSU_Connector.SchDoc	Floating Power Object GND at (10700mil,5700mil)
Warning	BSU_Power.SchDoc	Net 24V has no driving source (Pin C 19-2, Pin C 21-2, Pin D1-1, Pin PS1-1, Pin PS2-2, Pin R5-2, Pin X1-2)
Warning	BSU_Comm.SchDoc	Nets Wire RTD0- has multiple names (Net Label RTD0- (2), Net Label RTD1- (2), Net Label RTD2- (2), Net Label RTD3- (2), Net Label RTD4- (2), Net Label RTD5- (2), Net Label RTD6- (2), Net Label RTD7- (2), Net Label RTD8- (2), Net Label RTD9- (2), Net Label RTD10- (2), Net Label RTD11- (2), Net Label RTD12- (2), Net Label RTD13- (2), Net Label RTD14- (2), Net Label RTD15- (2), Power Object ADC_GND (18))

Design Rules Verification Report

Filename : D:\EE\BMS\BSU\BSU.PcbDoc

Warnings 0
Rule Violations 96

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (InNetClass('BT')),(All)	0
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=2mm) (Preferred=1mm) (InNetClass('PWR'))	0
Width Constraint (Min=0.127mm) (Max=1mm) (Preferred=0.254mm) (InNetClass('All Nets'))	0
SMD To Plane Constraint (Distance=0mm) (All)	0
SMD Neck-Down Constraint (Percent=1000%) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.05mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.5mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)	66
Silk to Silk (Clearance=0.127mm) (All),(All)	1
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	29
Matched Lengths(Tolerance=1mm) (InNetClass('EADC2'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('EADC2_HV'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('SWD'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('I2C'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('EADC1'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('USB'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('CAN1'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('UART2'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('UART1_HV'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('EADC1_HV'))	0
Matched Lengths(Tolerance=1mm) (InNetClass('CAN2'))	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	96

Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F26-1(193.6mm,22.505mm) on Top Cu And Track (193.6mm,23.392mm)(193.6mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F26-2(193.6mm,25.295mm) on Top Cu And Track (193.6mm,23.392mm)(193.6mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F27-1(192.5mm,22.505mm) on Bottom Cu And Track (192.5mm,23.392mm)(192.5mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F27-2(192.5mm,25.295mm) on Bottom Cu And Track (192.5mm,23.392mm)(192.5mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F28-1(191.4mm,22.505mm) on Top Cu And Track (191.4mm,23.392mm)(191.4mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F28-2(191.4mm,25.295mm) on Top Cu And Track (191.4mm,23.392mm)(191.4mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F29-1(190.3mm,22.505mm) on Bottom Cu And Track (190.3mm,23.392mm)(190.3mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F29-2(190.3mm,25.295mm) on Bottom Cu And Track (190.3mm,23.392mm)(190.3mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F30-1(189.2mm,22.505mm) on Top Cu And Track (189.2mm,23.392mm)(189.2mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F30-2(189.2mm,25.295mm) on Top Cu And Track (189.2mm,23.392mm)(189.2mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F31-1(218.9mm,22.505mm) on Bottom Cu And Track (218.9mm,23.392mm)(218.9mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F31-2(188.1mm,22.505mm) on Bottom Cu And Track (188.1mm,23.392mm)(188.1mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F31-2(188.1mm,25.295mm) on Bottom Cu And Track (188.1mm,23.392mm)(188.1mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F32-1(187mm,22.505mm) on Top Cu And Track (187mm,23.392mm)(187mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F32-2(187mm,25.295mm) on Top Cu And Track (187mm,23.392mm)(187mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder] clearance
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F33-1(185.9mm,22.505mm) on Bottom Cu And Track (185.9mm,23.392mm)(185.9mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F33-2(185.9mm,25.295mm) on Bottom Cu And Track (185.9mm,23.392mm)(185.9mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F4-1(217.8mm,22.505mm) on Top Cu And Track (217.8mm,23.392mm)(217.8mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F4-2(217.8mm,25.295mm) on Top Cu And Track (217.8mm,23.392mm)(217.8mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F5-1(216.7mm,22.505mm) on Bottom Cu And Track (216.7mm,23.392mm)(216.7mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F5-2(216.7mm,25.295mm) on Bottom Cu And Track (216.7mm,23.392mm)(216.7mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F6-1(215.6mm,22.505mm) on Top Cu And Track (215.6mm,23.392mm)(215.6mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F6-2(215.6mm,25.295mm) on Top Cu And Track (215.6mm,23.392mm)(215.6mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F7-1(214.5mm,22.505mm) on Bottom Cu And Track (214.5mm,23.392mm)(214.5mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F7-2(214.5mm,25.295mm) on Bottom Cu And Track (214.5mm,23.392mm)(214.5mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F8-1(213.4mm,22.505mm) on Top Cu And Track (213.4mm,23.392mm)(213.4mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F8-2(213.4mm,25.295mm) on Top Cu And Track (213.4mm,23.392mm)(213.4mm,24.408mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F9-1(212.3mm,22.505mm) on Bottom Cu And Track (212.3mm,23.392mm)(212.3mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.15mm) Between Pad F9-2(212.3mm,25.295mm) on Bottom Cu And Track (212.3mm,23.392mm)(212.3mm,24.408mm) on Bottom Overlay [Bottom Overlay] to [Bottom]
Silk to Silk (Clearance=0.127mm) (All),(All)
Silk To Silk Clearance Constraint: (0.1mm < 0.127mm) Between Text "C52" (109.7mm,28.2mm) on Top Overlay And Text "R19" (109.7mm,26.9mm) on Top Overlay Silk Text to Silk Clearance [0.1mm]

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (130.6mm,64.85mm)(137.4mm,64.85mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (130.6mm,75.15mm)(137.4mm,75.15mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (134mm,0mm)(134mm,100mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (0.102mm < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (205.702mm,57.43mm)(205.702mm,62.47mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (67.1mm,15.15mm)(73.9mm,15.15mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (67.1mm,19.85mm)(73.9mm,19.85mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (67.1mm,30.15mm)(73.9mm,30.15mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (67.1mm,4.85mm)(73.9mm,4.85mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (70.5mm,0mm)(70.5mm,55mm) on Top Overlay
Board Outline Clearance(Cutout Edge): (Collision < 0.3mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (70.5mm,55mm)(134mm,55mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.13mm < 0.3mm) Between Board Edge And Text "STM32" (0.33mm,71.095mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.123mm < 0.3mm) Between Board Edge And Track (0.25mm,0.25mm)(0.25mm,70.25mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.123mm < 0.3mm) Between Board Edge And Track (0.25mm,0.25mm)(57.75mm,0.25mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.123mm < 0.3mm) Between Board Edge And Track (0.25mm,70.25mm)(57.75mm,70.25mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (-0.78mm,76.1mm)(-0.78mm,83.9mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (-0.78mm,76.1mm)(0.7mm,76.1mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (-0.78mm,83.9mm)(0.7mm,83.9mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (129.9mm,-4.47mm)(129.9mm,12.53mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (129.9mm,-4.47mm)(129.9mm,12.53mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (134mm,0mm)(134mm,100mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (174.4mm,-4.15mm)(174.4mm,14.25mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (174.4mm,-4.15mm)(223.8mm,-4.15mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (223.8mm,-4.15mm)(223.8mm,14.25mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.123mm < 0.3mm) Between Board Edge And Track (57.75mm,0.25mm)(57.75mm,70.25mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (70.5mm,0mm)(70.5mm,55mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (89.3mm,-4.47mm)(129.9mm,-4.47mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (89.3mm,-4.47mm)(129.9mm,-4.47mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (89.3mm,-4.47mm)(89.3mm,12.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.3mm) Between Board Edge And Track (89.3mm,-4.47mm)(89.3mm,12.5mm) on Top Overlay