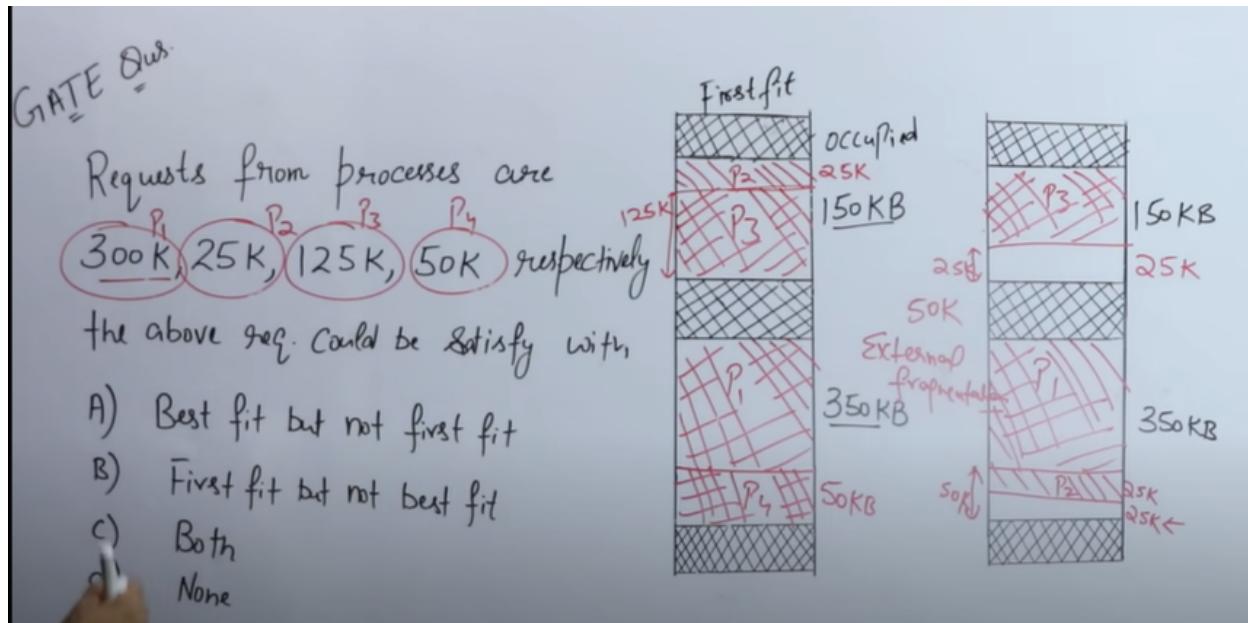
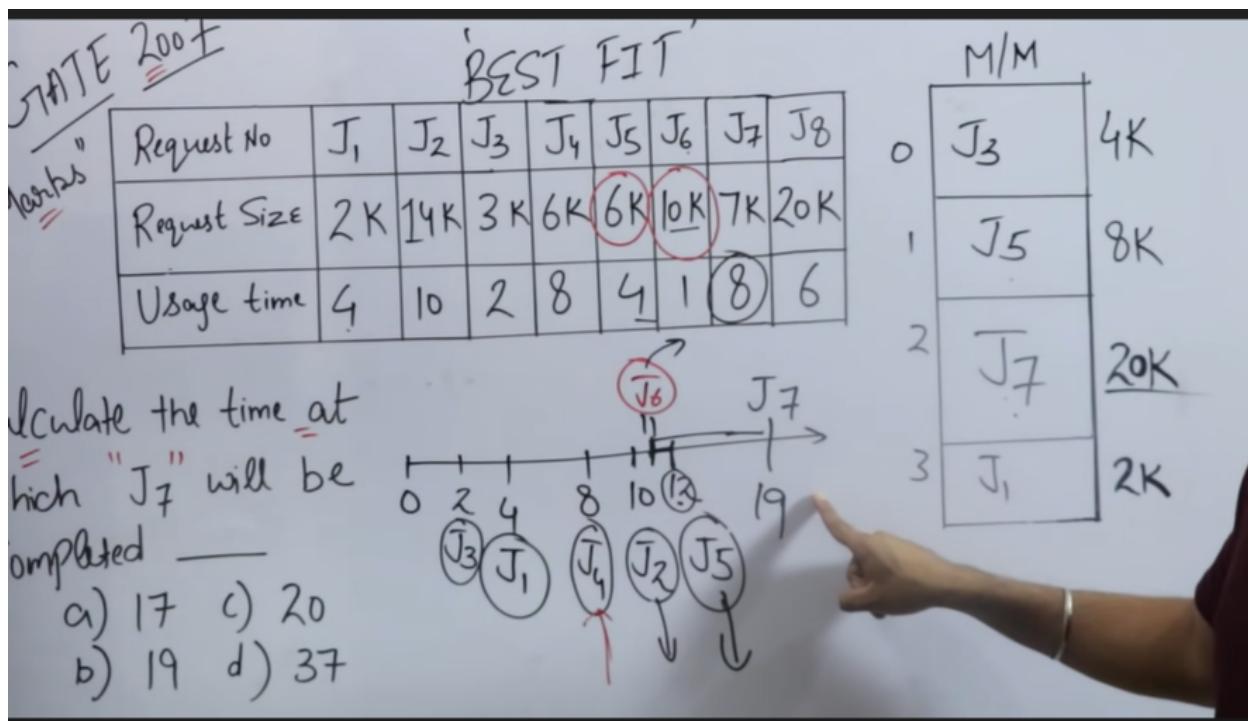


GATE Question Solved on First Fit, Best Fit and Worst fit Memory Allocation



Q2:



Non Contiguous Memory Allocation:

Need of Paging | Memory Management | Operating System

to avoid the problem of external fragmentation this concept is introduced which saved a lot of memory wastage:

Time consuming process - to avoid this process is divided into the pages outside the memory and then it is brought into the memory and pages are divided into the smaller frames:

So here the processes are divided into the pages and the main memory is divided into the frames.

page size = frame size

What is Paging | Memory management

Multiple page tables:

Mapping: Mapping is done by Memory Management Unit, in this case when CPU ask for the any bit of the process then it should check in the memory and get that bit but in memory it would be allocated at different address so MMU converts the logical address into the physical address with the help of PAGE TABLE.

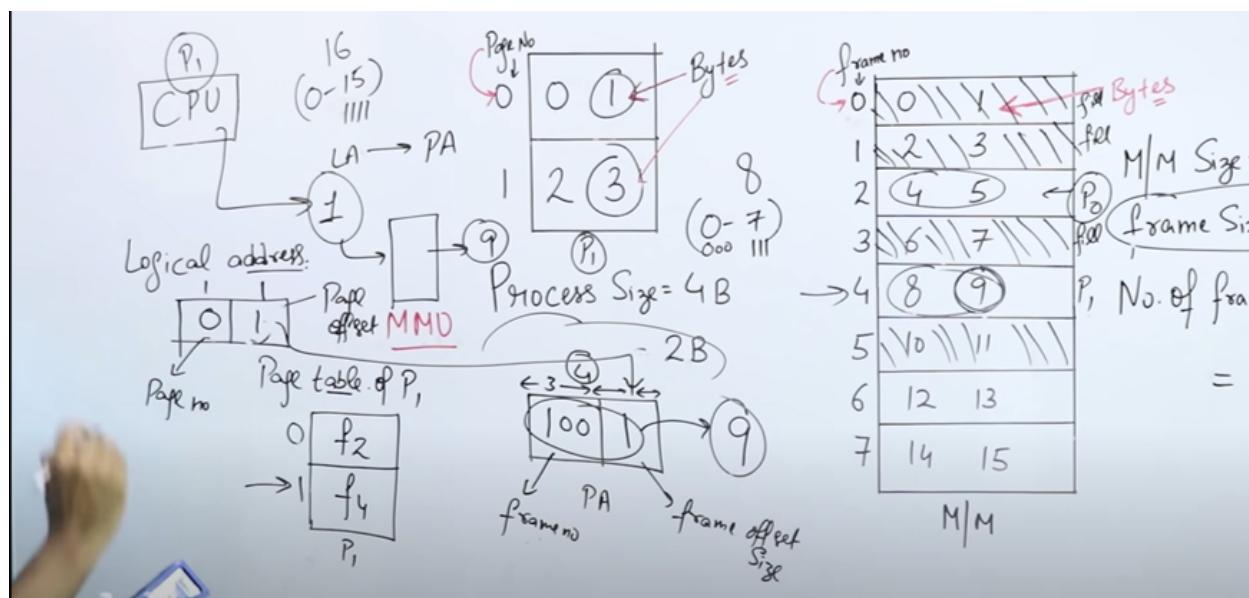
CPU always works on logical address:

Logical Address : **page no** **page offset** // (Virtual address space)

Page offset also called as page size and convert that into the binary!

Physical address :

Every process will have own page table and page table contains the frame numbers



Lets' say : Page P1 size is 4 B and page size is 2 B so the No of pages for P1 is 2

Main memory size is 16B and frame size is 2B so the no of frames are 8.

for every process page table would be different as pages for particular process would be in different frames.

lets say for P1, pages are in frame 2 and frame 4

so page table is ;

0 f2

1 f4

As CPU can access only main memory so when CPU askf for the 3rd byte of the process P1 its' not there at 3rd byte in main memory due to non contiguous allocation, so here logical address of P1 i.e. 3rd byte will converted into the physical i.e. actual address of that byte in the main memory which here in this e.g. is at 9th byte in MM

So the logical address is: 11 // here value is 3rd byte of Main Memory

(Logical Address : page no page offset)

here for 3rd byte the page no is 1st for P1 nad page offset is also 1.

here page offset is nothing but the no of bits required to represent the page size so in this e.g. it is 2B so the range is 0-1 as in binary no starts from 0 and to represent the 1 we need only 1 bit.

if page size would have been 8B then range would be 0-7 and to represent the 7 we need 3 bits i.e.(000-111 i.e. 0-7)

if page size would have been 16B then range would be 0-15 and to represent the 15 we need 4 bits i.e. (0000-1111 i.e. 0-15)

Physical address : It depends on the size of the main memory

In this eg size of MM is 16Bytes so to represent the range 0-15 we must need 4 bits so from this 4 bits also few allocated to the frame no and rest to the frame offset

so physical address size is 4 bits and 3 for frame no is 3 bits and frame offset is 1 bite so the PA is 1001

LAS : Logical address space always represents the size of the process

PAS: Physical address space always represents the size of the Main memory

MEMORY IS BYTE ADDRESSABLE

MSB bits for page no and LSB bits for page offsets

L-5.10: Question Explanation on Logical address and Physical address space | Operating System

Logical Address of Process = No. of P's

Memo is byte addressable.

$LAS = 4GB$

$PAS = 64MB$

$2^6 \times 2^{20} B$

$LA = 2^2 \times 2^{30} = 2^{32}$

16
 $(0-15)$
 1111

Page Size = 4 KB

Page no → $20 | 12$ → Page offset/size

Frame no → 32

No. of Pages = 2^{20} ?

No. of frames = 2^4 ?

No. of entries in Page table = 2^{20} ?

Size of Page table = $2^{20} \times 14$ bits

frame no → $14 | 12$ → PA.

Frame offset/size

PT

$2^0 = 2$
 $2^1 = 4$
 $2^2 = 8$
 $2^3 = 16$
 $2^4 = 32$
 $2^5 = 64$
 $2^6 = 128$
 $2^7 = 256$
 $2^8 = 512$
 $2^9 = 1K$
 $2^{10} = 1M$

Consider a system which has
 $LA = 16$ bits, $PA = 6$ bits, Page Size = 8 words/byte

then calculate no. of pages & no. of frames

$\frac{No. of entries in a PT of a process}{No. of pages in a process} = \frac{2^8}{2^4} = 2^4 = 16$

$LA = 7$ bits, $PA = 6$ bits, Page Size = 8 words/byte

$2^6 = 64$

$2^7 = 128$

$2^8 = 256$

$2^9 = 512$

$2^{10} = 1K$

$2^{20} = 1M$

$2^{30} = 1G$

$2^{40} = 1T$

Page offset

frame no.

frame size

Page table

'Page table entry'

Present/Absent

LRU

Enable/Disable

FRAME No.	Valid(1)/Invalid(0)	Protection(RWX)	Reference(0/1)	Caching	Dirty 1

Optional fields

Read, Write, Execute

$P_1 - W$

$X = 100$

User / 200

Handwritten notes: 'entry field' pointing to the first column, 'optional fields' pointing to the last four columns.

Level Paging in Operating System | Multilevel Paging

$2MB = 2^{21}$ bits

$2^{21} / 4KB = 2^{21} / 2^{12} = 2^9 = 512$

Frame size = 4KB

Page table Entry = 2B

512

32

20

2

25

26

27

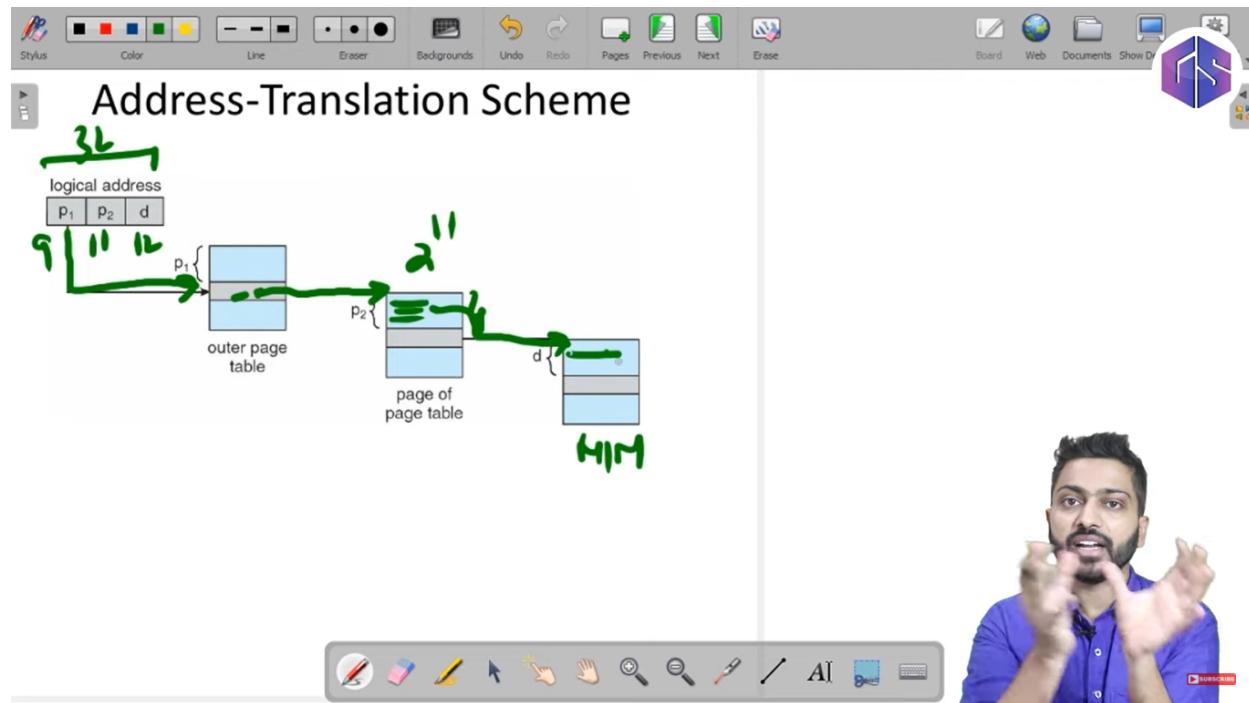
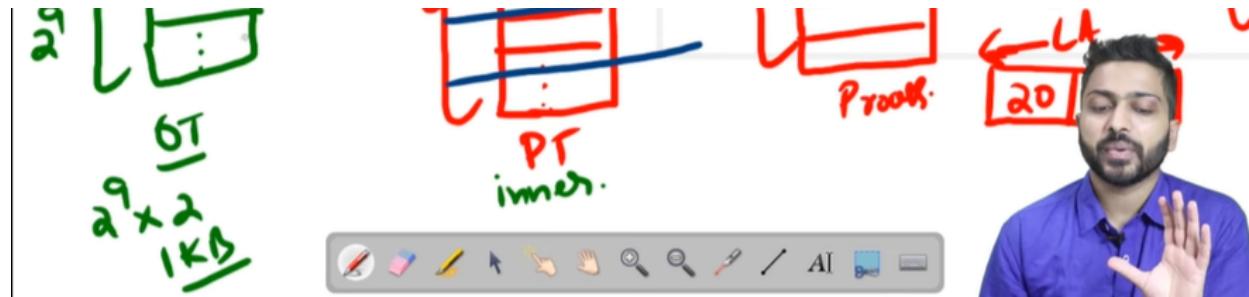
34KB

20

2

26

32



Inverted paging | Memory Management | Operating System

Reason to bring this concept:

Basically for every process page table will be created in normal paging and during its execution that page needs to be called and stored in the main memory from the secondary memory so if the no of processes increases then the no of page will in the main memory also gets increased due to which proper utilisation is not happening for main memory so to avoid this wastage inverted paging concept is introduced.

In this global page table will be created

frame no || page no || process ID

Searching time of the pages for the particular process is the biggest challenge in inverted paging:

Virtual address space

What is Thrashing | Operating System

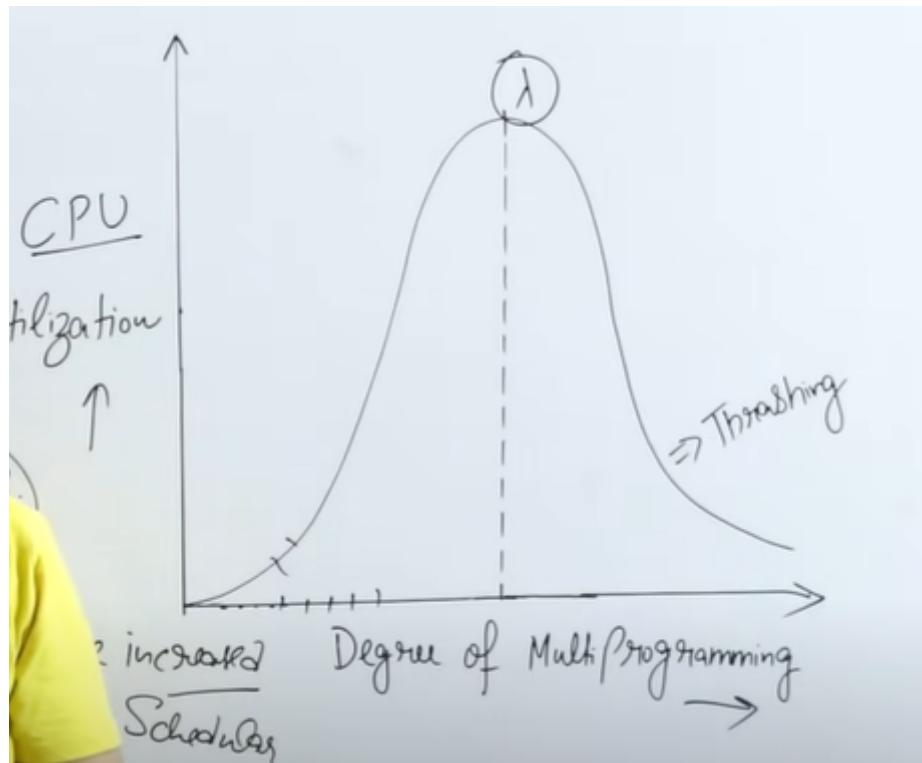
linked with the DoMP: Degree of Multi Programming

Page fault / PF service time

Due to rise in the page fault, system will get busy in bringing the missing pages of the processes from the secondary memory!

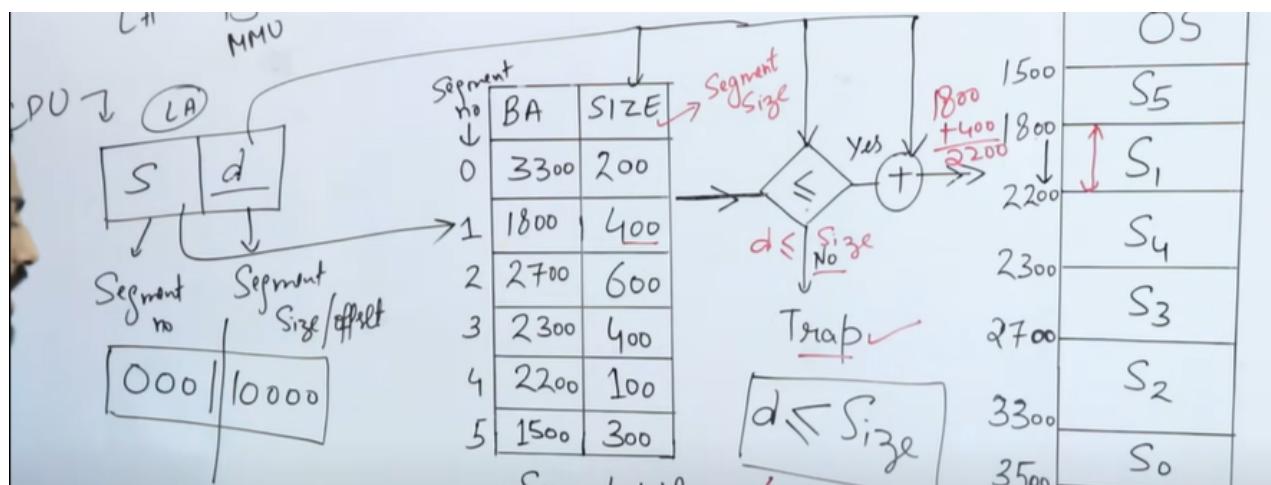
this can be reduced by making LTS bringing the less processes pages into the ready queue!

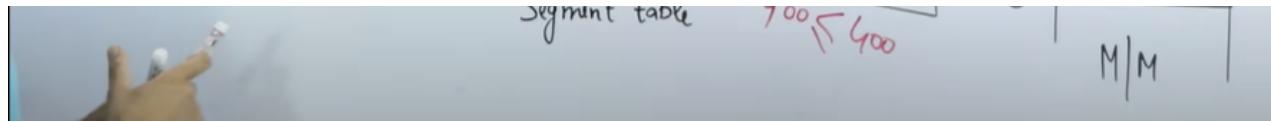
In below fig lambda is the point where LTS has brought first page of all the processes into the RAM and due to which inspite of having good CPU utilisation after lambda CPU utilisation will be decreased abruptly and that results in the thrashing:



Segmentation Vs Paging | Segmentation Working

Process will be divided into the no of segments of module but in case of paging we divided the process into the pages without knowing what's inside that page but in segmentation we know where we have broke the process into the page





Base address:

Limit address:

Size:

SIZE OF EACH SEGMENT IS DIFFERENT:

Overlay:

It's the method with which we can bring the process with the size greater than the main memory into the MM.

Widely used in embedded systems:

Virtual Memory | Page fault | Significance of virtual memory | Operating System

