Design of 9 Stage Ring Oscillator

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Jan 31 2022

Abstract

During the Fabrication of the Chip (Package) It is not Guaranteed that all the chips coming from the fab are going to come back with same specs as with which we have designed. So first we need to figure out how different these transistors are from our intended value so in every chip we are going to put a ring Oscillator. To make these measurements output frequency Has to be reduced significantly therefore large N (Number of Inverter Stages) has to be Chosen and we can measure the Frequency of operation using Oscilloscope. These Ring Oscillators are Called as

"GLOBAL PROCESS MONITORS"

REFERENCE CIRCUIT DETAILS

Ring Oscillator consists of odd number of Inverters connected in Series to form a closed loop with positive feedback. These ring oscillators does not require an input other than Vdd and Vss Supply Here the number of Stages taken are 9. Frequency of Oscillation of Ring Oscillator is given by

$$F_{OSC} = \frac{1}{N(tplh+tphl)}$$

Where N is (odd) number of inverters
tplh is a Low to High Delay
tphl is a High to Low Delay of an Inverter

if the Number of Stages chosen is high it reduces the power dissipation by the inverter which can be analysed by below equation.

$$I_{avg} = \frac{Q}{T}$$

If the **N** increases, $\mathbf{F_{Osc}}$ Reduces, which intern Increase the **T** and reduces the $\mathbf{I_{avg}}$. From **P = I.V** if **I** reduces **P** also Reduces which indicates the Reduction in the power Dissipated by the Inverters.as per the Table 1 from the **Reference [2]** analysis of Various parameters like Frequency and Power Consumption is done for different values of W_p, W_n, and L. Transient response for W_p = 370.55 W_n = 220.55 and L =172.51 (in nm) is as shown in the Reference Wave form Taken from **Reference [2].**

Reference Circuit Design

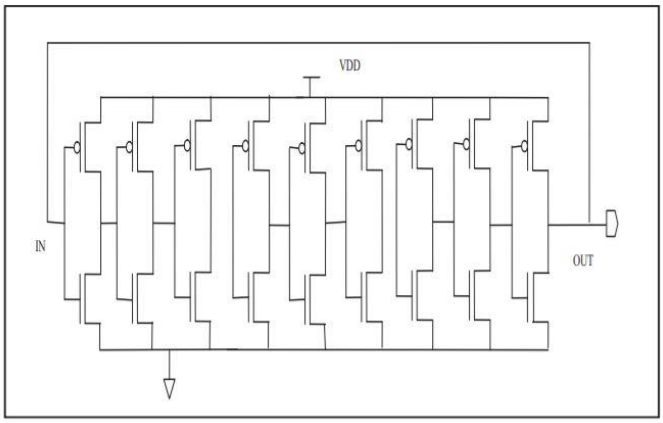

Fig. 3. Schematic of 9 stage ring oscillator

Taken from Reference [3]

Reference Waveform

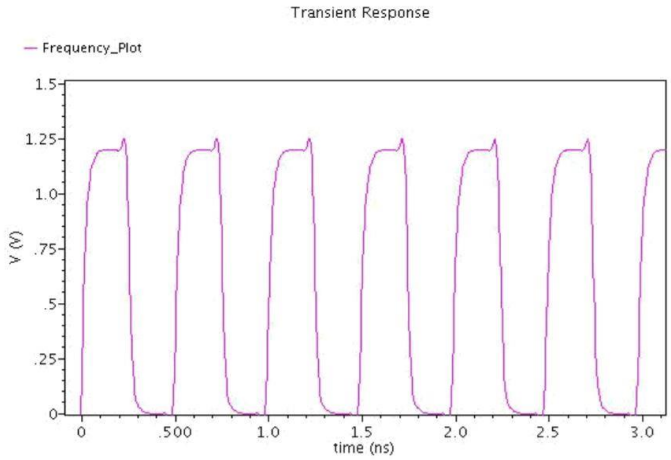

Fig.5 The output waveform for set-I of 9-stage RO

Taken from Reference [2]

References

[1] *CMOS Circuit design, Layout and Simulation 3rd edition* By R. JACOB BAKER

[2] *Design of a Nine Stage Ring Oscillator Using PSO* By Preeti Kumari, Madhuresh Suman

[3] *Design and analysis of CMOS ring oscillator using 45 nm technology* By Vandna Sikarwar, Neha Yadav, Shyam Akashe