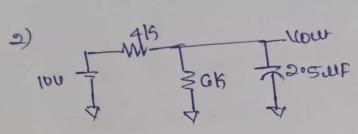


Find Yout,



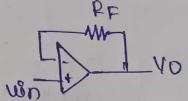
- > what is voltage across capacitor in steady state?
- > her he was mainly interested in approach
- ⇒ what is the wortage accords capacitor at time t=0.
- > How much time, it will take for a capacitor to reach
- =) Here he asked my approach towards calculating the time constant.
- 3) Interweever asked me to draw cmas inwiter. and asked about working of it.
 - => then he asked to draw same inverter by keeping
- =) asked like what will happen if I swap the positions

1-said it behaus a buffer and output win will of pmos fomos, not swing from rail to rail (upp - GND)

> asked why do we connected load capacitor our the output of the inverter while simulating the circuit on the simulator 9

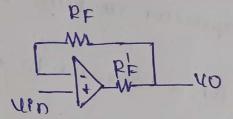
- 4) Then he started asking guistions on Buffer
 - → asked to draw buffer using op-amp
 - > asked about importance of Buffer while designing circuits
 - =) asked about properties of Buffer

=)

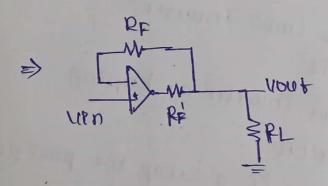


asked about empact of bat Resistor in the feedback

=>



asked about impact Rt on output wether the current thouse through Rt or?



now current tows through Rf (br) not ?

Win Right SRL

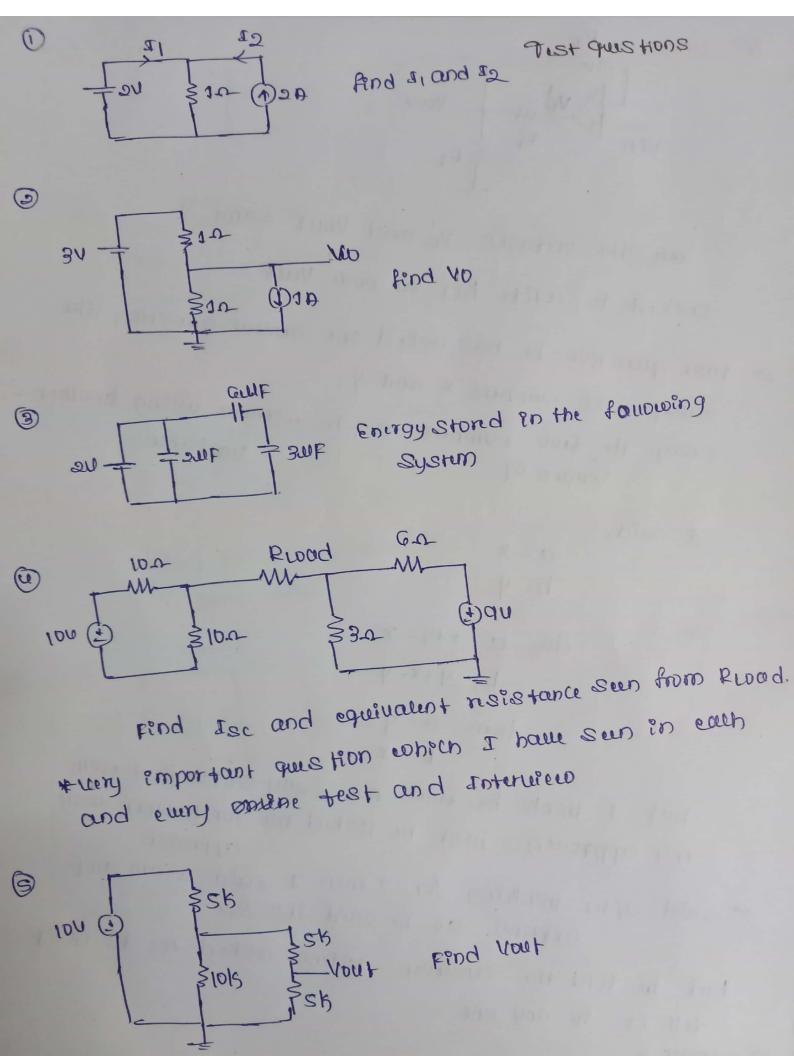
4

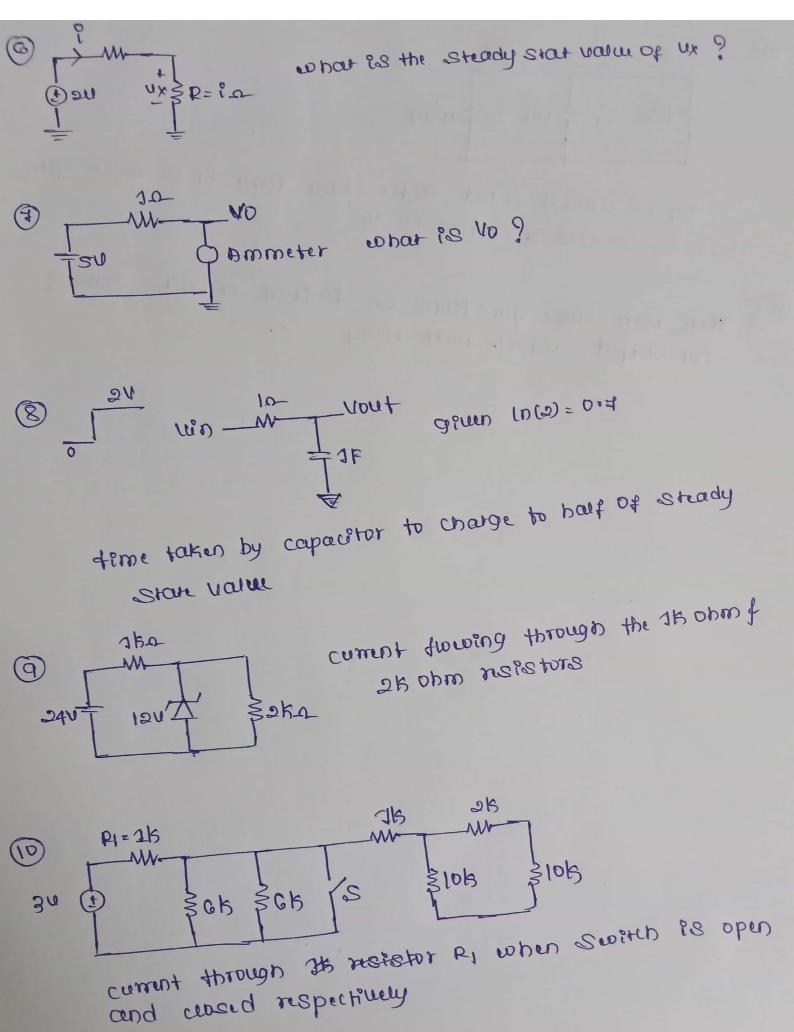
are the voltages vo and vout same ? asked to exite kcl at node vout

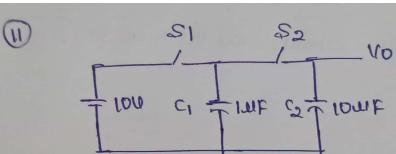
> Last question he has asked one general question like

swap two numbers x' and y

swap the two numbers a 4 b without using another
values of - variable







Si is closed first, after some time si is made open Si is closed what is vo

for output, which were easy