KIRAN JAYARAMA

kiranj.com | kiran760043@gmail.com | LinkedIn profile | Dayton, OH

RESEARCH EXPERIENCE

Graduate Research Assistant

Digital Receiver System Lab, Wright State University 2018 – Ongoing

Digital receiver lab focuses on designing mono-bit and multi-bit receiver for Instantaneous Frequency Measurement (IFM).

- Studied and evaluated the performance of a mono-bit receiver in wide-band (1-GHz) digital receiver.
- Proposed, evaluated and implemented new design algorithms for accurate frequency estimation in wide-band receiver.
- Implemented a 512-point dynamic kernel FFT on system generator tool.
- Implemented the optimized hardware design for twiddle factors for the dynamic kernel.

Digital Design Lab 2014 – 2017

Digital design lab research focus on trojan free design implementation for FPGAs. Analyzed the benefit of partial reconfiguration designs in FPGAs for error-free designs.

- Demonstrated the application of partial reconfiguration in a FPGA to tolerate stuck-at zero or stuck-at-one faults.
- Presented three new methods to design a system that rectifies itself when an error is detected by implementing the partial bit file.

TEACHING EXPERIENCE

Graduate Teaching Assistant

Assisted junior level and graduate level students in analyzing, designing, building and testing digital designs using various software's such as Vivado, Cadence, Multisim, etc.

Digital Integrated Circuit Design Lab	EE6620
Digital VLSI Design Lab	EE6540
Electronic Devices and Circuits Lab	EE3310
Circuit Analysis Lab	EE2010

PASSION PROJECTS

1. AMBA Protocol: Designed AMBA specification master and slave interface which can communicate between one or more AMBA master or slave
2. 32-bit Multiplier: A 32-bit multiplier was designed, simulated for functional verification. An efficient hardware implementation of the design was achieved using Wallace tree technique.
3. ATPG and fault simulation: Designed a 16-bit ALU using Verilog for ATPG, targeting stuck-at-fault models to determine fault coverage. Test pattern generators such as D-algorithm and PODEM was implemented to generate test vectors for the faults.
4. 6X6 Booth Multiplier: A transistor schematic of 6x6 Booth multiplier is designed and optimized using the cadence design system. The adder circuit, which is the primary source of delay is constructed with mirror adders using inversion property to decrease propagation delay.
5. I2C Protocol: Implemented I2C protocol using Verilog where a single master could communicate to one or more slave on a single line.
6. Ping-Pong game: Simple ping-pong game was implemented on a Spartan 3E FPGA. On board encoder rotor was used to control the ball, dipswitches were used for additional customizations such changing color of the game and speed of the ball.

EDUCATION

PhD, Electrical Engineering

Wright State University
2016 - Present

M.S, Electrical Engineering

Wright State University
2014 - 2016

TECHNICAL SKILLS

Programming Language

Verilog, VHDL, SytemVerilog, C, C++, Python, HTML, CSS

Tools

Vivado, Quartus Prime, Modelsim, Cadance Virtuoso, System generator for DSP, Matlab

Protocols

I2C, SPI, JTAG, AMBA AHB, AMBA APB

Development Boards

Virtex 7 VC707, Zynq 7000[zedboard], Virtex 6, Spartan 3E, DE0-Nano_Altera Cyclone, Arduino Mega 2560

PUBLICATIONS

CONFERENCE PAPER

FFT Based Novel Algorithm for Frequency Estimation using Polynomial Interpolation and Array Indexing – Kiran Jayarama & Henry Chen (under review IMS 2020)

MASTER'S THESIS

Implementation of Fault Tolerance on a dynamically reconfigurable FPGA

COURSE WORK

Digital IC Design with PLDs and FPGAs, VLSI Circuit Design, VLSI Design Synthesis and Optimization, Low Power VLSI System Design, VLSI Testing and Design for Testability, Trust in Integrated Circuits and Combinatorics and Graph theory

VOLUNTEERING

Volunteered at Wight State University Friendship food pantry.