B.Tech III Semester End Examinations, 2021

DIGITAL ELECTRONICS & LOGIC DESIGN (19APCO404)

(Electronics & Communication Engineering)

Time: 3 Hours | Max Marks: 70

PART-A(Compulsory) (10*2= 20 M)

		Answer the following	UNIT	Marks
1	a)	9's complement of 546700 and 012398	I	2
	b)	What are Don't care conditions? Explain their importance.	I	2
	c)	What is the difference between Adder and Subtractor?	II	2
	d)	What is difference between Master-slave & Edge-triggered Flip flops?	II	2
	e)	What is the difference between Moore & Mealy machine models?	III	2
	f)	What is the difference between Ripple counter & Synchronous counter?	III	2
	g)	What is the difference between RAM and ROM?	IV	2
	h)	What is the difference between PLA and PAL?	IV	2
	i)	Draw TTL characteristics	V	2
	j)	Draw CMOS characteristics	V	2

PART-B (5*10= 50 M)

Answer One Full Question from each unit; All questions carry EQUAL marks.

		UNIT-I	
2		With the help of an example explain the concept of Sum-of-products & Product-of-sum representations.	**10 M**

(OR)

3		Explain the concept of how to minimize a function using Quine-McCluskey method using an example.	**10 M**
		UNIT-II	
4	**a)**	Implement the following Boolean function with a 4 x1 multiplexer and external gates (a) F1(A, B, C, D) = Σ (1,3,4,11,12,13,14,15) (b) F2(A, B, C, D) = Σ (1,2,5,7,8,10,11,13,15)	**5 M**
	b)	Design a code converter that converts a decimal digit from (a)The 8, 4, –2, –1 code to BCD (b) The 8, 4, –2, –1 code to Gray code.	**5 M**

(OR)

5		Explain briefly how SR and D flip flops can be converted to other Flip flops	**10 M**
		UNIT-III	
6.		Explain the procedure of Synthesis for JK Flip flops and T flip flops	**10 M**

(OR)

7		Explain in detail about Johnson counter & Up-Down counter	**10 M**

UNIT-IV

8	The following is a truth table of a three-input, four-output combinational circuit: **Inputs** / **Outputs** x y z | A B C D 0 0 0 | 0 1 0 0 0 0 1 | 1 1 1 1 0 1 0 | 1 0 1 1 0 1 1 | 0 1 0 1 1 0 0 | 1 1 1 0 1 0 1 | 0 0 0 1 1 1 0 | 1 0 1 0 1 1 1 | 0 1 1 1 Tabulate the PAL programming table for the circuit, and mark the fuse map in a PAL diagram	**10 M**

(OR)

9.	Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table for the following combinational circuit components: (a) a binary multiplier that multiplies two 4-bit binary words, (b) a 4-bit adder–subtractor, (c) a quadruple two-to-one-line multiplexer with common select and enable inputs, and (d) a BCD-to-seven-segment decoder with an enable input.	**10 M**

UNIT-V

10	Explain Interface aspects of TTL to CMOS & SMOS to TTL.	**10 M**

(OR)

11.	Explain the characteristics of Digital ICS such speed, power dissipation, fan-out and Noise immunity.	**10 M**

ECE