19AOE0404

B.Tech DEGREE EXAMINATION, OCTOBER/NOVEMBER 2022.

End Examinations

Sixth Semester

(ECE)

BASICS OF VLSI

(Academic Year 2021-2022)

(RU 19 Regulations)

(Regular)

Time : 3 Hours *Max. Marks : 70*

PART — A

(Compulsory question) **(10 × 2 = 20 Marks)**

1. Answer the following.

(a) Write down the equations for I_{ds} of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region.

(b) Why is VLSI design process presented in NMOS only? Justify with an example.

(c) Give the different scaling models and scaling factors.

(d) Define stick diagram and layout diagram.

(e) Explain about the constraints in choice of layers.

(f) What is sheet resistance? Derive the Expression for RS.

(g) What is serial access Memories ?

(h) What is comparator?

(i) What information from the targeted FPGA device is required in RTL synthesis?

(j) Explain about Clock Design.

PART – B

Answer ONE full question from each Unit; **(5 × 10 = 50 Marks)**

All questions carry equal marks.

UNIT I

2. (a) Explain the nMOS enhancement mode fabrication process for different conditions of V_{ds}. (5)

(b) Derive an expression for transconductance of an n-channel enhancement MOSFET operating in active region. (5)

Or

3. (a) Explain in detail the p-well process for CMOS fabrication indicating the masks used. (5)

(b) Compare the relative merits of three different forms of pull-up for an inverter circuit. What is the best choice for realization in nMOS and CMOS technology? (5)

UNIT II

4. (a) What are the λ-based design rules? Give them for each layer. (5)

(b) Explain about double poly CMOS rules. (5)

Or

5. (a) Design a layout diagram for CMOS 3-input NAND gate. (5)

(b) Explain 2 μm Double Metal, Double Poly CMOS / BiCMOS Rules. (5)

UNIT III

6. (a) Explain the issues involved in driving large capacitor loads in VLSI circuit regions. (5)

(b) Calculate the gate capacitance value of 5 mm technology minimum size transistor withgate to channel value is 4×10^{-4} pF/mm^2. (5)

0.8×10^{-4}

Or

7. (a) What is inverter delay? How delay is calculated for multiple stages? Explain. (5)

(b) Two nMOS inverters are cascaded to drive a capacitive load $C_L = 16C_g$. Calculate pair delay V_{in} to V_{out} in terms of τ. (5)

UNIT IV

8. (a) Briefly Explain about array Multipliers (5)

(b) Explain the operation of UP/Down Counter (5)

Or

9. (a) Draw and explain about 4-bit comparator using its equivalent IC. (5)

(b) Differentiate Between different types of Memories (5)

UNIT V

10. (a) Give the steps in FPGA design flow with flow diagram and briefly discuss about each step. (5)

(b) Explain briefly about PLD with its functional diagram and suitable example. (5)

Or

11. Illustrate with a neat architecture diagram about various functional blocks of FPGAs. (10)
