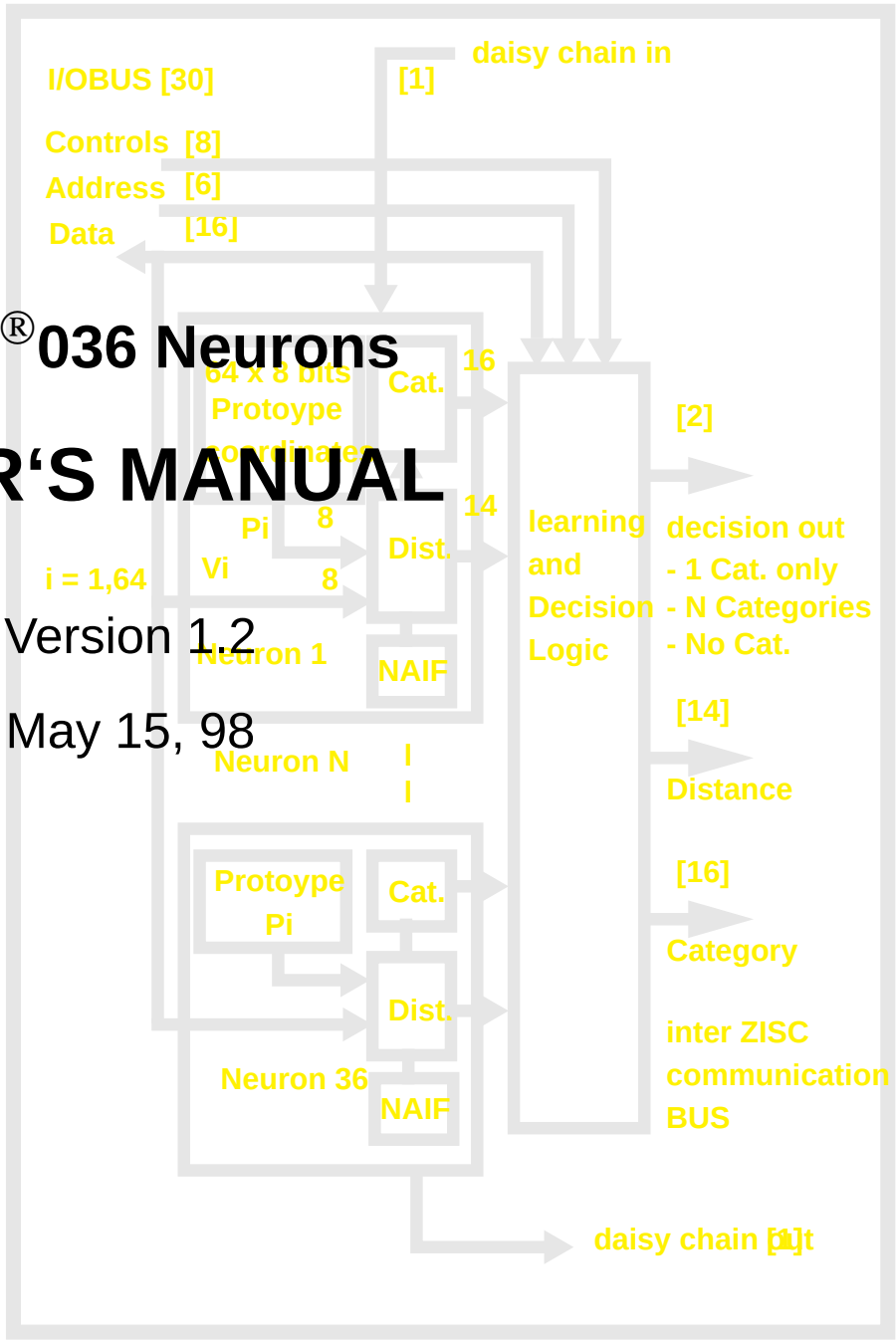
ZISC
(Zero Instruction Set Computer)



ZISC®036 Neurons

USER'S MANUAL

Version 1.2

May 15, 98

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Abstract

This document provides a detailed technical description of the ZISC 36 digital Neuronal Network integrated circuit It is intended to be used by programmers, test engineers and other development engineers as a «first source» of information.

The ZISC036 is manufactured under a patent and a technology licence from Nestor Inc.

CHAPTER 1

Preface

1 - INTRODUCTION

1•1 NEURAL NETWORKS, A NEW CONCEPT?

Neural network concepts were introduced in 1943 by McCulloch and Pitts, who devised formal interconnected neurons, based on biological models, and demonstrated their ability to compute some arithmetic or logical functions. In this model, the neuron sums up its weighted inputs received from stimulating and inhibiting synapses, and becomes active if the sum is larger than a fixed threshold, as shown in figure 1. In 1949, Hebb outlined the first learning scheme for modification of the synapse weights between neurons.

Rosenblatt in 1958 described the perceptron, the first operational neural network model that had some learning capability through a simple reinforcement rule.

This was refined into a supervised learning procedure, using error feedback. The perceptron encouraged research until Minsky and Papert showed, in 1969, the theoretical limits of networks using linear transfer functions such as the perceptron, which are not able to solve non-linear classification problems. This led to a decline in the level of investment in neural networks, and a redirection of research in this area towards artificial intelligence.

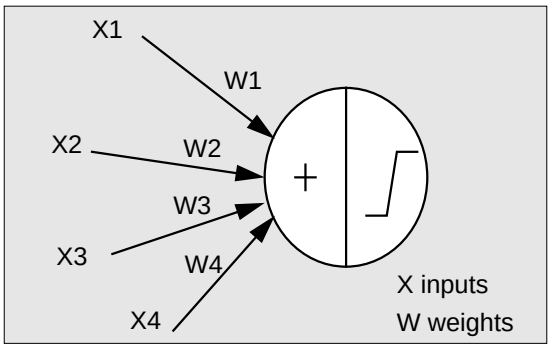


FIGURE 1. Simple Neuron Model

New neuron model developments such as Hopfield and-Kohonen revived the interest in neural networks in the 1980's. Varieties of neural network models and learning rules have been developed and implemented mainly as software programs on computers and dedicated hardware. The spectacular advances in VLSI technology, as well as the relative failure of the symbolic artificial intelligence approach, contributed to further spark interest in the field of neural networks.

1•2 . WHY SHOULD NEURAL NETWORKS BE ON SILICON?

The first integrated neural networks were based on analog technology, with the advantage of speed and integration, but with significant disadvantages in terms of precision and sensitivity to noise and crosstalk. Digital implementations do not suffer the inherent drawbacks of analog circuits, as they allow arbitrary precision, strong noise immunity and easy interfacing to other system components. Although software programs can handle various neural network models and learning algorithms, they do not permit the performance required for real time applications. Implementing neural networks on silicon, overcomes this performance limitation.

1•3 APPLICATIONS

The main reason for using a neural network is that it can solve problems that conventional methods cannot, or at least not within acceptable cost or performance criteria. Unlike conventional computing techniques, which handle problems through mathematical models and algorithms, neural network techniques require little knowledge of the system, as they are taught by example. They are trained, not programmed. Neural networks are very good at pattern recognition, pattern matching and classification tasks, making them appropriate for signal processing applications.

1•4 RBF-LIKE APPROACH

The RBF-like (Radial Basis Function) approach consists of mapping an N-dimensional space by prototypes. Each prototype is associated with category and an influence field representing a part of the N-dimensional space around the prototype, where generalization is possible. A

prototype is a vector defining the co-ordinates of a point within the N-dimensional space. Within the network, several prototypes may be associated with one given category, and influence fields can partially overlap each other.

Figure 2 shows how an RBF-like approach can map a two-dimensional space.

The classification task consists of evaluating if an N-dimension input vector lies within the influence field of any prototype stored in the network. This is done by computing the distance between the input vector and all stored prototypes, and comparing it to the influence field associated with the prototype.

The network decision is taken upon the result of the following comparisons:

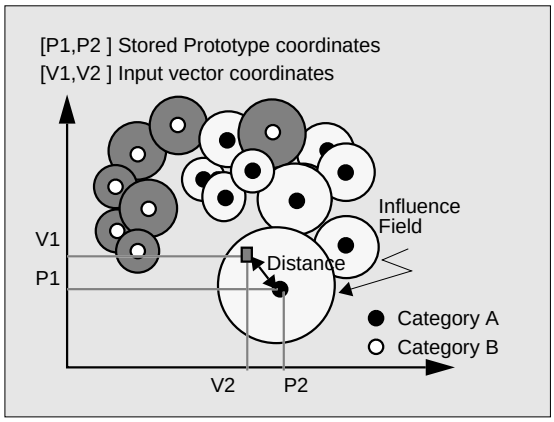


FIGURE 2. RBF Mapping of Space

If the input vector does not lie within any influence fields, it is not recognized. If the input vector lies within the influence field of one or more prototypes associated with one category, it is declared as belonging to that category. If the input vector lies within the influence field of two or more prototypes associated with different categories, it is declared as recognized but not formally identified. The learning task consists of mapping the space by prototypes and adjusting the influence fields according to all neighbours. Learning, as opposed to classification, requires that the correct answer associated to the prototype be given to the network. The learning mechanism rearranges the network content in function of the proximity between the new input and the map already residing in the network. The result of presenting a prototype and its category to the network can result in: No change in the network content One or more influence fields are modified (reduced). The new prototype is stored in the network.

1•4•1 RBF-like Network Topology

The RBF-like neural network topology, is a three layer network where each input node, corresponding to component (Vi) of a feature vector is connected to every node of the second layer (hidden layer), each node of the hidden layer is connected to one output node which corresponds to a category (see fig 3).

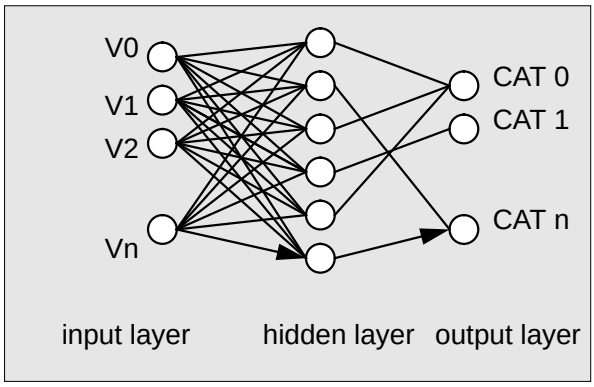


FIGURE 3. RBF-like Network Topology

Connections between first and second layers are static, corresponding weights established by the learning process are stored in the second layer. Connections between second and third layers are dynamically established by the learning process.

1•5 NEIGHBORHOOD EXPLORATION

Many recognition and classification applications require an exploration of the input vector neighbourhood This is the case in probabilistic approaches where the final decision is taken upon the probability of the input vector to belong to a category or another. In these cases, the exploration of the neighbourhood is a very resource consuming task. Hyper parallel structures like integrated neural networks give a very efficient solution to that class of problems.

Later in this document the word ‘Neuron’ will be used to define the resource capable of storing a prototype, the corresponding category and the influence field, as well as handling distance computation between an input vector and the prototype, and comparison with the influence field. A neuron is declared ‘fire’ when, following an evaluation, the input vector lies within its influence field.

CHAPTER 2

ZISC Overview

2 - ZISC OVERVIEW

2•1 ZISC - Zero Instruction Set Computer

ZISC036 is the first of a family of integrated circuit based on neural network designed for recognition and classification applications which generally require super-computers. ZISC products provide a very cost-effective way to solve such problems with sufficient performance to match real time constraints.

The performance level achieved by ZISC makes it suitable for real time applications such as video and signal processing.

ZISC can be considered as an expert system which can recognize and classify objects or situations and take instantaneous decisions based upon accumulated knowledge. ZISC does not need to be programmed, it does not even require rules to work from, as it learns 'by example' from samples of data. The built-in learning mechanism just requires to enter pairs of examples and solutions. ZISC generalization capability allows it to react correctly to objects or situations which were not part of the learning examples.

ZISC learning capability is not limited in time, as opposed to other implementations. ZISC is always capable of additional learning while performing classification tasks.

ZISC learning capability is not limited in volume; thanks to the full cascadability of chips. This feature is very important as it ensures that the system architecture will not change when more neurons become available on chip, as technology density increases. With ZISC, cascadability means several chips can be associated together to build a wider network, without additional logic. Only re-powering devices may be required if the number of chips exceeds eight. Extension of the network by cascading chips does not affect the classification or learning performances.

These features make the ZISC very easy to operate, capable of solving non-linear or not exactly defined problems.

ZISC robustness when processing incomplete, noisy or polluted data, associated with its performance, makes it suitable for signal processing, with its ability to separate noise from the signal.

ZISC036 can provide innovative and low-cost solutions in many domains such as:

- *Image recognition (security, military, satellite, factory automation, quality control, medical)*
- *Image compression (data storage)*
- *Video compression (video conferencing, video storage)*
- *Character recognition (printed, hand-written)*
- *Voice processing (recognition, synthesis from text)*
- *Signal recognition (radar, sonar, biological, voice, engine noise diagnostic)*
- *Data analysis (statistics, finance, risk assessment, stock trading)*
- *Robotics*
- *Equipment monitoring (industrial, medical)*
- *Database navigation*

2•2 ZISC036 FEATURES

ZISC036 is a fully integrated, digital implementation of the RBF-like (Radial Basis Function) model.

One ZISC036 device hosts 36 neurons, but due to its cascadability the total number of neurons in a network is not limited.

Each neuron features a register file for prototype storage, and a distance evaluation unit to ensure a high level of parallelism.

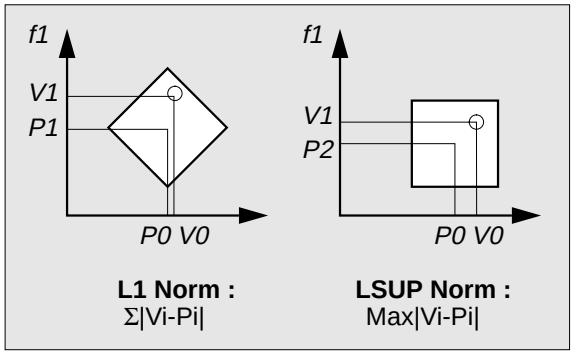


FIGURE 4. Effect of Norm L1 or LSUP

Up to 16,382 different categories can be defined in the network.

ZISC036 is capable of identifying a vector within a one to 64 dimensional space, each component of the vector is coded on an 8-bit number.

Distance can be computed according to two selectable norms L1 and LSUP as shown in fig 4.

- *NORM L1:* $dist = \sum_{k=1}^{64} abs(Vk - Pk))$

  which corresponds to a polyhedral volume influence field, where V and P represent the input vector and the stored prototype, and i the component index within the vector.

- *NORM LSUP : dist = Max(abs(Vi - Pi)) which corresponds to a hyper-cube influence field.*

The maximum and minimum size of the influence fields is under application control. Two internal resources 'Maximum Influence Field' and 'Minimum Influence Field' are accessible for that purpose. (see chapter 4 and 5 for detailed operations).

The Maximum Influence Field defines the maximum setting value when a neuron is committed by the learning process to store a new prototype. This value is set for the new neuron if no constraint is given by the neighbourhood.

The Minimum Influence Field defines the minimum setting value when an influence field reduction occurs, due to the learning process. When a neuron influence field is reduced and limited to this value, this generally means that the neuron prototype lies close to the boundary of its category space, and may be largely overlapped by another category space. The neuron is said 'degenerated' and a special flag is set to identify such a case.

In ZISC036, distance calculations are carried on 14 bits.

For ZISC036 to perform a classification, the vector components are fed in sequence. and processed in parallel by every neuron.

With a ZISC operating at 20MHz, 64 components can be fed and processed in 3.2 µs and the evaluation achieved within 0.5 µs after the last component has been fed. This level of performance allows more than 250,000 evaluations per second.

It would require a 2,000 MIPS machine to achieve the same level of performance on a Von-Neuman processor.

2•3 Nearest neighbours feature

ZISC036 allows efficient neighbourhood analysis around a set of data. A the specific 'K' Nearest Neighbours (KNN) mode ZISC036 calculates the distances between an input vector and the stored prototypes. Distance calculation is performed in parallel, the same way as for a normal evaluation. An efficient built-in sorting mechanism allows ZISC to deliver pertinent information by ascending order of distance. Distances and associated categories can be read from ZISC036 at a rate of one pair of distance and category per two microseconds.

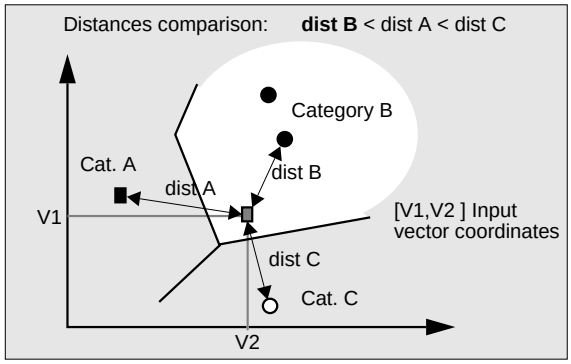


Figure 5 (KNN) K-Nearest Neighbours classification

2•4 Save/ Restore function

A Save/Restore function which allows the content of the network to be saved, to restore it and possibly clone the knowledge to another network is available in ZISC036.

2•5 ZISC CIRCUIT DIAGRAMS

2•5•1 Chip block diagram

Figure 6 shows a block diagram of the ZISC036 chip that illustrates how the neurons are connected and how to access them.

A 16-bit data bus handles input vectors as well as other data transfers (as Category and Distance) and chip controls.

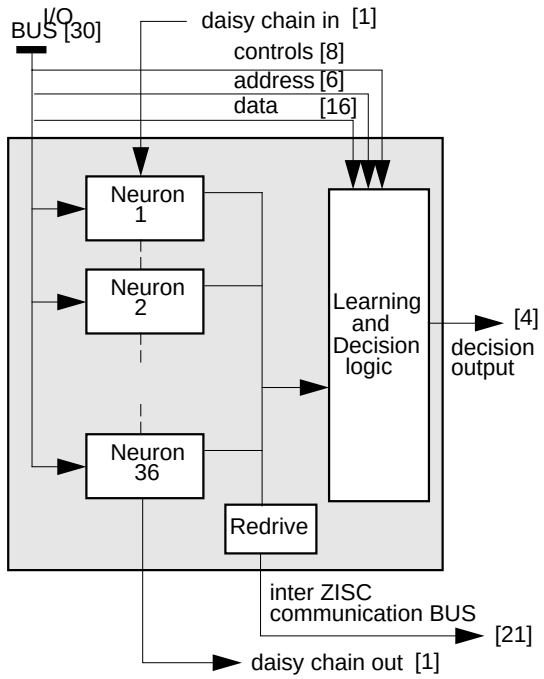


FIGURE 6. ZISC036 block diagram

Control access to various data in the network is performed through a 6-bit address bus.

The inter-ZISC communication Bus is used to connect several devices in parallel within the same network.

The decision bus which carries classification information allows the use of the ZISC in a stand alone mode.

2•5•2 Neuron block diagram

The neuron block diagram is shown in figure 7.

Each neuron has a memory to store one prototype along with the associated influence field and category.

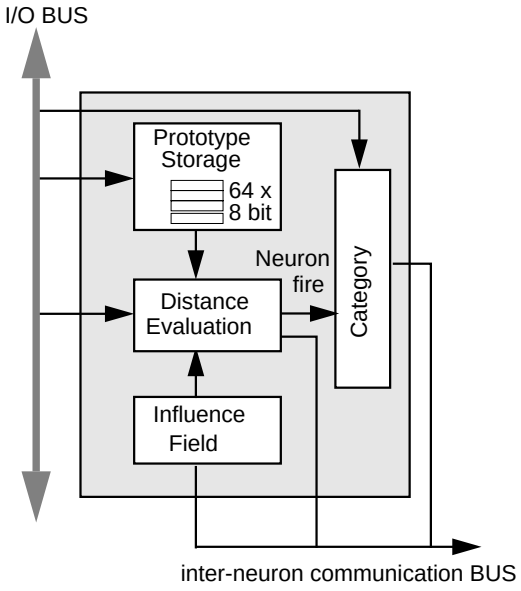


FIGURE 7. Neuron Block Diagram

Each neuron has its own logic to perform distance calculation and comparison with the influence field and to handle the built-in learning process.

2•6 DAISY CHAIN

A daisy chain connects all neurons of the chip. This feature is used to manage the commitment of new neurons during the learning process. The daisy chain works across devices in case of multi-device networks.

2•7 NEURON CONNECTIVITY

All neurons communicate together via the 'Inter-ZISC communication Bus'. An efficient protocol allows a true parallel operation of all neurons of the network including learning.

The 'Inter-ZISC communication Bus' is internally redriven to allow connection of several ZISC modules, without impact on performance.

2•8 MULTI-DEVICE CONNECTIVITY

The ZISC family is designed to extend the neural network beyond the boundary of a single chip without impact on performance.

Physical implementation guidance is discussed in chapter 7.

Some applications can also benefit from multi-layer configurations where decisions of a layer can feed the input features of a second layer. This can be achieved either by connecting several chips or by using subsets of the network operating in a time-multiplexed mode.

2•9 CONTEXT FEATURE

A context feature is available on ZISC036, which allows the sub-setting of neurons of a single device or of a multi-device network into independent clusters.

Context is managed by a user-accessible seven-bit resource called ‘GLOBAL CONTEXT’.

Each neuron belongs to the context value set in Global Context when it is committed by the learning process.

In recognition mode, only neurons belonging to the current global context are exercised. However, if Global Context is set to zero, all neurons are exercised whatever context they belong to. Up to 127 different contexts can be defined in a network of ZISC036.

Contexts can correspond to different vector size, and heterogeneous characteristics. In case of using context ‘ZERO’ to cluster several contexts, it is highly recommended that all contexts have the same vector size and have homogeneous characteristics.

2•10 I/O BUS

The I/O bus of ZISC036 has been designed to allow a wide variety of attachments from simple state machine interface to standard microcontrollers or bus. The choice is given to the user:

- *To allow for full hand-shaking or synchronous protocols.*
- *To interface with big or little Endian conventions.*

I/O bus protocols are detailed in chapter 6. Examples of connection to standard controllers and bus are given in chapter 7.

CHAPTER 3

Registers

3 - REGISTERS DESCRIPTION

ZISC036 has two categories of register:

Global Registers holding information for the device (or full network when several devices are cascaded). These registers are referred to as G in the following table.

Neuron Registers holding local data for each neuron. These registers are referred to as N in the following table.

Global Registers can be individually accessed in read or write mode whatever the status of the device. Neuron Registers access differs depending on the bit-9 of the Control and Status register (Save/Restore Mode). Register access is discussed at the end of this chapter.

When ZISC036 devices are connected in single network, Global registers are synchronized to hold the same content on every device, thanks to a bi-directional data bus automatically managed. A write operation is sent to all devices. For read operation, only one device of the cascaded devices, selected by wiring (see chapter 6), is physically accessed.

Table 1: ZISC Registers

Register Name	Acronym	G/N
Control & Status register	CSR	G
Vector Component Register	VCR	G
Global Context Register	GCR	G
Min. Influence Field	MIF	G
Max. Influence Field	MAF	G
Neuron Weight Register	NWR	N
Neuron Context Register	NCR	N
Category	CAT	N
Distance	DIST	N
Neuron Actual Influence Field	NAIF	N

3•1 GLOBAL REGISTERS

3•1•1 Control and Status Register (CSR)

The control and status register holds information related to device operation. Its layout is shown in the following table.

Table 2: Control and Status Register (CSR)

Bit	Acronym	Name	Notes	
15	ERR	Error	Set to one if any error occurs . Reset by the next read status operation. or by CLEAR signal.	R/O
14	DEG	Degenerated flag	Modified only during the learning process (WRITE CAT). Set to one if a neuron is 'degenerated'. Set to Zero in the other cases	R/O
13	UNC	Unclassified flag	- Set to one if at least two neurons with different categories have fired simultaneously. - Set to zero after a put CAT when a new neuron is engaged and if the category is different to zero. - Reset by the following WRITE COMPONENT	R/O
12	FULL	Network full flag	Set to one when no further neuron is available in the network, following a learning action, or during a Restore operation. Reset by CLEAR signal.	R/O
11	ID	Identified signal	Set to one when all firing neurons belong to the same category. Reset by the following WRITE COMPONENT	R/O
10	TST	Reserved	This bit must be forced to zero by any write status operation.	R/W
9	SR	Save/ restore mode	Controls the Save/Restore mode setting. (see section 4.3). SR=0, Normal mode SR=1, Save/ Restore mode R/W	
8	KNN	KNN mode	KNN=0 sets the RBF-LIKE MODE KNN=1 allows to access all neurons of the context whether they have fired or not and get distance between all prototypes and the Input Vector.	R/W
7	SM	Synchronous Mode	Defines the protocol to be used in transferring characteristics to the network. SM=0, Asynchronous Hand shaking protocol. SM=1, Synchronous protocol or burst mode. (see section 6.4)	R/W

Table 2: Control and Status Register (CSR)

Bit	Acronym	Name	Notes	
6	SBY	Stand By mode	When set to one , stops internal chip activity to save power. Chip is restarted by writing the status again with bit SBY =0. (see section 6.9)	R/W
5	SCHP	Several Chips	This bit must be set to one by user when two or more devices are cascaded. In Save/Restore mode , this bit should be set to zero, whatever the number of chips are in the network.	RW
4	reserved		must be left to zero	R/W
3	reserved		must be left to zero	R/W
2	reserved		must be left to zero	R/W
1	reserved		must be left to zero	R/W
0	reserved		must be left to zero	R/W

CSR is set to x'0000' by reset.

Access to CSR will be referred to as either

- *READ STATUS*
- *READ / WRITE GSR*

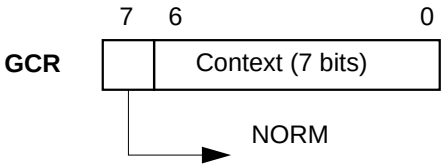
3•1•2 Vector Component register (VCR)

This 8-bit register holds the 8-bit integer value of the current component of input vector for the evaluation process. Its content is broadcast to all neurons of the device. All components of the input vector must be written in sequence into VCR (see chapter 4 for mode of operation).

Access to that register will be referred to as:

- *WRITE COMPONENT or*
- *WRITE LAST COMPONENT.*

3•1•3 Global Context Register (GCR)



The context number allows the network to be divided in several subsets of neurons. Up to 127 contexts can be defined.

When a new neuron is committed, following a write category operation, it is given the context value stored in the GCR. For any operation in normal mode, only the neurons having the same context as the GCR are activated.

When GCR is set to 0, all neurons are activated whatever their specific context.

The Norm defines the function to be used for distance calculation between incoming vector and prototype stored in each neuron. Two norms are supported by ZISC036 architecture:

- *L1 where d= S |Vi - Pi | for Norm = b'0'*
- *LSUP where d = Max.|Vi-Pi | for Norm = b'1'*

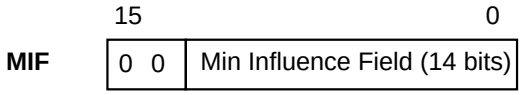
Neurons operate with the Norm value held in the GCR when they are committed. Bit 7 of GCR is OR'ed with Device Norm input, so norm Lsup can be forced from input pin.

The GCR can be written any time, but not during a recognition or learning process.

Access to that register will be referred to as

- *SET/GET CONTEXT REGISTER*
- *SET/GET NORM*
- *SET/GET CONTEXT*

3•1•4 Minimum Influence Field (MIF)



This register holds the minimum value of Influence Field which can be set in a neuron by the learning mechanism.

The value is coded in a 16-bit binary format.

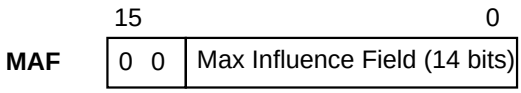
Its value is limited within the range 0 to +16383. (x'0000' to x'3FFF').

MIF is set to x'0002' by the CLEAR signal:

Distinct MIF values can be associated to distinct contexts. In such a case, MIF has to be rewritten each time the GCR is modified.

Access to that register will be referred to as SET/GET MINIF.

3•1•5 Maximum Influence Field (MAF)



This register holds the maximum value of Influence Field which can be set in a neuron by the learning mechanism.

The value is coded in a 16-bit binary format.

Its value is limited within the range 0 to +16383. (x'0000' to x'3FFF').

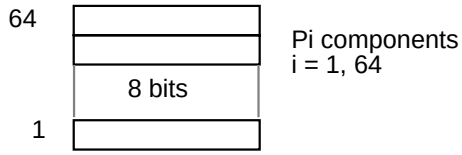
MAF is set to x'1000' by the CLEAR signal.

To ensure a correct operation of the neuron network there must be only one MIF/MAF value set per context, and the MAF must be greater than the MIF in each set, in such a case MAF has to be rewritten each time the GCR is modified.

Access to that register will be referred to as SET/GET MAXIF.

3•2 NEURON REGISTERS

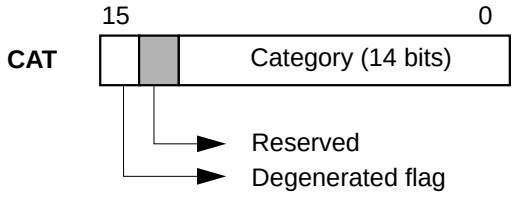
3•2•1 Neuron Weight Register (NWR)



In each neuron, a register file holds the prototype coordinates Pi by means of 64 components of 8-bit integer. Values are set when the neuron is committed. User access to that register is indirect and is only possible in Save/Restore mode. For this reason, it shares the same address and commands, and its access will be referred to as:

- *PUT COMPONENT*
- *PUT LAST COMPONENT*
- *PUT/GET NCOMPONENT*
- *PUT/GET NPROTOTYPE*
- *PUT VECTOR*
- *PUT COMPONENTS*
- *PUT/GET NLAST COMPONENT*

3•2•2 Category Register (CAT)



In each neuron, a register holds the category associated to the prototype weights.

The CAT is automatically loaded when the neuron is committed. CAT can be read and written in save/restore mode and can be reset only by the CLEAR signal.

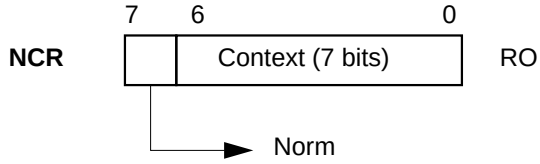
Only 16,382 categories are valid (x'0001' to x'3FFE'). Category x'0000' and x'3FFF' are reserved values.

Bit 15 of the Category Register is set when the neuron gets degenerated, but it can also be written in Save/Restore mode.

Access to that register will be referred to as

- *GET CAT*
- *GET/PUT CAT REGISTER*
- *GET DEG*

3•2•3 Neuron Context register (NCR)



In each neuron, a register holds a context value and a Norm type. The Neuron Context number is a way to select Sub-Networks of Neurons solving the same problem.

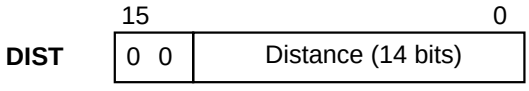
Up to 127 contexts can be defined.

The Context values and the Norm are set from the Global Context Register (GCR) during a write category operation.

Writing to NCR is handled by ZISC internal mechanism, so the register can be considered as user readable only and access to that register will be referred to as

- *GET NNORM*
- *GET NCONTEXT*
- *GET NCONTEXT REGISTER.*

3•2•4 Distance register (DIST)



For each neuron, a register accumulates an integer absolute value representing the global distance

$$\Sigma\,|Vi\text{-}Pi| \quad or\ Max\,|Vi\text{-}Pi|$$

computed in accordance with the neuron Norm;

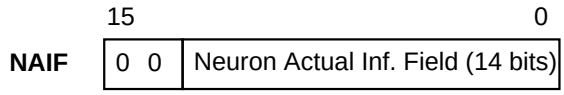
(L1 or LSUP)

The Distance Register is automatically reset at the beginning of an evaluation process when the first component is entered.

The distance is represented in 16-bit integer format and can range from 0 to 16,383 (x'0000' to x'3FFF').

The Distance register is user readable only and its access will be referred to as GET DIST.

3•2•5 Neuron Actual Influence Field Register (NAIF)



For each neuron, a register holds the actual influence field used as the threshold for a Fire/No Fire decision after the global distance

$$\Sigma\,|Vi\text{-}Pi\,| \qquad or\ Max\,|Vi\text{-}Pi\,|$$

has been computed.

It is automatically set when the neuron is committed. The setting value depends on the neighbourhood (proximity of other prototypes). If no constrain exits, it is set to MAF value.

NAIF is automatically reduced, by the learning process, if required, in function of the neighbourhood. Automatic NAIF reduction is however limited to MIF value.

The neuron influence field is represented in 16-bit integer format and can range from 0 to 16,383 (x'0000' to x'3FFF').

NAIF can only be read or written in Save/Restore mode.

Access to NAIF will be referred to as GET/PUT NAIF

Table 3: Binary and Hexadecimal Address correspondence

Hexadecimal	High		Low order Hex. Digit			
	A(5)	A(4)	A(3)	A(2)	A(1)	A(0)
x'02' x'03	0	0	0	0	1	X
x'04' x'05'	0	0	0	1	0	X
x'06' x'07'	0	0	0	1	1	X
x'0C' x'0D'	0	0	1	1	0	X
x'10' to x'1F'	0	1	0	0	0	0
x'20'	1	0	0	0	0	0
x'22'	1	0	0	0	1	0
x'30'	1	1	0	0	0	0
x'32'	1	1	0	0	1	0
x'34'		1	1	0	1	0
x'36'		1	1	0	1	1
x'00'		0	0	0	0	0

.

3•3 REGISTER ACCESS BY USER

Register access is controlled by a 6-bit address bus. Global registers are directly accessed, neuron registers are accessed one neuron at a time by register type (one address per type of register). Individual neuron selection is based upon a chaining scheme automatically set up for the chip or the cascade of chips (See section 4.5 Neuron Data Access for more details).

The following tables give the addresses for each register type, as well as possible read/write operations in normal and save /restore.

Table 4: Addresses and possible operations

address	Normal Mode		Save/Restore Mode		data length	command acronym
	Register accessed	access allowed	Register accessed	access allowed		
x02-03	GCR	R/W	GCR	R/W	byte	READ/WRITE CONTEXT
x04-05	VCR	Write	VCR	R/W	byte	READ/WRITE-COMPONENT
x06-07	NCR	Read	NCR	Read	byte	READ NEURON CONTEXT
x0C-0D	VCR (note 1)	Write	VCR	R/W	byte	READ/WRITE LAST COMPONENT
x10-1F	reserved (note 4)	Read			byte	Reserved use
x20	MIF	R/W	MIF	R/W	word	READ/WRITE MIF
x22	MAF	R/W	MAF	R/W	word	READ/WRITE MAF
x30			NAIF	R/W	word	READ/WRITE NAIF
x32	CSR	R/W	CSR (note 3)	R/W	word	READ/WRITE CSR
x34	DIST	Read			word	READ DIST
x36	CAT (note 2)	R/W	CAT (note 2)	R/W	word	READ/WRITECAT
x00	note 5					Forbidden

Note 1 Accessing addresses x'OC' or X'OD' triggers evaluation operation in normal mode. (see chapters 4 & 6)

Note 2 Accessing CAT triggers the learning mechanism or prepare access to the next neuron (see chapter 4)

Note 3 In Save /Restore mode Read CSR sets access to the first neuron. (see chapter 4)

Note 4 A read operation at address x'10' returns x'00'

Note 5 Access to that address will cause unexpected results.

CHAPTER 4

Mode Of Operation

4 - MODE OF OPERATION

This chapter explains the principles of ZISC036 processes for:

- *Recognition/Classification.*
- *Self-Learning.*
- *Save/Restore.*

4•1 INITIALIZATION

Hardware initialization of the network is required prior to operation, after ZISC devices have been powered up. Hardware initialization is done activating the CLEAR signal. CLEAR signal must be activated for a minimum of six clock periods, to operate properly. (see section 5.2.1.1)

4•2 RECOGNITION / CLASSIFICATION

4•2•1 Vector input feeding

Each component of the feature vector is fed in sequence to the network by means of WRITE COMPONENT.

Vector feeding protocol depends on the SM bit of the CSR, or the SM input pin level (see section 6.4). The classification process is automatically completed by ZISC036 after the last component has been fed.

4•2•2 Distance computation flow

As vector components are fed in sequence to the network, each neuron computes the absolute distance |Vi - Pi | between each component and corresponding prototype coordinate stored in its NWR. The result is accumulated in the neuron Distance Register (DIST), in accordance with the norm L1 or LSUP recorded in the Neuron Context Register (NCR).

4•2•3 Neuron Response

Once the last component has been fed, DIST is compared to the Neuron Actual Influence Field Register (NAIF). Every neuron, for which DIST< NAIF and Neuron Context equals Global Context, fires automatically.

If Global Context equals zero, all neurons are subject to fire whatever their specific context is.

4•2•4 Network Response

For a device operating at 20 MHz, network response requires only one half a microsecond after the last component has been fed.

At the end of the evaluation process, decision group signals (ID, UNC_, NID, DEG_) and bits UNC and ID of the CSR are set according to neuron responses. Categories of all firing neurons are screened:

If all categories are identical, the ID signal and the ID bit of the CSR are set. In addition, if one of the firing neurons is degenerated (CAT bit 15 =1) the DEG_ signal is set.

If firing neuron categories are different (at least two categories), the UNC_ signal and the bit UNC of the CSR are set.

If no neuron has fired the NID signal is set and the ID and UNC bits of the CSR are set to ‘0’.

The application can check the result of the evaluation either by monitoring the output signals or by reading the CSR.

Above signals and CSR bits will be reset as soon as a component of a new vector is fed.

4•2•5 Category and distance output

DIST and CAT information for every firing neuron can be accessed by the application. Subsequent READ DIST and READ CAT will access to neuron data in the sequence order detailed in section 4.5. A returned value of x’3FFF’ has a special meaning, defining end of read sequence.

4•2•6 K Nearest Neighbour mode

If the KNN bit of the CSR is set to one, neurons are inhibited to fire at the end of the evaluation process. However neurons, belonging to the Global Context, (Neurons for which NCR equals GCR) compute the distance between

the input vector and their prototype. Calculated distance and categories associated to neurons can then be read by the application in ascending order of distance (see 4.5, Neuron Data Access).

If Global Context =0 all neurons perform the calculation.

The signals ID, NID, UNC_ and DEG_ are not activated, nor the bits ID, UNC and DEG of the CSR.

4•3 LEARNING

An RBF-like learning mechanism is implemented in ZISC036 with a very simple user interface scheme.

Triggering the ZISC036 learning mechanism just requires to write the correct category, by a WRITE CAT command, once the evaluation of input vector has been completed.

For a proper operation of the learning mechanism the KNN bit of the CSR must be set to zero prior to the evaluation.

The ZISC036 learning mechanism may be active at any time and is triggered by WRITE CAT operation. This normally occurs during the initial learning process, or possibly, under supervision of the application, as a result of an evaluation, to refine the knowledge.

The learning mechanism automatically manages NAIF reduction and/or new neuron commitment depending on the input vector position, with regard to prototypes already stored in the network. Such a process is completed in less than one microsecond for a device operating at 20MHz.

Neuron commitment is controlled by a Daisy Chain linking all neurons of the ZISC036. The Daisy Chain ends are connected to I/Os for multi-device network extension.

4•3•1 End of chain neuron pre-charge

While the vector components are fed into the ZISC036 and processed by committed neurons, they are also stored in the Neuron Weight Register (NWR) of the first free neuron in chain, as a potential new prototype. That free neuron is then ready to be committed, if required by the learning mechanism.

4•3•2 New neuron commitment

The first available neuron in a chain, referred as new neuron, will be committed if the category written is different from any category of the firing neurons.

The new neuron NAIF is set as the minimum distance between input vector and prototypes of all neurons already committed in the present context. This value is clamped by MIF and MAF. The new Neuron Context Register is loaded with the Global Context Register content.

Writing CAT with x' 0000' has a specific behaviour, it triggers NAIF reduction as described in the following section without selecting the new neuron.

4•3•3 NAIF reduction

An NAIF reduction occurs for firing neurons which do not belong to the written category. NAIF of such neurons is reloaded with the distance between the neuron prototype to the input vector.

However, neurons for which the distance is smaller than the MIF, have their NAIF set to the MIF value.

4•3•4 Degenerated flags setting

Degenerated flags (DEG) indicate that the MIF value has been used instead of a distance, following a Write CAT operation.

If that occurred for at least one neuron, the DEG-bit of the CSR is set.

The bit-15 is set in the Category Register (CAT) for every neuron which NAIF reduction is limited by MIF.

4•3•5 Chip Full flag

When the last neuron of a device is committed, the DCO signal is asserted for the next device to operate. In case of a single device, (or the last device in a row within a multi-device network) the bit 'FULL' of the CSR and the output signal 'FULL' are set.

4•4 SAVE/RESTORE AND KNOWLEDGE TRANSFER

The Save/Restore mode allows :

- *Using the same ZISC for different applications.*
- *Saving the ZISC content before powering down.*
- *Loading a network with a pre-established knowledge.*

Save/Restore mode is entered by setting the SR-bit of the CSR.

In Save/Restore mode neuron registers can be individually accessed to transfer the network content. Save/Restore mode allows read/write operations from/to the following neuron registers:

Neuron Weight Register (NWR), Neuron Actual Influence Field (NAIF) and Neuron Context Register (NCR).

4•4•1 Save

Saving network content consists of reading and storing out the global registers, and then the neuron registers, neuron by neuron. Neurons are accessed according to the daisy chain order.

In Save/Restore mode, the Daisy Chain pointer is reset to the first neuron by READ CSR operation. Neuron registers can be then read in sequence, Category Register (CAT) is the last register to read for a neuron as READ CAT increments the Daisy Chain pointer. If there are free neurons in the network, the value x'0000' returned by READ CAT indicates the first neuron not committed by the learning process. It is not necessary to pursue the save operation of the following neurons as they hold meaningless data.

Once the process of saving neuron registers has been started, no READ CSR should be performed until the last neuron content has been saved. Violation of that rule would result in the reset the Daisy Chain pointer to the first neuron.

Fig 8. shows a typical Save sequence.

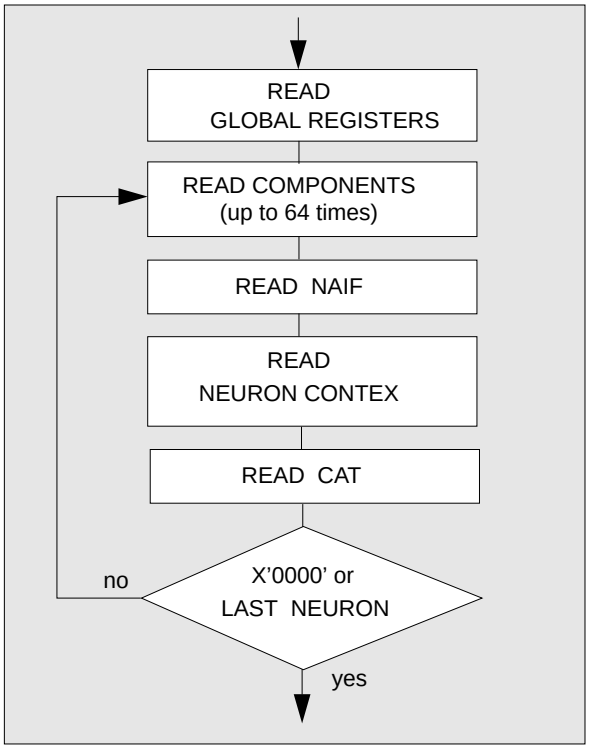


FIGURE 8. Typical Save Sequence.

4•5 Restore

Restoring or 'cloning' a network content consists of writing the global registers, and then the neuron registers, neuron by neuron. The neuron pointer is incremented every time a WRITE CAT is performed so network data can be restored in the same order they were saved. Note the WRITE CAT operation also transfers the GCR into the selected Neuron NCR. A READ CSR operation must be performed prior to restore the registers of the first neuron.

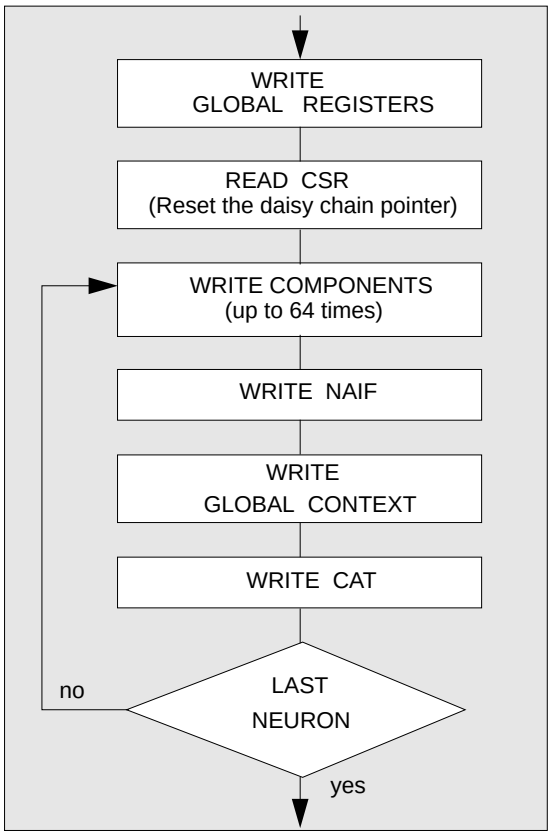


FIGURE 9. Typical Restore sequence

Once the process of restoring neuron registers has been started, no READ CSR should be performed until the last neuron content has been restored. Violation of that rule would result in the reset of the Daisy Chain pointer to the first neuron.

Fig 9 shows a typical Restore sequence.

4•6 NEURON SELECTION FOR DATA

ACCESS

In Normal mode, each evaluation sets an hidden list making pertinent neurons accessible in sequence, neuron by neuron.

Neuron set in the list by an evaluation are:

- *Firing neurons if KNN-bit of the CSR equals zero.*
- *All neurons belonging to the Global Context if KNN-bit of the CSR equals one.*

READ CAT and READ DIST operations manage the list of neurons set by the evaluation, as follows:

READ CAT returns the lowest category present in the list and eliminates corresponding neuron(s) from the list. Subsequent READ CAT returns next category in ascending order. A returned value of x'3FFF' means that the list is exhausted. READ DIST returns the distance of the closest neuron(s), in the list and generates a 'sub-list' of equidistant neuron(s). This generation of sub-list allow exploration of neurons by mixed sequences of READ DIST and READ CAT. A first READ DIST returns the distance of the closest neuron(s). READ CAT returns the lowest category within the sub-list and excludes the corresponding neuron(s) from the sub-list. Subsequent READ CAT return the categories present in the sub-list, in ascending order. X'3FFF' returned as a category means that no other neuron lies at the current distance. A new READ DIST returns the next distance within the remaining neuron(s), and generate a new sub-list. The process can be iterated until READ DIST returns a distance of x'3FFF' meaning that the list of relevant neuron(s) is exhausted.

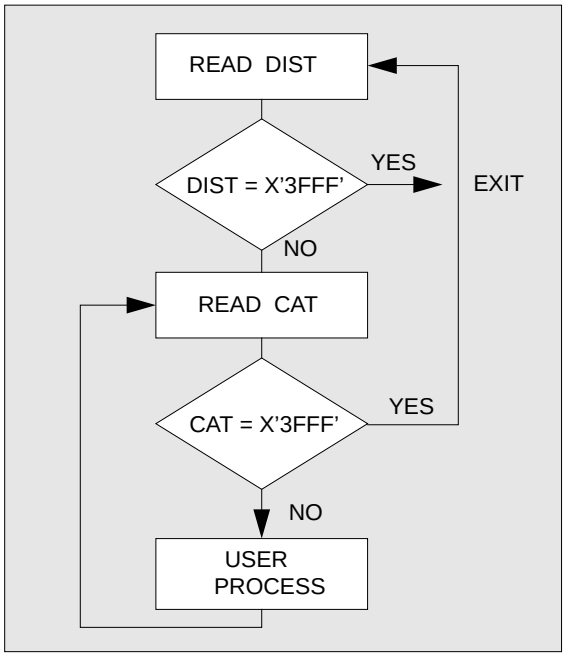


FIGURE 10. Mixed use of READ DIST & READ CAT

Fig 10 shows a typical example of using a mixed sequence of READ DIST and READ CAT. NAIF and NCR of selected neuron(s) are also readable via a READ NAIF or READ NCR command. In case there is more than one neuron in the list or sub-list, the returned value corresponds to the logical AND of register contents. It is user responsibility to ensure that only one neuron is present or that returned value is meaningful for the application. This is the case, for example, when there is one neuron per category.

In Save/Restore mode, neuron pointer initialization is performed by any READ CSR, and incremented by READ/WRITE CAT. Increment only occurs if the bit SCHP of the CSR is reset to zero. Neuron order is fixed and determined by the daisy chain. First meaningless neuron (not committed) returns a category x'0000'.

No READ CSR operation should be executed after initialization until the last neuron data has been correctly saved/restored. Violation of that rule will result in the reset of the neuron pointer, giving an unwanted access to the neurons already processed.

4•6•1 Neuron data access summary

The following table summarizes neurons access and ordering according to the network status.

Table 5:

operation	save/restore SR bit=1 SCHP bit = 0	Recognition Mode SR bit=0, KNN bit=0	KNN Mode SR bit=0, KNN bit =1
accessible neurons	All	Firing Neurons	Neurons belonging to Global Context
accessible neuron registers	All	CAT, DIST, NCR, NAIF (1)	CAT, DIST, NCR, NAIF (1)
neuron access order	Daisy Chain	Ascending order of Distance and/or Category	Ascending order of Distance and/or Category
pointer initialization	READ CSR	evaluation process complete	evaluation process complete
pointer increment	READ CAT WRITE CAT	READ CAT READ DIST	READ CAT READ DIST
end of chain indicator	CAT='0000'	CAT='3FFF'	CAT='3FFF '
Note 1: READ NCR and READ NAIF return the logical AND of pointed neuron registers.			

CHAPTER 5

Signal Description

5 - SIGNAL DESCRIPTION

This Chapter describes the ZISC036 module external signals. It contains a concise description of individual signals, showing behavior when the signal is asserted or negated, and when the signal is bi-directional.

NOTE :
A bar at the end of a signal name indicates that the signal is active low (such as AS_ : Address Strobe). Active low signals are referred to as asserted (active) when low, and negated when they are high. Signals that are not active low, such as SM (Synchronous Transfer Mode), are referred to as asserted when they are high and negated when they are low.

5•1 SIGNAL TYPES :

The ZISC036 input and output signals can be functionally organized into groups as shown in Figure 11. The signal functions are described in the following paragraphs.

- *System Control Group: This group includes the Clear signal, the Interface Bus Inhibit signal, the Norm Choice signal, the Synchronous Transfer Mode signal and the Stand-by Mode signal.*
- *Address Transfer Group: This group includes the Address Bus, the Chip Select, the Address Strobe and the Address Acknowledge signals.*
- *Data Transfer Group: This group includes the Data Bus and the Read/Write, the Data Strobe, the 16 Bit Port, the Wait and Ready signals.*
- ***Inter-ZISC Communication Group**: This group includes the signals for neuron communication and network extension over ZISC036 devices. Four signals of this group (ID, NID, UNC_, DEG_) summarize the evaluation process and constitute the Decision Status. This decision status can be used by the application, instead of reading the CSR, to have the overall result of an evaluation. Two signals (ERROR and FULL) summarize the network status. - In a single device network the unused pins corresponding to the inter-ZISC communication group can be left unconnected, with the exception of the following signals: NID, NIDIN, UNC, UNCIN_, DEG_, DEGIN_, DCI. (refer to individual signal sections and chapter 7 "INTERFACING TECHNIQUES").*
- *Clock Signal: This signal determines the system clock frequency.*
- *Test Interface Group: Reserved for manufacturing test and can be left unconnected.*

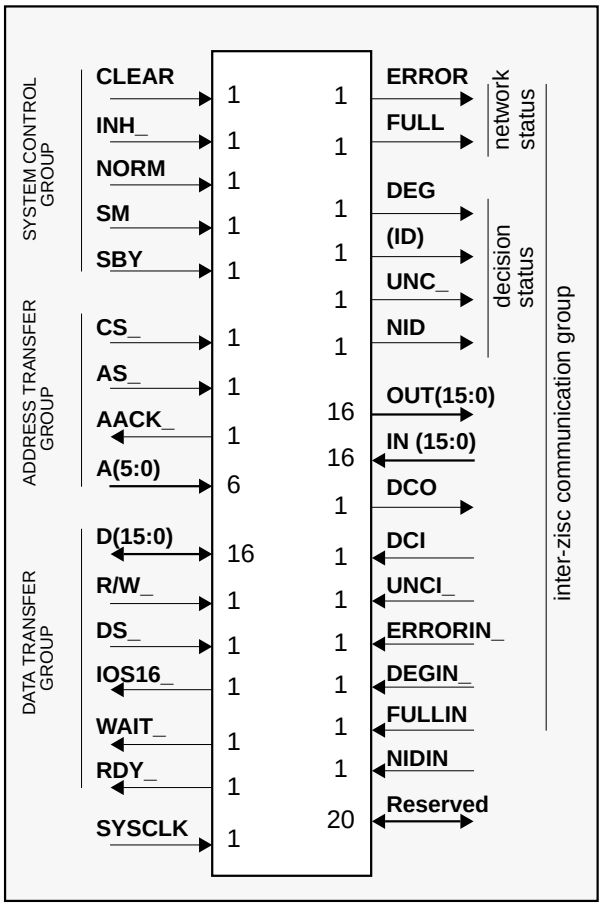


FIGURE 11. : ZISC036 Signal groups

5•2 SIGNAL DESCRIPTION:

This section describes individual ZISC036 signals, grouped according to figure 11. Note that the following sections are intended to provide a quick summary of signal functions. Chapters 6 ,"I/O Bus and Access Protocols" and 7 "Interfacing techniques", describe some of these signals in greater detail, with respect to both individual signals function and signal interaction.

5•2•1 System Control group :

System Control Group signals are input signals either to reset the ZISC036 chip, or select a specific operation mode.

(1) Reset : CLEAR

The hard reset signal (CLEAR) is input only and must be used at power-on to reset correctly the Neural Networkl.

- *State meaning :*

Asserted -- Initiates a complete hard reset operation and clears registers as described in Chapter 3, "Register description".

Negated -- allows operations to proceed.

- *Timing comments :*

Assertion -- May occur at any time and may be asserted non-synchronously to the ZISC036 input clock.

Negation -- May occur at any time if the minimum reset pulse width has been meet. (Minimum pulse width is six system clock cycles).

(2) Interface Bus Driver Inhibit : INH

The Interface Bus Driver Inhibit (INH_) signal is input only and defines which ZISC036 module may drive the Data Transfer Bus in a multi-device Neural Network. Only this specific device may drive the Data Bus, but during a Write operation.

- *State meaning :*

Asserted -- Indicates the Bi-directional I/O Bus drivers are disabled (High Impedance State).

Negated -- Indicates that this specific ZISC036 device drives the Interface Bus.

- *Timing comments :*

Assertion/Negation -- This signal is normally hard wired at card level.

(3) Norm Choice : NORM

The Norm Choice (NORM) signal is input only. It defines the distance calculation to be used by any new neuron committed by the learning process. This input has no impact during the recognition process. Note that this input is internally OR'ed with Bit-7 of the Global Context Register. All necessary cares must be taken if both norms were used in the same network, the learning mechanism does not normally supports norm mix. A safe rule is to associate each norm to a specific Context value different from zero.

- *State meaning :*

Asserted -- Forces LSUP norm for any neuron committed.

Negated -- Leaves the control to bit-7 of the GCR.

- *Timing comments :*

Assertion/Negation -- This input is sampled every low state clock cycle. The selection of desired norm must be carefully performed outside the learning sequence to not perturb functionality . A safe rule is not to change the polarity of this pin while an evaluation or a learning process is in progress.

(4) Synchronous Multiplexed Mode: SM

The Synchronous Multiplexed Mode (SM) signal is input only and defines protocol used on the Interface Bus. Note that the function induced by asserting this pin is different from the one defined by Bit-7 of the Control and Status Register, which defines a burst mode with totally independent Address and Data Strobes. PCI-like Synchronous Multiplexed Mode implies only one bus and one strobe is used to transfer Address and Data . Pin function supersedes the Control and Status Register setting.

- *State meaning :*

Asserted -- Indicates that a Synchronous Multiplexed bus (PCI-like) interfaces the ZISC.

Negated -- Indicates that a separate address and data bus interfaces the ZISC. Asynchronous/Synchronous protocol is function of the CSR bit-7.

- *Timing comments :*

Assertion/Negation -- This input is intended to be wired as a function of the interface protocol. No signal transition should occur when the device is operating.

(5) Standby Mode : SBY

The Standby Mode (SBY) signal is input only. It allows to reduce ZISC036 power consumption when it is not operating. SBY controls internal clock distribution shut off and sets chip drivers to High Impedance State. It is recommended to set SBY signal in conjunction with the software Standby Mode (Bit 6 of the Control and Status Register) before activating SBY signal. (See section 6.9).

- *State meaning :*

Asserted -- Forces the device in power saving mode.

Negated -- allows device normal operation.

- *Timing comments :*

Assertion/Negation -- This input is sampled every low state clock cycle. To prevent from incorrect operation, the SBY signal transitions must occur when Chip Select (CS_), Address Strobe (AS_) and Data Strobe (DS_) are negated.

5•2•2 Address Transfer Group :

The Address Transfer group signals are used to transmit the address and to monitor the address transfer. For a detailed description of how these signals interact, refer to chapter 6 “I/O Bus and Protocols”.

(1) Chip Select : CS

The Chip Select (CS_) signal is an input signal on the ZISC036.

This signal must be connected to all devices in case of a multi-device network..

- *State meaning :*

Asserted -- The Chip Select (CS_) signal selects the Neural Network for bus transaction.

Negated -- The Interface Bus of the Neural Network is in High Impedance state.

- *Timing comments :*

Assertion/Negation -- This input is sampled every clock cycle.

(2) Address Strobe : AS

The Address Strobe (AS_) signal is an input signal on the ZISC036. This signal must be connected to all devices in case of a multi-device network.

- *State meaning :*

Asserted -- The Address Strobe (AS_) signal indicates a bus transaction has begun and that the Address lines are valid on the Interface Bus. Address lines must be stable while AS_ is asserted.

Negated -- On the rising edge of the Address Strobe (AS_) signal, the Address lines are latched internally. As soon as the Address Strobe is negated , the Address lines on the Interface Bus may change with no effect.

- *Timing comments :*

Assertion/Negation -- This input is sampled every clock cycle.

(3) Address Bus lines : A(5:0)

The Address Bus lines A(5:0) consist of six input signals on the ZISC036. The Address Bus must be connected to all devices in case of a multi-device network.

- *State meaning :*

Asserted/Negated -- The Address Bus lines A(5:0) represent the address of the internal register to be accessed.

- *Timing comments :*

Assertion/Negation -- The Address Bus lines must be valid at least when the Address Strobe signal (AS_) is active. Refer to both chapters 6, “I/O Bus and Protocols” and 9, “AC Specifications”.

(4) Address Acknowledge : AACK

The Address Acknowledge (AACK_) signal is an output signal on the ZISC036.

- *State meaning :*

Asserted -- The Address Acknowledge (AACK_) signal indicates the Address Bus lines are processed by the ZISC036 Neural Network.

Negated -- TheAddress Acknowledge (AACK_) signal indicates the Address lines have been latched in the previous clock Cycle.

- *Timing comments :*

Assertion/Negation -- The Address Acknowledge (AACK_) signal is generated by latching internally the Address Strobe signal.Transition occurs on the rising edge of the system clock following the transition of the Address Strobe signal.

5•2•3 Data Transfer Group :

Data Transfer Group Signals are used to transmit the data and monitor data transfers. For a detailed description of how these signals interact, refer to chapter 6 “I/O Bus and Protocols”.

(1) Transfer direction : R/W

The Transfer Direction (R/W_) signal is an input signal on the ZISC036. This signal must be connected to all devices in case of a multi-device network.

- *State meaning :*

Asserted -- A high level initiates a transfer from the Neural Network to the Interface Bus (Read operation).

Negated -- A low level initiates a transfer from the Interface Bus to the Neural Network (Write operation).

- *Timing comments :*

Assertion/Negation -- The Transfer Direction signal must be valid at least when the Address Strobe signal (AS_) is active. Refer to section 9, “AC Specifications”.

(2) Data Strobe : DS

The Data Strobe (DS_) signal is an input signal on the ZISC036.

This signal must be connected to all devices in case of a multi-device network.

- *State meaning :*

Asserted -- Indicates valid data on the Data Bus for a write operation, or the Master is ready to process data for a read operation.

Negated -- Indicates the data are not available on the Interface Bus during a write operation, or the Master is not ready to process data for a read operation.

- *Timing comments :*

Assertion/Negation -- In Asynchronous Mode, the signal must stay negated for a delay equivalent to 1.5 cycles before it is asserted again.

(3) Data Bus lines : D(15:0)

The Data Bus D(15:0) consists of 16 bi-directional signals on the ZISC036. This Bus must be connected to all devices in case of a multi-device network.

- *State meaning :*

Asserted/Negated -- The Data Bus lines D(15:0) represent the data to write into or to read from the internal resources to access.

- *Timing comments :*

Assertion/Negation -- For write operation, the Data Bus lines must be valid at least when the Data Strobe signal (DS_) is active. For read operation, the Data Bus lines are valid when and as long as the Ready signal (RDY_) is active.

Refer to chapter 6 “IO BUS AND PROTOCOLS”, and chapter 9 “AC SPECIFICATIONS”.

(4) 16 Bit Port : IOS16

The 16 Bit Port (IOS16_) signal is an output signal on the ZISC036..

- *State meaning :*

Asserted -- Indicates that the current transfer is handled on 16 bits.

Negated -- Indicates the current transfer is handled on only 8 bits.

- *Timing comments :*

Assertion/Negation -- This signal is generated by inverting the A(5) signal. This signal is enabled when the Chip Select signal (CS_) is active, otherwise the output is in High Impedance state.

(5) Extend Bus Cycle : WAIT

The Extend Bus Cycle (WAIT_) signal is an output signal on the ZISC036.

- *State meaning :*

Asserted -- Indicates to the bus master that the Neural Network requires a delay to complete the transfer. It allows the Master to adapt to ZISC access time. In Synchronous Mode, this signal can not be used as a hand-shaking signal. Refer to the RDY_ signal status to determine if ZISC has completed the transfer.

Negated -- The rising edge of the Extend Bus Cycle (WAIT_) signal indicates the data on the Interface Bus have been processed by ZISC or ZISC is putting data on the Interface Bus.

- *Timing comments :*

Assertion -- This signal is asserted as soon as the signals CS_ and DS_ are both active.

Negation -- This signal is negated as soon as either RDY_ is asserted. It is also negated if either CS_ or DS_ are negated before READY_ is asserted (this case should not happen in a normal transfer).

Depending on the type of transfer, the WAIT_ signal is asserted X cycles from the Data Strobe DS_ signal assertion (X defined by the following table).

Table 6: ZISC Wait cycles

Mode	Normal	Normal	Save/ Restore
Configuration	Single Device	Multi-Device	Single or Multi-Device
Read Component	Invalid Op.	Invalid Op.	5
Read Category	5/17 (1)	6/18 (1)	4
Read Distance	17	18	4
Read NCR or Read NAIF	4	5	4
Read Global Register	1	1	1
Write Component	1	1	1
Write Last Component	8	9	1
Write Category	18	19	1
Write Distance	Invalid Opertion	Invalid Op.	Invalid Op.
Write Local Register	Invalid Operation	Invalid Operation	1
Write Global Register	1	1	1
(1) The first number is relative to a Read Category Operation when the recognition process has identified the Category (ID=1), the second one when the recognition is uncertain.			

(6) Ready : RDY

The Ready (RDY_) signal is an output signal on the ZISC036.

- *State meaning :*

Asserted -- For a Read operation, indicates that ZISC has presented valid data on the Data Bus. For a Write operation, indicates that the data present on the Data Bus have been processed by ZISC and that any subsequent internal processing has terminated.

Negated -- Has no meaning

- *Timing comments :*

Assertion/Negation -- This signal is active for at least one cycle, but in the asynchronous mode, Data and RDY_ signals remain valid until either the DS_ or the CS_ signal is negated.

Depending on the type of transfer, the RDY_ signal is asserted X cycles from Data Strobe DS_ signal assertion (X is defined in the following table).

The RDY_ signal for a write operation is asserted as AACK_ signal.

Table 7: ZISC Ready cycles

Mode	Normal	Normal	Save/ Restore
Configuration	Single Device	Multi-Device	Single or Multi-Device
Read Component	Invalid Operation	Invalid Operation	5
Read Category	5/17 (1)	6/18 (1)	4
Read Distance	17	18	4
Read NCR or Read NAIF	4	5	4
Read Global Register	1	1	1
Write Component	1	1	1
Write Last Component	8	9	1
Write Category	18	19	1
Write Distance	Invalid Operation	Invalid Operation	Invalid Operation
Write Local Register	Invalid Operation	Invalid Operation	1
Write Global Register	1	1	1
(1) The first number is relative to a Read Category Operation when the recognition process has identified the Category (ID=1) the second one when the recognition is uncertain.			

5•2•4 Inter-ZISC Communication Group

Inter-ZISC communication Group allows cascading of ZISC036 chips without any limit except for electrical constraints. For a detailed description on how to connect these signals, refer to section 7.1 “Multi-Device Network”.

(1) Inter-ZISC Out lines : OUT(15:0)

The Inter-ZISC Data Out OUT(15:0) lines are output signals in the ZISC036. In case of a multi-device network , all these lines must be respectively dotted and connected to a pull-up resistor.

- *State meaning :*

Asserted/Negated -- The Inter-ZISC Data Out lines OUT(15:0) represent the physical data exchanged on the Inter-ZISC Communication Bus for operations.

- *Timing comments :*

Assertion/Negation -- The Inter-ZISC Data Out OUT(15:0) are driven (from high impedance to active state) to process the Inter-ZISC communication, two cycles after the Data Strobe DS_ signal assertion. Bus activity proceeds until the RDY_ signal is assertion. The Inter-ZISC Data Out returns to the High Impedance State when RDY_ signal is negated.

The Inter_ZISC Data Out lines can possibly be used to capture Category information at the end of an evaluation without the need to perform a READ CAT. The category is valid only if ID is asserted.

The safest way to use the ZISC Data Out is to sample them by RDY_, however data are valid earlier, as soon as they have been stable during two consecutive cycles.

Table 8: Inter-ZISC output information

OPERATION	DATA OUT LINE INFORMATION
WRITE LAST COMPONENT	CATEGORY if ID asserted
READ CAT	CATEGORY
READ DIST	DISTANCE
READ NCR	Logical AND of NCR of pointed Neurons
READ NAIF	Logical AND of NAIF of pointed Neurons

The above table indicates which information is present on the Inter-ZISC Data Out lines as a function of the operation.

(2) Inter-ZISC Data In lines : IN(15:0)

The Inter-ZISC Data In lines IN(15:0) are input signals in theZISC036. In a multi-device network, the dotted OUT(15:0) lines of all devices must be respectively co nected to the IN(15:0) lines.

- *State meaning :*

Asserted/Negated -- The Inter-ZISC Data In lines IN(15:0) represent the physical data exchanged on the Inter-ZISC Communication Bus for operations.

- *Timing comments :*

Assertion/Negation -- In a multi-device configuration, it is recommended to buffer the dotted bus OUT(15:0) every 10 cascaded devices before driving the IN(15:0) lines to avoid timing problems.

(3) Degenerated Category : DEG

The Degenerated Category (DEG_) signal is an output signal on the ZISC036. This signal must be connected to a pull-up resistor and to DEGIN_ input. In a multi-device network, DEG_ signals from every device must be dotted and connected to a pull-up resistor and DEGIN_ inputs. This signal may be used as a decision output.

- *State meaning :*

Asserted -- In a recognition process, indicates that at least one firing neuron is declared Degenerated. In a learning process, indicates that at least one Neuron Actual Influence Field was reduced to the MIF value.

Negated -- Indicates no recognized category is declared Degenerated.

- *Timing comments :*

Assertion/Negation -- The Degenerated Category signal DEG_ is driven (from High Impedance to active state) two cycles after the Data Strobe DS_ signal assertion. It returns to the High Impedance State when RDY_ signal is negated.

The safest way to use DEG_ signal as a decision information is to sample it by RDY_ however it is valid earlier. The following table indicates how many cycles DEG_ becomes valid after DS_ assertion.

Table 9:

Operation	DEG_ valid
Write Category	3
Write Category	6

(4) Degenerated Category : DEGIN

The Degenerated Category (DEGIN_) signal is an input signal on the ZISC036. In a multi-device network, the dotted DEG_ signal must be connected to the DEGIN_ signal of each device.

- *Timing comments :*

Assertion/Negation -- In a multi-device configuration, it is recommended to buffer the dotted signal DEG_ every ten cascaded device before driving the DEGIN_ signal to avoid timing problems.

(5) Uncertain Recognition : UNC

The Uncertain Recognition (UNC_) signal is an output signal on the ZISC036. This signal must be connected to a pull-up resistor and to UNCIN_ input. In a multi-device network , UNC_ signals from every device must be dotted and connected to a pull-up resistor and UNCIN_ inputs..

- *State meaning :*

Asserted -- Indicates that at least two different categories have been identified during the recognition process.

Negated -- If both UNC_ and NID are negated during the recognition process, it indicates the vector has been identified

- *Timing comments :*

Assertion/Negation -- The Degenerated Category signal DEG_ is driven (from High Impedance to active state) two cycles after the Data Strobe DS_ signal assertion. It returns to the High Impedance State when RDY_ signal is negated. The safest way to use UNC_ signal as a decision information is to sample it by RDY_ however it is valid earlier.

The following table indicates how many cycles UNC_ becomes valid after DS_ assertion.

Table 10:

Operation	UNC_ valid
Write Category	5
Write Last Component	8

(6) Uncertain Recognition : UNCIN

The Uncertain Recognition (UNCIN_) signal is an input signal on the ZISC036. In a multi-device network, the dotted UNC_ signal must be connected to the UNCIN_ signal of each device.

- *Timing comments :*

Assertion/Negation -- In a multi-device network, it is recommended to buffer the dotted signal UNC_ every ten cascaded devices before driving the UNCIN_ signal to avoid timing problems.

(7) No Identified Category : NID

The No Identified Category (NID) signal is an output signal on the ZISC036. This signal must be connected to a pull-up resistor and to NIDIN_ input. In a multi-device network ,NID_ signals from every device must be dotted and connected to a pull-up resistor.

- *State meaning :*

Asserted -- Indicates that no category has been identified during the recognition process.

Negated -- If both UNC_ and NID are negated during the recognition process, it indicates the vector has been identified.

- *Timing comments :*

Assertion/Negation -- The Non Identified signal NID_ is driven (from High Impedance to active state) two cycles after the Data Strobe DS_ signal assertion. It returns to the High Impedance State when RDY_ signal is negated. The safest way to use NID_ signal as a decision information is to sample it by RDY_ however it is valid earlier. The following table indicates how many cycles NID_ becomes valid after DS_ assertion.

Table 11:

Operation	NID valid
Write Category	5
Write Last Component	6

(8) No Identified Category : NIDIN

The No Identified Category (NIDIN) signal is an input signal on the ZISC036. In a multi-device network, the dotted NID signal must be connected to the NIDIN signal of each device.

- *Timing comments :*

Assertion/Negation -- In a cascaded configuration, it is recommended to buffer the dotted signal NID every ten cascaded chips before driving the NIDIN signal to avoid timing problems. Identified Category : ID

The Identified Category (ID) signal is an output signal on the ZISC036.

- *State meaning :*

Asserted -- Indicates that one single category has been identified during the recognition process.

Negated -- Indicates either that no category or more than one category has been identified during the recognition process. NID and UNC_ can be used for additional information.

- *Timing comments :*

Assertion/Negation -- The Identified Category signal ID is driven (from High Impedance to active state) two cycles after the Data Strobe DS_ signal assertion. It returns to the High Impedance State when RDY_ signal is negated. The safest way to use ID signal as a decision information is to sample it by RDY_ however it is valid earlier. The following table indicates how many cycles ID becomes valid after DS_ assertion.

Table 12:

Operation	ID valid
Write Category	2
Write Last Component	6

(9) Exception : ERROR

The Exception signal (ERROR_) is output only on the ZISC036. In a multi-device network, ERROR signals from every device should be dotted, connected to a pull-up resistor and to the ERRORIN_ signal of the "driving device" (see section5.2.4.11 ERRORIN_ signal, and chapter 7 "INTERFACING TECHNIQUES" for more details). Inobservance of that rule has no catastrophic impact on normal operations, it may only hide bad connection problems at assembly level, due to incomplete error report in the CSR..

- *State meaning :*

Asserted -- Indicates that an exception error has occurred (for instance, access to an invalid address). For more details, refer to section 6.8 "ERROR_ CONDITIONS".

Negated -- Indicates that no exception error was detected.

- *Timing comments :*

Assertion -- Set on the next cycle after exception is detected.

Negation -- Reset by a reset operation (CLEAR) or a Read operation of the Control and Status Register. ERROR_ signal is negated one cycle after the Neural Network acknowledges the Read Operation by asserting RDY_ signal.

(10) Exception : ERRORIN

The Exception (ERRORIN_) signal is an input signal on the ZISC036. It is used in a multi-device network to collect ERROR status of every device and reflect it in the CSR (refer section 5.2.4.10 "ERROR Signal").

- *Timing comments :*

Assertion/Negation -- It is recommended to buffer the dotted signal ERROR_ every ten cascaded devices before driving the ERRORIN_ signal, to avoid timing problems.

(11) Full Neural Network : FULL

The Full Neural Network (FULL) signal is output only on the ZISC036. In a multi-device network, FULL signals from every device should be dotted, connected to a pull-up resistor and to the FULLIN signal of the "driving device" (see section5.2.4.12 FULLIN_ signal, and chapter 7 "INTERFACING TECHNIQUES" for more details). Inobservance of that rule has no impact on normal operations, it would only prevent the setting of FULL bit in the CSR..

- *State meaning :*

Asserted -- Indicates that all the neurons of a single or a multi-device Neural Network are committed.

Negated -- Indicates that at least one neuron is free to store a new prototype if necessary.

- *Timing comments :*

Assertion -- The FULL signal is asserted X cycles from the DS_ signal assertion for Write Category operation in Normal mode, and Read or Write Category operation in Save/Restore mode (X defined by the following table).

Table 13:

xecution Mode	Configuration	Cycle Number
Normal Mode	Single Chip	19
Normal Mode	Multi-device	20
Restore Mode (Write Operation)	Single Device	3
Save Mode (Read Operation)	Single Device	6 + (Y-1) note 1
note 1: Y is the cycle number for which RDY_ and DS_ signals are both active.		

Negation -- Reset by a reset operation (CLEAR) or in Save/Restore mode. Once Save/Restore mode is set in the Control and Status Register, the FULL signal is negated when a READ CSR is performed.

(12) Full Neural Network : FULLIN

The Full Neural Network (FULLIN) signal is input only on the ZISC036. It is used in a multi-device network to set the network full status in the CSR (refer section 5.2.4.12 “FULL Signal”).

- *Timing comments :*

Assertion/Negation -- In a cascaded configuration, it is recommended to buffer the dotted signal FULL every ten cascaded devices before driving the FULLIN signal to avoid timing problems.

(13) Neuron Daisy Chain Output : DCO

The Neuron Daisy Chain Output (DCO) is intended to be connected to the Daisy Chain Input (DCI) of the next device in a row to form a multi-device network.

- *State meaning :*

Asserted -- Indicates that the current device has committed all its neurons. The next neuron to be committed must be in the next device in the row. In Save/Restore mode, this signal indicates that all the neurons of the current device have been saved or restored, and the process is to be pursued on the next device in the row.

Negated -- Indicates that the current chip has at least one free neuron for future learning, or the Save/Restore process on the current chip is not complete.

- *Timing comments :*

Assertion -- The DCO signal is asserted X cycles from DS_ signal assertion for Read or Write Category operation (X is defined by the following table).

Table 14:

Mode	Operation	Configuration	Cycle Number
Normal mode	Write Category	Single Device	19
Normal Mode	Write Category	Multi-Device	20
Save-Restore Mode	Write Category	Single or Multi-Device	3
Save Mode	Read Category	Single Chip	6 + (Y-1) note 1
note 1: Y is the cycle number for which RDY_ and DS_ signals are both active.			

Negation -- Reset by CLEAR signal or, in Save/Restore mode, by any READ STATUS operation. Once Save/Restore mode is set in the Control and Status Register, the DCO signal is negated when a READ CSR is performed.

(14) Neuron Daisy Chain : DCI

The Neuron Daisy Chain (DCI) signal is an input signal on the ZISC036.

In a single device network, the DCI input must be tied up to VDD. In a multi-device network, the DCI input of the first device in the row must be tied up to VDD. The DCI input of subsequent devices must be connected to the DCO output of the previous device in the row.

- *State meaning :*

Asserted -- Indicates that the previous device has committed all its neurons. In Save/Restore mode, this signal indicates that all the neurons of the previous chip have been saved or restored.

Negated -- Indicates that the previous chip has at least one free neuron for future learning, or Save/ Restore process on the previous chip is not complete.

- *No timing comments.*

5•2•5 System Clock : SYSCLK

The System Clock signal (SYSCLK) is input only on the ZISC036. It determines the system clock frequency.

5•2•6 Test signals :

These signals are reserved for module manufacturing test and must be left unconnected.

5•3 SIGNAL Summary and Pin assignment :

Table 18 is a summary of all the signals discussed in the previous sections. All inputs are TTL compatible. All three state outputs are CMOS compatible. All Open Drain outputs are TTL and CMOS compatible and must be tied to VDD through an external resistor with a maximum sink current of 24mA. Tables 19 and 20 give the module pin position of each individual signal. Tables are organized according to the four sides of the package.

Table 15: Signal Summary and Driver /Receiver type

Signal Name	Driver Type			Active	Function
CLEAR	In	---	TTL	High	Hard Reset
INH_	In	---	TTL	Low	Interface bus driver Inhibit
NORM	In	---	TTL	High	Norm choice
SM	In	---	TTL	High	Synchronous Multiplexed Mode
SBY	In	---	TTL	High	Standby Mode
CS_	In	---	TTL	Low	Chip Select
AS_	In	---	TTL	Low	Address Strobe
AACK_	Out	Three State	CMOS	Low	Address Acknowledge
A(5:0)	In	---	TTL	High	Address [0:5]
R/W_	In	---	TTL	High=RD Low=WR	Read/Write = Data Transfer direction
DS_	In	---	TTL	Low	Data Strobe
IOS16_	Out	Open Drain	TTL	Low	Data transfer on 16 bit
D(15:0)	In/Out	Three State	CMOS	High	Data [15:0]
WAIT_	Out	Three State	CMOS	Low	Extend bus cycle
RDY_	Out	Three State	CMOS	Low	Ready
OUT(15:0)	Out	Open Drain	TTL	High	Inter-ZISC Output [15:0]
IN(15:0)	In	---	TTL	High	Inter-ZISC Input [15:0]
DEG_	Out	Open Drain	TTL	Low	Degenerated Category Output
DEGIN_	In	---	TTL	Low	Degenerated Category Input
UNC_	Out	Open Drain	TTL	Low	Uncertain Recognition Output
UNCIN_	In	---	TTL	Low	Uncertain Recognition Input
NID	Out	Open Drain	TTL	High	No Identified Category Output
NIDIN	In	---	TTL	High	No Identified Category Input
ID	Out	Three State	CMOS	High	Identified Category Output
DCO	Out	Three State	CMOS	High	Neuron Daisy Chain Output
DCI	In	---	TTL	High	Neuron Daisy Chain Input
ERROR_	Out	Open Drain	TTL	Low	Error Output
ERRORIN_	In	---	TTL	Low	Error Input
FULL	Out	Open Drain	TTL	High	Full Neural Network Output
FULLIN	In	---	TTL	High	Full Neural Network Input
SYSCLK	In	---	TTL	High	System Clock

Table 16: Module PIN assignment SOUTH and EAST side

S0	1	SSYD	E01	37	OUT(1)
S02	2	SSYIN	E02	38	IN(1)
S03	3	ERROR	E03	39	OUT(2)
S04	4	BCLKA	E04	40	IN(2)
S05	5	VDD	E05	41	GND
S06	6	GND	E06	42	OUT(3)
S07	7	TCLK	E07	43	IN(3)
S08	8	WAIT_	E08	44	OUT(4)
S09	9	VDD	E09	45	IN(4)
S10	10	GND	E10	46	OUT(5)
S11	11	RDY_	E11	47	IN(5)
S12	12	CS_	E12	48	OUT(6)
S13	13	AACK_	E13	49	IN(6)
S14	14	VDD	E14	50	VDD
S15	15	GND	E15	51	GND
S1	16	BCLK7	E16	52	OUT(7)
S17	17	SO0	E17	53	IN(7)
S1	18	BCLK8	E18	54	OUT(8)
S1	19	TEST	E19	55	IN(8)
S20	20	DI	E20	56	OUT(9)
S21	21	SO1	E21	57	IN(9)
S2	22	BCLK5	E22	58	OUT(10)
S23	23	VDD	E23	59	IN(10)
S24	24	GND	E24	60	GND
S25	25	BCLK	E25	61	OUT(11)
S26	26	VDD	E26	62	IN(11)
S27	27	GND	E27	63	OUT(12)
S28	28	CCLK	E28	64	IN(12)
S29	29	SO3	E29	65	OUT(13)
S30	30	AS_/frame	E30	66	IN(13)
S31	31	SBY	E31	67	VDD
S32	32	VDD	E32	68	GND
S33	33	GND	E33	69	OUT(14)
S3	34	VALZB	E34	70	IN(14)
S35	35	OUT(0)	E35	71	OUT(15)
S36	36	IN(0)	E36	72	IN(15)

Table 17: Module PIN assignment NORTH and WEST side

N01	73	DCO	W01	10	DCI
N02	74	IOS16_	W02	110	FULL
N03	75	ACLK	W03	111	FULLIN
N04	76	VDD	W04	112	RI
N05	77	GND	W05	113	SM /siglb
N06	78	INH_	W06	114	GND
N07	79	D(0)	W07	115	ID
N08	80	D(1)	W08	116	NID
N09	81	D(2)	W09	117	NIDIN
N10	82	GND	W10	118	UNC_
N11	83	D(3)	W11	119	UNCIN_
N12	84	D(4)	W12	120	DEG_
N13	85	D(5)	W13	121	DEGIN_
N14	86	VDD	W14	12	VDD
N15	87	GND	W15	123	GND
N16	88	D(6)	W16	124	BCLK6
N17	89	D(7)	W17	125	SO6
N18	90	VDD	W18	126	Reserved
N19	91	GND	W19	127	Reserved
N20	92	D(8)	W20	128	Reserved
N21	93	D(9)	W21	129	Reserved
N22	94	D(10)	W22	130	RAMC
N23	95	GND	W23	131	GND
N24	96	D(11)	W24	132	A(5)
N25	97	D(12)	W25	133	A(4)
N26	98	D(13)	W26	134	A(3)
N27	99	VDD	W27	135	A(2)
N28	100	GND	W28	136	A(1)
N29	101	D(14)	W29	137	A(0)
N30	102	D(15)	W30	138	DS_
N31	103	CLEAR	W31	139	VDD
N32	104	VDD	W32	140	GND
N33	105	GND	W33	141	IRQ
N34	106	SYSCLK	W34	142	R/W_
N35	107	SO2	W35	143	BCLK2
N36	108	VALD	W36	144	BCLK3

CHAPTER 6

I/O bus and protocols

6 - I/O BUS and PROTOCOLS

ZISC036 I/O are managed through:

- *The Chip Select signal CS_*
- *The 6-bit Address Bus and two control signals:*
  A(5:0)
  *AS_*
  *AACK_*
- *The 16-bit Data Bus and five control signals: D(15:0)*
  *DS_*
  *RDY_*
  *IOS16_*
  *WAIT_*
  *RW_*

ZISC is a coprocessor device which must be controlled by a master, (state machine or micro-controller) this can be done via a standard I/O bus. Later in this chapter the master will be called controller.

Controlling the ZISC036 is, by definition, accessing its registers and requires an Address definition via the Address Bus and Data transfer via the Data Bus.

This chapter describes I/O operations and functional timings, it also explains how to connect ZISC036 to standard busses and micro-controllers.

6•1 Conventions

Conventions taken to define ZISC busses are:

Bit numbering : BUS(N:M) where the highest number represents the high order bit.

Byte ordering : Little Endian convention. For example on a word(two Byte), bits(15:8) represent the high order Byte.

ZISC036 can however communicate with either a Big or Little Endian bus (see discussion section 6.7).

6•2 CHIP SELECT CS_

The Chip Select signal (CS_) must be activated low to validate any access. It is user's choice to deactivate CS_ between consecutive accesses. In any case, the delays specified in table chapter 9 "AC Specifications" must be obeyed.

6•3 Asynchronous communications

ZISC036 supports asynchronous protocols, but in order to operate properly, DS_ must be re-synchronized before controlling the ZISC inputs. The re-synchronization mechanism must ensure DS_ does not switch to active level, at ZISC inputs, within a 10ns window centered on the rising edge of SYSCLOCK.

An example of asynchronous communication is given in figure 12.

6•3•1 write Operation

For a Write operation, (from controller to ZISC, R/W=0) the controller places simultaneously the address on the Address Bus, the data on the Data Bus) and asserts the AS_ and DS_ signals.

ZISC immediately activates the WAIT_ signal, until the completion of any subsequent process and assertion of the RDY_ signal .

Upon negation of WAIT_ or assertion of

RDY_, the controller can remove address and data and release DS_ and AS_ which makes ZISC release RDY_.

Using WAIT_ or RDY_ as acknowledgment depends upon whether the controller requires an external signal to force wait states or not.

The controller must not reinitiate a new transfer and reassess DS_ within the interval of time equivalent to one and a half (1.5) SYSCLOCK periods starting at the previous DS_ deactivation.

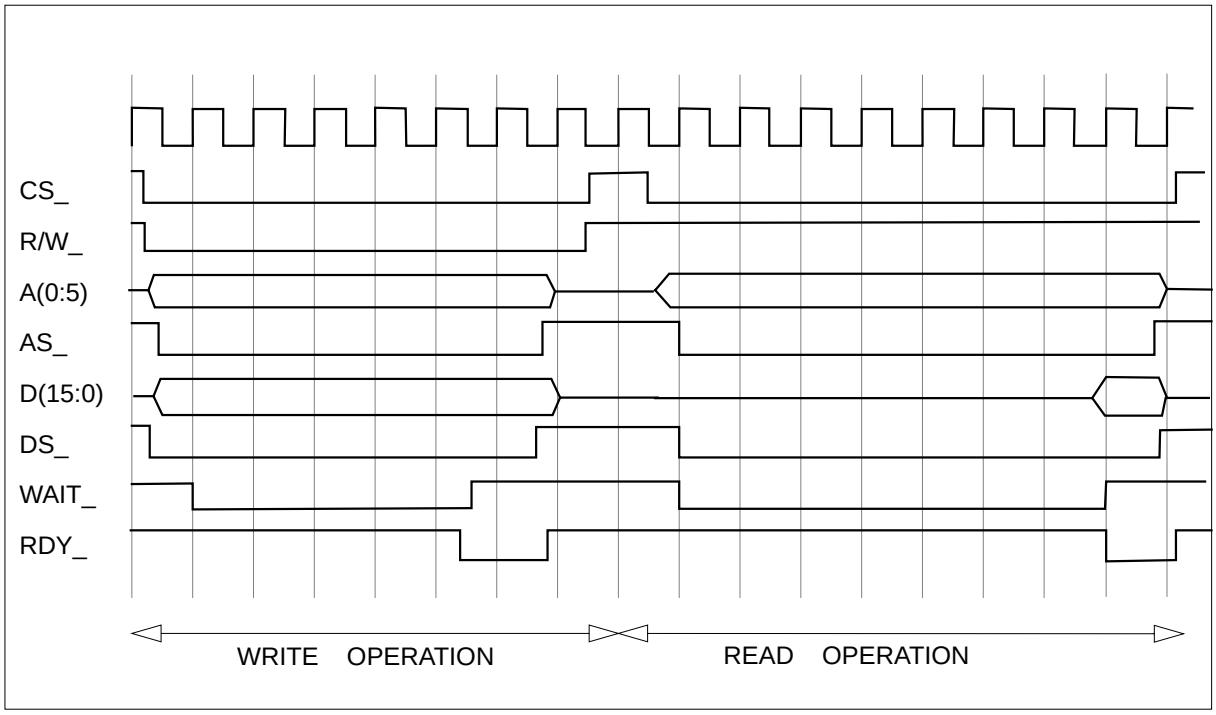


FIGURE 12. **Asynchronous communication example**

6•3•2 Read operation

For a Read operation, (from ZISC to controller, R/W=1) the controller places the address on the Address and assert the AS_ and DS_.

ZISC immediately activates the WAIT_ signal, until it places the data on the Data Bus (D(15:0)) and asserts the RDY_ signal.

Upon negation of WAIT_ or assertion of RDY_, the controller can remove the address and release CS_ and DS_ which makes ZISC release RDY_.

Using WAIT_ or RDY_ as acknowledgment depends upon whether the controller requires an external signal to force wait states or not.

The controller must not reinitiate a new transfer and reassess DS_ within the interval of time equivalent to one and a half (1.5) SYSCLOCK periods starting at the previous DS_ deactivation.

6•4 SYNCHRONOUS communications

When a common clock can be shared between ZISC and the controller, it is possible to take full advantage of a synchronous protocol, transfer homogeneous data by burst, and so get the maximum performance of ZISC. ZISC is conditioned for synchronous mode by setting bit-7 of CSR to one. Two modes of operation are possible depending on the input signal SM.

SM=0 Use of separate Address and Data bus.

SM=1 Use of multiplexed Address and Data bus.

In synchronous mode, the level of a signal or the value of a bus, for a cycle is determined at the rising edge of the SYSCLOCK signal, with respect to the minimum set-up and hold time given in chapter 9.

In this mode of operation ZISC supports single or multiple (burst) transfers.

Burst transfers are specifically suitable to transfer vector components.

6•5 SYNCHRONOUS COMMUNICATIONS ON SEPARATE ADDRESS & DATA BUS

Example of such a mode of operation is given in figure 13

6•5•1 Write Operation

1 : Single Transfer:

The controller places the address on the Address Bus and asserts AS_ for at least one cycle.

ZISC asserts AACK_ within the following cycle, and keeps it asserted until the cycle following AS_ release.

In the same cycle as AS_ assertion, or later, the controller places the data on the Data Bus and asserts DS_ for one cycle only, which makes ZISC latch the data.

Assertion of RDY_ by ZISC depends on the operation. For WRITE LAST COMPONENT or WRITE CAT, it occurs when the subsequent process is complete. For any other write operation, it occurs within the cycle following AS_ assertion

2 : Multiple Transfer:

The controller places the address on the Address Bus and asserts AS_ for at least one cycle.

ZISC asserts AACK_ within the following cycle, and keeps it asserted until the cycle following AS_ release.

In the same cycle as AS_ assertion, or later, the controller starts placing data on the Data Bus (a new data every cycle), and asserts DS_ and keeps it asserted for as many cycles as there are data to transfer.

ZISC latches data every cycle DS_ is asserted.

Assertion of RDY_ by ZISC depends both on the operation performed and the assertion of AS_ by the controller.

- *For WRITE LAST COMPONENT or WRITE CAT, it occurs for one cycle, when the subsequent process is complete.*
- *For a WRITE CAT operation Data must be kept stable on Data Bus until RDY_ assertion.*
- *For other write operations, it occurs within the cycle following AS_ assertion, and remains asserted one cycle after AS_ is released.*

The Address can be changed during a multiple transfer to access different resources. Any address change must be validated by AS_ assertion. A vector transfer can be performed in a single burst by raising the bit A(3) and when putting the last component data on the Data Bus. Care must be taken, not to overrun the ZISC, that no other data should follow a WRITE LAST COMPONENT or WRITE CAT.

6•5•2 Read Operation

The controller places the address on the Address Bus and asserts AS_ for at least one cycle.

ZISC asserts AACK_ within the following cycle, and keeps it asserted until the cycle following AS_ release.

Starting the same cycle as AS_ assertion, or later, the controller asserts DS_ for as many cycles as there are data to transfer.

After the needed latency, ZISC starts placing data on the Data Bus every cycle, asserts RDY_ and keeps it asserted for the number of cycles as requested by the controller.

6•6 SYNCHRONOUS COMMUNICATIONS ON MULTIPLEXED ADDRESS AND DATA BUS

When interfacing ZISC to a multiplexed address and data bus, A(5:0) must be connected to five lines of D(15:0).

AS_ is used as a single strobe, and DS_ must be connected to GND.

In this mode of operation, multiple (burst) transfers are specifically reserved for components. For an evaluation, the address X'0C' or X'0D' (WRITE LAST COMPONENT) must be used for the whole block of components, and ZISC automatically completes the evaluation upon the end of the transfer.

Example of such a mode of operation is given in figure 14.

6•6•1 Write Operation

1 : Single Transfer:

The controller places the address on the Bus and asserts AS_ for one cycle only.

ZISC asserts AACK_ within the following cycle.

The controller places the data on the Bus the cycle following AS_ assertion.

Assertion of RDY_ by ZISC depends on the operation performed: For WRITE LAST COMPONENT or WRITE CAT, it occurs for one cycle, when the subsequent process is complete.

For a WRITE CAT operation Data must be kept stable on Data Bus until RDY_ assertion.

For other write operations, it occurs within the cycle following AS_ assertion.

2 : Burst Transfer:

The controller places the address on the Bus and starts asserting AS_ for as many cycles as there are component data to transfer.

ZISC asserts AACK_ within the following cycle, and keeps it asserted until the cycle following AS_ release.

The cycle following AS_ assertion, the controller starts placing data on the Bus (a new data every cycle).

ZISC latches data every cycle until the cycle following AS_ release.

ZISC asserts RDY_ within the cycle following AS_ assertion, keeps it asserted until AS_ release, and reasserts RDY_ for one cycle when the evaluation process is complete.

6•6•2 Read Operation

1 : Single Transfer:

The controller places the address on the Bus and asserts AS_ for one cycle.

ZISC asserts AACK_ within the following cycle.

After the needed latency, ZISC places the data on the Bus and asserts RDY_ for one cycle.

2 : Multiple Transfer:

The controller places the address on the Bus and starts asserting AS_ for as many cycles as there are data to transfer.

ZISC asserts AACK_ within the following cycle, and keeps it asserted until the cycle following AS_ release.

After the needed latency, ZISC starts placing data on the Data Bus every cycle, asserts RDY_ and keeps it asserted for the number of cycles as requested by the controller.

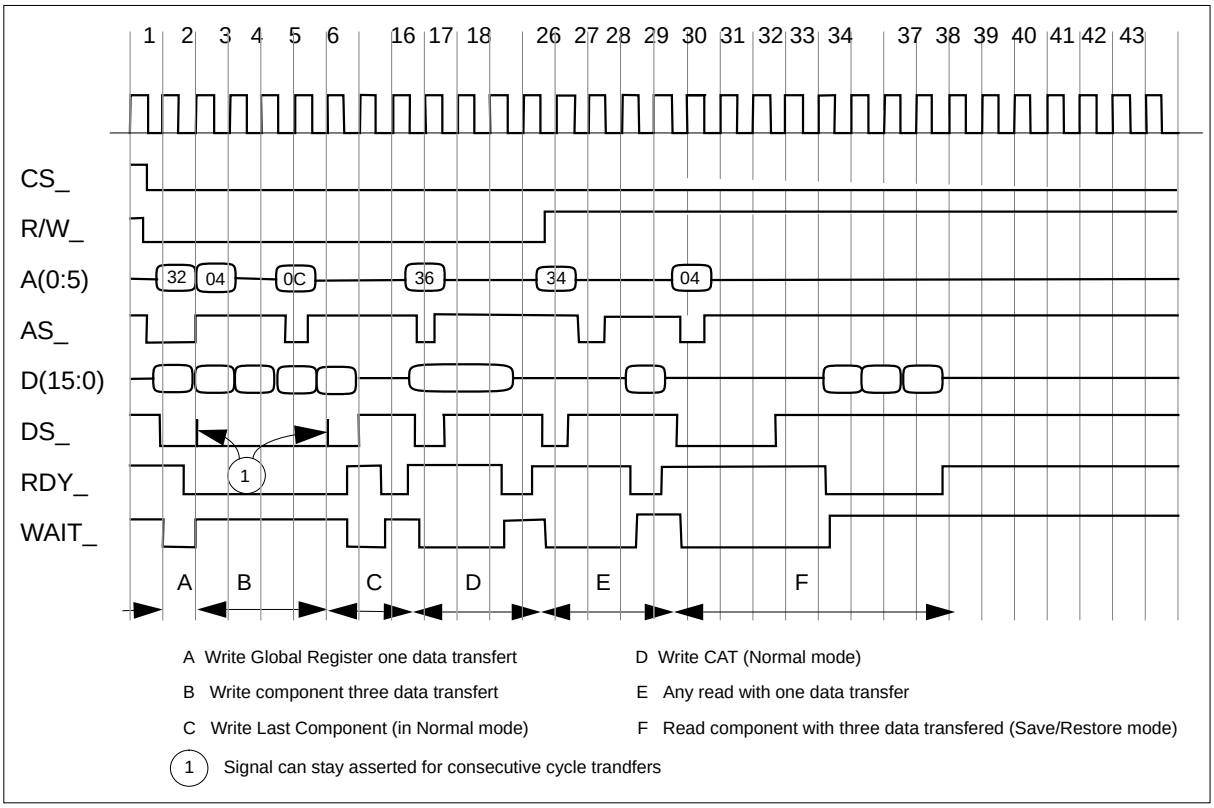


FIGURE 13. Synchroneous Communication on separated Address and Data bus

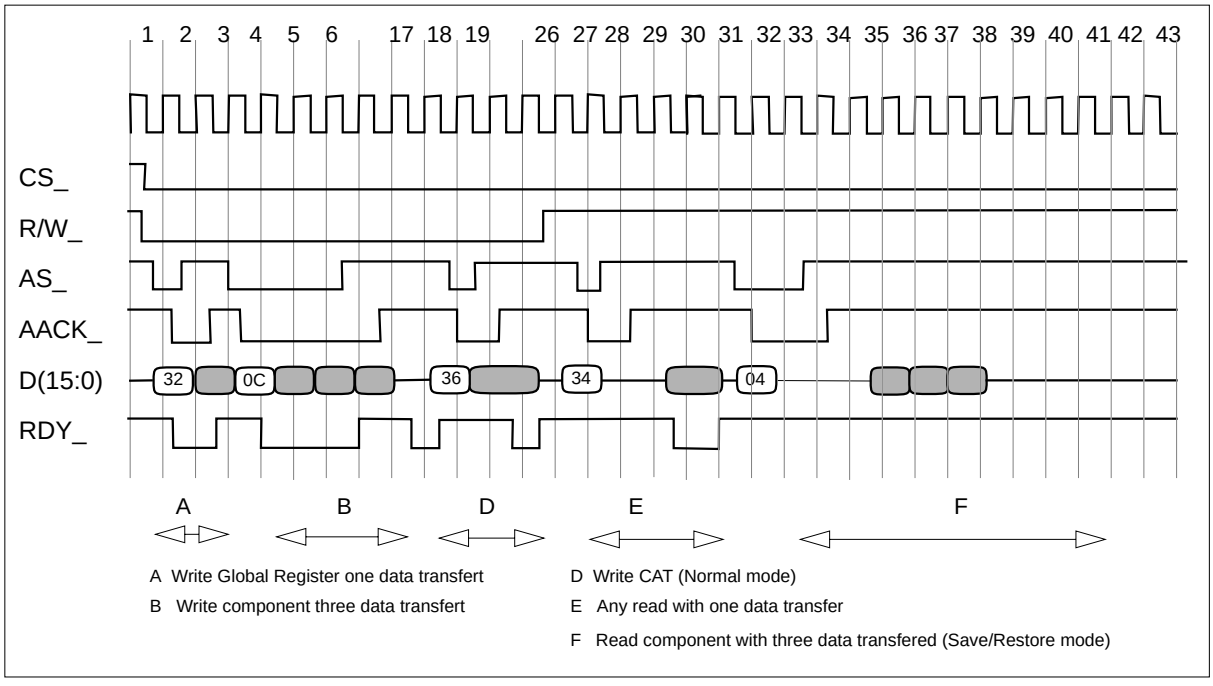


FIGURE 14. Synchroneous Communication on multiplexed Address and Data bus

6•7 Word/byte Addressing hints

The address bit(0) is not fully decoded by ZISC036 but only used for alignment checking of word transfer. In which case, the address must be even for a word transfer. Two consecutive addresses (even and odd) are possible for a byte transfer.

This scheme gives the maximum of flexibility to interface Big and Little Endian processors.

For write transfers of a single byte, Address parity (odd/even) must be chosen to transmit data on D(7:0). For a read transfer both addresses can be used, as ZISC duplicates the byte on D(7:0) and D(15:8).

Addresses of ZISC word resources are above X'1F', so A(5) can be connected to a size signal if the controller generates such a signal.

If no alignment checking is desired for word transfers, the low order bit address can be omitted and A(0) tied to GND at ZISC input.

6•8 ERROR_ CONDITIONS

An Error signal is provided by ZISC036 which can be monitored by the controller. This signal is asserted within the next clock cycle of the following events:

- *Component overloading:*
  An attempt to read or write more than 64 components has been made. This can happen if the address specified for the 64th component is not X'0C' or X'0D' or if, in PCI-like mode, the AS_ has not been released when the 64th component is put on the Data Bus.
- *Mis-aligned data:*
  An attempt has been made to access a word resource with an odd address.
  This occurs when A(5)=A(0)='1'.
- *Invalid address:*
  An invalid address has been decoded by ZISC. This can happen if both CS_ and AS_ are asserted and the address present on the bus is not one of the values specified in section 3.3. Monitoring ERROR_ is very important in this case as ZISC will not assert RDY_ which could deadlock the Address Bus.
  Special care must Special care must be taken to prevent having CS_ and DS_ active with all address bits A(5:1) equal to zero as neither ERROR_ nor RDY_ would be activated by ZISC.
- *Forbidden operation:*
  An access has been attempted to a resource not allowed in the current state of the device .A read component or a Write NAIF are not allowed in normal mode.

ERROR_ can be reset by a read status or by asserting the CLEAR signal.

6•9 STANDBY MODES

ZISC036 is a fully static implementation. The system clock can be gated off without loss or damage for data content, permitting power saving when ZISC is not in use.

Two standby modes are available:

- *CSR bit-6:*
  When set to one by a write status, internal clocking of all functions but interface and state machine is gated off.
- *SBY input:*
  when asserted by the controller, the clock is gated off right at the input of the device and all tri-state drivers set to high impedance.

It is recommended to set the CSR bit-6 to one by a WRITE CSR, and only then, when the transfer is completed, set the input SBY. This sequence prevents from stopping the ZISC state machine and disabling the interface while a transfer is ongoing. Activating the CS_ signal when SBY is asserted may result in activating the signal IOS16_.

CHAPTER 7

Interfacing Techniques

7 - Interfacing Techniques

Unused outputs can be left unconnected. Open drain output must be pulled up when used, to guaranty the positive level. Pull up resistance value depends on the desired signal rising time, but must not drive a current higher than 24 mA when the signal is at low level.

Unless otherwise specified, unused inputs must be polarized in accordance with the desired mode of operation. This mention applies even more especially to the signals CS_, INH_ ,SBY. If left unconnected these signals may prevent ZISC036 from operating.

In all cases, even in a single device network, signals DEG_ , DEGIN_, UNC, UNCIN, NID, NIDIN, must be connected by pair, and each pair must be pulled up by a resistor.

7•1 MULTI-DEVICE NETWORK

7•1•1 Small ZISC network

Several ZISC036 devices can be 'cascaded' in order to build multi-device networks. The maximum number of devices which can be 'cascaded' without need for external active components is card technology dependent (wire capacitance, etc....). In most cases, re-powering devices will not be required if the number of ZISC's is lower than or equal to ten.

In order to build such a network, connections have to be made which can be divided in four classes.

- *Interface Bus*
- *Daisy chain*
- *Inter-Chip Communication Bus*
- *Special connections*

• 1• Interface Bus :

The Interface Bus is identical in a Single or Multi-Device Neural Network. All input signals including Address and bi-directional Data Busses must be applied in parallel to each chip. These signals are CS_, AS_, A(5:0), R/W_, DS_, D(15:0), CLEAR, NORM, SM, SBY, and SYSCLK.

• 2• Daisy Chain :

Each DCO output of the device (n) must be connected to the DCI input of the device (n+1). The DCI input for the device (1) must be connected to an up level (VDD). The DCO output of the last device does not need to be connected.

• 3• Inter-ZISC Communication Bus:

Inter-ZISC communication Bus is made of input and output signals which must be connected by pair, each pair to a pull-up resistor. The following 21 pairs of input/output signals must be connected according to the following table:

TABLE 18. I/O interconnection

N(15:0)	OUT(15:0)
DEGIN_	DEG_
UNCIN_	UNC_
NIDIN	NID
FULLIN	FULL
ERRORIN_	ERRROR_

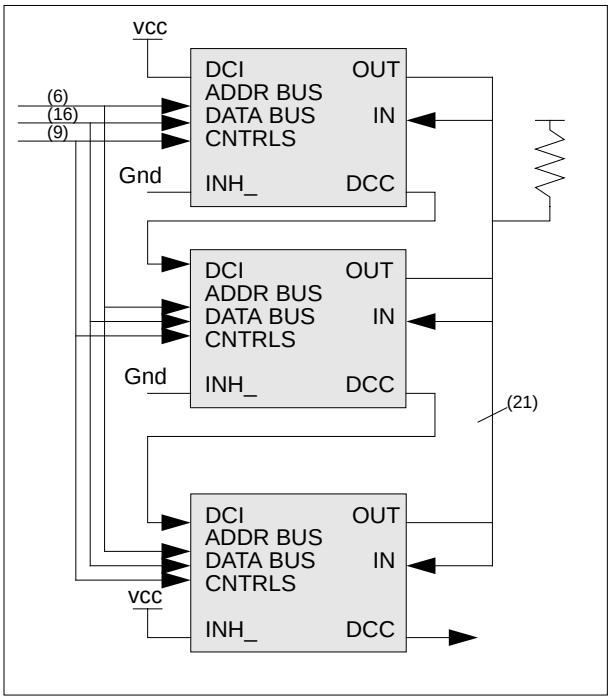


FIGURE 15. Interconnection of ZISC Modules

In a Single Chip Neural Network, the IN and OUT busses do not need to be connected together as the connection is implemented inside the ZISC036 chip when the CSR bit-5 (SCHP) is set to zero.

• 4• Special Connections :

The signal INH_ of only one device, whatever it is, must be tied up (connected to V+) while all other devices must have the input INH_ tied down (connected to GND). The device whose INH_ is tied up drives the bi-directional bus. This device is referred to as the driving device. The following output signals need to be connected only to the driving device: ID, WAIT_ , RDY_ , AACK_ , IOS16_.

The figure 15 shows connections between devices in a small chain. The lead location and type of connection are given in tables within chapter 5 “Signal Description”.

7•1•2 Large ZISC Network

Building a large ZISC network is a matter of grouping small networks together by placing re-powering devices where needed. The only specifics are related to the inter-ZISC Communication Bus which must be pulled up through resistors and re-powered by sub-networks. Sub-networks must be then AND’ed together, and the AND outputs connected to corresponding inputs of every device. Twenty-one AND devices are required, with a fan-in equal to the number of sub-networks.

See fig 16 below for “large ZISC chain connection”

.

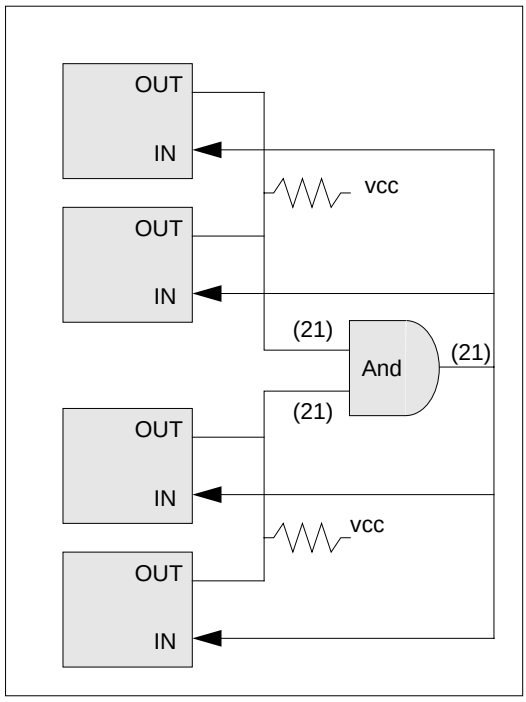


FIGURE 16. large ZISC chain connection

7•2 - I/O BUS INTERFACE EXAMPLES

The following sections show examples of how ZISC can interface some of the standard busses and common microcontrollers.

7•2•1 - ISA Bus

The necessary wait cycles can be generated by connecting the ZISC WAIT_ output to the ISA Bus WAIT input.

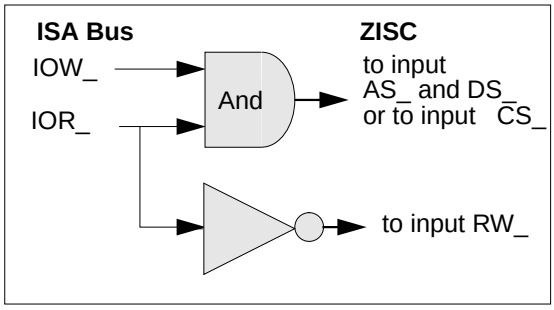


FIGURE 17. ZISC signal from ISA bus

The simple logic shown in figure 17 can generate the ZISC interface signals from the WRITE STROBE and READ STROBE signals of the ISA Bus.

7•2•2 PCMCIA Bus

The -CE2 signal, from the PCMCIA bus, can be connected to A(5) acting as SIZE . CS_ input can be generated from the PCMCIA -REG and -CE1 signals as shown in figure 18.

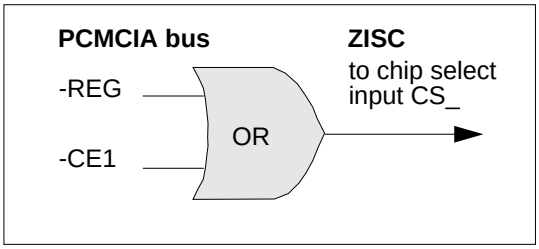


FIGURE 18. ZISC signal from PCMCIA bus

The same simple logic as described in fig 17 can be used to generate ZISC interface signals from WRITE STROBE and READ STROBE signals delivered by the PCMCIA Bus.

*7•2•3 Micro Channel bus**

No extra logic is needed to communicate with the Micro Chanel Bus : the Micro Channel output signals -ADL, -CMD and -S0 can be respectively connected to the ZISC inputs AS_ , DS_ and R/W_.

*7•2•4 80286 Microprocessor**

If the ZISC036 is connected to a microprocessor such as 80286, the microprocessor output -S0 can be connected to the ZISC input RW_ .

*7•2•5 I486 Microprocessor**

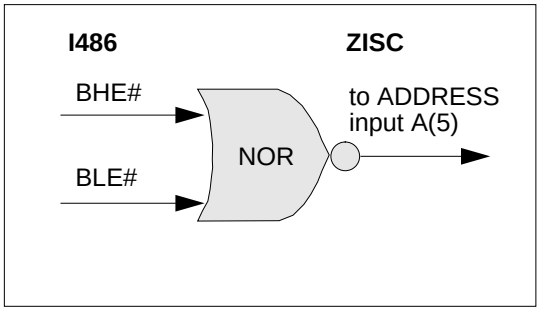


FIGURE 19. ZISC signal from I486 signals

A SIZE signal connected to A(5) can be generated from BHE# and BLE# as shown in fig 19..

For a word transfer, ZISC responds by activating its output IOS16_.

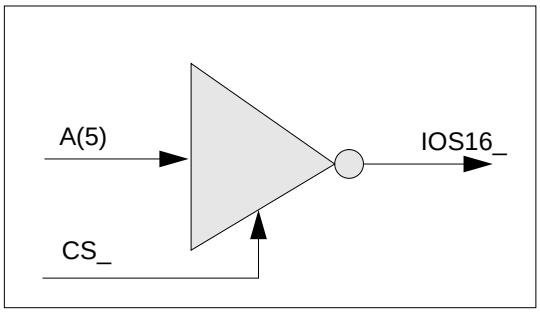


FIGURE 20. ZISC Signal for word transfer

This output is driven by an open drain driver and returns to high impedance when the chip is not selected.

*7•2•6 M6800 Microprocessor family**

The output SIZ1 of the microprocessor can be directly connected to the ZISC input A(5).

*7•2•7 PowerPC**

The example of the interface described here is a synchronous protocol. It uses the two separate strobes generated by the processor for address and data, so the ZISC input signal SM must be grounded. Bit-7 of the CSR must be set to one. With this setting, one component can be input in ZISC every clock cycle as long as DS_ is kept active.

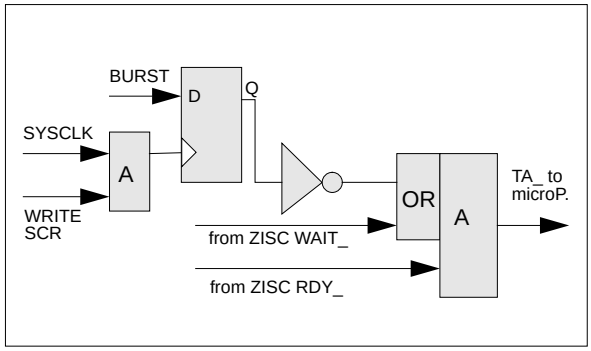


FIGURE 21. PowerPC TA signal from ZISC

A specific single beat transfer must be executed for the last component with the correct address specification.

ZISC output AACK_ must be connected to the AACK_ input of the processor. The additional logic shown in fig 21 has to be implemented to generate the TA input for the processor to allow burst transfers.

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M6800 is a trademark of MOTOROLA Inc

Micro Channel and PowerPC are trademarks of IBM Corporation

DC Characteristics

8 - DC Characteristics

8•1 ELECTRICAL SPECIFICATIONS :

8•1•1 Absolute Maximum ratings :

The following table lists absolute maximum ratings for the ZISC036 device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to conditions beyond the “Absolute Maximum Ratings” will reduce device reliability and result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near “Absolute Maximum Ratings” may also result in reduced useful life and reliability.

Parameter	symbol	Value	Unit
Supply Voltage	VDD	-0.5 to +6	V
Input Voltage	Vin	-0.5 to VDD+0.5	V
Ambient Temperature	Ta	0 to 80	øC
Case Temperature	Tc	0 to 100	øC
Power Dissipation	P	1.00	W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs except reserved ones, are tied to an appropriate logic voltage level (e.g., either GND or VDD).

8•1•2 Undershoot and Overshoot Specifications

The following tables summarize the maximum over and undershoot signals allowed on the output pin of a driver or the input pin of a receiver.

Pulse Width (ns)	Overshoot (V)	Undershoot (V)
DC	VDD + 0.5	GND - 0.5
100 ns	VDD + 2.0	GND - 0.8
50 ns	VDD + 3.0	GND - 0.9
20 ns	VDD + 3.0	GND - 1.3
10 ns	VDD + 3.0	GND - 2.9

Maximum Pulse Amplitude above VDD or below GND (V)	Maximum Allowed Duty Cycle (%)
3.00	5
2.50	7.5
1.30	15
1.20	45

8•1•3 Recommended Operating Conditions :

Parameter	Symbol	Value	Unit
Supply Voltage	VDD	0 to 5.5	V
Input Voltage	Vin	0 to VDD	V
Ambient Temperature	Ta	0 to 70	øC
Case Temperature	Tc	0 to 85	øC

8•1•4 I/O Electrical Specifications :

The specifications for the interface circuit are given below. These specifications are applicable for a power supply from 4.5V to 5.5V.

• 1• Term Definitions :

- ***MAUL** : Maximum Allowable UpLevel. The maximum voltage that may be applied for extended periods without affecting reliability.*
- ***MPUL** : Most positive UpLevel. The most positive voltage that maintains circuit functionality. The maximum positive logic level.*
- ***LPUL** : Least Positive Up Level. The least positive voltage that maintains circuit functionality. The minimum positive logic level.*
- ***MPDL** : Most Positive Down Level. The most positive voltage that maintains circuit functionality. The maximum negative logic level.*
- ***LPDL** : Least Positive Down Level. The least positive voltage that maintains circuit functionality. The minimum negative logic level.*
- ***MADL** : Minimum Allowable Down Level. The minimum voltage that may be applied for extended periods without affecting reliability.*

8•1•5 Driver DC Voltage Specifications :

Type	MAUL	MPUL	LPUL	MPDL	LPDL	MADL
TTL	5.5	4.5	2.4	0.4	0	-0.5
CMOS	5.5	5.5	4.1	0.4	0	-0.5

8•1•6 Receiver DC Voltage Specifications:

MAUL	MPUL	LPUL	MPDL	LPDL	MADL
5.5	5.5	2	0.6	0	-0.5

8•1•7 Receiver DC Current Specifications

I_{il} (uA)	I_{ih}(uA)
> -60 at Vin = LPDL	<60 at Vin = MPUL

8•1•8 Driver DC Currents at Rated Voltage

Driver Type	V high (V)	I high (uA)	V low (V)	I low (uA)
8 mA CMOS	2.4	-6	0.5	8
24 mA Open Drain	None	None	0.5	24

8•1•9 Receiver Input Capacitance

Maximum receiver input capacitance is 3pF.

8•2 THERMAL CHARACTERISTICS

Characteristic	Value	Unit
Thermal Resistance		øC/W

CHAPTER 9

AC Specifications

9 - AC specifications

Table 9.1 gives AC specification values and reference signals.All AC specification outputs are measured at 2V level and inputs at 1.5V.

Fig 22 shows reference for asynchronous operation.

Fig 23 shows SYSCLOCK specification references for all cases and setup/hold time definition.

In asynchronous operation, DS_ must be re-synchronized before controlling the ZISC input. The re-synchronization mechanism must ensure these signals do not switch to active level, at ZISC inputs, within a 10ns window centered to the rising edge of SYSCLOCK as illustrated in figure 22.

In synchronous mode, the reference signal is SYSCLOCK, set-up and hold times references are given in figures 23 and 24. Input setup and hold times are specified as minimum, defining the smallest acceptable sampling window. Within the sampling window, the input signal must be stable for correct operation.

Inputs must be driven to the voltage levels indicated in chapter 8 when AC specifications are measured.

The ZISC output delays are specified with maximum Worst Case and minimum Best Case limits. The minimum delays times are hold times provided to external circuitry.

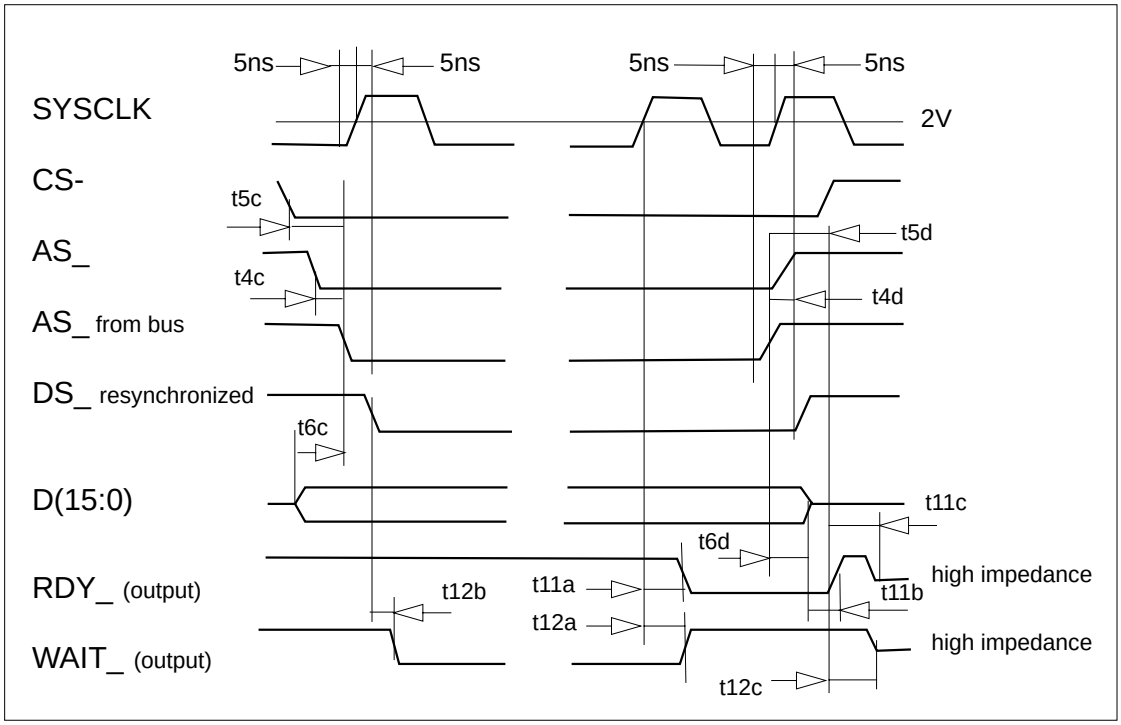

FIGURE 22. **AC specification for asynchronous operation**

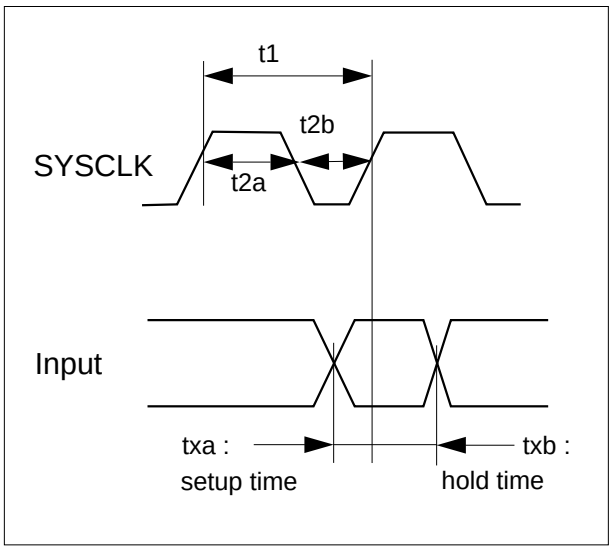

FIGURE 23. AC specifications for SYSCLOCK and synchronous operation

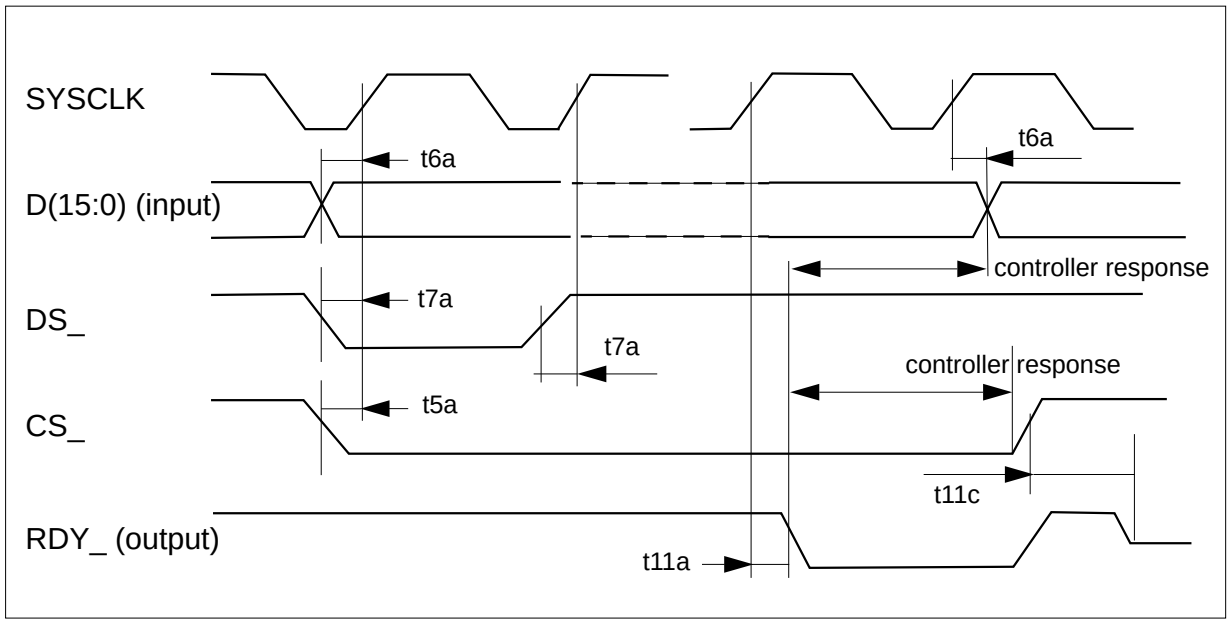

FIGURE 24. AC specifications for synchronous operation

Table 28: AC Specification - Output load 50pF -

Symbol	Parameter	Min.	Max.	Reference Signal	Notes
t1	SYSCLK Period	50 ns			square clock
t2a	SYSCLK High Time	10 ns			at 2V
t2b	SYSCLK Low Time	16 ns			at 2V
t3a	A(5:0) Setup Time	3 ns		SYSCLK	Synchronous Mode
t3b	A(5:0) Hold Time	1 ns		SYSCLK	Synchronous Mode
t3c	A(5..0) Set up time	0 ns		AS_	Asynchronous mode
t3d	A(5:0) Hold Time	2ns		AS_	Asynchronous mode
t4a	AS_ Setup Time	5.5 ns		SYSCLK	Synchronous Mode
t4b	AS_ Hold Time	.5 ns		SYSCLK	Synchronous Mode
t4c	AS_ Setup Time	2 ns		DS_	Asynchronous mode
t4d	AS_ Hold Time	0 ns		DS_	Asynchronous mode
t5a	CS_ Setup Time	5.5 ns		SYSCLK	Synchronous Mode
t5b	CS_ Hold Time	.5 ns		SYSCLK	Synchronous Mode
t5c	CS_ Setup Time	2 ns		DS_	Asynchronous mode
t5d	CS_ Hold Time	0 ns		DS_	Asynchronous mode
t6a	D(15:0) Setup Time	3.5 ns		SYSCLK	Synchronous Mode
t6b	D(15:0) Hold Time	1 ns		SYSCLK	Synchronous Mode
t6c	D(15:0) Setup Time	0 ns		DS_	Asynchronous mode
t6d	D(15:0) Hold Time	0 ns		DS_	Asynchronous mode
t7a	DS_ Setup Time	3.5 ns		SYSCLK	Synchronous Mode
t7b	DS_ Hold Time	.5 ns		SYSCLK	Synchronous Mode
t8a	SM Setup Time	5 ns		SYSCLK	Synchronous Mode
t8b	SM Hold Time	.5 ns		SYSCLK	Synchronous Mode
t9a	RESET Setup Time	0 ns		SYSCLK	Synchronous Mode
t9b	RESET Hold Time	3 ns		SYSCLK	Synchronous Mode
t10a	D(15:0) Access Time	8 ns	45.5 ns	SYSCLK	
t10b	D(15:0) Float Delay	8 ns	40 ns	SYSCLK	
t10c	D(15:0) Float Delay	5.5 ns	37 ns	DS_	note 1
t11a	RDY_ fall delay	8 ns	42 ns	SYSCLK	
t11b	RDY_ Rise delay	8 ns	26 ns	DS_	
t11c	RDY_ Float Delay	5.5 ns	20 ns	CS_ & SBY	note 1
t12a	WAIT_ Access Rise Delay	9 ns	45.5 ns	SYSCLK	
t12b	WAIT_ Access Time	7 ns	21 ns	DS_ & CS_	
t12c	WAIT_ Float Delay	6 ns	20 ns	CS_ & SBY	note 1
t13a	AACK_ Access Time	8 ns	27 ns	SYSCLK	
t13b	AACK_ Float Delay	5.5 ns	20 ns	CS_ & SBY	

Table 28: AC Specification - Output load 50pF -

Symbol	Parameter	Min.	Max.	Reference Signal	Notes
t14a	IOS16_ Access Time	8 ns	33 ns	A(5)	
t14b	IOS16_ Float Delay	13 ns	32 ns	CS_	
t15a	ID_ Access Time	14.5 ns	65 ns	SYSCLK	note 3
t15b	ID_ Float Delay	9 ns	33 ns	SYSCLK	note 4
t15c	ID_ Float Delay	5.5 ns	31 ns	CS_ & DS_	note 1
t16a	NID_ Access Time	14.5 ns	57 ns	SYSCLK	note 2
t16b	NID_ Float Delay	17 ns	49 ns	CS_ & DS_	note 1
t16c	NID_ Float Delay	12 ns	33.5 ns	SYSCLK	note 5
t17a	UNC_ Access Time	14.5 ns	41.5 ns	SYSCLK	note 2
t17b	UNC_ Float Delay	17 ns	49 ns	CS_ & DS_	note 1
t17c	UNC_ Float Delay	10 ns	33.5 ns	SYSCLK	note 5
t18a	DEG_ Access time	14.5 ns	59 ns	SYSCLK	note 2
t18b	DEG_ Float Delay	17 ns	49 ns	CS_ & DS_	note 1
t18c	DEG_ Float Delay	12 ns	33.5 ns	SYSCLK	note 5
t19a	FULL Access Time	8 ns	53.5 ns	SYSCLK	
t19b	FULL Float Delay	10 ns	41.5 ns	SYSCLK	note 4
t20a	DCO Access Time	8 ns	45 ns	SYSCLK	
t20b	DCO Float Delay	10.5 ns	33 ns	SYSCLK	note 4
t21a	ERROR_ Access Fall Time	11 ns	36 ns	SYSCLK	
t21b	ERROR_ Float Delay	10 ns	41.5 ns	SYSCLK	note 4
t22a	IRQ_ Access Fall Time	8 ns	36 ns	SYSCLK	
t22b	IRQ_ Float Delay	10 ns	20 ns	SYSCLK	note 4
t23a	OUT_ Access Time	8 ns	53 ns	SYSCLK	note 2
t23b	OUT_ Float Delay	8 ns	48 ns	CS_ & DS_	note 5
t23c	OUT_ Float Delay	10 ns	33 ns	SYSCLK _	note 1

Notes: 1. These timing delays are valid for the asynchronous mode. In Synchronous mode these outputs return to HZ in the cycle following the assertion of RDY_.

Notes: 2. These timing delays are given for information purpose. These outputs are evaluated in the cycles prior to the assertion of RDY_. When RDY_ is asserted or when WAIT_ is negated these outputs are already valid and they return to HZ when RDY_ returns to HZ.

Notes: 3. The signal ID remains valid until the next WRITE LAST COMPONENT.

Notes: 4. The signals are driven into high state by the bit SBY of the CSR.

Notes: 5. The signals are driven HZ at the end of the operation when RDY_ returns to ‘1’ .

CHAPTER 10

Mecanical Specifications

The ZISC036 is packaged in a thin profile 144 PFP module. Packaging thickness is compatible with PCM-CIA type 1 requirements.

Module dimensions and pin locations are given in the following figure and in table 29.

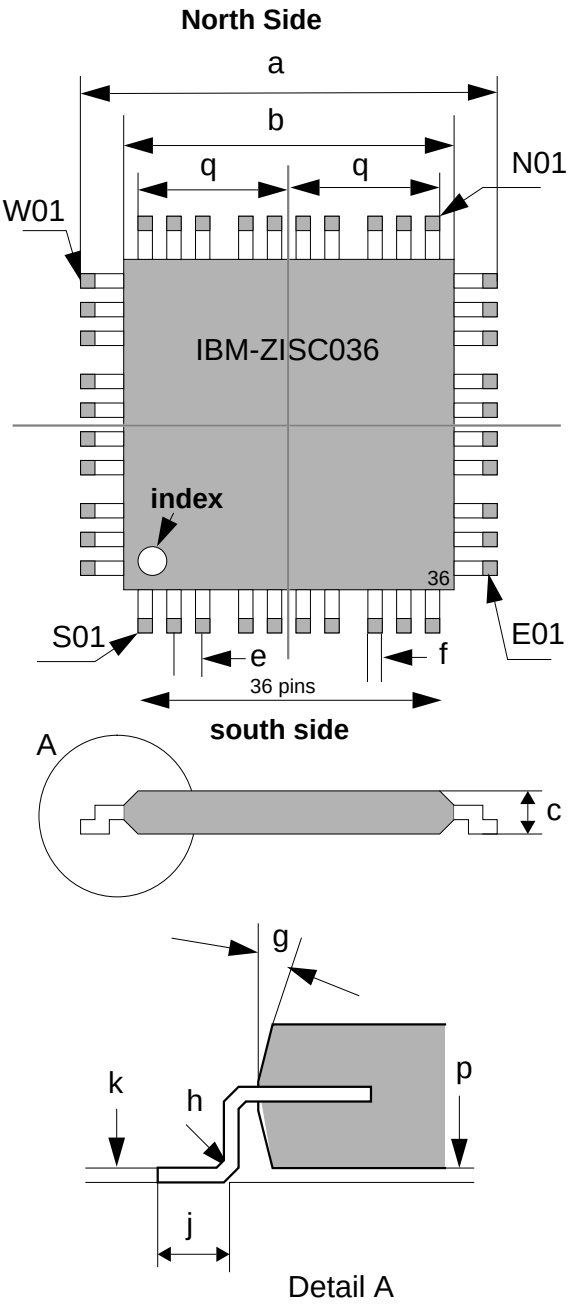

Table 29: 144PFP package dimensions

name	ref.	dimension	unit
total width	a	22	mm
body width	b	20	mm
total thickness	c	1.6 max.	mm
lead pitch	e	0.5	mm
lead width	f	0.2+ - 0.05	mm
body side angle	g	15	deg
lead bend radius	h	0.2 max.	mm
foot length	J	0.5	mm
lead thickness	k	0.15	mm
body guard	p	0.05	mm
	q	9.75	mm

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The ZISC036 is manufactured under a patent and a technology licence from Nestor Inc.

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