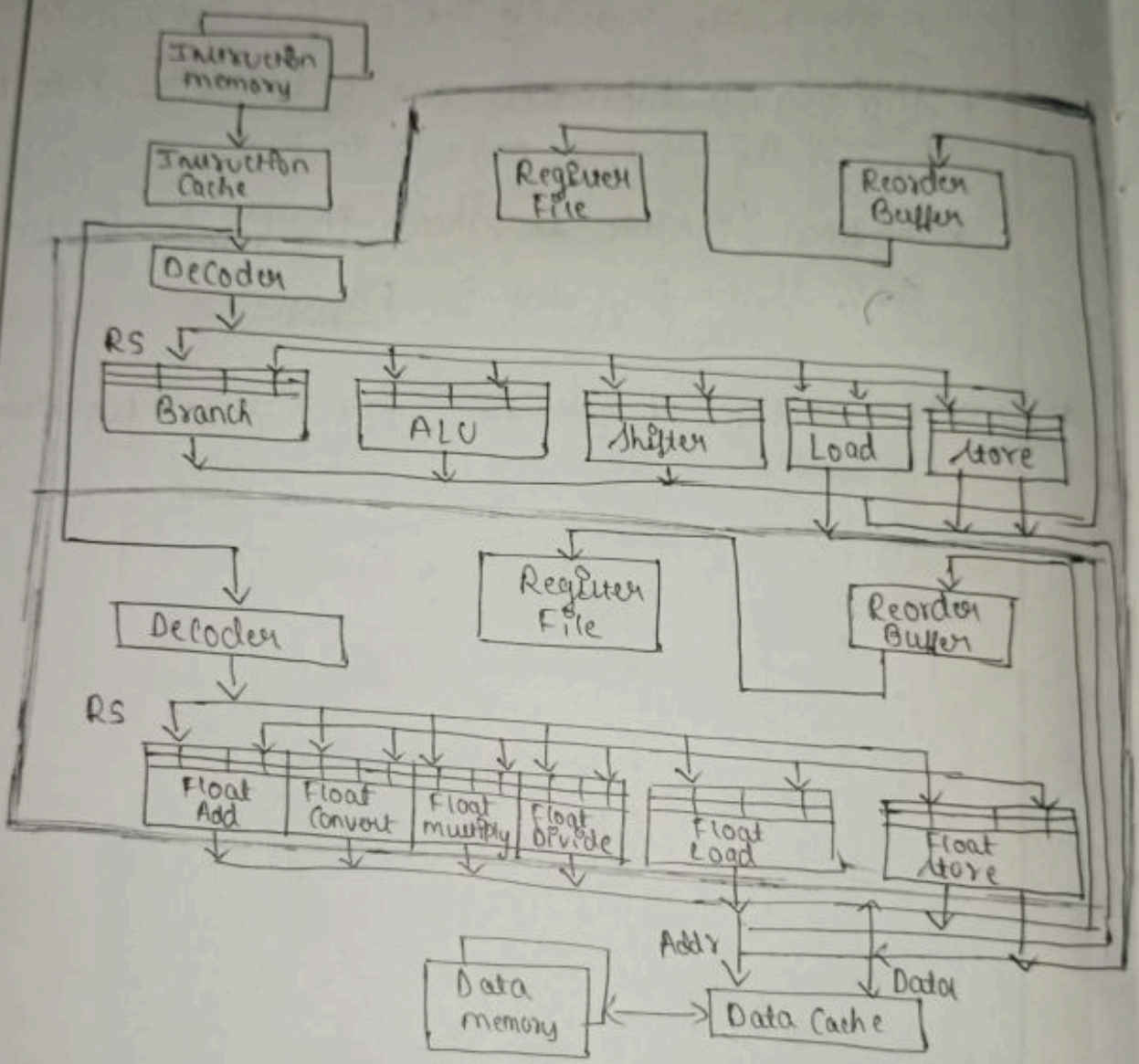
Assignment - II

1) With diagram, explain the pipeling in Super Scalar Processors and VLIW Processors.



Typical Superscalar Architecture

- A typical superscalar will have
  - multiple instruction pipelines
  - an instruction cache that can provide multiple instructions per

Fetch
- multiple buses among the function units.
- In theory, all functional units can be simultaneously active.

VLIW Architecture

* VLIW = Very long Instruction word.
* Instruction usually hundreds of bits long.
* Each Instruction word essentially carries multiple - short instructions.
* Each of the - short instructions are effectively fired at the same time.
* Compilers for VLIW architectures should optimally try to predict branch outcomes to properly group instructions.

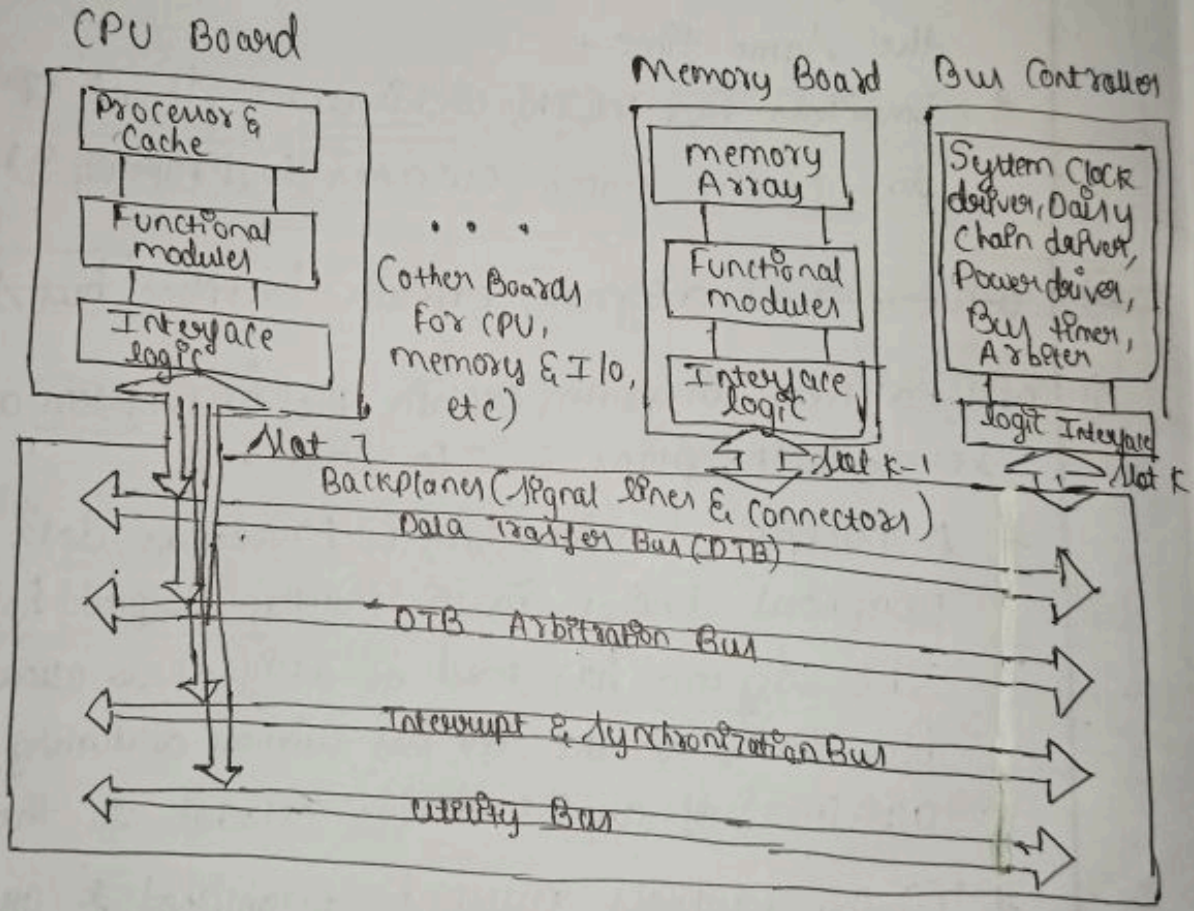
~~2) With a neat diagram, explain backplane bus systems.~~

2) With a neat diagram, explain the bus system at board level, back plane & I/O level:

* A backplane bus interconnects processors, data storage & peripheral devices in a tightly coupled hardware.
* The system bus must be designed to allow communication blw devices on the ~~dev~~ bus without disturbing the internal activities of all the devices attached to the bus.
* Timing protocols must be established to arbitrate among multiple requests, Operational rules must be set to ensure orderly data transfers on the bus.

Data Transfer Bus (DTB)

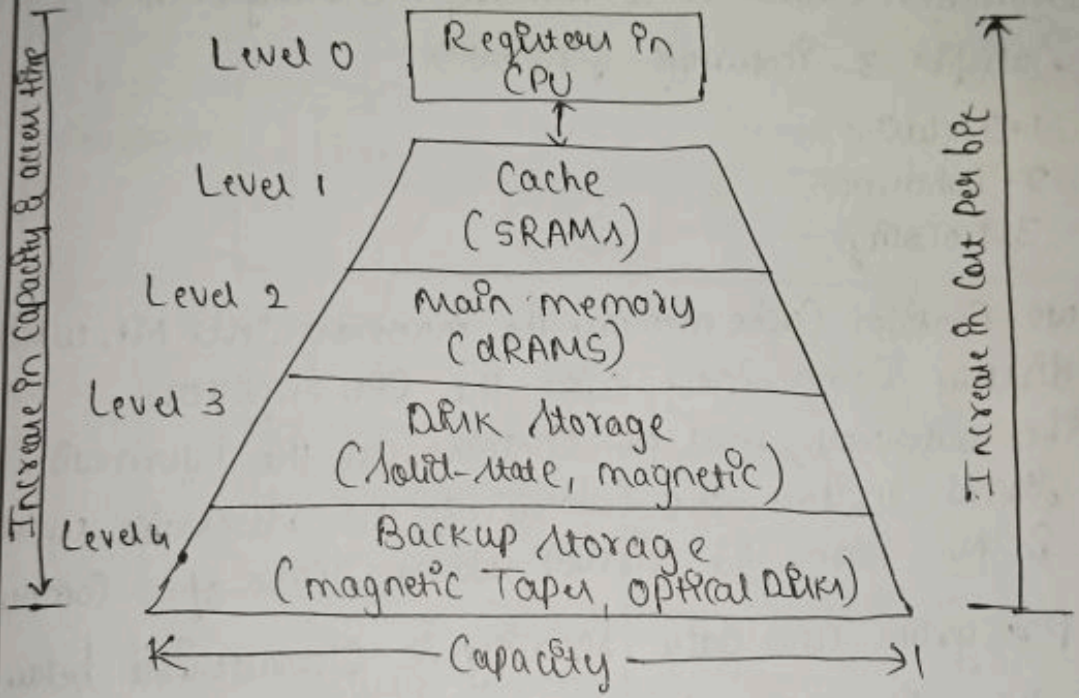
* Data address & Control lines From the data transfer bus in VME bus.
* Address lines broadcast data & device address.
  - Proportional to log of address space size.
* Data lines proportional to memory word length.
* Control lines Specify Read/write, timing & bus error conditions.



3) Explain ~~the Pachuton~~ with a neat diagram Hierarchical memory technology.

* Storage devices such as registers, Cache, main memory, disk devices, & backup storage are often organized as a hierarchy.
* The memory technology & storage organization at each level is characterized by 5 parameter.

1. access time t_i
2. memory size s_i
3. Cost per byte c_i
4. transfer bandwidth b_i
5. Unit of transfer x_i



memory devices at a lower level are:

* faster to access,
* are smaller in capacity
* are more expensive per byte
* have a higher bandwidth, &
* have a smaller unit of transfer.

In general, $t_{i-1} < t_i$, $s_{i-1} < s_i$, $c_{i-1} > c_i$, $b_{i-1} > b_i$ & $x_{i-1} < x_i$ for $i = 1, 2, 3$ & 4 in the hierarchy where $i = 0$ corresponds to the CPU register level.

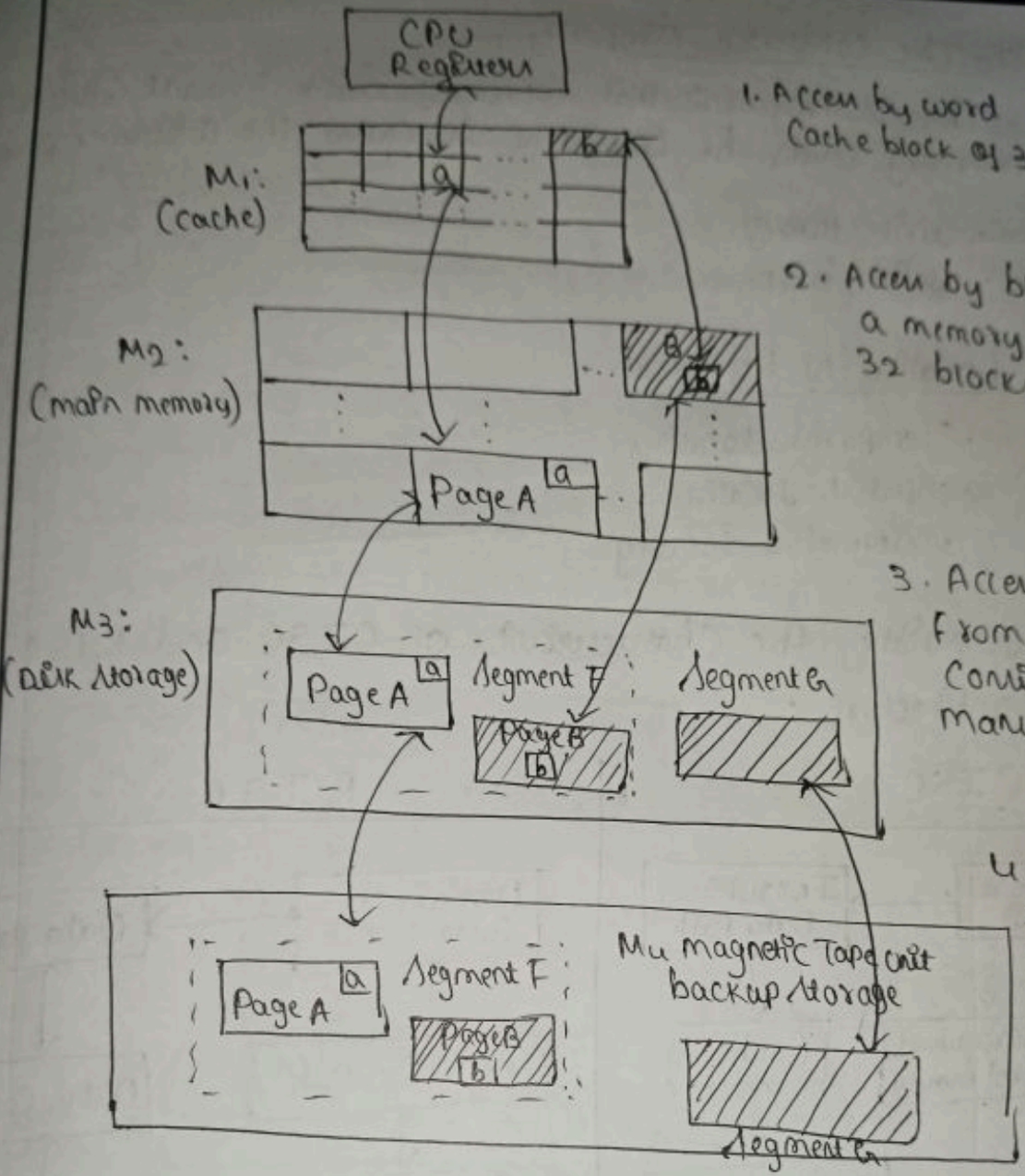
The cache is at level 1, main memory at level 2, the disk at level 3 & backup storage at level 4.

4) Explain the inclusion property & locality of reference along with its types in multilevel memory hierarchy.

⇒ Information stored in a memory hierarchy ($M_1, M_2, \ldots M_n$) satisfies 3 important properties:

1. Inclusion
2. Coherence
3. Locality

* we consider cache memory the innermost level M_1, which directly communicates with the CPU registers.
* The outermost level M_n contains all the information words stored. In fact, the collection of all addressable words in M_n forms the virtual address space of a computer.
* program and data locality is characterized below as the foundation for using a memory hierarchy effectively.



1. Access by word from a cache block of 32 Bytes.

2. Access by block from a memory page of 32 blocks.

3. Access by page from a file consisting of many pages.

4. Segment transfer with different no. of pages.

1. The Inclusion property

* The Inclusion property is stated as

$M_1 \subset M_2 \subset \ldots \subset M_n$

* The Implication of the Inclusion Property is that all items of information in the innermost memory level.

2. The Coherence Property.

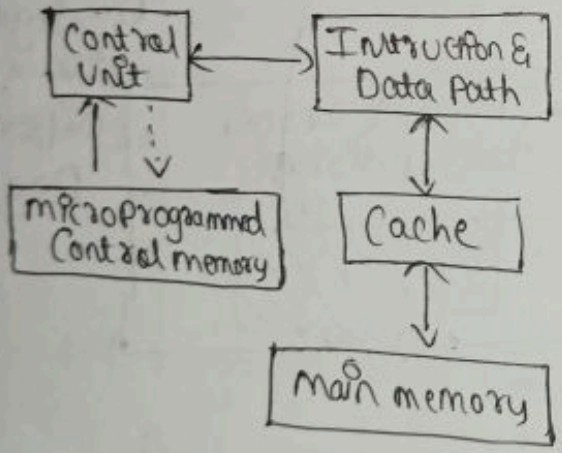
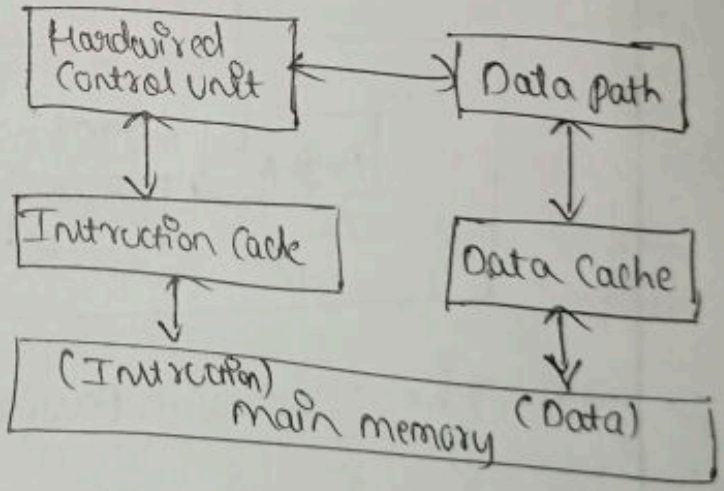
The requirement that copies of data item at successive memory levels be consistent is called the coherence property.

- write-through
- write-back.

3. Locality of References

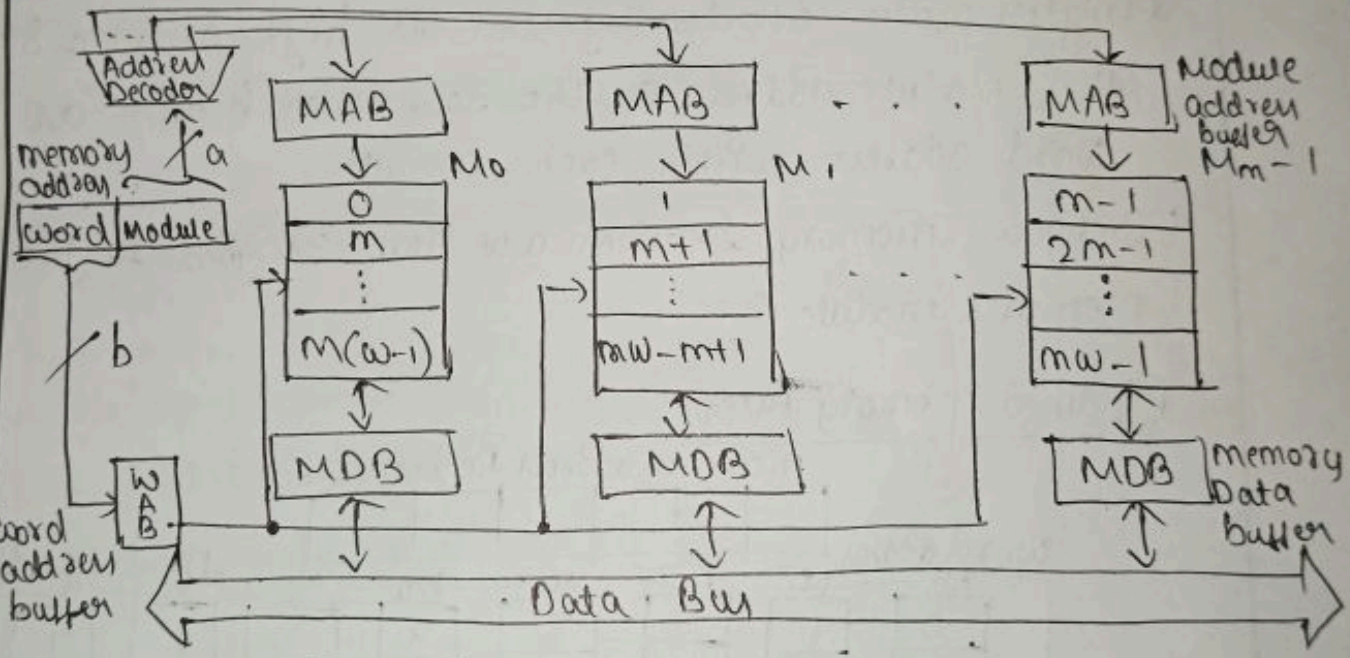
- Temporal locality
- Spatial locality
- Sequential locality.

5) Differentiate the characteristics of CISC and RISC Architecture.

CISC	RISC
	
* Complex Instruction Set Computer	* Reduced Instruction Set Computer.
* Large set of instructions with variable formats	* Small set of instructions with fixed format.

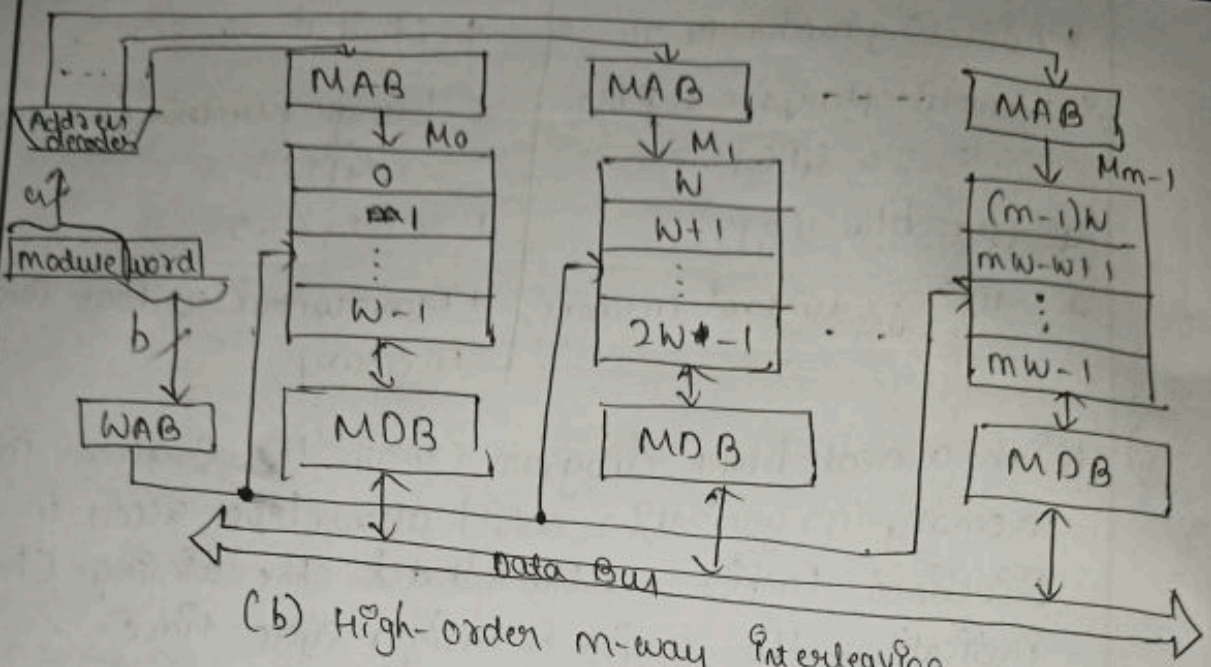
* Addressing modes (2-24	* Limited to 3-5
* General-purpose registers 8-24 GPR's.	* Large numbers (32-192) of GPR's.
* CPI b/w 2 & 15	* CPI < 1.5
* Using Control memory	* Hardwired without Control memory.

6) With a neat block diagram, explain the C-access Interleaved memory organization which allows block access in a pipelined fashion. Also sketch the timing chart indicating the major & minor cycle time.



(a) Low-order m-way Interleaving.

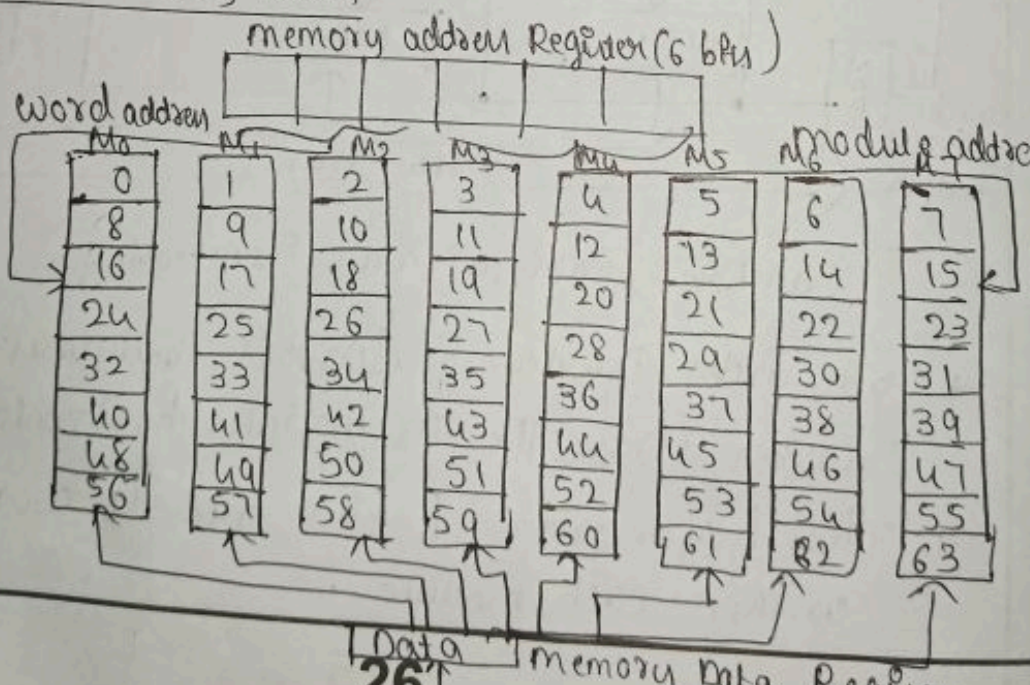
* Low-order Interleaving spreads contiguous memory locations across the m modules horizontally.
* The high-order b bits are the word addresses within each module.

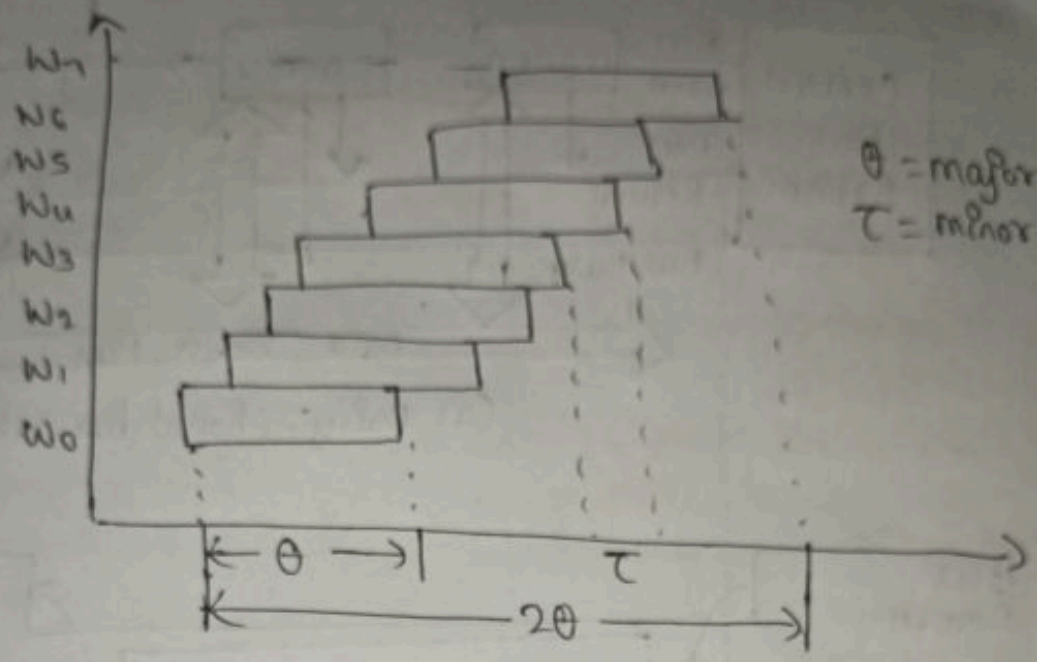


(b) High-order m-way Interleaving.

* Higher-order interleaving uses the high-order a bits as the module address & the low-order b bits as the word address within each module.
* Consecutive memory locations are thus assigned to the same memory module.

Pipelined memory Access





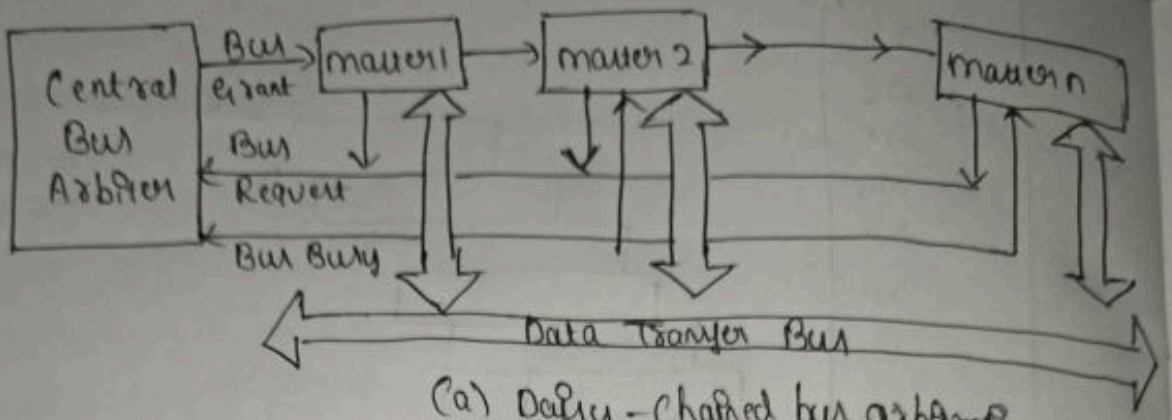
7) What is arbitration? Describe Central arbitration & distributed arbitration with relevant sketches.

⇒ Arbitration

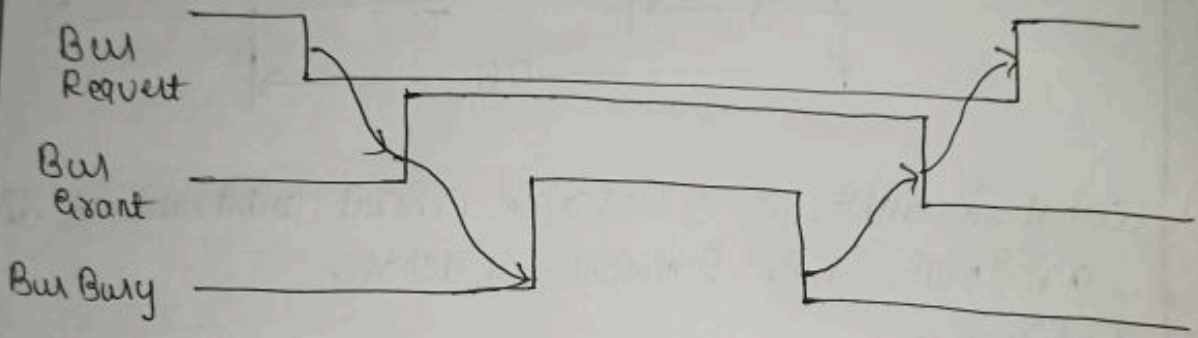
* Procen of selecting next bus master.
* Bus tenure is duration of master's control.
* It restricts the tenure of the bus to one master at a time.
* Competing requests must be arbitrated on a fairness or priority basis.

Central Arbitration

* uses a central arbiter as shown in fig.
* Potential masters are daisy chained in a cascade.
* A special signal line propagates bus-grant from first master to the last master.
* All requests share the same bus-request line.



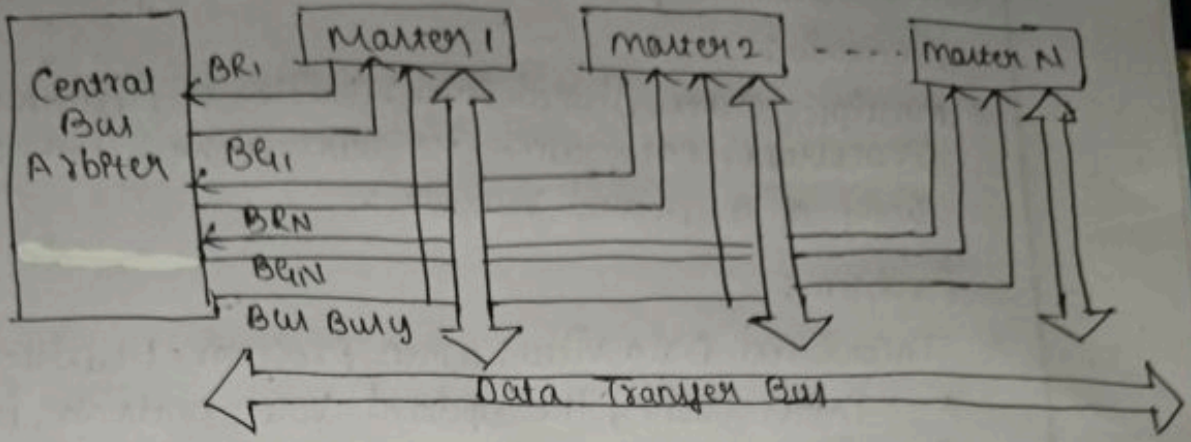
(a) Daisy-Chained bus arbitration.



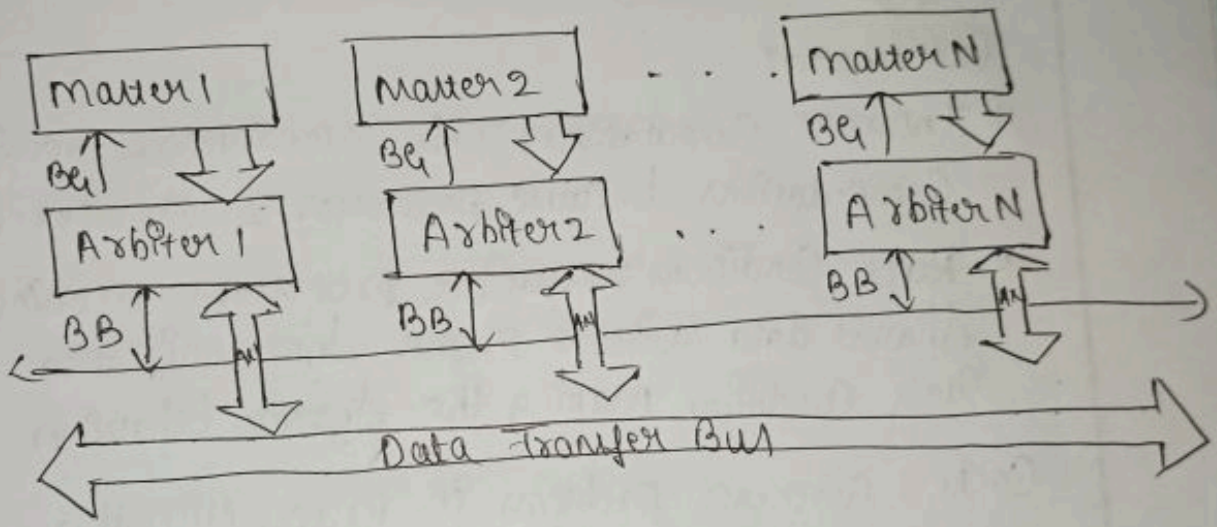
(b) Bus transaction timing.

Distributed Arbitration

* Each master has its own arbiter & unique arbitration number
* use arbitration number to resolve arbitration competition.
* When two or more devices compete for the bus, the winner is the one whose arbitration number is the largest determined by Parallel Contention Arbitration.
* Priority based scheme.



(a) Independent Requests with a Central arbiter.



(b) using distributed arbiters.

8) Define Cache Coherence Problem. Describe Cache Coherence problems in data Sharing & process migration.

=) Cache Coherence is a crucial concept in multiprocessor systems where multiple processors have their own cache memories.

Cache Coherence Problems in Data Sharing

Scenario:

* Multiple Caches, Shared Data: Consider a System with two processors, each with its own cache. Both caches store a copy of a shared variable x

Problem:

* Inconsistent Data View: When processor 1 updates the value of x in its cache, the updated value needs to be reflected in processor 2's cache. If processor 2 does not receive this update, it continues to work with an outdated value of x.

Consequences:

* Incorrect Computations: This inconsistency can lead to incorrect computations because processor 2 operates on stale data.
* Race Conditions: Multiple processors accessing & modifying shared data without proper synchronization can lead to race conditions, making the system behavior unpredictable.

Cache Coherence problems in process Migration

Scenario:

* process migration: A process running on processor 1, with some data cached locally, is moved to processor 2 for load balancing or other reasons.

problem:

* Stale Cache Data: The data cached in processor 1's cache is not immediately available in processor 2's cache.