E0 217: Efficient and Secure Digital Circuits and Systems

Project

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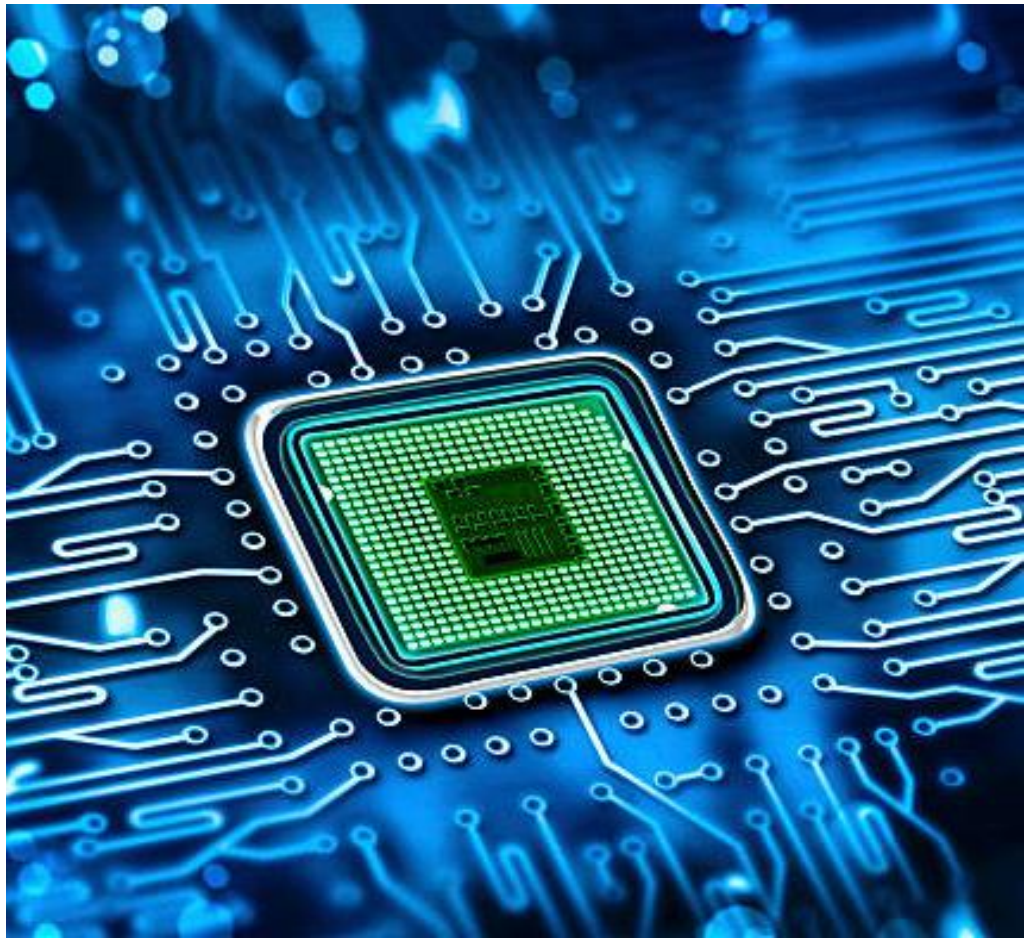
Project Objectives

- Understand design trade-offs
- Optimize a circuit from gate level to architecture level
- Appreciate the economics of electronics industry



Project Objectives

Project Tasks:

- ❑ Design a digital circuit for Fast Fourier Transform (FFT) in Verilog
- ❑ Create an appropriate test bench in Verilog to test the design
- ❑ Simulate the design using Icarus Verilog and visualize the simulated VCD waveforms using GTKWave to verify functionality
- ❑ Synthesize the design using Yosys with the Nangate Open Cell 45nm standard cell library in the typical TT corner
- ❑ Analyze timing and power of the implementation using OpenSTA

Project Overview

FFT Specifications:

- Input $x = \{x_0, x_1, \cdots, x_7\}$
- Output $X = \{X_0, X_1, \cdots, X_7\}$
- Output X is the 8-point FFT of input x
- Output related to input as follows:

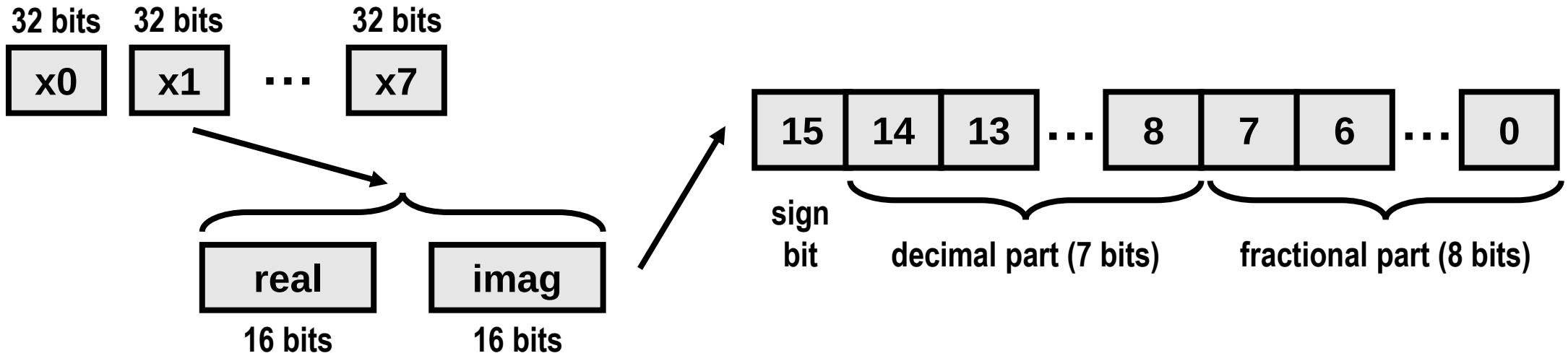
$$X_k = \sum_{m=0}^{7} x_m e^{-i\left(\frac{2\pi km}{8}\right)} \text{ for } k = 0,1,\cdots,7$$

- Reference: https://en.wikipedia.org/wiki/Fast_Fourier_transform

Project Overview

FFT Specifications:

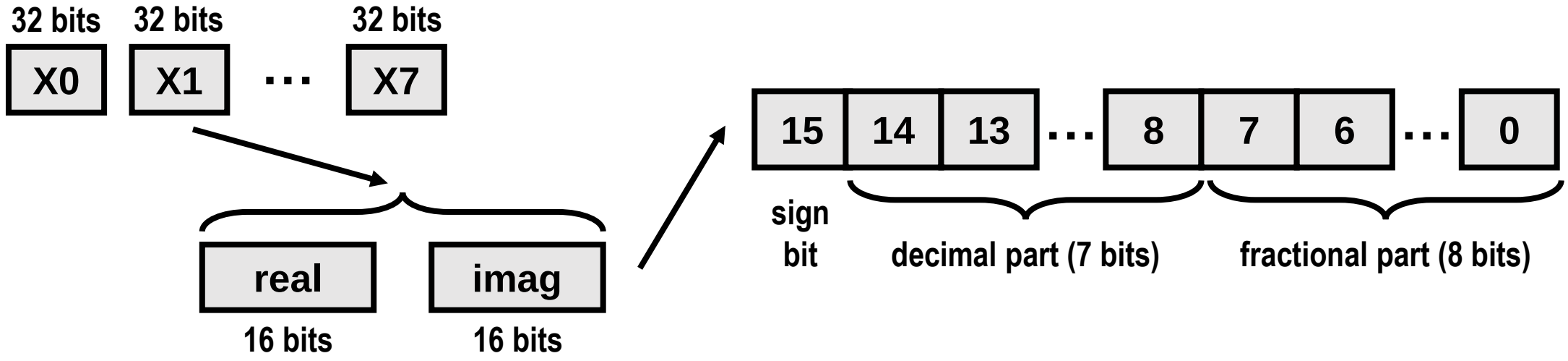
- Each input element x_m (for $m = 0,1, \ldots, 7$) is a complex number with real and imaginary parts each represented as a signed 16-bit fixed-point quantity with 1 sign bit, 7 bits for decimal part and 8 bits for fractional part, as shown below:



Project Overview

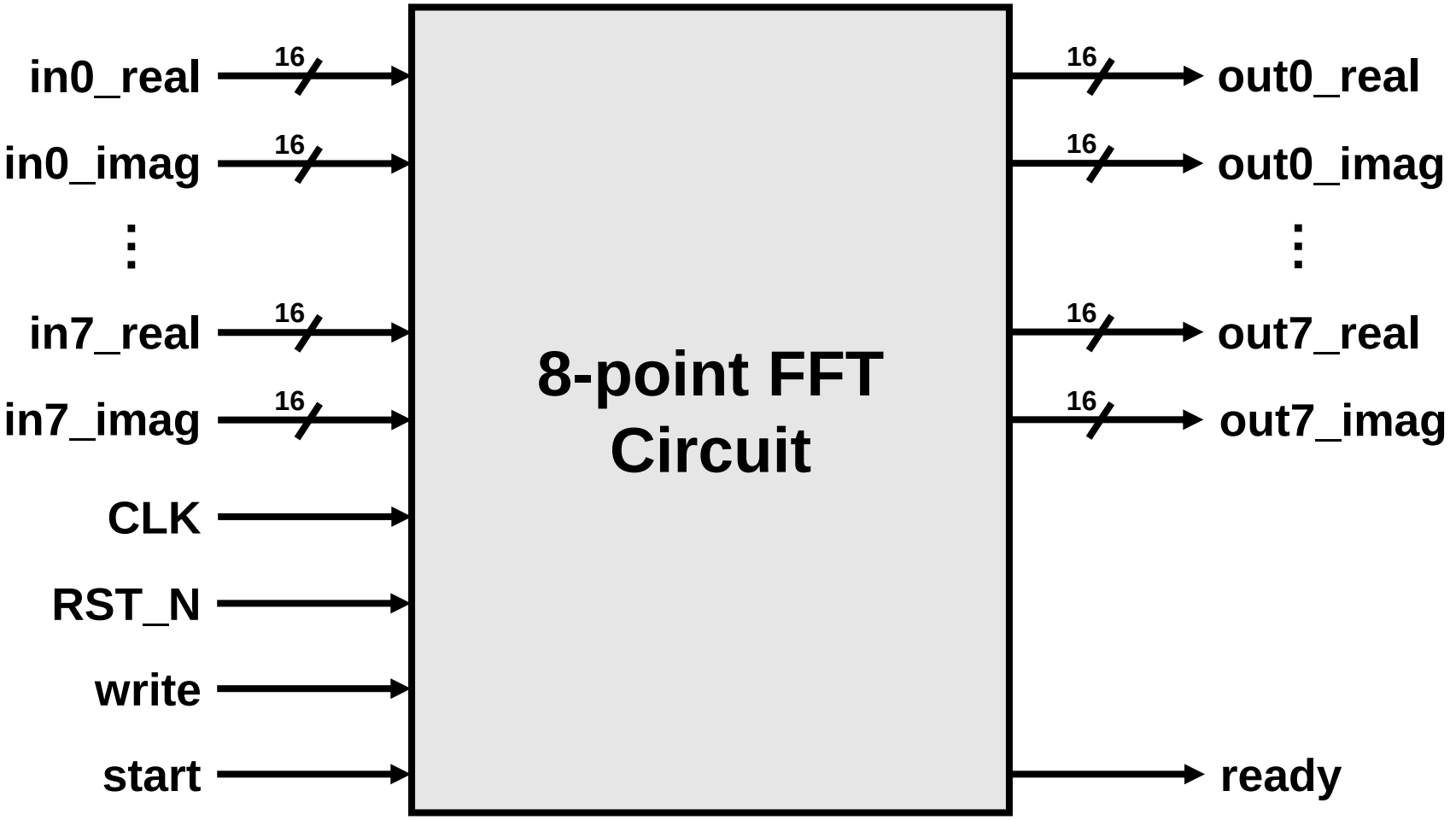
FFT Specifications:

- Each output element X_k (for $k = 0,1,\ldots,7$) is a complex number with real and imaginary parts each represented as a signed 16-bit fixed-point quantity with 1 sign bit, 7 bits for decimal part and 8 bits for fractional part, as shown below:



Project Overview

Block Diagram:



Project Overview

Design Specifications:

Signal	Type	Description
in0_real [15:0]	Input	16-bit real part of x_0
in0_imag [15:0]	Input	16-bit imaginary part of x_0
in1_real [15:0]	Input	16-bit real part of x_1
in1_imag [15:0]	Input	16-bit imaginary part of x_1
in2_real [15:0]	Input	16-bit real part of x_2
in2_imag [15:0]	Input	16-bit imaginary part of x_2
in3_real [15:0]	Input	16-bit real part of x_3
in3_imag [15:0]	Input	16-bit imaginary part of x_3

Project Overview

Design Specifications:

Signal	Type	Description
in4_real [15:0]	Input	16-bit real part of x_4
in4_imag [15:0]	Input	16-bit imaginary part of x_4
in5_real [15:0]	Input	16-bit real part of x_5
in5_imag [15:0]	Input	16-bit imaginary part of x_5
in6_real [15:0]	Input	16-bit real part of x_6
in6_imag [15:0]	Input	16-bit imaginary part of x_6
in7_real [15:0]	Input	16-bit real part of x_7
in7_imag [15:0]	Input	16-bit imaginary part of x_7

Project Overview

Design Specifications:

Signal	Type	Description
out0_real [15:0]	Output	16-bit real part of X_0
out0_imag [15:0]	Output	16-bit imaginary part of X_0
out1_real [15:0]	Output	16-bit real part of X_1
out1_imag [15:0]	Output	16-bit imaginary part of X_1
out2_real [15:0]	Output	16-bit real part of X_2
out2_imag [15:0]	Output	16-bit imaginary part of X_2
out3_real [15:0]	Output	16-bit real part of X_3
out3_imag [15:0]	Output	16-bit imaginary part of X_3

Project Overview

Design Specifications:

Signal	Type	Description
out4_real [15:0]	Output	16-bit real part of X_4
out4_imag [15:0]	Output	16-bit imaginary part of X_4
out5_real [15:0]	Output	16-bit real part of X_5
out5_imag [15:0]	Output	16-bit imaginary part of X_5
out6_real [15:0]	Output	16-bit real part of X_6
out6_imag [15:0]	Output	16-bit imaginary part of X_6
out7_real [15:0]	Output	16-bit real part of X_7
out7_imag [15:0]	Output	16-bit imaginary part of X_7

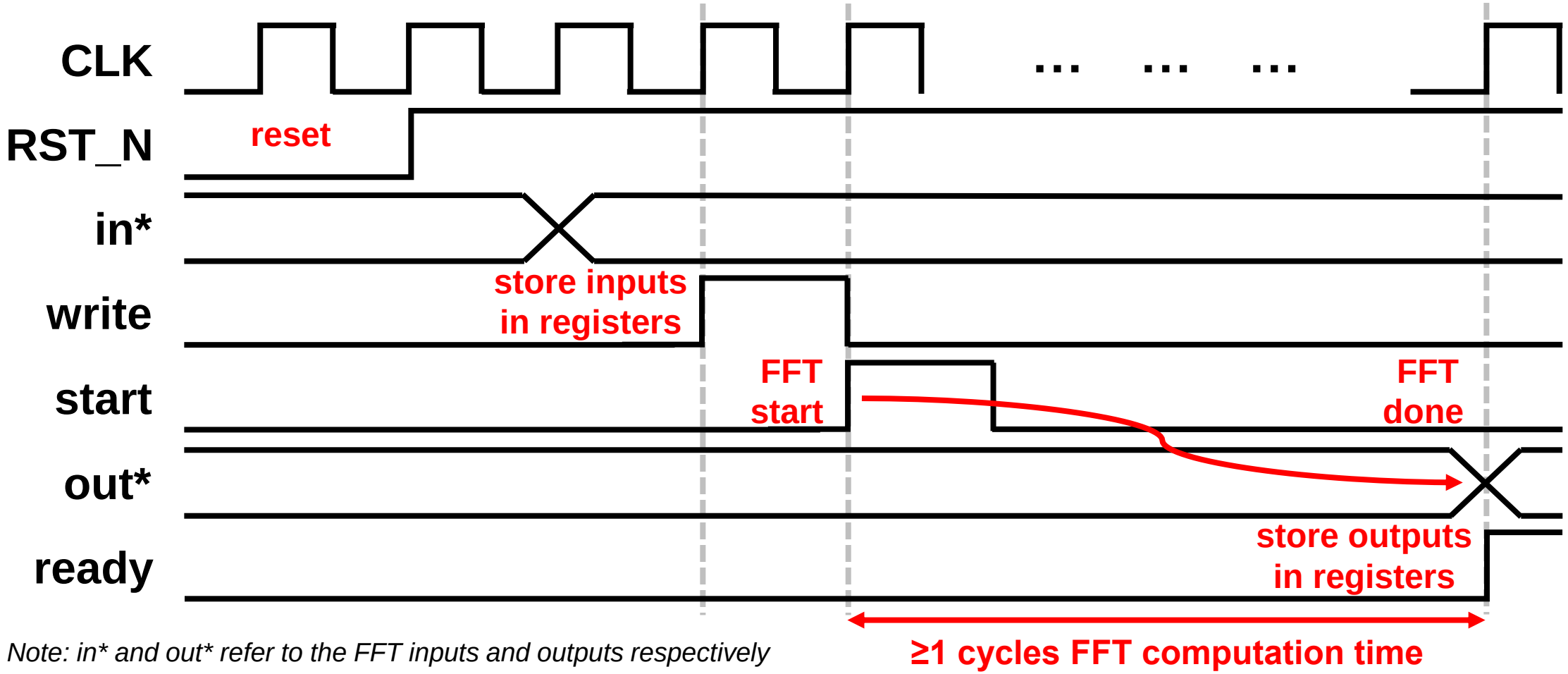
Project Overview

Design Specifications:

Signal	Type	Description
CLK	Input	Clock signal
RST_N	Input	Active-low reset signal
write	Input	Input write signal
start	Input	FFT computation start signal
ready	Output	FFT computation done signal

Project Overview

Timing Diagram:



Note: in and out* refer to the FFT inputs and outputs respectively*

Project Overview

Functional Verification:

- Must use the following in the test bench to verify functionality
- Inputs:

$$x_0 = 0.0 + i0.0, x_1 = 1.0 + i0.0, x_2 = 2.0 + i0.0, x_3 = 3.0 + i0.0,$$
$$x_4 = 4.0 + i0.0, x_5 = 5.0 + i0.0, x_6 = 6.0 + i0.0, x_7 = 7.0 + i0.0$$

- Calculate the expected outputs $X_0', X_1', \cdots, X_7'$ corresponding to 8-point FFT of $x_0, x_1, \cdots, x_7$ using MATLAB or Python

Project Overview

Functional Verification:

- Expected Outputs:

$$X_0' = 28.0 + i0.0, X_1' = -4.0 + i4.0(\sqrt{2} + 1),$$

$$X_2' = -4.0 + i4.0, X_3' = -4.0 + i4.0(\sqrt{2} - 1),$$

$$X_4' = -4.0 + i0.0, X_5' = -4.0 - i4.0(\sqrt{2} - 1),$$

$$X_6' = -4.0 - i4.0, X_7' = -4.0 - i4.0(\sqrt{2} + 1)$$

Project Overview

Functional Verification:

- Obtain the FFT circuit simulated outputs $X_0, X_1, \cdots, X_7$
- Calculate the maximum absolute error by comparing the real and imaginary parts of each element of the simulated outputs and the expected outputs as

$$\max(\ |\mathrm{Re}(X_0') - \mathrm{Re}(X_0)|,\ |\mathrm{Im}(X_0') - \mathrm{Im}(X_0)|,\ |\mathrm{Re}(X_1') - \mathrm{Re}(X_1)|,\ |\mathrm{Im}(X_1') - \mathrm{Im}(X_1)|,\ \ldots,\ |\mathrm{Re}(X_7') - \mathrm{Re}(X_7)|,\ |\mathrm{Im}(X_7') - \mathrm{Im}(X_7)|,\ )$$

Project Overview

Functional Verification:

- Although verified with one input/output combination (test vector), circuit must be functional for all possible input/output combinations
- Feel free to simulate with additional random test vectors
- Note the number of clock cycles required by the circuit to complete 8-point FFT computation, that is, from rising edge of “start” signal to rising edge of “ready” signal

Project Overview

Implementation Aspects:

- Inputs $x_0, x_1, \cdots, x_7$ stored in input register (8 × 2 × 16 = 256 bits) and outputs $X_0, X_1, \cdots, X_7$ stored in output register (8 × 2 × 16 = 256 bits)
- Contains both combinational and sequential logic
- Arithmetic circuits are very important components in the design
- Need not be restricted to what has been taught in lectures
- Feel free to refer to books, papers and online resources
- Must cite all references in final project report

Project Overview

Implementation Metrics:

- ❑ Number of clock cycles per FFT (from Icarus Verilog & GTKWave)
- ❑ Area of synthesized design (from Yosys)
- ❑ Maximum clock frequency (from OpenSTA)
- ❑ Total power consumption (from OpenSTA)
- ❑ Energy consumption per FFT
- ❑ Accuracy of FFT computation

Project Overview

Implementation Aspects:

- Optimize the implementation for one of the following:
  - low power
  - low latency
  - high throughput
  - low area
  - low energy
  - high accuracy

Project Overview

Implementation Aspects:

- ❑ Implementation must be functionally correct with small error
- ❑ Explore different data flows (butterfly operations in FFT)
- ❑ Analyze architectures for signed fixed-point arithmetic
- ❑ Implement arithmetic with complex numbers
- ❑ Tune precision of twiddle factors
- ❑ Understand design trade-offs
- ❑ …

Project Report

- One implementation and one final report per group
- Both team members must submit same report separately in Teams
- Clearly document the following in report (format to be shared later):
  - architecture details with block diagrams
  - screenshots of simulation and synthesis results
  - Verilog descriptions for design and test bench
  - contributions of each team member

Project Grading

- Project has 20% weightage in course
- Total 20 points
  - 5 points for implementing / simulating circuit and preparing report
  - 5 points for explaining design and providing Verilog descriptions
  - 5 points for calculating implementation metrics
  - 5 points for design trade-offs
- Implementations with very similar design and/or metrics will receive less score ⇒ do not copy each other's designs!