BE-820: Project Phase II

Studies on SiGe based Stacked Drain FDSOI MOSFET

A Project Report

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Bachelor of Technology

in

Electronics & Communication Engineering

by

KISHAN KUMAR

B. Tech 8th Semester

Enrollment No- U2051068

Under the Supervision of

Dr. Nilesh Anand Srivastava

(Assistant Professor)

Department of Electronics and Communication,

J.K. Institute of Applied Physics & Technology

University of Allahabad, Prayagraj (211002), India

May 2024

CANDIDATE'S DECLARATION

I**, Kishan Kumar**, hereby certify that the work, which is being presented in the report, entitled "**Studies on SiGe based Stacked Drain FDSOI MOSFET"** in partial fulfillment of the requirement for the award of the Degree of **Bachelor of Technology (ECE)** and submitted to the institution is an authentic record of my own work carried out during the period Jan.-2024 to May-2024 under the supervision of "**Dr. Nilesh Anand Srivastava"** at the Department of Electronics and Communication, University of Allahabad. The matter presented in this report has not been submitted elsewhere for the award of any other degree or diploma from any Institutions.

Date:- Signature of the Candidate

KISHAN KUMAR

B. Tech (ECE) 8th Semester

Enrollment No-U2051068

CERTIFICATE

This is to certify that **Kishan Kumar,** has carried out this project/dissertation entitled "**Studies on SiGe based Stacked Drain FDSOI MOSFET".**

Date-

Signature of the Supervisor

(Dr. Nilesh Anand Srivastava)

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ABSTRACT

This study explores the advancements in Silicon-On-Insulator (SOI) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) technology, focusing on novel design approaches and their impact on device performance. The research investigates various aspects, including device architecture, material choices, and aiming to enhance the overall efficiency and reliability of SOI MOSFETs. Through comprehensive simulations, experimental validations, and comparative analyses, the study highlights the potential advantages and challenges associated with novel SOI MOSFET structures. Furthermore, the investigation delves into the implications of these advancements for applications in high-performance integrated circuits, low-power electronics, and emerging technologies. The findings contribute to the ongoing evolution of semiconductor devices, providing valuable insights for engineers, researchers, and industry stakeholders engaged in the development and implementation of cutting-edge SOI MOSFET technologies.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

About current trends in MOS Technology:

- CMOS technology evolution in the past few decades has followed the path of device scaling to achieve density, speed and power improvement.
- As indicated by the Moore's law, the number of transistors inside the chip's doubles in every two years because of the shrinking size of MOSFETs.
- It is well known that reducing the source-to-drain spacing, i.e., the channel length of a MOSFET, the driving current in the channel increases. It also leads to the Short Channel Effects (SCEs) in the device. The most undesirable SCE is the reduction in the threshold voltage (V_{th}) at which the device turns on, especially at high drain voltage. The reduced threshold voltage causes the subthreshold leakage current to increase dramatically, which makes the device difficult to turn off.
- New high-resolution lithographic techniques therefore required for the development of new device designs, technologies, and the structures that can keep the SCEs under control at very small dimensions.
- The development in nano MOS devices has almost accepted the technological challenges in electronics and the Internet of Things [4].
- However, the further demand for high-density memory processors is evolving the hyper scaling trends in current running complementary-metal-oxide-semiconductor (CMOS) technology [4].
- Thin-film, fully depleted silicon-on-insulator (SOI) MOSFETs offer superior electrical characteristics over bulk MOS devices, such as reduced junction capacitances, increased channel mobility, excellent latch up immunity and reduced Short Channel Effects (SCEs) [5].

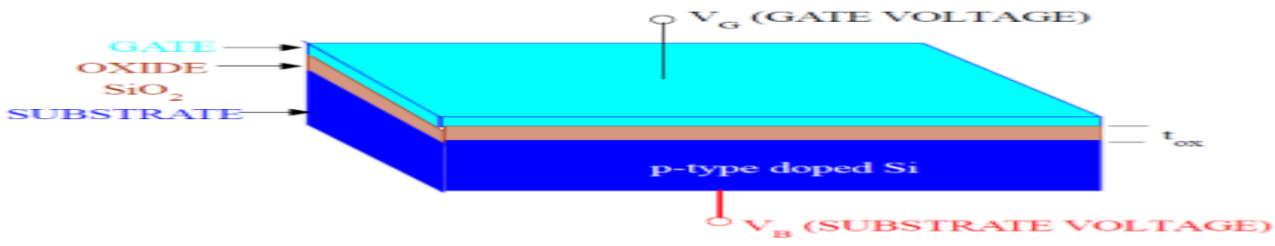

Figure 1.1– MOS structure

1.2 Scaling

Scaling in MOSFETs refers to the process of reducing the physical dimensions of the transistor to improve performance and increase the density of transistors on a chip. This concept is closely tied to Moore's Law, which predicts the doubling of the number of transistors on an integrated circuit approximately every two years, leading to improvements in speed, power efficiency, and cost per transistor.

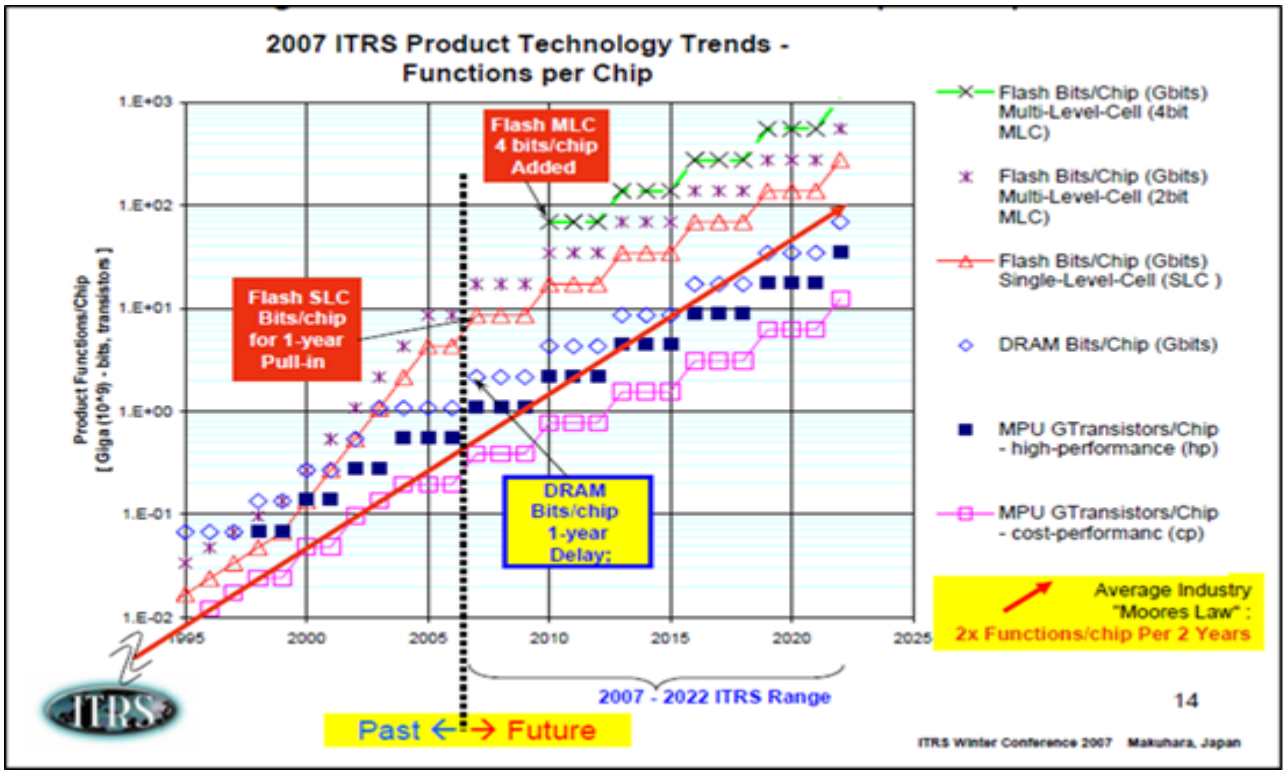

Figure 1.2 - Product functions per chip vs. time (tracking Moore's law)

1.2.1 Scaling Challenges

Scaling of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) is a driving force in the semiconductor industry. Here are the primary scaling challenges faced in MOSFET technology:

1.2.1.1 Short Channel Effects

When the channel length is of same order of magnitude as the depletion layer widths of Source and Drain junction, the short channel effect arises. The short channel effects are the collection of several different problems that arise in a highly scaled MOSFET having a small channel length. As the channel length (L) decreases, there is an increase in both operation speed and number of components per chip. But there is a modification in threshold voltage and electron drift characteristics.

- The main short-channel effects are: -
  - ❖ Drain Induced Barrier lowering and Punch through
  - ❖ Velocity Saturation
  - ❖ Surface Scattering

Drain Induced Barrier Lowering & Punch through

- Drain-induced barrier lowering (DIBL) is the drain voltage-induced decrease in threshold voltage in a short-channel MOSFET at high drain voltages.
- It arises from electrostatic coupling between the drain and the source. In consequence to this coupling, the potential barrier of the source-to-channel junction is depressed.

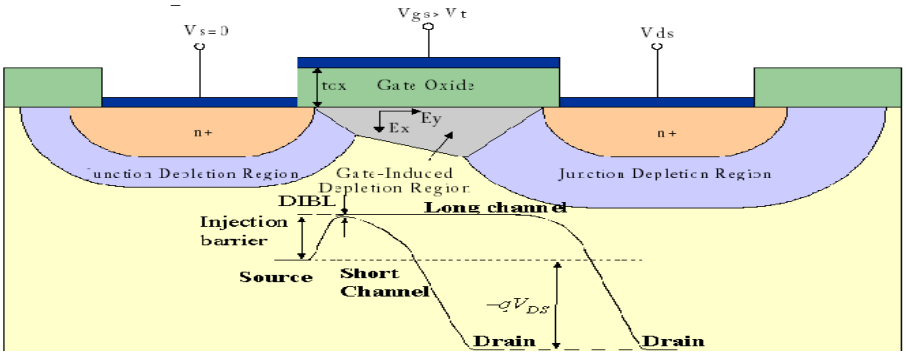

Figure 1.3 – The physical mechanism of DIBL in MOSFET

Velocity Saturation:

- As the gate length is decreased to smaller values, the longitudinal electric field E_x between the source and drain increases and becomes larger.
- At low values of E_x, the carrier velocity v_d is proportional to E_x. But at higher values of E_x, the proportionality relations.

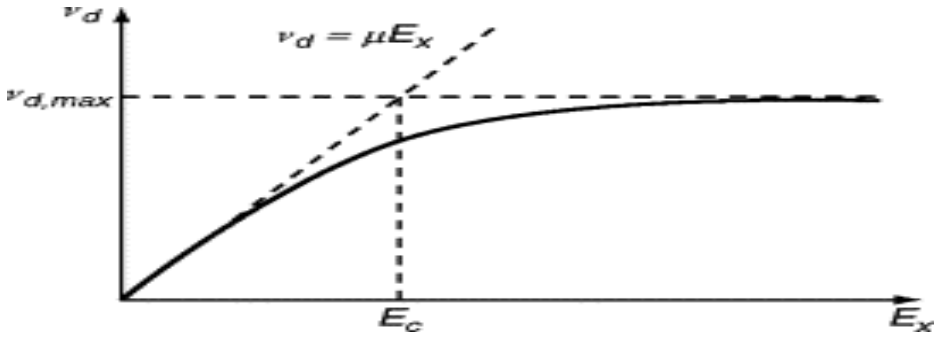

Figure 1.4 - Variation of Drift Velocity and Electric Field

Hot Electron Effect:

- Hot carriers are charged particles, either electrons or holes. They include particles which have acquired very high kinetic energies upon acceleration by the large electric *fi*eld prevalent across the channels of MOSFETs.
- These carriers have higher energies than those of carriers normally found in semiconductor devices. Due to their high energies, hot carriers may migrate.

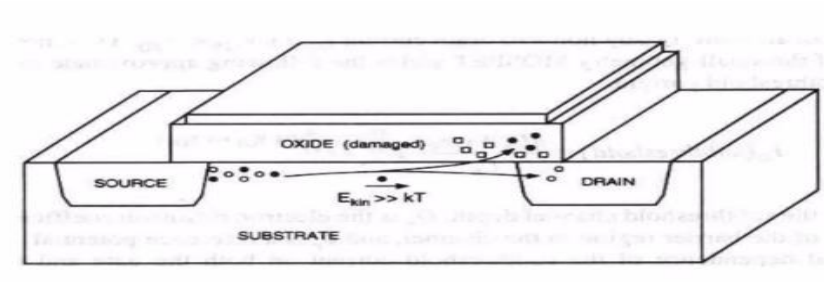

Figure 1.5 – hot Electron Effect

1.2.1.2 Increased leakage Currents

- Subthreshold leakage - As the threshold voltage decreases, the off-state current increases, leading to higher power consumption even when the transistor is off.
- Gate Leakage - Thinner gate oxides lead to higher gate tunneling currents, exacerbating power consumption and impacting the reliability of the device.

1.2.1.3 Parasitic Capacitance & Resistance

As devices scale, parasitic capacitances and resistances become more significant:

- **Gate Capacitance**: Scaling down the gate length increases the gate capacitance, which can limit the speed of the transistor.
- **Source/Drain Resistance**: Higher resistance in the source/drain regions affects the drive current and overall performance of the transistor.

1.3 NOVEL MOS DEVICES

1.3.1 SOI Technology

SOI (Silicon on Insulator) technology is a semiconductor manufacturing technique used to enhance the performance of integrated circuits (ICs). It involves constructing semiconductor devices on a layered silicon-insulator-silicon substrate rather than the traditional bulk silicon substrate.

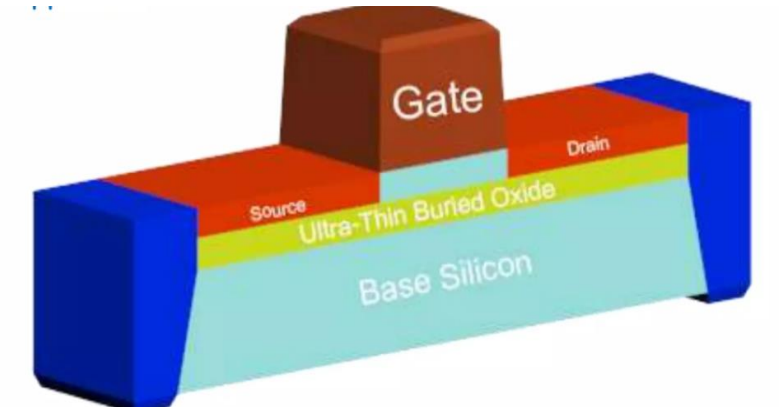

Figure 1.6 – SOI MOSFET structure

1.3.1.1 PDSOI

PD-SOI (Partially Depleted Silicon on Insulator) is a type of SOI technology where the top silicon layer is thick enough that the transistor channel region is not fully depleted of charge carriers during operation. This characteristic leads to distinct electrical properties and performance attributes.

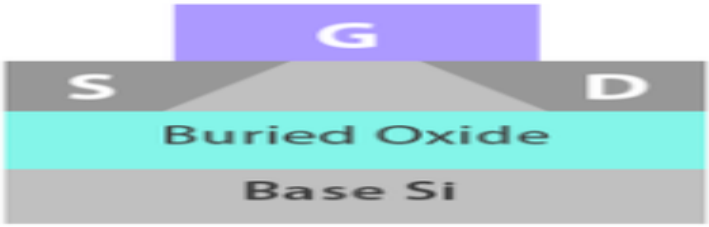

Figure 1.7 – PDSOI MOSFET

1.3.1.2 FDSOI

FD-SOI (Fully Depleted Silicon on Insulator) is a type of SOI technology characterized by a very thin silicon layer on top of an insulating buried oxide (BOX) layer. In FD-SOI, the top silicon layer is thin enough that the entire transistor channel can be fully depleted of charge carriers during operation. This fully depleted state leads to various advantageous electrical properties and performance attributes.

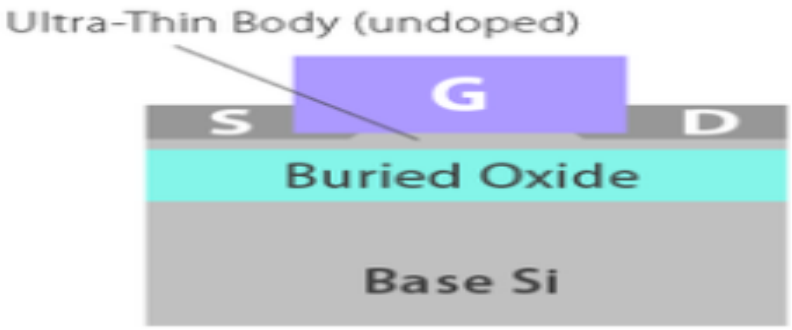

Figure 1.8 – FDSOI MOSFET

1.4 Summary

- In this chapter, first recent trend in MOS devices has been discussed.
- Further, scaling and its challenges has been taken under study.
- Also, SOI technology has been discussed in detail.

CHAPTER 2
LITERATURE REVIEW

2.1 INTRODUCTION

- Initial Concept and Research (1960s-1970s)- The concept of using an insulating layer in semiconductor devices was proposed to reduce parasitic capacitance and improve performance.
- SIMOX (Separation by IMplanted OXygen) - It involves implanting oxygen ions into silicon and annealing to form a buried oxide layer.
- BESOI (Bond & Etch- back SOI) - It involves bonding a silicon wafer to an oxidized wafer and then etching back to achieve the desired silicon layer thickness.
- PD-SOI (Partially Depleted Silicon on Insulator) (1990s) is a type of SOI technology where the top silicon layer is thick enough that the transistor channel region is not fully depleted of charge carriers during operation. This characteristic leads to distinct electrical properties and performance attributes.
- FD-SOI (Fully Depleted Silicon on Insulator) (2000s) is a type of SOI technology characterized by a very thin silicon layer on top of an insulating buried oxide (BOX) layer. In FD-SOI, the top silicon layer is thin enough that the entire transistor channel can be fully depleted of charge carriers during operation. This fully depleted state leads to various advantageous electrical properties and performance attributes.

2.2 LITERATURE SURVEY

- In 1989, Young had proposed very first model of FDSOI MOSFET. The short- channel effect in fully depleted SOI MOSFET's has been studied by a two dimensional analytical model. The vertical field through the depleted film strongly influences the lateral field across the source and drain regions. He observed that , in thin SOI MOSFET's the reduction in threshold voltage due to the short channel effect decreases with decreasing silicon film thickness [1].
- In 1994 , AGGARWAL et al. has proposed that the present model breaks down for the channel lengths below a critical value, of the order of 0.017 μm. In any case, at this kind of dimensions, the carrier transport becomes ballistic and the standard semiconductor equations are no longer valid. For very short lengths, the present model predicts a critical gate voltage beyond which gate losses its control on the drain current. The present two dimensional analysis gives accurate results for the threshold voltage calculation of both short and long channel SO1 MOSFETs [2].
- In 2003, Suzuki et al. had modified the analytical model of FD SOIMOSFET. They proposed that Considering 2-D effects in both SOI and buried-oxide layers, they derived an analytical model for

threshold voltage for short channel single-gate SOI MOSFETs. Their model predicts much less short-channel immunity than the former models and agrees better with numerical data than the former models. The short channel immunity is independent of channel-doping concentration, and the threshold voltage is controlled with channel-doping concentration. Therefore, the device should be designed to satisfy $\lambda \sim L_G/5$ to ensure short-channel immunity, and the value of the threshold voltage can be controlled by N_A [3].

- In 2004, Kumar et al. had proposed multi metal gate based FD SOI MOSFET. Their results unambiguously establish that the introduction of the DMG structure in a fully depleted SOI MOSFET leads to subdued SCEs due to a step-function in the channel potential profile. The shift in the surface channel potential minima position is negligible with increasing drain biases. The electric field in the channel at the drain end is also reduced leading to reduced hot-carrier effect. Also, the variation of the minimum channel potential with de creasing thin-film thickness can be more effectively reduced in the DMG structure at shallow thin-film thicknesses [5].
- In 2008 , Agarwal et al. had proposed a model that by solving the 1-D Poisson equation using appropriate boundary conditions, we report a closed-form sur face potential solution for all the three surfaces (gate oxide–silicon film interface, silicon-film–buried oxide interface, and buried oxide–substrate interface) of fully depleted silicon-on-insulator (SOI) MOSFETs by considering the effect of substrate charge explicitly. During the model derivation, it is assumed that the silicon film is always fully depleted and the back silicon film surface is never inverted [15].
- In 2009 , Rao et al. proposed a unified analytical threshold voltage model for DMG as well as SMG FDSOI MOSFETs with two-dimensional variation in doping concentration is presented for the first time. The model is based on the solution of 2D Poisson's equation and is therefore able to predict the variation of threshold voltage due to short-channel effects even in sub-50 nm channel length devices [7].

- In 2018, Sonam Rewari et al. had proposed an analytical model of dual-metal hetero-dielectric (DM-HD) cylindrical gate all around (GAA) MOSFET has been proposed to address and solve a substantial issue of gate induced drain leakage (GIDL) current in order to improve the device reliability [13].

CHAPTER 3

PERFORMANCE ANALYSIS OF SiGe BASED STACKED DRAIN FDSOI MOSFET

3.1 DEVICE STRUCTURE & SPECIFICATIONS:

Figure 3.1 shows the cross-sectional view of proposed SiGe based stacked drain FDSOI MOSFET & the complete specifications are listed in Table 3.1. Channel length is 50 nm & SiGe is the material used in channel region. Source is upto 25 nm & doping is N^+-type . Drain region is divided into two regions – first region is of N^+- type material which is of 10 nm length & second region is of N- type material that is why the name is entitled as Performance Analysis of SiGe based stacked drain FDSOI MOSFET.

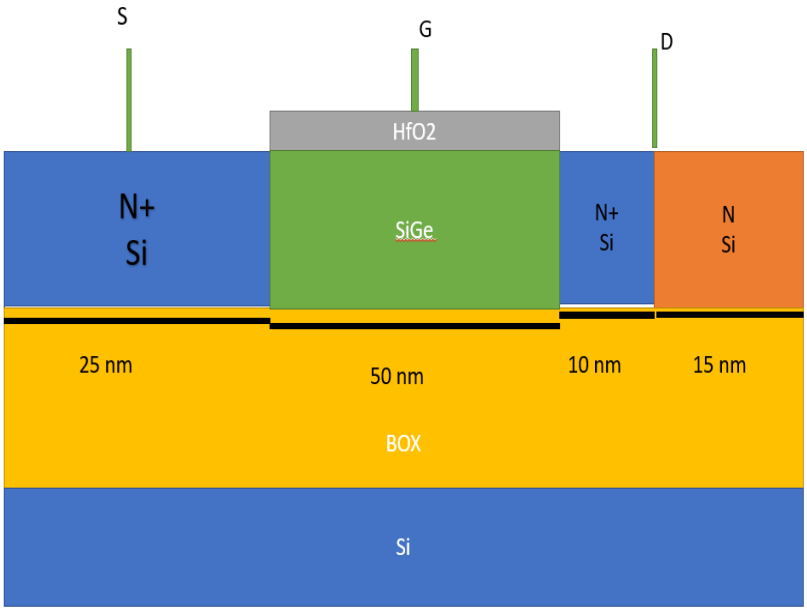

Figure 3.1 – Device Structure

Table 3.1 Device parameters and specifications for device under study

Region	Length (in nm)	Doping (in cm^{-3})
1. Source	25	10^{20}
2. Drain (N+)	10	10^{20}
3. Drain (N)	15	10^{18}
4. Channel	50	10^{16}
5. P- type Substrate	10	10^{16}

3.2 Simulation Platform

3.2.1 **Silvaco** - Silvaco is a prominent provider of software tools for the design and simulation of semiconductor devices, integrated circuits (ICs), and photovoltaic systems. Here are key points about Silvaco:

- **Overview** –
- ❖ Founded: 1984
- ❖ Headquarters: Santa Clara, California, USA
- ❖ Primary Focus: Electronic Design Automation (EDA) tools for semiconductor device simulation and IC design.
- **Key Software Tools** –

TCAD (Technology Computer-Aided Design)

- ❖ Purpose: Simulates the physical and chemical processes in semiconductor devices.
- ❖ Modules: Includes tools like Athena for process simulation and Atlas for device simulation**.**

EDA (Electronic Design Automation)

- ❖ Purpose: Aids in the design and analysis of integrated circuits.
- ❖ Products: SmartSpice for circuit simulation, Expert for layout design, and Gateway for schematic capture.

3.2.2 Models –

Table 3.2 – Carrier Statistics Models

Model	Syntax	Notes
Boltzmann	BOLTZMANN	Default model
Fermi-Dirac	FERMI	Reduced carrier concentrations in heavily doped regions.
Incomplete Ionization	INCOMPLETE	Accounts for dopant freeze-out. Typically, it is used at low temperatures.
Silicon Ionization Model	IONIZ	Accounts for full ionization for heavily doped Si. Use with INCOMPLETE.
Bandgap Narrowing	BGN	Important in heavily doped regions. Critical for bipolar gain.

Table 3.3 - Mobility Models

Model	Syntax	Notes
Concentration Dependent	CONMOB	Lookup table valid at 300K for Si and GaAs only. Uses simple power law temperature dependence.
Concentration and Temperature Dependent	ANALYTIC	Caughey-Thomas formula. Tuned for 77- 450K.
Carrier-Carrier Scattering	CCSMOB	Dorkel-Leturq Model. Includes n, N and T dependence. Important when carrier concentration is high (e.g., forward bias power devices).
Parallel Electric Field Dependence	FLDMOB	Si and GaAs models. Required to model any type of velocity saturation effect.
Watt Model	WATT	Transverse field model applied to surface nodes only.
Klaassen Model	KLA	Includes N, T, and n dependence. Applies separate mobility to majority and minority carriers. Recommended for bipolar devices
Lombardi (CVT) Model	CVT	Complete model including N, T, E//, and E_I effects. Good for non-planar devices.

3.3 Result and Discussion

Performance Metrics Evaluated:

- **Drive Current (I_{ON}):** The study examines the drive current capabilities, indicating how effectively the transistor can switch and drive loads.
- **Leakage Current (I_{OFF}):** Leakage current is analyzed to understand the off-state power consumption, which is critical for low-power applications.
- **Subthreshold Slope (SS):** This metric reflects how effectively the transistor can switch from off to on states, impacting switching speed and power consumption.

The performance of the SiGe stacked drain FDSOI MOSFET is analyzed through extensive simulations, often using tools like TCAD (Technology Computer-Aided Design) to model the device behavior under various conditions. These simulations help in understanding the impact of different material properties and device configurations on overall performance.

Fig. 3.3. shows the linear plot of I_d vs V_{gs} characteristics at V_{ds}=1V. The threshold voltage of the device is calculated as 0.31 V. Further, Fig. 3.3. shows the logarithmic plot of I_d vs V_{gs} characteristics at V_{ds}=1V. It is clear from the figure that the device offers very low off state current in order of 1nA. So, device performance is better at low dimensions and could be a suitable device for future low power circuit and systems.

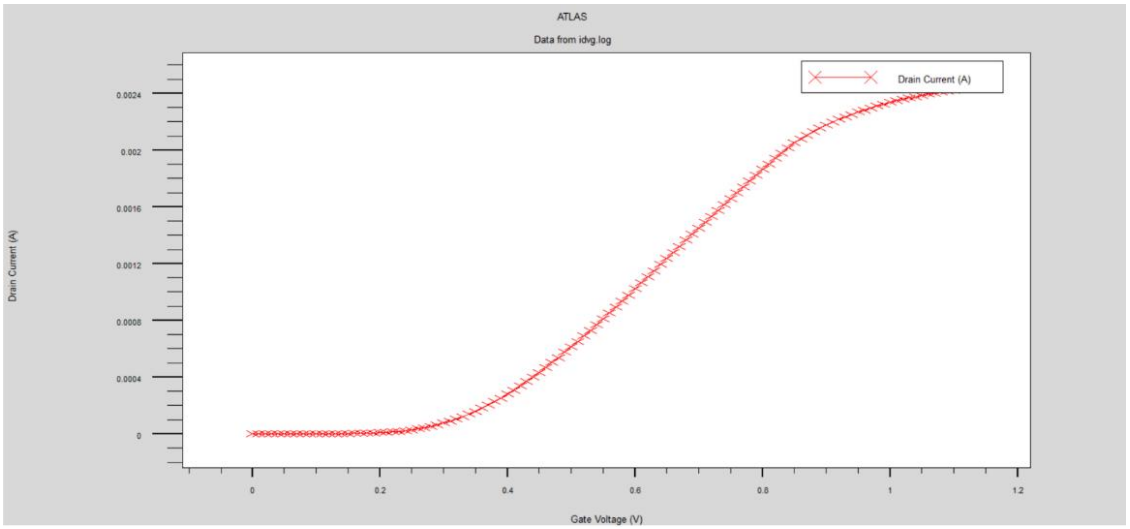

Figure 3.2 – I_d vs V_{gs} linear plot

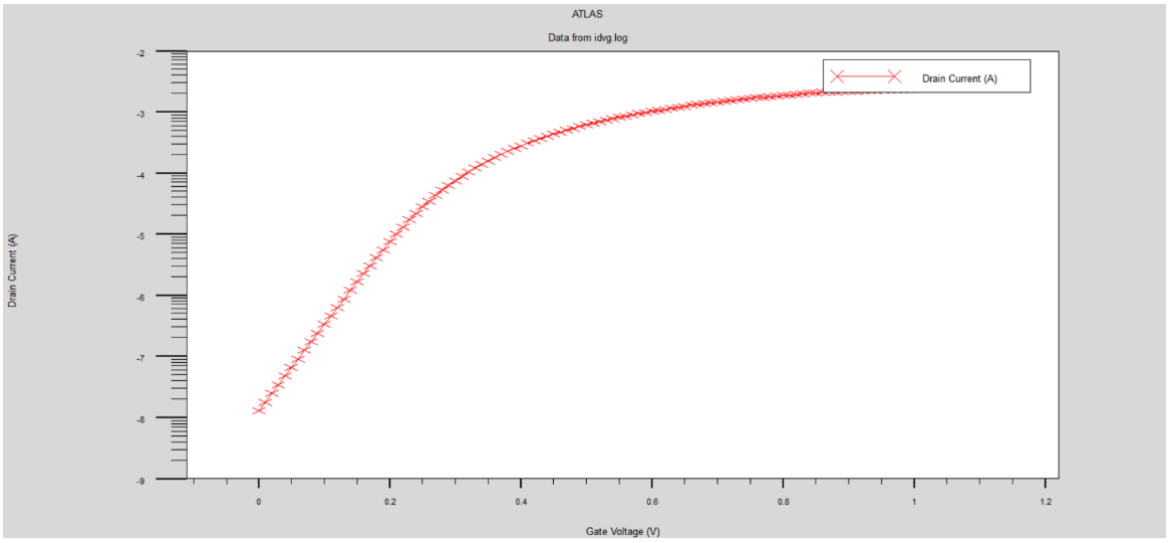

Figure 3.3 – I_d vs V_{gs} logarithmic plot

- **Potential curve of SiGe based stacked drain FDSOI MOSFET**

  Figure 3.4 shows the surface potential variation along the channel for the device under study. In proposed device, it has been found that the location of the minima surface potential is moved more along the source side of the channel.

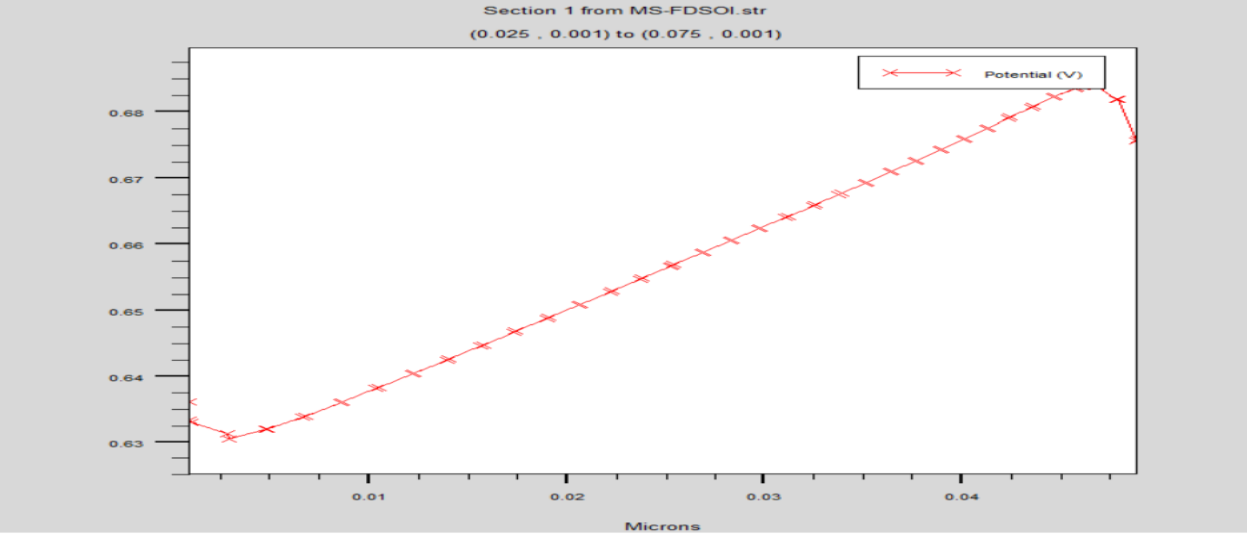

Figure 3.4 - Surface potential profile versus channel length of the studied MOSFETs (cutline at channel length starting from 25 nm to 75 nm)

- **Electric field curve of SiGe based stacked drain FDSOI MOSFET :**

  Figure 3.5 shows the surface potential variation along the channel for the device under study. In proposed device, in channel region electric field first increases. Further, it has seen that electric field decreases linearly. After that, electric field increases linearly for a small duration and after that again electric field decreases. Maximum peak of electric field is observed nearer to source.

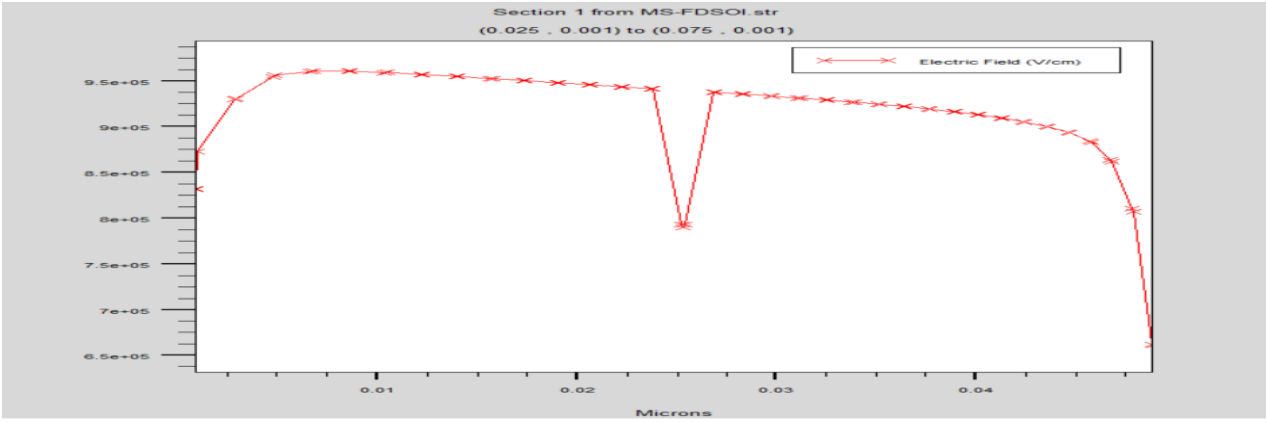

Figure 3.5 – Electric field profile versus channel length of the studied MOSFETs (cutline at channel length starting from 25 nm to 75 nm)

- **Total electron concentration curve of SiGe based stacked drain FDSOI MOSFET :**

  Figure 3.6 shows the total electron concentration variation along the channel for the device under study. Electron concentration near to source is maximum and after that it decreases slowly.

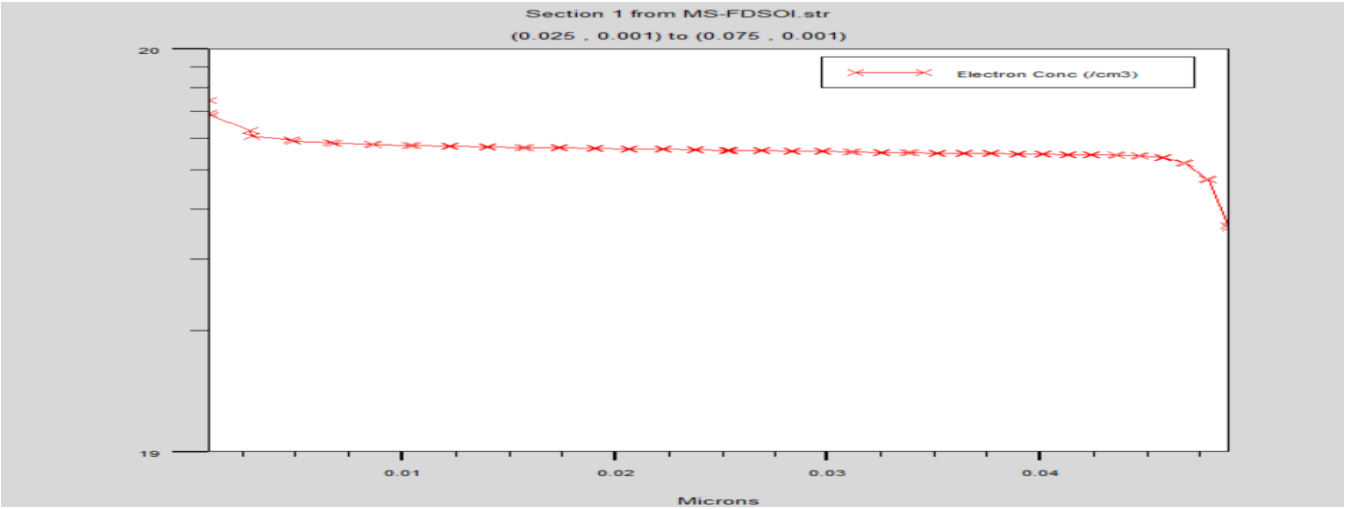

Figure 3.6– total electron concentration profile versus channel length of the studied MOSFETs (cutline at channel length starting from 25 nm to 75 nm)

3.4 Summary

Impact of SiGe and FDSOI Technology:

- ❖ SiGe offers enhanced carrier mobility compared to pure silicon, which can improve device performance.
- ❖ FDSOI technology provides better electrostatic control, reduced short-channel effects, and improved scalability, making it suitable for advanced node transistors.

Impact of Stacked Drain Configuration:

The stacked drain structure is employed to further optimize the device performance. This involves vertically stacking the drain regions to enhance current handling capabilities and improve overall device robustness.

CHAPTER 4
CONCLUSION & FUTURE WORK

4.1 Conclusion:

A comprehensive performance analysis of Silicon-Germanium (SiGe) based stacked drain Fully Depleted Silicon on Insulator (FDSOI) MOSFETs has been taken under study. The conclusions are as follows.

- **Enhanced Performance:** SiGe-based FDSOI MOSFETs demonstrate superior electrical performance compared to their traditional silicon counterparts. The incorporation of SiGe in the channel region effectively enhances carrier mobility due to the reduced effective mass of holes and electrons, leading to improved drive current and transconductance.
- **Improved Short-Channel Effects:** The stacked drain configuration in SiGe FDSOI MOSFETs significantly mitigates short-channel effects (SCEs). This is attributed to the enhanced electrostatic control provided by the fully depleted body and the buried oxide (BOX) layer, which reduces leakage currents and drain-induced barrier lowering (DIBL).
- **Reduced Power Consumption:** The improved subthreshold slope and reduced off-state leakage current contribute to lower power consumption, making SiGe-based FDSOI MOSFETs suitable for low-power applications, particularly in portable and battery-operated devices.
- **Scalability:** The SiGe FDSOI technology shows promise for scalability to smaller technology nodes. The ability to maintain performance and control over SCEs at reduced dimensions positions SiGe FDSOI MOSFETs as a viable option for future semiconductor technologies.
- **Thermal Stability:** SiGe-based devices exhibit better thermal stability, which is crucial for high-performance and high-temperature applications. The improved thermal conductivity of SiGe helps in efficient heat dissipation, thereby maintaining device reliability and performance over extended periods.

4.2 Future Work

To further advance the understanding and application of SiGe-based stacked drain FDSOI MOSFETs, several areas of future work are proposed:

- **Advanced Simulation and Modeling:** Developing more sophisticated simulation models that incorporate quantum mechanical effects and detailed material properties of SiGe can provide deeper insights into device behavior at nanoscale dimensions. These models can help optimize device design and predict performance more accurately.

- **Experimental Validation:** Fabrication and experimental characterization of SiGe-based FDSOI MOSFETs under various operating conditions are necessary to validate the theoretical and simulation results. This includes assessing the impact of process variations and real-world operating conditions on device performance.
- **Exploration of Alternative Materials:** Investigating other semiconductor materials and alloy compositions in conjunction with SiGe, such as III-V group materials or GeSn, could potentially enhance device performance further. These materials might offer even higher carrier mobilities and better thermal properties.
- **Integration with Advanced Architectures:** Studying the integration of SiGe FDSOI MOSFETs with advanced device architectures like FinFETs, Gate-All-Around (GAA) FETs, or nanosheet FETs could provide pathways to further improve performance and scalability.
- **Reliability and Aging Studies:** Long-term reliability studies, including the effects of aging, radiation hardness, and extreme environmental conditions, are essential to ensure the robustness of SiGe-based FDSOI MOSFETs for various applications, including aerospace and defense.
- **Application-Specific Optimization:** Tailoring the design and optimization of SiGe FDSOI MOSFETs for specific applications such as high-speed communication, high-performance computing, and low-power Internet of Things (IoT) devices could maximize their impact and commercial viability.

References

1. K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," in *IEEE Transactions on Electron Devices*, vol. 36, no. 2, pp. 399-402, Feb. 1989.
2. K. Suzuki, Y. Tosaka, T. Tanaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFETs," IEEE Trans. Electron Devices, vol. 40, pp. 2326–2329, 1993.
3. K. Suzuki and T. Sugii, "Analytical models for n-p double-gate SOI MOSFETs," IEEE Trans. Electron Devices, vol. 42, pp. 1940–1948, 1995.
4. K. Suzuki and S. Pidin, "Short-channel single-gate SOI MOSFET model," in *IEEE Transactions on Electron Devices*, vol. 50, no. 5, pp. 1297-1305, May 2003
5. M. J. Kumar and A. Chaudhry, "Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs," in *IEEE Transactions on Electron Devices*, vol. 51, no. 4, pp. 569-574, April 2004
6. P.E Allen, R. Dobkin, and D.R. Holberg , 2011. *CMOS analog circuit design*. Elsevier.
7. R. Rao, G. Katti, D. S. Havaldar, N. Dasgupta, and A. Dasgupta, "Unified analytical threshold voltage model for non-uniformly doped dual metal gate fully depleted silicon-on-insulator MOSFETs," Solid State Electron., vol. 53, no. 3, pp. 256–265, Mar. 2009
8. G. K. Saramekala, A. Santra, S. Dubey, S. Jit, and P. K. Tiwari, "An analytical threshold voltage model for a short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET," Superlattices and Microstructures, vol. 60, pp. 580-595, 2013.
9. N. A. Srivastava, V. K. Mishra and R. K. Chauhan, "Analytical Modelling of Surface Potential of Modified Source FD-SOI MOSFET," IEEE Inter. Conference on Emerging Trends in Communication Technologies (ETCT), Nov. 2016.
10. A. Priya and R. A. Mishra, "A two dimensional analytical modeling of surface potential in triple metal gate (TMG) fully-depleted Recessed-Source/Drain (Re-S/D) SOI MOSFET," Superlattices and Microstructures, vol. 92, pp. 316-329, 2016
11. V. K. Mishra and R. K. Chauhan, "Performance analysis of modified source and TDBC based fully-depleted SOI MOSFET for low power digital applications," Journal of Nano Optoelectronics, vol. 12, no. 1, pp. 59–66, 2017.
12. N.A. Srivastava, A. Priya, and R.A. Mishra, 2019, November. Performance evaluation of hetero-gate-dielectric Re-S/D SOI MOSFET for low power applications. In *2019 International Conference on*

Electrical, Electronics and Computer Engineering (UPCON) (pp. 1-6). IEEE.

13. S. Rewari, V. Nath, S. Haldar, S. S. Deswal and R. S. Gupta, "Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate All Around MOSFET," in *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 3-10, Jan. 20

14. N.A. Srivastava, , A. Priya and R.A. Mishra, 2021. Interface trap charge-based reliability assessment of high-k dielectric-modulated nanoscale FD SOI MOSFET for low power digital ICs: Modeling and simulation. *Superlattices and Microstructures*, *154*, p.106871.
15. G. Gildenblat, H. Wang, T. L .Chen, X. Gu , and X. Cai, "SP: An advanced surface-potential-based compact MOSFET model," IEEE J. Solid State Circuits,vol.39,no.9,pp.1394–1406,Sep.2004.
16. K .Joardar, K . K. Gullapalli, C. McAndrew, M. E. Burnham ,and A. Wild, "An improved MOSFET model for circuit simulation," IEEE Trans. ElectronDevices,vol.45,no.1,pp.134–148,Jan.1998.
17. J .He, M. Chan, X. Zhang ,and Y. Wang, "A physics-based analytic solution to the MOSFET surface potential from Accumulation to strong-inversion region," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2008–2016, Sep.2006.
18. S. R. Banna, P. C. H. Chan, P. K. Ko, C. T. Nguyen, and M. Chan, "Threshold voltage model for deep-submicrometer fully depleted SOI MOSFETs," IEEE Trans. Electron Devices, vol. 42, pp. 1949–1955, 1995.
19. S. Pidin and M. Koyanagi, "Two-dimensional analytical subthreshold model and optimal scaling of fully-depleted SOI MOSFET down to 0.1 μm channel length," in Solid State Devices Mat. Tech. Dig., 1996, pp. 309–310.
20. ATLAS User Manual, Device simulation software, Silvaco International, Santa Clara 2016