Dear Kishan,

Just for your knowledge purpose. Please go through this mail in your free time.

The background of the work is related to LINT errors in the report, which in turn can be called as

"Design Rules Check"  (DRC) for RTL designers.

Every Front end design engineer (ASIC/FPGA Design engineer) should follow some set of rules to avoid

any possible failures during simulation and synthesis.

Hence the LINT stage will act as first step to clean up the RTL before proceeding to the next stages of

ASIC or FPGA design flow.

Many of the DRC rules are standard rules as per the industry standard (Defined in the Rule set of Tool Vendor).

Few rules are appended or removed based on the company's prior experience and requirements.

While we execute the DRC rules, we may encounter errors, which are classified into many categories.

Some of the errors are mandatory and some are known errors.

When we look at the report (Tool generated report),  we may need to fix the error in RTL and re-run again.

Or if the error is intentional or known error, it is important to give valid reason and waive off the error.

Exact rule set from the Atrenta  Spyglass (Tool) cannot be shared with you. Hence I am providing the other source of information.

Just for your Knowledge, please go through the following links and attached document:

<http://webdocs.cs.ualberta.ca/~amaral/courses/329/labs/VHDL_Guideline.html>

<http://www.sigasi.com/vhdl-lint>

<http://www.alteraforum.com/forum/showthread.php?t=39073>

<http://www.techdesignforums.com/practice/topics/eda-topics/?type=guide>

As and when I find any information on the general rules, I shall share with you.

And also please do get back to me in case of any information required in this regard.

Thanks and Regards,

Praveen TV