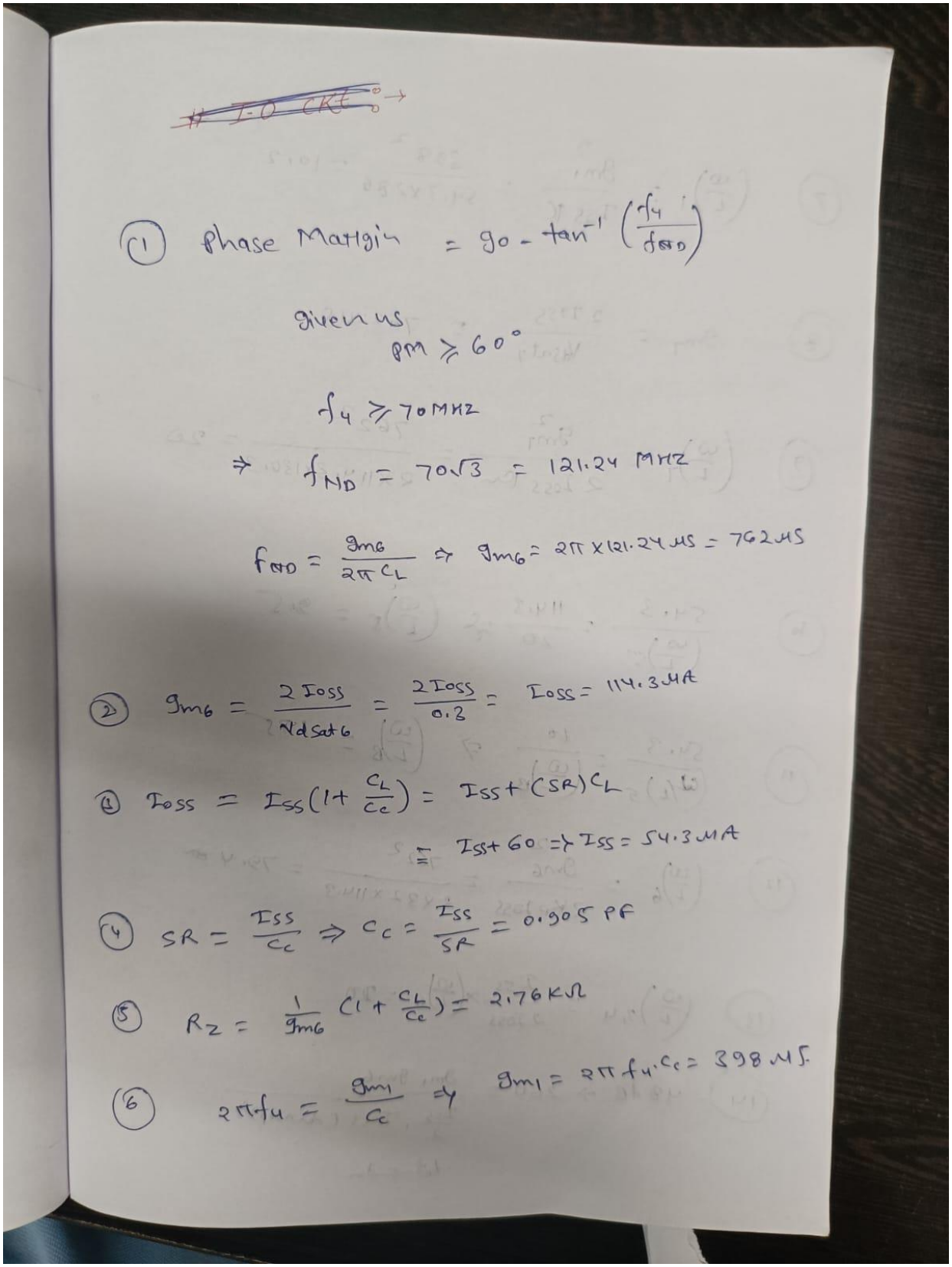
Design Parameters

Design the schematic of a Low Power 2-stage Operational Transconductance Amplifier (OTA) with RC compensation in GPDK 45nm technology (differential input, single ended output) to meet the following specifications:

- DC gain ≥ 48 dB
- Unity gain frequency ≥ 70 MHz
- Output voltage swing ≥ 0.6 Vpk-pk
- Slew rate ≥ 60 V/µs
- Phase Margin ≥ 60°
- Input referred spot noise (at 10 MHz) ≤ 80 nV/√Hz
- Input referred spot noise (at 0.1 MHz) ≤ 90 nV/√Hz
- Input Common mode voltage = 0.6 V
- Output load capacitance = 1 pF (From analogLib)
- VDD = 1.2 V
- Power consumption ≤ 0.25 mW

2 Hand calculations



(7) $\left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{I_{SS}\,KC} = \frac{398^2}{54.3 \times 286} = 10.2$

(8) $g_{m7} = \frac{2 I_{DSS}}{V_{dsat7}} = 762\,\mu S$

(9) $\left(\frac{W}{L}\right)_7 = \frac{g_{m7}^2}{2\, I_{DSS}\, K_n} = \frac{762^2}{2 \times 114.3 \times 130.3} = 20$

(10) $\frac{54.3}{\left(\frac{W}{L}\right)_5} = \frac{114.3}{20} \Rightarrow \left(\frac{W}{L}\right)_5 = 9.5$

(11) $\frac{54.3}{\left(\frac{W}{L}\right)_5} = \frac{10}{\left(\frac{W}{L}\right)_B} \Rightarrow \left(\frac{W}{L}\right)_B = 1.75$

(12) $\left(\frac{W}{L}\right)_6 = \frac{g_{m6}^2}{2 K_p I_{DSS}} = \frac{762^2}{2 \times 32 \times 114.3} = 79.4$

(13) $\left(\frac{W}{L}\right)_{3,4} = \frac{I_{SS}}{2 I_{DSS}} \times \left(\frac{W}{L}\right)_6 = 20$

(14) $48\,dB \rightarrow 260 = \frac{g_{m1}\, g_{m6}}{\frac{I_{SS}}{2} \cdot I_{DSS} (\lambda_n + \lambda_p)^2}$

~~$L_d = L_n$~~

if $\lambda_n = \lambda_p = \lambda$

$$\Rightarrow \lambda^2 = \frac{298 \times 762}{54.3 \times 114.3 \times 2 \times 260}$$

$$\Rightarrow \lambda = 0.307$$

So $\quad$ Nut $\rightarrow$ $0.585 \times 45 = 0.307 \times L_n \Rightarrow L_n = 90\text{mm}$

$0.41 \times 45 = 0.307 \times L_p \Rightarrow L_p = 60\text{mm}$

nat $\rightarrow$ $0.694 \times 300 = 0.307 \times L_{nat} \Rightarrow L_{nat} = 680\text{mm}$

3 DC Operating point

3.1 Testbench

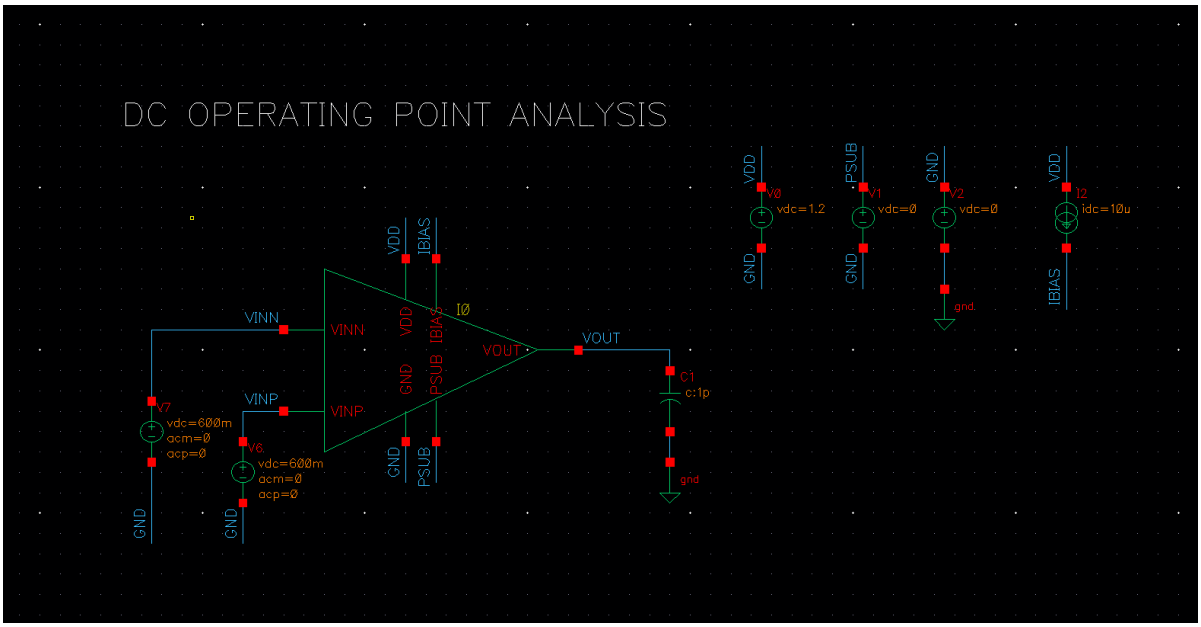


Figure 1: DC Testbench

3.2 Schematic with operating points

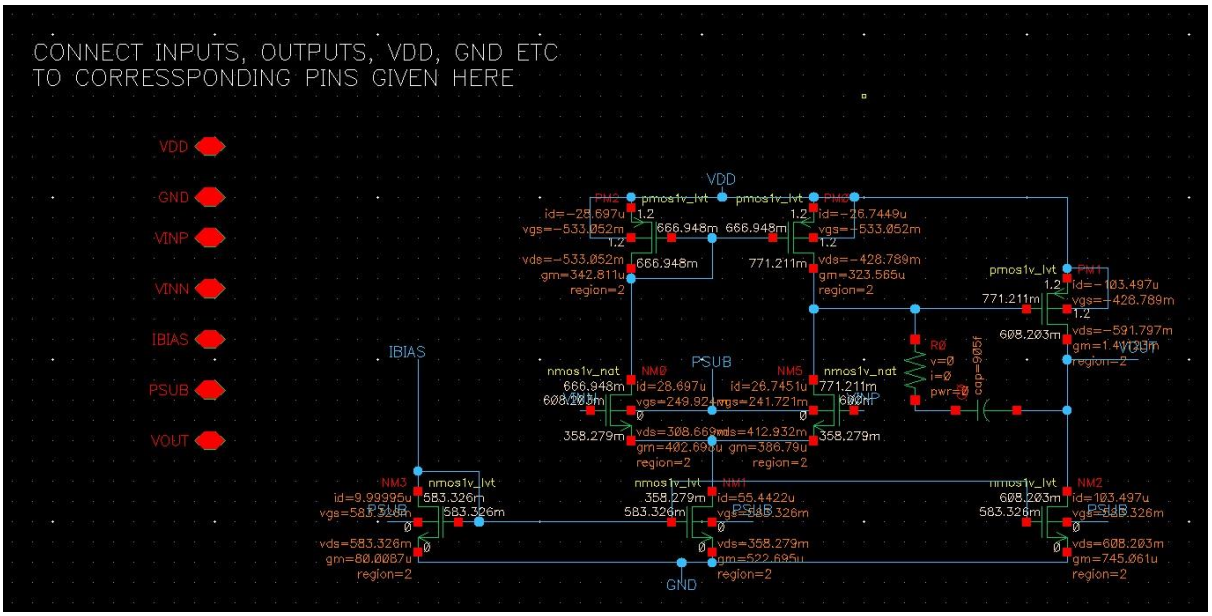


Figure 2: Schematic with DC operating points

4 Stability Analysis

4.1 Testbench

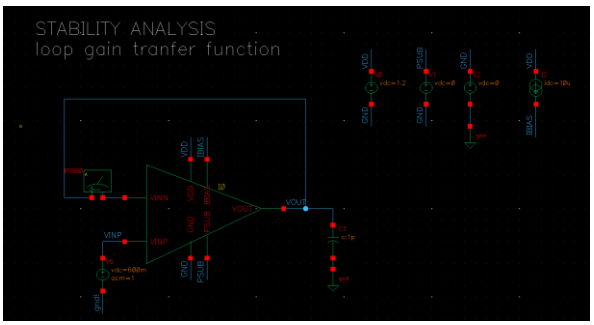


Figure 3: Stability Analysis Testbench

4.2 Stability plots

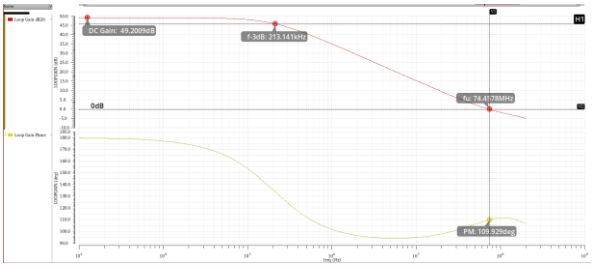


Figure 4: Stability plots

4.3 Stability Summary

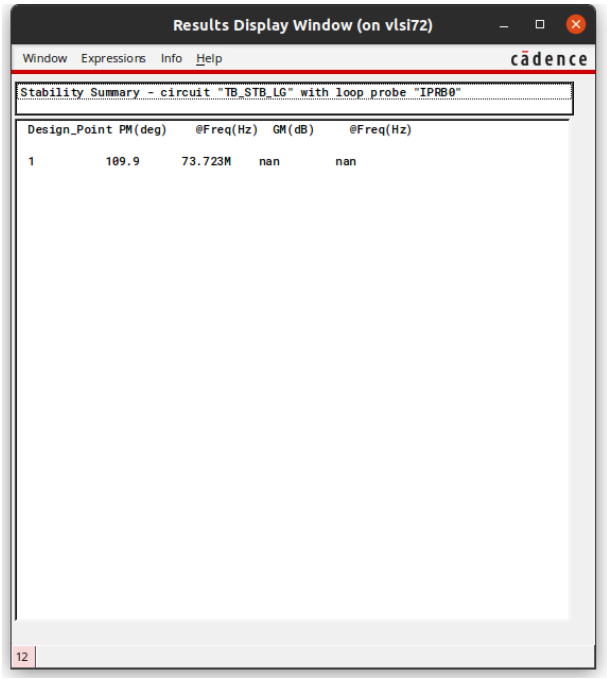


Figure 5: Stability Summary

5 AC analysis: Differential Gain

5.1 Testbench

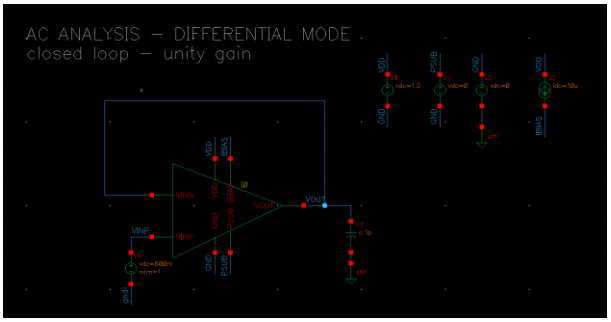


Figure 6: Differential Mode Testbench

5.2 Gain and Phase Plots

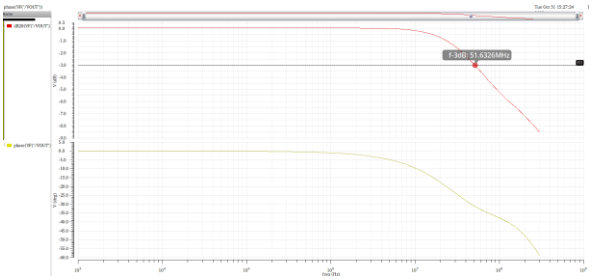


Figure 7: Closed loop gain and phase

5.3 Input Referred Offset

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_23M1222:TB_AC_DM:1	dB20(VF("/VOUT"))				
EE618_CP1_23M1222:TB_AC_DM:1	phase(VF("/VOUT"))				
EE618_CP1_23M1222:TB_AC_DM:1	Input reffered offset	-8.203m			

Figure 8: Input referred offset

5.4 DC operating points

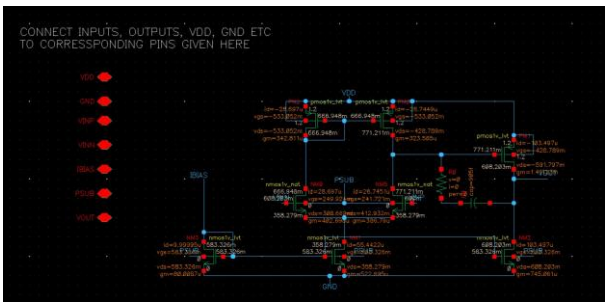


Figure 9: Schematic with DC operating points

6 AC analysis: Common mode gain

6.1 Testbench

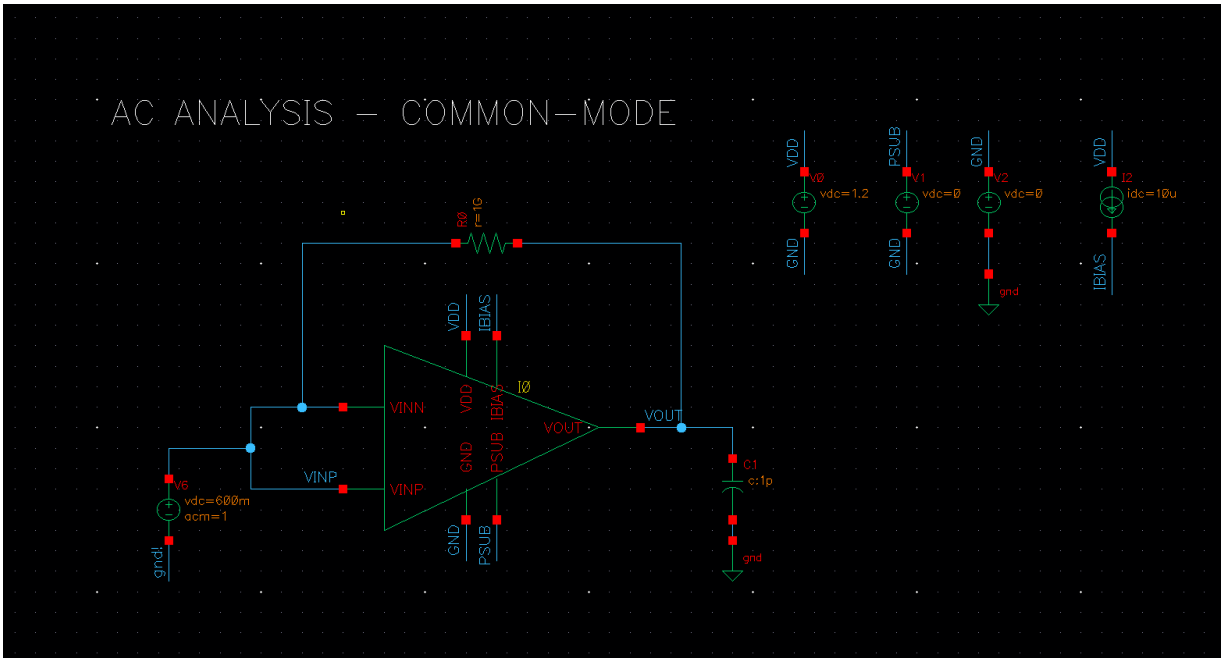


Figure 10: Common Mode Testbench

6.2 Common Mode Gain

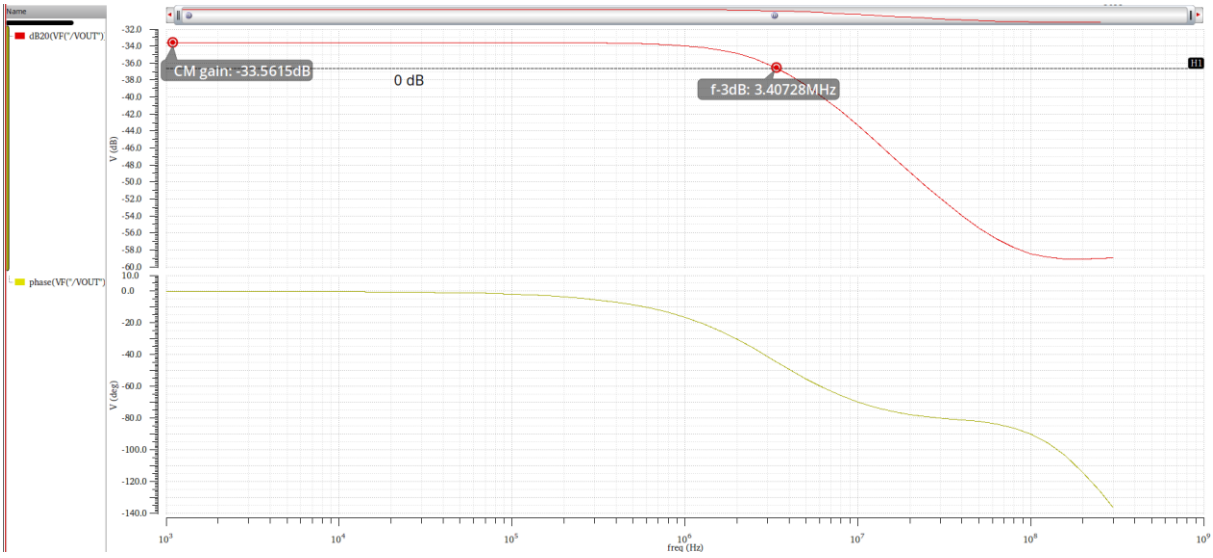


Figure 11: Common mode gain

7 Transient analysis: Sinusoidal input

7.1 Testbench

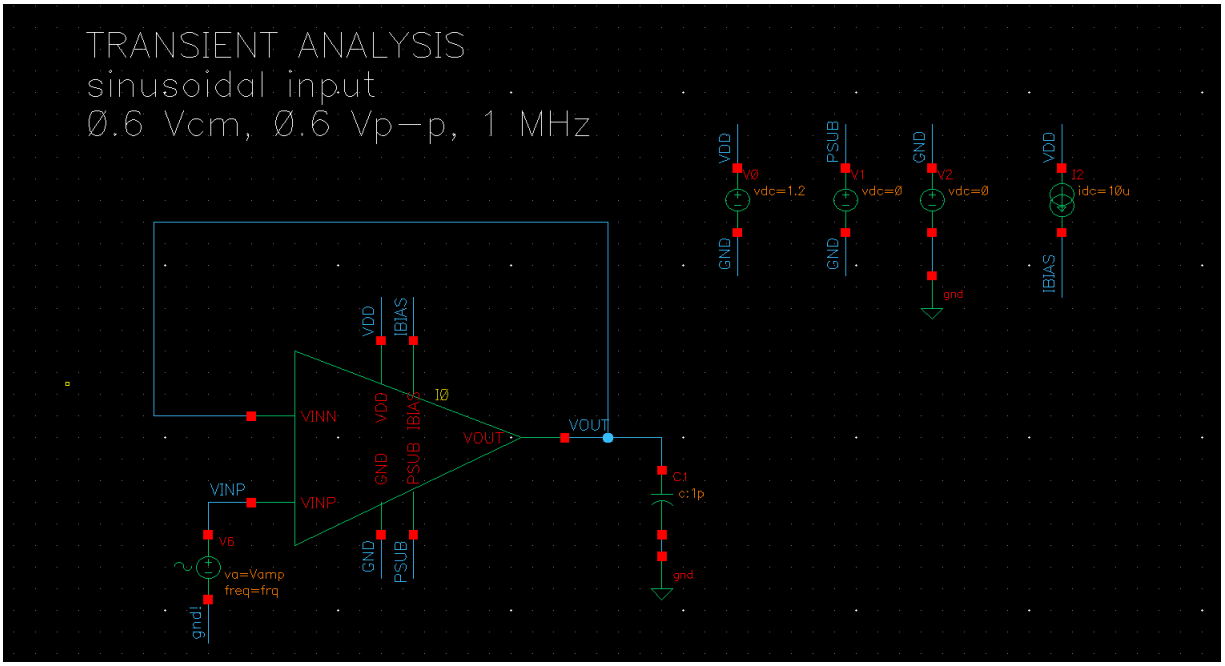


Figure 12: Testbench for voltage swing analysis

7.2 Voltage Swing

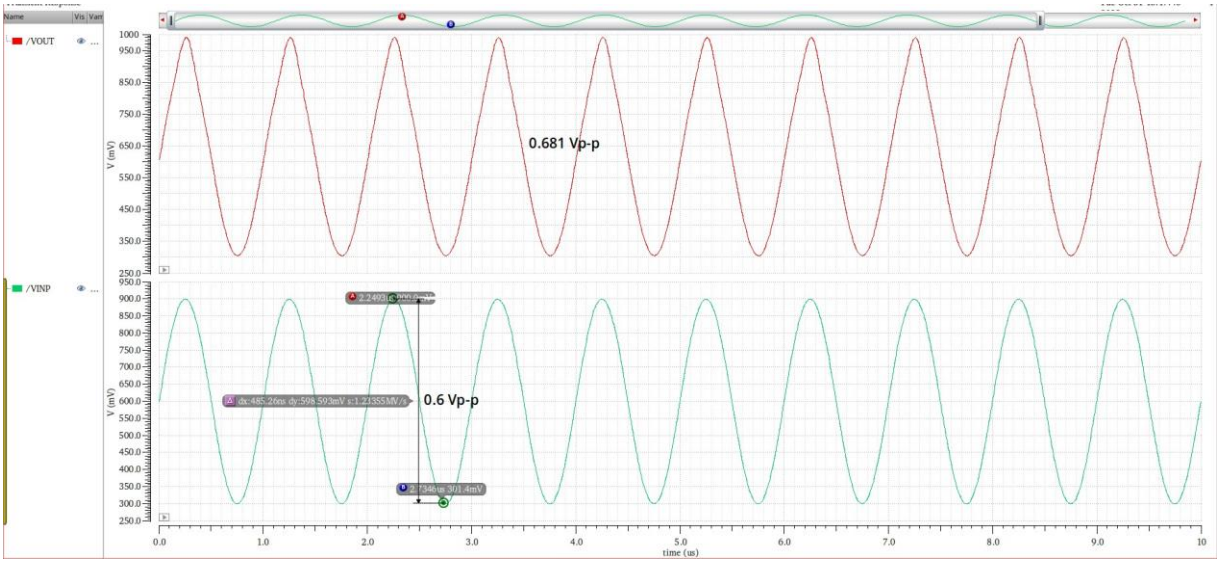


Figure 13: Voltage Swing

8 Transient analysis: Step input

8.1 Testbench

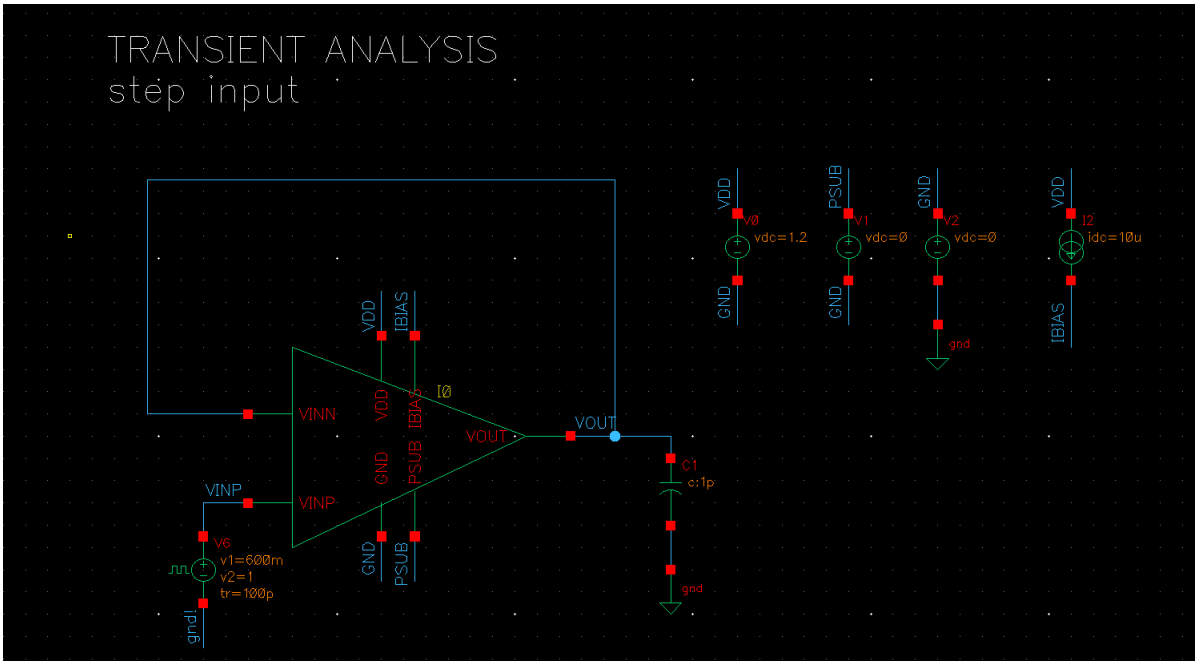


Figure 14: Testbench for slew rate analysis

8.2 Slew Rate

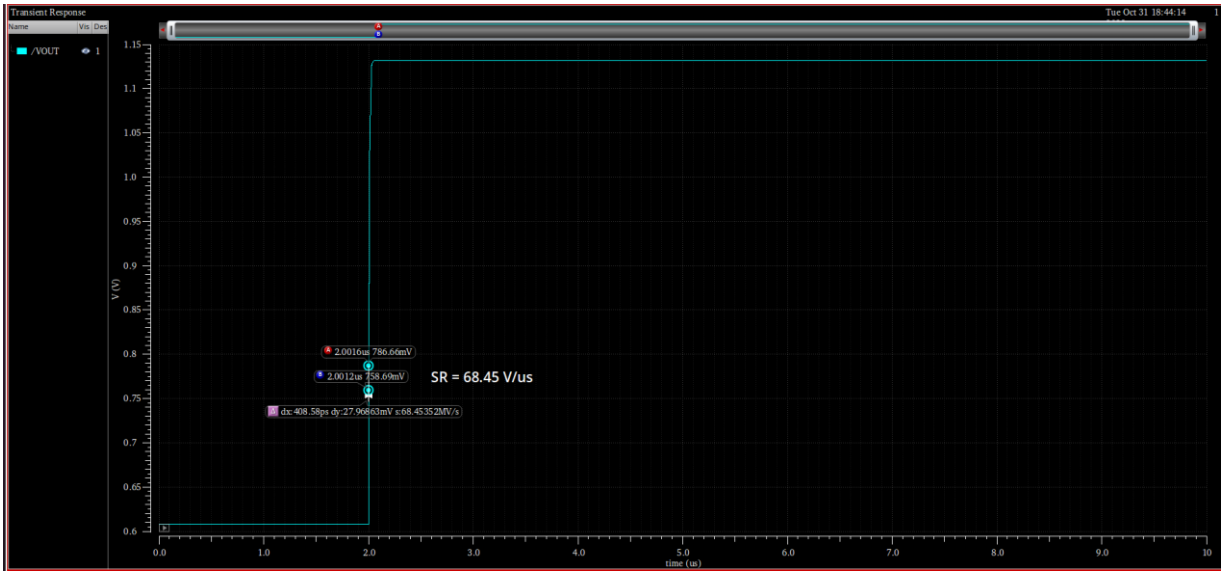


Figure 15: Slew rate

9 Noise analysis

9.1 Testbench

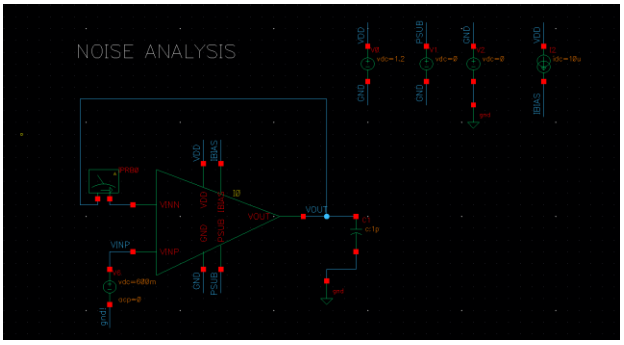


Figure 16: Testbench for noise analysis

9.2 Input Referred Noise

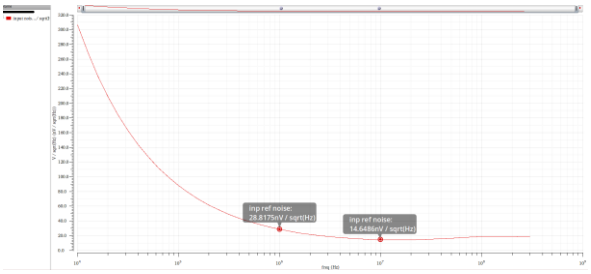


Figure 17: Input referred noise

9.3 Noise Summary

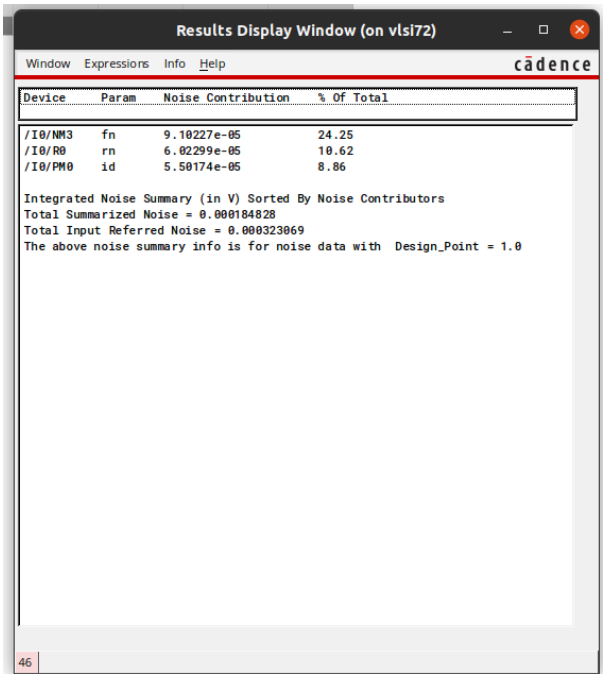


Figure 18: Noise summary

10 Summary of Results obtained

Tabulate all the OTA Specifications achieved by your design from Q2 to Q8 in typical corner as shown below: [Typical corner: TT, 27^0C]

Q.No	Parameters	Value (Unit)
2	Power Consumption	0.19 mW
3	DC gain	49.20 dB
	f-3dB	213.141 kHz
	Unity Gain frequency	74.458 kHz
	Phase margin	109.93°
4	Closed Loop Gain	1
	f-3dB	51.63 MHz
	Input referred offset (DC analysis)	-8.203 mV
5	Common-mode gain	0.02
	CMRR	25
6	Output Swing (Vpk−pk)	0.681Vp-p
7	Slew rate	68.45 V/us
	Settling Time (1% accuracy)	11.7 ns
8	Input referred spot noise (at 1 MHz)	28.8175 nV/√Hz
	Input referred spot noise (at 10 MHz)	14.65 nV/√Hz
	Total summarized Noise	0.000185
	Total input referred Noise	0.000323

Figure 19: Results Summary