DESIGN OF DIFFERENTIAL INPUT SINGLE ENDED OUTPUT SINGLE STAGE AMPLIFER

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DESIGN SPECIFICATIONS

To design a differential-input single-ended output Single-Stage amplifier, using CMOS 0.13um technology. The amplifier is powered from a 1.6V power supply. The amplifier to have one current source with a capacitive load as 4pF.

Design Parameter	Specification Value
Differential Voltage Gain, A_{vd}	≥ 75 dB
Output Voltage Swing Range, OVSR	≥ 1 V
Average Slew Rate, SR	≥ 10 V/μs
Common Mode Rejection Ratio, CMRR	≥ 80 dB
Unity Gain Bandwidth, GBW	≥ 8 MHz
Phase Margin, PM	≥ 60°
Power Dissipation, P_{diss}	≤ 0.5 mW

Design Considerations and Approach

1. The operational amplifier was designed using Folded-Cascode Topology due to its capability to output a higher impedance, therefore a higher dc gain. The process technology is CMOS 0.13um which has Lmin of 400nm.
2. While designing the transistors, larger transistor lengths (approximately 4 times Lmin = 1.6um) were considered so that the device will not be impacted by channel width modulation (λ). It is evident that the value of λ decreases for increasing value of channel length modulation parameter. The relationship is given by: $\lambda \propto 1/L$.
3. Given the value of VGS and VTH, each of the transistors (NMOS and PMOS) was put into saturation region by formulating VDS value greater than or equal to the overdrive voltage. Overdrive voltage is the difference between VGS and VTH. The below conditions were satisfied for each of the transistors. For NMOS:VDS ≥ VGS – VTH and For PMOS: VSD ≥ VSG – |VTH|

4. Upon fixing the W/L ratio to achieve the specified Differential Gain, Phase Margin and Unity Gain Bandwidth, the ratio was further fine-tuned to meet the other design specifications. Especially for power consumption, the ratio was chosen so that the current flowing through each branch is reduced.
5. The maximum rate at which the output of an Operational Amplifier can change is limited by the finite Bias Current. Due to the additional effect of parasitic capacitances, the W/L ratio of tail transistor was designed so that the bias current has additional leverage to obtain the required average slew rate. Average Slew Rate was calculated by taking the average between positive and negative slew rate. Average Slew Rate $\propto$ Bias Current/Load Capacitance.
6. Lastly in the final design, the ideal current source of 25uA was replaced by self-biased current source. The current from startup circuit design is 25.12uA. The resistance value was hand calculated to match the desired current rating.

Mathematical Gain Calculation

The gain of folded cascode amplifier (single-stage amplifier) is given by $G_m \times R_{out}$

$G_m = \frac{2i}{V_{in}}$ and $G_{m\ of\ 2,3} = = \frac{i}{\frac{V_{in}}{2}}$. Therefore, $G_m = G_{m\ of\ 2,3} = 362.2\mu A/V$

$Rout \approx g_{m7}.r_{o7}.r_{o5} \parallel g_{m9}.r_{o9}.r_{o11} = 43.84M\Omega$

Here, $g_{m7} = 219.4\mu A/V$ and $g_{m9} = 340.6\mu A/V$ and r_o values found from IV characteristics slopes respectively.

Mathematical Voltage Ratio Gain $\frac{V_{out}}{V_{in}} = 362.2\mu \times 43.84M$

$$\approx 15864.36\ V/V$$

The Amplification Factor expressed in decibels is given by $20 \times \log \left[\frac{V_{out}}{V_{in}}\right]$|

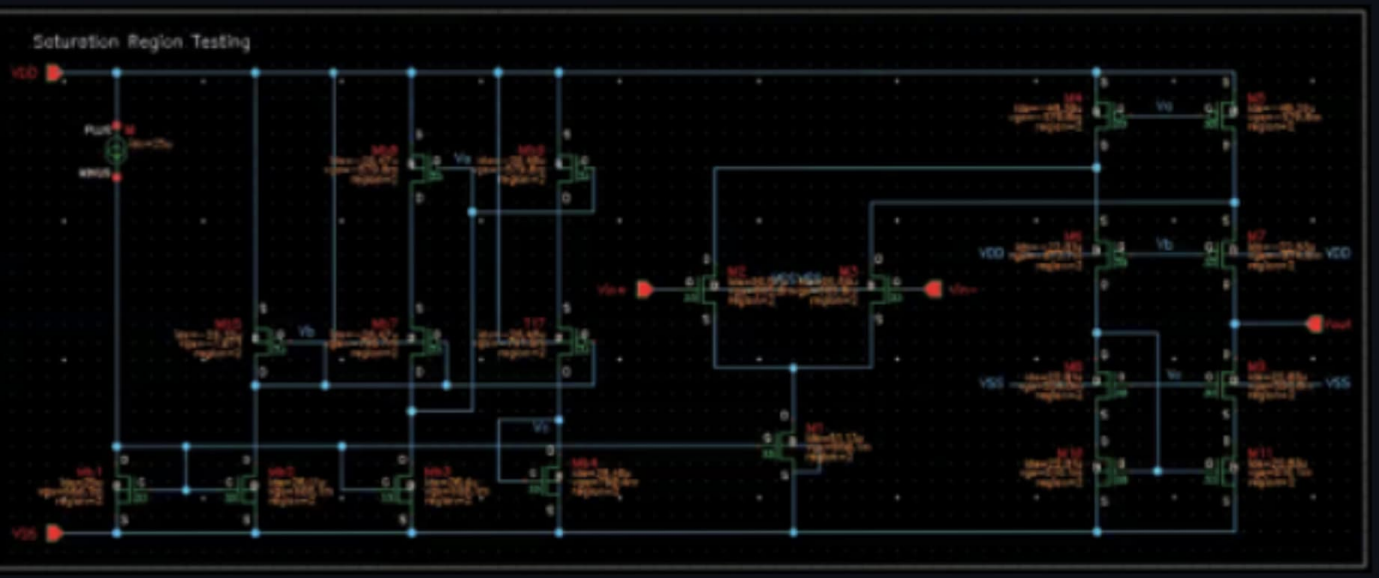
Mathematical Voltage Gain in dB $= 20 \times \log [15864.36]$

$$= 20 \times 4.2004$$

$$\approx 84.008\ dB$$

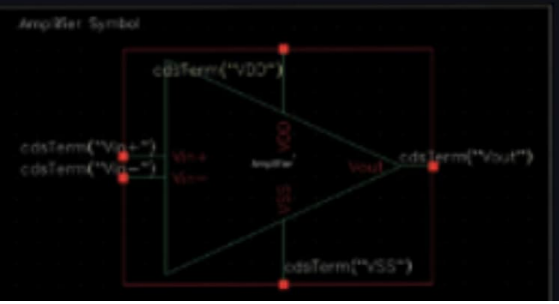
The W/L Ratio of the transistors were tuned to approximately match the mathematical voltage ga

DESIGN LAYOUT



> *Firstly, DC analysis was performed to check if all the transistors were put into saturation region. This is essential to have a constant drain current, controlled by the gate-source voltage. The MOS device is useful only if operated in the saturation region.*

Symbol

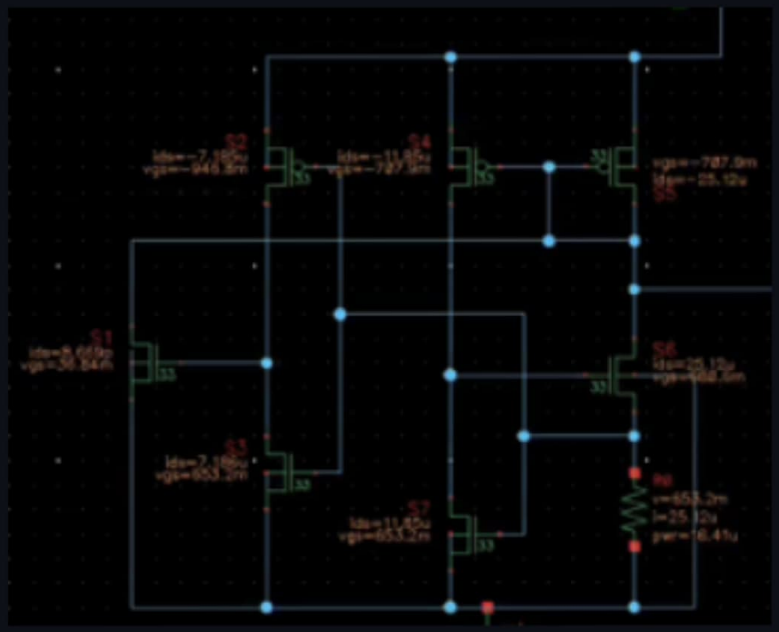


SELF BIASED CURRENT SOURCE CIRCUIT

An ideal current source is an independent current source that has high degree of precision and stability, independent of power supply and temperature variations. For greatly reducing the power supply sensitivity, self-biasing technique is used. Startup circuit is always needed in self-biasing to avoid zero current state. Also, the start-up circuit doesn't interfere with the normal operation of the reference once the desired operating point is reached.

After designing the amplifier to meet the desired specifications, in the final design, an attempt to design a self-biased current source was made. The ideal current source (25uA) was replaced with self-biased current source circuit directly on the circuit schematic without creating extra symbol/pin. The current from the startup circuit design was found to be 25.12uA.

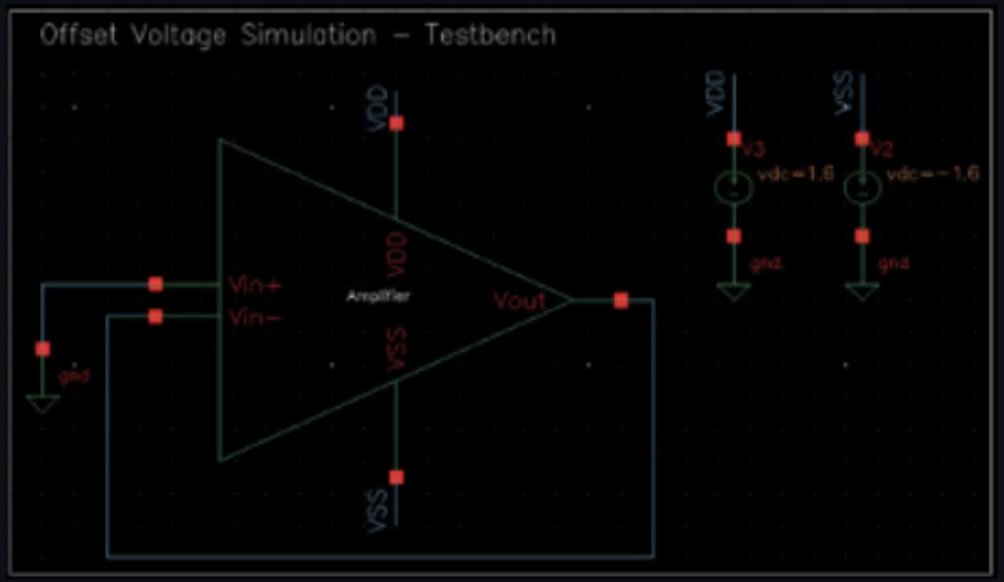
Schematic Layout



SIMULATIONS

Offset Voltage

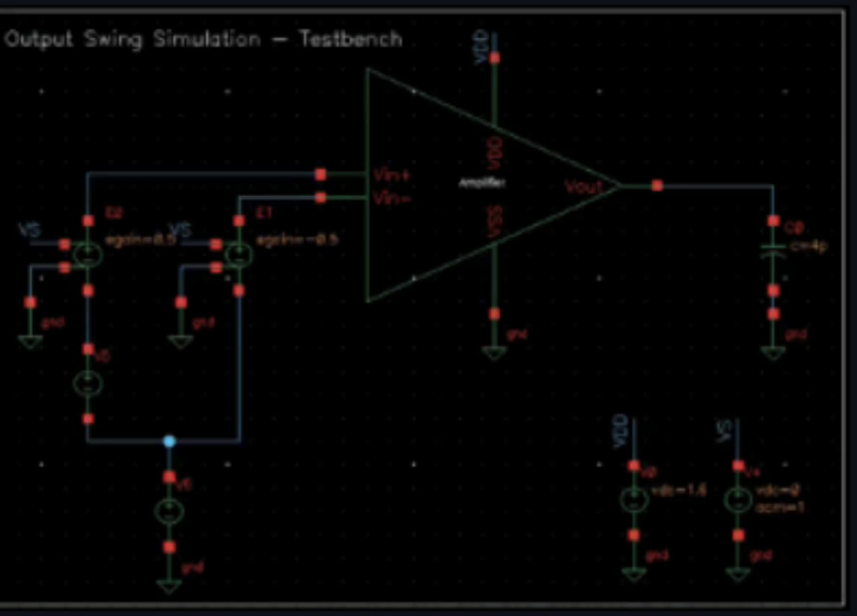
When real amplifiers are connected in unity gain configuration (output voltage is negative input voltage), there will be a voltage difference between the positive and negative inputs called the offset voltage of the amplifier. This Voff was obtained by performing DC analysis and annotating the node voltages.



Result: OFFSET VOLTAGE = 9.235mV

Output Voltage Swing

Output voltage swing is the range of output voltages that allow linear operation of output signals. The output swing was simulated using two voltage-controlled voltage sources (VCVS) with voltage gain 0.5 and -0.5 respectively. A linear sweep on VS dc voltage from -100mV to 100mV was performed in the DC Analysis.

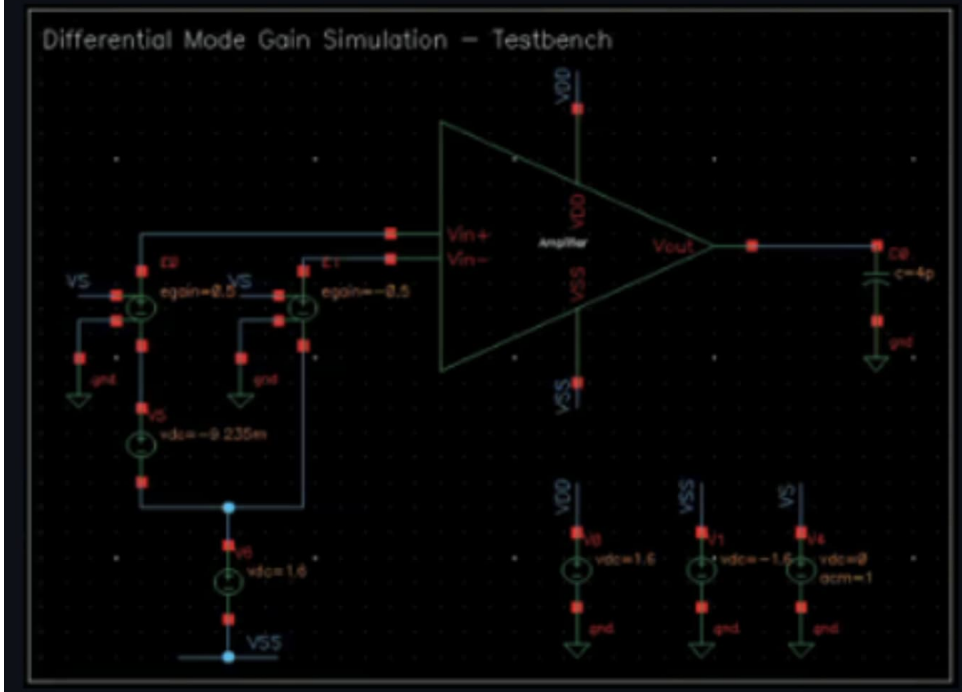


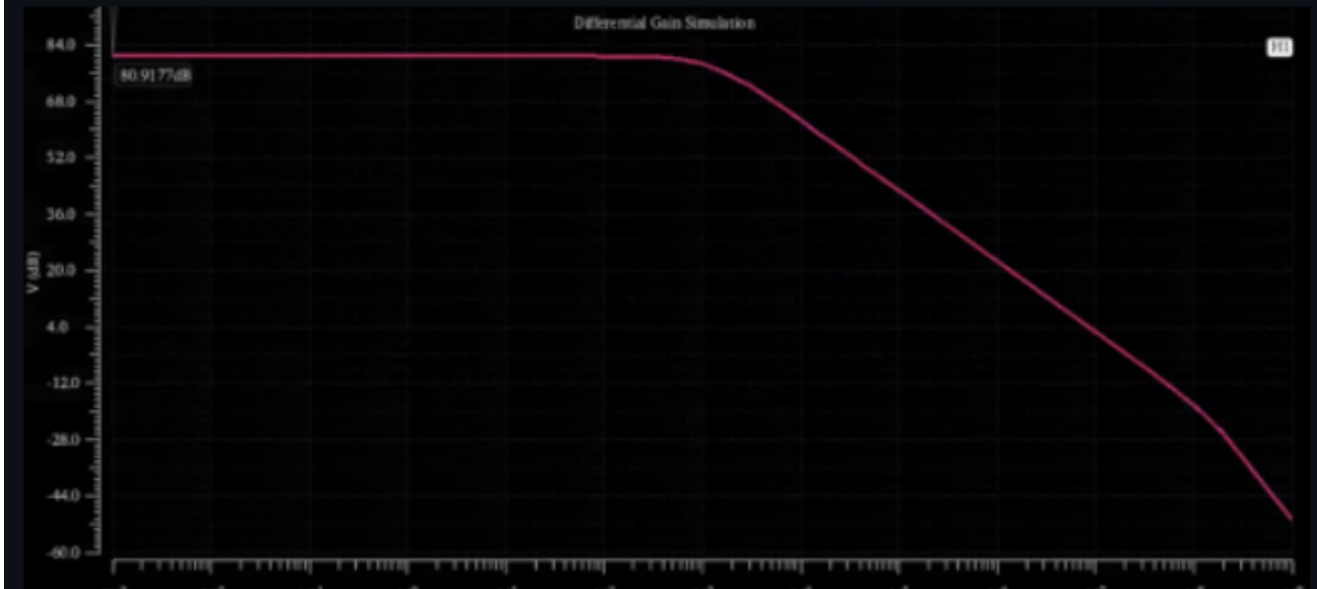
The waveform shows a finite DC range (output swing) that the amplifier has a high output resistance for high differential gain. OVSR = VO(max) – VO(min) = 1.32V – 220mV = 1.1 V

Result: OUTPUT VOLTAGE SWING RANGE (OVSR) = 1.1V

Differential Mode Voltage Gain

Differential Gain is the gain by which the amplifier boosts the difference of the input signals. The differential gain was obtained by performing AC Analysis, sweeping variable frequency from 1mHz to 1GHz.

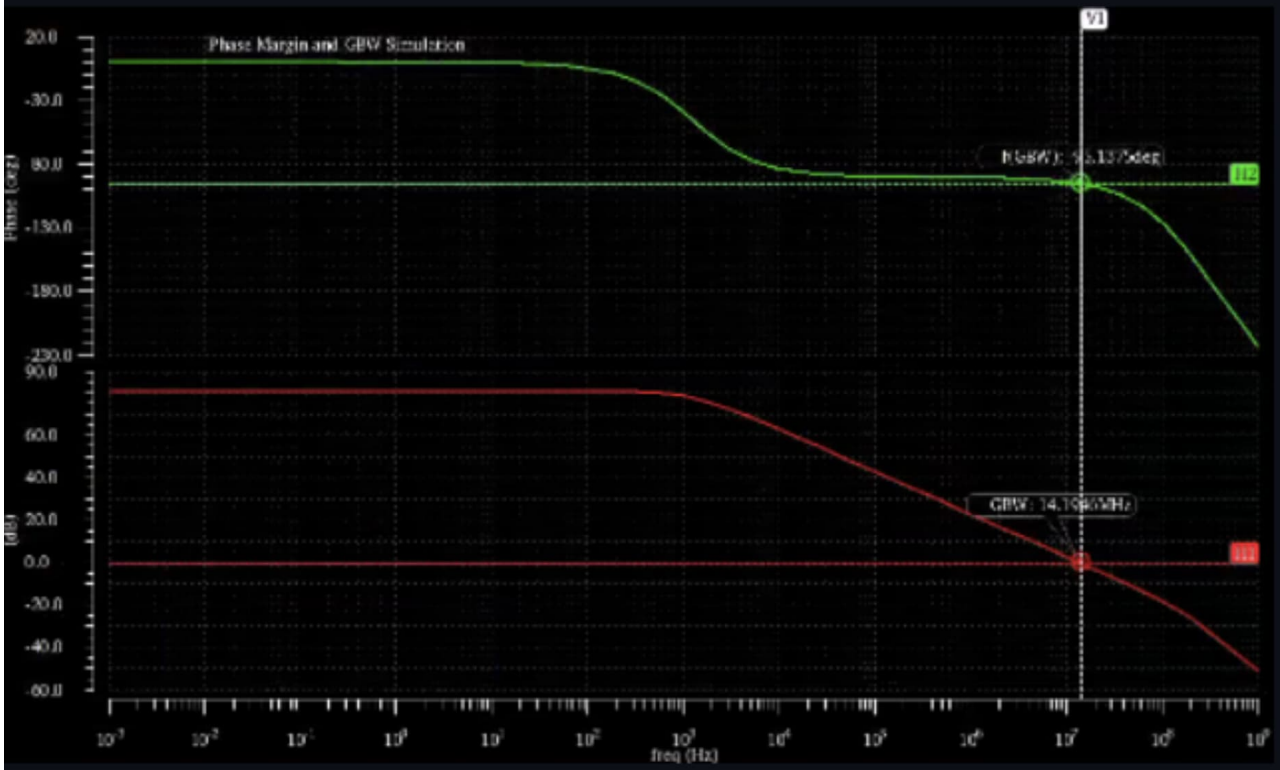




Result: DIFFERENTIAL MODE VOLTAGE GAIN = 80.9dB

Phase Margin and Unity Gain Bandwidth

GBW is the maximum frequency of the input signal that amplifier provides a voltage gain higher than 1 (magnitude of 0 dB in log scale). Phase Margin is the difference between the phase of the gain at 0 dB and 180°.



Frequency at 0 dB gives the GBW.

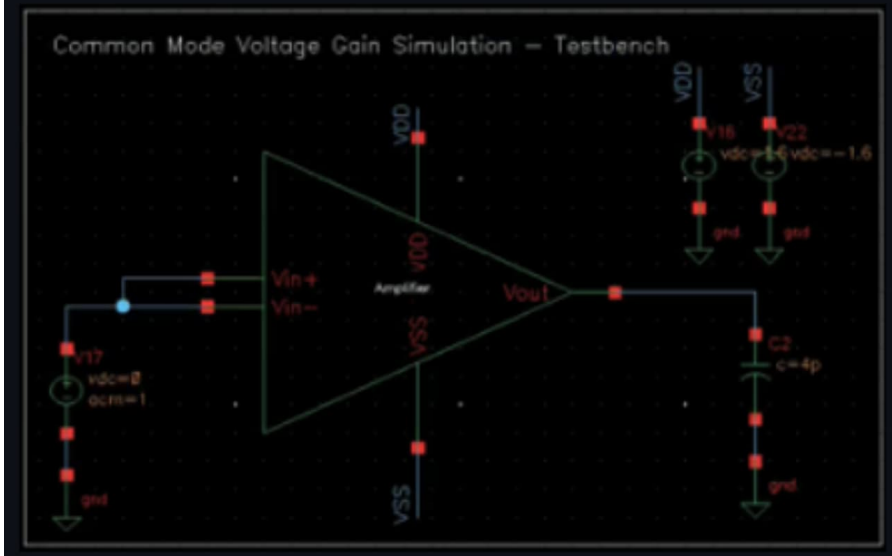
Result: UNITY GAIN BANDWIDTH (GBW) = 14.19 MHz

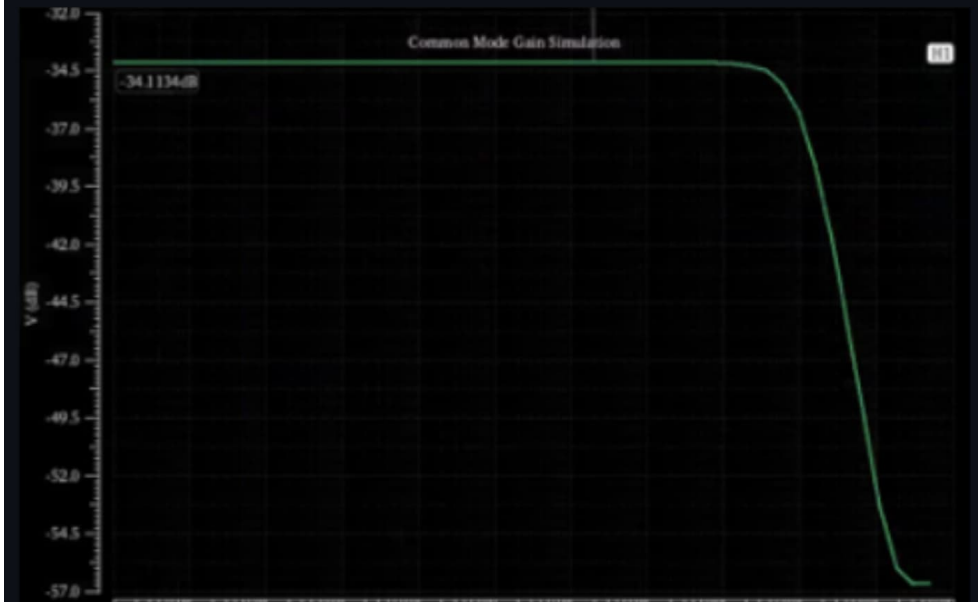
f(GBW) = -95.1375° and Phase Margin (PM) = 180 + (-95.1375°) = 84.86°

Result: PHASE MARGIN (PM) = 84.86°

Common Mode Rejection Ratio

While the purpose of a differential amplifier is to amplify just the difference between the input signals, it also passes through some of the common-mode component of the input signal. The ability of amplifier to ignore the average of the two input signals is called the common mode rejection ratio (CMRR). Similar to differential gain AC response, the common mode gain was simulated.





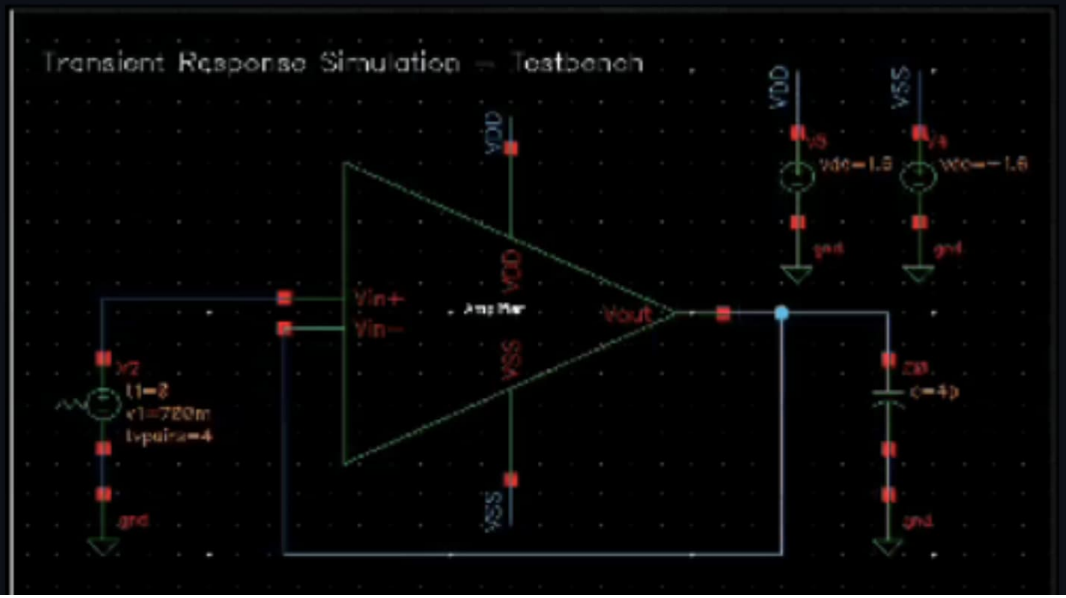
Result: Common Mode Gain = -34.1134°

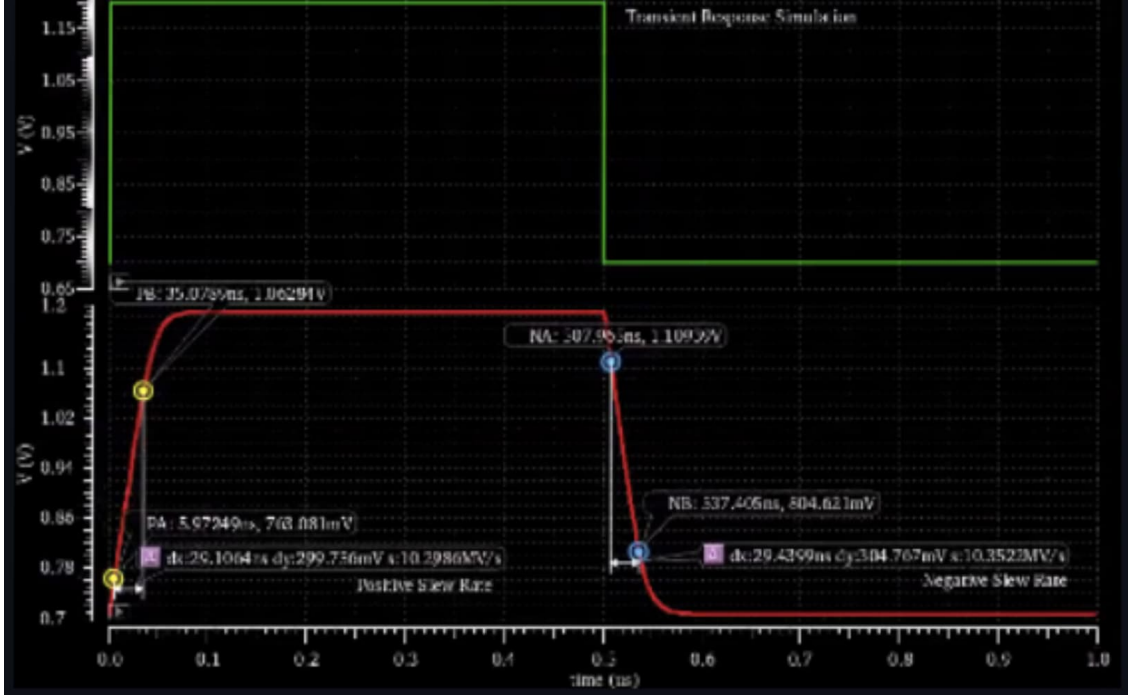
CMRR = (Differential Mode Gain)/(Common Mode Gain) CMRR = 20 log((Differential Mode Gain)/(Common Mode Gain))
= 80.9 – (–34.1134) = 115 dB

Result: Common Mode Rejection Ration (CMRR) = 115dB

Transient Response

The concept of finding the Average Slew Rate lies on measuring how close the output voltage waveform follows the input voltage waveform. While the positive slew rate occurs when the signal is rising, the negative slew rate occurs when the signal is falling. Slew rate is not related to frequency response. To find the average slew rate, transient response was performed by having a square wave input with unity gain amplifier configuration.





Average Slew Rate = (positive SR + negative SR)/2 = (10.298 + 10.3522)/2 = 10.3251 MV/S or 10.3251 V/µS Average Slew Rate (SR) = 10.3251 V/us

Power Dissipation

The total current includes from all current mirrors and current source also. Power is product of current and supply voltage. The total current was also verified using simulation.

Power Dissipation (P_diss)= Sum of currents flowing through all branches × VDD = 200.8 uA × 1.6 V = 0.321 mW

Power Dissipation (PDISS) = 0.321 mW

RESULTS

Design Parameter	Specification Value	Simulation Value
Differential Voltage Gain, A_{vd}	≥ 75 dB	81 dB
Output Voltage Swing Range, OVSR	≥ 1 V	1.1 V
Average Slew Rate, SR	≥ 10 V/µs	10.33 V/µs
Common Mode Rejection Ratio, CMRR	≥ 80 dB	115 dB
Unity Gain Bandwidth, GBW	≥ 8 MHz	14.2 MHz
Phase Margin, PM	≥ 60°	85°
Power Dissipation, P_{diss}	≤ 0.5 mW	0.321 mW