Monday	**EE 671: VLSI Design**	Due on Saturday
Oct. 16, 2023	**Assignment 4**	Oct. 28, 2023

Describe a Multiply-Accumulate circuit which will multiply two 16bit unsigned integer operands and add it to a 32 bit unsigned accumulator. The multiplier should use the Dadda reduction scheme and the 32 bit Brent Kung adder designed by you in the previous assignment for the final addition.

Your description should include a test bench which reads its operands from a file

Your description should use `std_logic` types for various signals. You can use the public domain tool "ghdl" for VHDL simulation.

Compose half adders and full adders using the basic gates (with roll number dependent gate delays) described for the previous assignment.

Test data should contain 10 randomly chosen input combinations. The test bench should use assert statements to flag errors if there is a mismatch between the computed sum/carry and the stored sum/carry.