Digital Logic
EG2103CT

Year: II
Part: I

Total: 5 hours/week
Lecture: 3 hours/week
Tutorial: hour/week
Practical: hours/week
Lab: 2 hours/week

Course Description:
This course introduces logic design and the basic building blocks used in digital systems, in particular digital computers. It starts with a discussion of digital signal, number system, logic gates, minimization techniques, and combinational as well as sequential circuits and concludes with digital logic families and digital displays.

Course Objective:
After completing this course, the students will be able to:
1. Design the combinational logic circuits
2. Explain the sequential logic circuits
3. Design problem based / predefined logic-based circuits

Course Contents:

Theory

Unit 1. Introduction to Digital Signal **[3 Hrs.]**
- 1.1. Analog Signal and Digital Signal
- 1.2. Advantages of Digital over Analog Signals
- 1.3. Representation of Digital Signal
- 1.4. Applications of Digital Signal

Unit 2. Number Systems and Codes **[4 Hrs.]**
- 2.1. Two State Devices
- 2.2. Decimal Number System
- 2.3. Binary Number System
- 2.4. Octal Number System
- 2.5. Hexadecimal Number System
- 2.6. Conversions among Different Number Systems
- 2.7. Fractions Conversion
- 2.8. BCD Code
- 2.9. Gray Code
- 2.10. Alphanumeric Code
  - 2.10.1. ASCII Code
  - 2.10.2. EBCDIC Code

Unit 3. Arithmetic Logic Operations **[5 Hrs.]**
- 3.1. Binary Arithmetic
  - 3.1.1. Binary Addition
  - 3.1.2. Binary Subtraction
- 3.2. r's Complement and (r-1)'s Complement Method for decimal and binary system

Unit 4. Logic Gates and Boolean Function **[10 Hrs.]**
- 4.1. Basic Gates: AND, OR, NOT
- 4.2. Universal Gates: NAND, NOR
- 4.3. Exclusive Gates: XOR, XNOR

4.4. DeMorgan's Theorems
4.5. The Universal Properties of the NAND Gates
4.6. The Universal Properties of the NOR Gates
4.7. Pulse Operation in Logic Gates
4.8. Combination of Logic Gates
4.9. Boolean Algebra and its Properties/Laws
4.10. Boolean Expression in Logic Gates
4.11. Simplification of Boolean Expressions

Unit 5. Logic Simplification **[5 Hrs.]**

5.1. Karnaugh Map
  5.1.1. K-Map Simplification for Two Input Variables
  5.1.2. K-Map Simplification for Three Input Variables
  5.1.3. K-Map Simplification for Four Input Variables
5.2. Sum of Product (SOP) Simplification
5.3. Product of Sums (POS) Simplification
5.4. K-Maps with *Don't Care* Conditions

Unit 6. Combinational Logic Circuits **[8 Hrs.]**

6.1. Half Adder, Full Adder and Parallel Adder
6.2. Half Subtractors and Full Subtractors
6.3. Decimal to Binary Encoder and Decimal to BCD Encoder
6.4. Binary to Decimal Decoder, BCD to Decimal Decoder and Seven Segment Display Decoder
6.5. Data Transmissions, 4-to-1 Multiplexer and 8-to-1 Multiplexer
6.6. Demultiplexer and Decoder Relations
6.7. 1-to-4 Demultiplexer and 1-to- 16 Demultiplexer

Unit 7. Sequential Logic Circuits **[8 Hrs.]**

7.1. Flip-Flops
  7.1.1. RS Flip-Flop and its Truth Table
  7.1.2. D Flip-Flop and its Truth Table
  7.1.3. JK Flip-Flop and its Truth Table
  7.1.4. T Flip-Flop and its Truth Table
  7.1.5. Master-Slave Flip-Flops
  7.1.6. Applications of Flip-Flop
7.2. Shift-Registers
  7.2.1. Flip-flop as a One-bit Memory Device
  7.2.2. Arithmetic Right/Left Shift Registers
  7.2.3. Serial-in Serial-out (SISO) Shift Register
  7.2.4. Serial-in Parallel-out (SIPO)Shift Register
  7.2.5. Parallel-in Serial-out (PISO)Shift Register
  7.2.6. Parallel-in Parallel-out (PIPO)Shift Register

7.2.7. Applications of Shift Registers

7.3. Counters

7.3.1. Synchronous Counters

7.3.2. Ripple Counters

7.3.3. M- Modulus Counters

7.3.4. Decade Counters

7.3.5. Ring Counters

7.3.6. Applications of Counters

Unit 8. Digital Displays **[2 Hrs.]**

8.1. LED Display

8.2. 7-Segments Display

Practical: **[30 Hrs.]**

1. Verify the truth tables of basic gates and other gates: AND, OR, NOT, NAND, NOR, XOR and XNOR Gates
2. Realize and verify truth tables applying DeMorgan's Theorems
3. Verify the universal properties of the NAND gate and NOR gate.
4. Realize and verify truth tables of binary half adder/Subtractor and full adder/Subtractor
5. Implement decimal to 3-4-bit binary encoder
6. Realizing the function of 4-bit binary decoder
7. Realizing the function of 4-to-1 multiplexer and 1-to- 4 demultiplexer circuits.
8. Realizing the function of flip-flops, RS, D, JK, T flip-flops
9. Realizing the function shift-registers: SISO, SIPO, PISO and PIPO
10. Realizing the function ripple counters
11. Realizing the function synchronous counters
12. Realizing and designing of seven-segment display-decoder logic circuit

Final written exam evaluation scheme			
Unit	**Title**	**Hours**	**Marks Distribution***
1	Introduction to Digital Signal	3	5
2	Number Systems and Codes	4	7
3	Arithmetic Logic Operations	5	9
4	Logic Gates and Boolean Function	10	18
5	Logic Simplification	5	9
6	Combinational Logic Circuits	8	14
7	Sequential Logic Circuits	8	14
8	Digital Displays	2	4
	Total	**45**	**80**

* There may be minor deviation in marks distribution.