Summer Project Report

IIT Kanpur

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Project:	Design of a single stage Differential Amplifier

Project Overview

Our goal is to design a PMOS input single stage distinct amplifier using GPDK-45nm process technology in Cadence Virtuoso, which follows the following constraints at room temperature :

Loop Gain (min): 40 dB

Closed Loop Bandwidth: 50 MHz

CMRR (@ DC): 80 dB

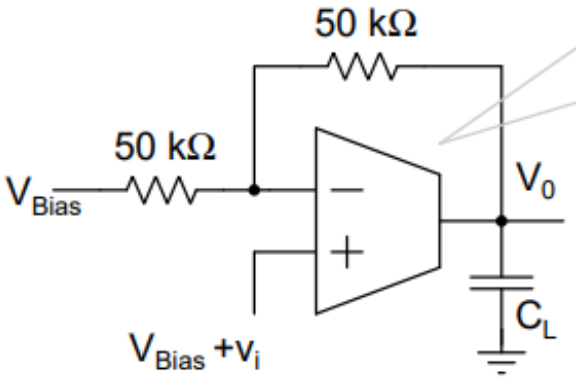

Figure 1: Negative feedback setup

Given,

- $\boldsymbol{V_{DD}} = 1.8$ V
- $\boldsymbol{v_i} = 150$ mV $\sin(\omega t)$
- $\boldsymbol{C_L} = 10$ pF

Initial Plan

We decide to start with a simple setup of just a differential to single ended conversion setup with an active NMOS load to sink current in both branches as shown :

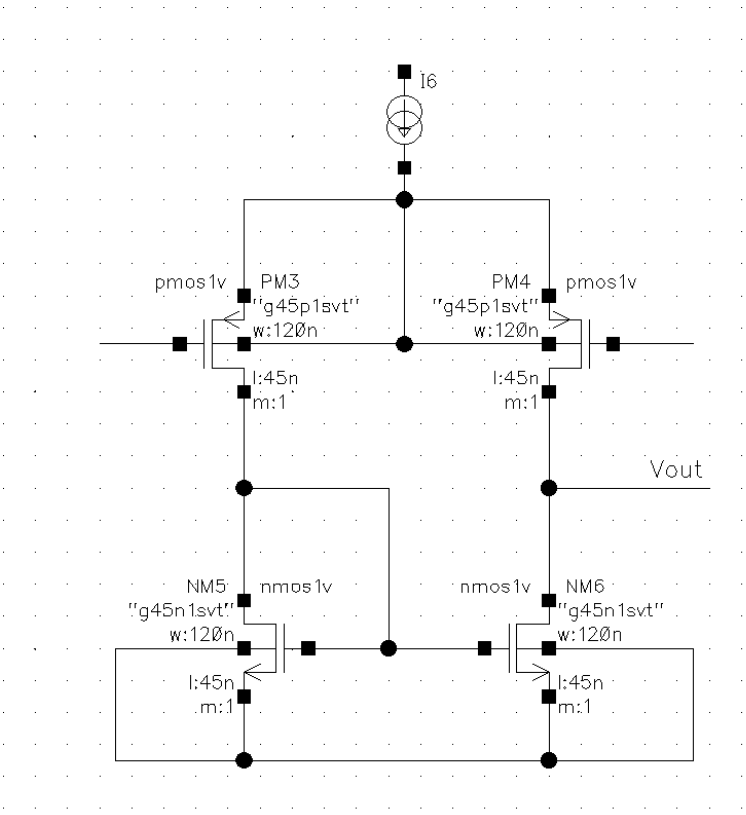

Figure 2: Differential to single-ended converter with active NMOS load

Design Challenges and Considerations

There are several challenges with the proposed configuration for our application.

1. Gain Requirement

We require a loop gain of at least **40 dB**, which corresponds to a voltage gain of:

$$0.5 \cdot A_v \geq 100 \quad \text{(since the feedback factor is 0.5)}$$

The voltage gain of a differential amplifier is approximately given by:

$$A_v = g_m \left(r_{0p} \parallel r_{0n} \right)$$

This implies:

$$\frac{g_m}{g_{ds}} = g_m \cdot r_0 \geq 400 - 500$$

Achieving such a high intrinsic gain would demand large channel lengths, as evident from the corresponding plots (provided later). This requirement places stringent demands on the device sizing and layout and can degrade other performance metrics such as speed and area.

2. Bandwidth Requirement

Given a desired bandwidth of 50 MHz, we use the gain-bandwidth product relationship to estimate the necessary transconductance. The unity-gain bandwidth is approximated as:

$$f_{\text{unity}} \approx \frac{g_m}{2\pi C_L}$$

Since we desire a gain of 2 at 50 MHz, the bandwidth can be approximated as:

$$\text{Bandwidth} = \frac{f_{\text{unity}}}{\text{Gain}} = \frac{g_m}{4\pi C_L}$$

Given:

- $C_L = 10\,\text{pF}$
- Bandwidth $= 50\,\text{MHz}$

Solving for g_m:

$$\frac{g_m}{4\pi \cdot 10 \times 10^{-12}} = 50 \times 10^6 \Rightarrow g_m > 6.28\,\text{mS}$$

This is a relatively high transconductance, which again pushes for larger device sizes or bias currents.

3. CMRR Requirement

We require a **Common-Mode Rejection Ratio (CMRR)** of at least **80 dB**, which corresponds to a common-mode gain of:

$$\text{CMRR} = 20\log_{10}\left(\frac{A_{dm}}{A_{cm}}\right) = 80\text{ dB} \Rightarrow \frac{A_{dm}}{A_{cm}} = 10^4 \Rightarrow A_{cm} = -40\text{ dB}$$

For a differential pair with a current mirror load, the common-mode gain is given by:

$$A_{cm} = \frac{g_{mp}}{g_{mn}(1 + 2g_{mp}R_{SS})}$$

Where:

- g_{mp}, g_{mn} are the transconductances of PMOS and NMOS respectively,
- R_{SS} is the output resistance of the current source.

With a simple (non-cascoded) current mirror, $\boldsymbol{g_{mp}R_{SS} = \frac{g_{mp}}{g_{dsp}}}$, which is relatively low and not enough to achieve the required CMRR. Therefore, to improve CMRR, we adopt a Cascode Current Mirror too. Also, a higher Differential Gain helps us in CMRR improvement too as the common mode rejection can then go below 40dB too. SO, we dicide the following:

- A **cascode differential amplifier**
- A **cascoded current mirror load**

These enhancements increase the output resistance and suppress the common-mode gain effectively.

4. Voltage Headroom Constraints

The biggest challenge with cascoding is **voltage headroom**. Given:

$$V_{DD} = 1.8\,\mathrm{V}$$

A cascode configuration consumes additional headroom due to stacking of multiple transistors. This makes it difficult to ensure that all devices remain in saturation.

Therefore, the design must carefully allocate the available headroom to each transistor in the stack to maintain proper operation.

Final Design

1. Topology

We use the following topology for differential to single ended conversion.

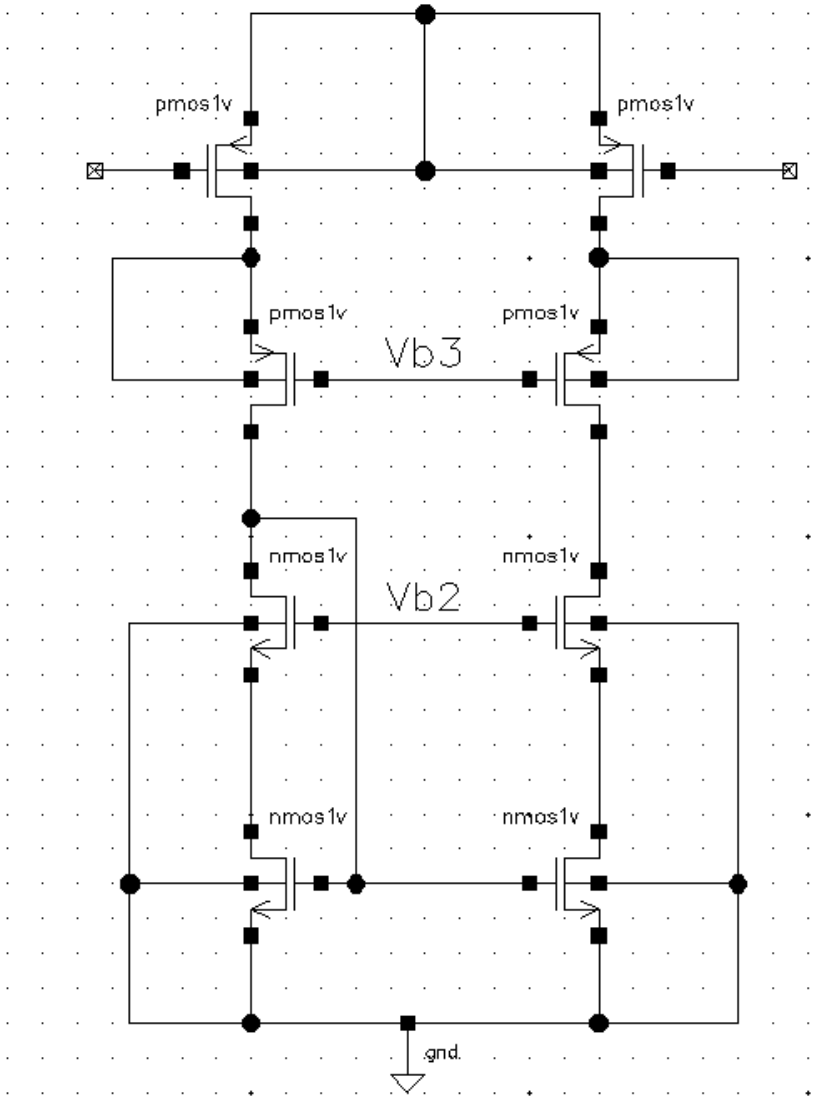

Figure 3: PMOS input Cascoded differential to single ended converter part

Here, we incorporate a design similar to the **high swing cascode** variation, i.e., biasing **vb2** separately in order to maintain control over and maximize our ICMR and headroom for the cascoded current mirror.

For our current mirror. we go with the following simple topology, again biasing **vb1** separately for optimum control, and incorporate headroom constraints.

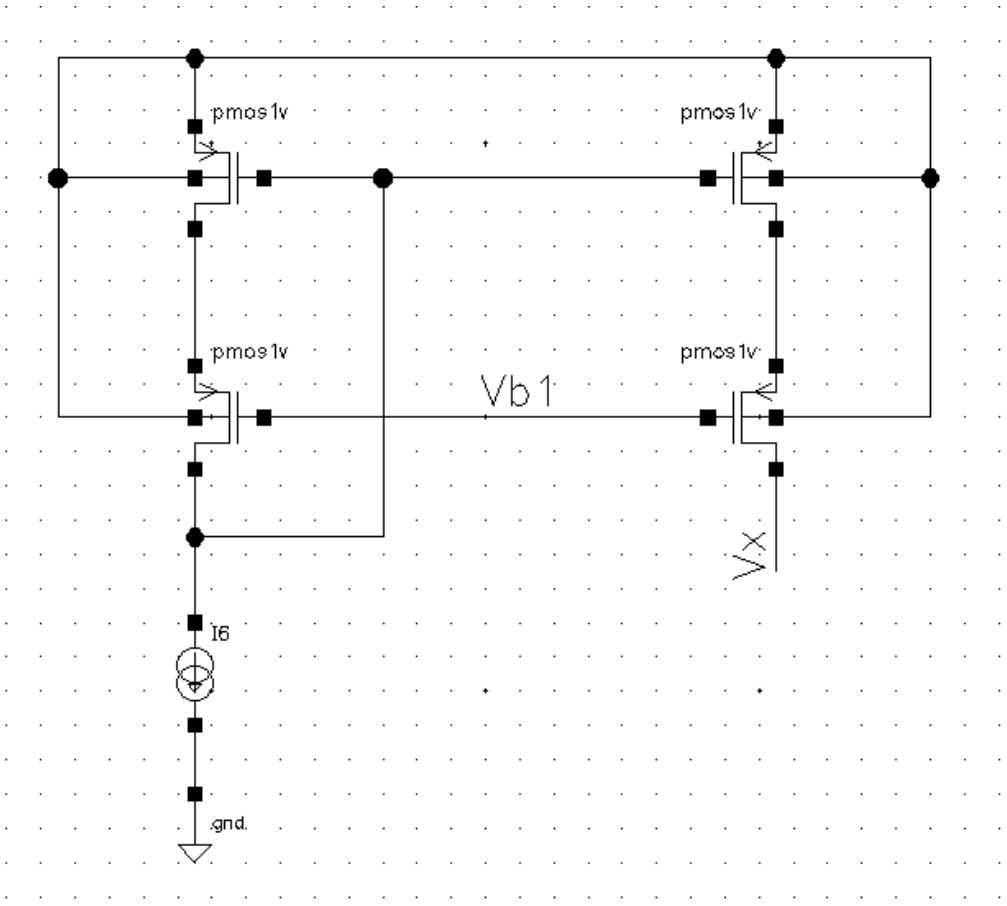

Figure 4: Cascoded current mirror

2. Proper Biasing

Now, we need to determine proper biasing points $\boldsymbol{V_{b1}}$, $\boldsymbol{V_{b2}}$, and $\boldsymbol{V_{b3}}$ such that the following conditions are satisfied:

1. All transistors remain in saturation and provide **loop gain** $> 40\,\text{dB}$ throughout the full range of common-mode input voltage:

$$V_{\text{CM}} \in [V_{\text{bias}} - 150\,\text{mV},\ V_{\text{bias}} + 150\,\text{mV}]$$

2. The output voltage $\boldsymbol{V_{out}}$ must swing over a range of 600 mV without pushing any transistor out of saturation as it sees a swing of gain (=2) times the swing in input.

From our knowledge of saturation constraints, we have:

- **NMOS:**

$$V_{DS} > V_{GS} - V_{th} \quad \text{or} \quad V_D > V_G - V_{th}$$

- **PMOS:**

$$|V_{DS}| > |V_{GS}| - |V_{th}| \quad \text{or} \quad V_D < V_G + V_{th}$$

Using the saturation constraints, we arrive at the following conditions for $\boldsymbol{V_{b1}}$, $\boldsymbol{V_{b2}}$, $\boldsymbol{V_{b3}}$ and $\boldsymbol{V_{cm}}$:

$$V_{in+} < V_{DD} - V_{\text{ov,current\_source}} - V_{GS,\text{PM1}} \tag{1}$$

$$V_{in+} > V_{b3} + V_{GS,\text{PM5}} - V_{th,\text{PM1}} \tag{2}$$

$$V_{b3} > V_{GS,\text{NM1}} - V_{th,\text{PM5}} \tag{3}$$

$$V_{b2} < V_{GS,\text{NM1}} + V_{th,\text{NM3}} \tag{4}$$

$$V_{b2} > V_{GS,\text{NM3}} + V_{GS,\text{NM1}} - V_{th,\text{NM1}} \tag{5}$$

$$V_{out} > V_{b2} - V_{th,\text{NM4}} \tag{6}$$

$$V_{out} < V_{b3} + V_{th,\text{PM6}} \tag{7}$$

Based on our earlier requirements, we ensure the following condition:

$$\text{Equation (1)} - \text{Equation (2)} > 300 \text{ mV} \tag{8}$$

This guarantees an input common-mode swing of at least 300 mV.

This constraint gives us an **upper bound** for $\boldsymbol{V_{b3}}$. However, we choose $\boldsymbol{V_{b3}}$ to be close to its **minimum allowable value** to allow:

- Higher $V_{\text{ov,current\_source}}$,
- Better common-mode response, since a higher V_{DS} across the current mirror PMOS transistors reduces their output conductance (g_{ds}).

Note: $\boldsymbol{V_{b3}}$ cannot be made too small, as it directly reduces the available swing for $\boldsymbol{V_{out}}$. Therefore, a careful **trade-off** must be made.

Additionally, it is evident that $\boldsymbol{V_{b2}}$ should be chosen **as high as possible** in order to:

- Maximize the output voltage swing,
- Ensure that the lower NMOS transistors have sufficient V_{DS}, which in turn improves the loop gain.

Biasing Voltage for Current Mirror: $\boldsymbol{V_{b1}}$

To properly bias the current mirror, the bias voltage $\boldsymbol{V_{b1}}$ must satisfy the following constraints:

$$V_{b1} < V_{DD} - V_{GS,\text{PM10}} - V_{GS,\text{PM8}} + V_{th,\text{PM10}} \tag{9}$$

$$V_{b1} > V_x - V_{th,\text{PM7}} \tag{10}$$

Here, V_x is the **voltage at the internal node** of the current mirror that connects to the **differential amplifier section**.

> **Note:** There is one *very important* additional design consideration — ensuring **sufficient $\boldsymbol{V_{DS}}$** across all transistors. This is crucial to maintain desirable **small-signal characteristics** such as high g_m, high g_m/g_{ds}, and other performance metrics.
>
> Given the **tight voltage headroom**, we **design with $\boldsymbol{V_{DS} = 0.3\,\text{V}}$** for each device as a guideline and select the bias voltages V_{b1}, V_{b2}, V_{b3} accordingly.

3. Design using gm/Id method

Now we need to decide the values of the Width and Channel Length for each of the MOSFETS. Now, we might think we can do so relying on our trusty equation :

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

But, even with the CLM term, this is just a first order model of the NMOS. So, using this would cause our final observed values to change a lot making designing painful. So, what we do is characterize the MOSFETS and plot and store some graphs, namely of some Width(W) independent(almost) parameters like

$$\frac{\mathbf{g_m}}{\mathbf{I_D}}, \quad \frac{\mathbf{I_D}}{\mathbf{W}}, \quad \frac{\mathbf{g_m}}{\mathbf{W}}, \quad \frac{\mathbf{g_m}}{\mathbf{g_{ds}}}$$

along with **Vov, Vgs, Vth** too; we record values of these parameters and plot as we sweep **Id** through the MOSFET and plot them. Note that we dont account for vds and dont sweep through it, even though it has a decent say on the properties, just for simplicity. We will adjust our design accordingly later.

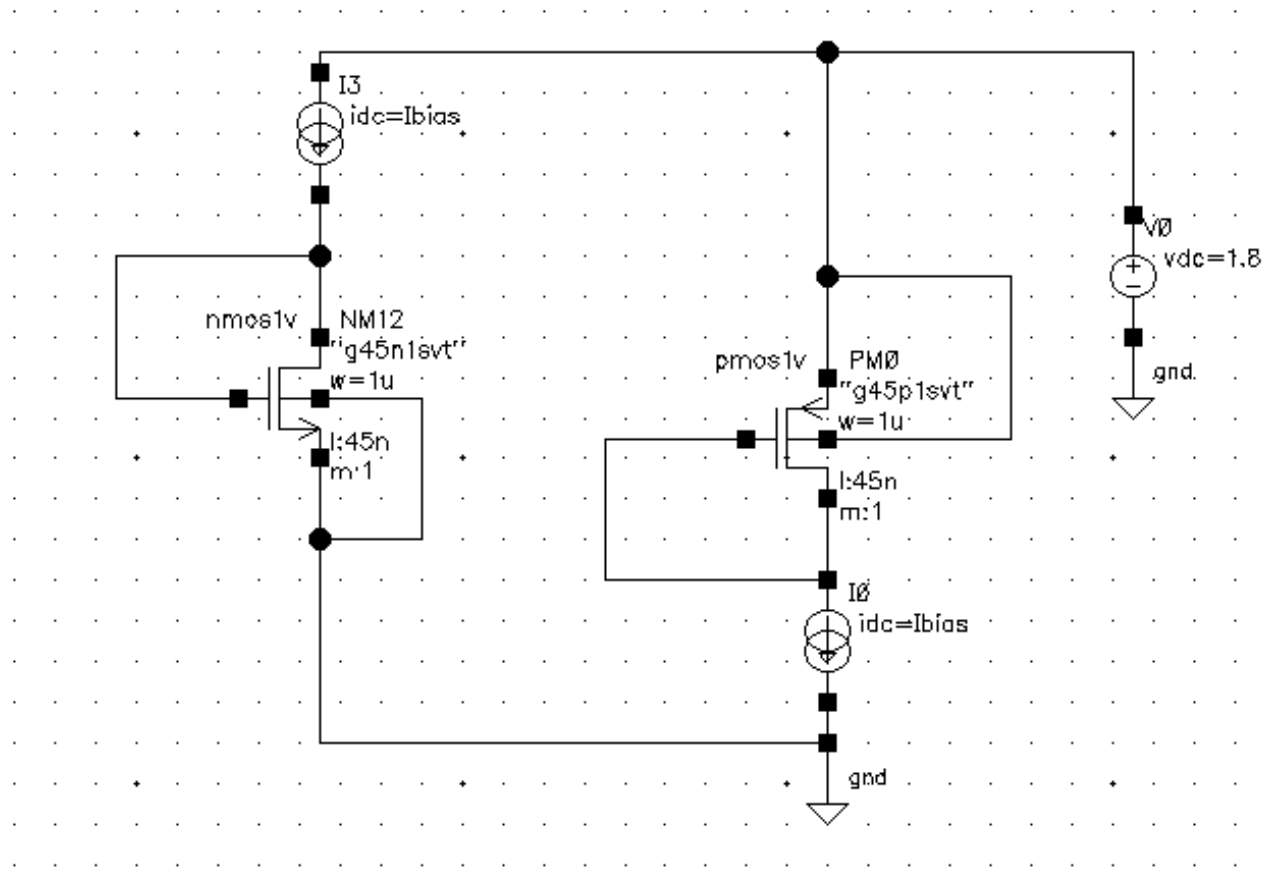

Figure 5: PMOS and NMOS characterization circuit

Now, following are plots for the **NMOS** for varyting lengths and sweep of Id:

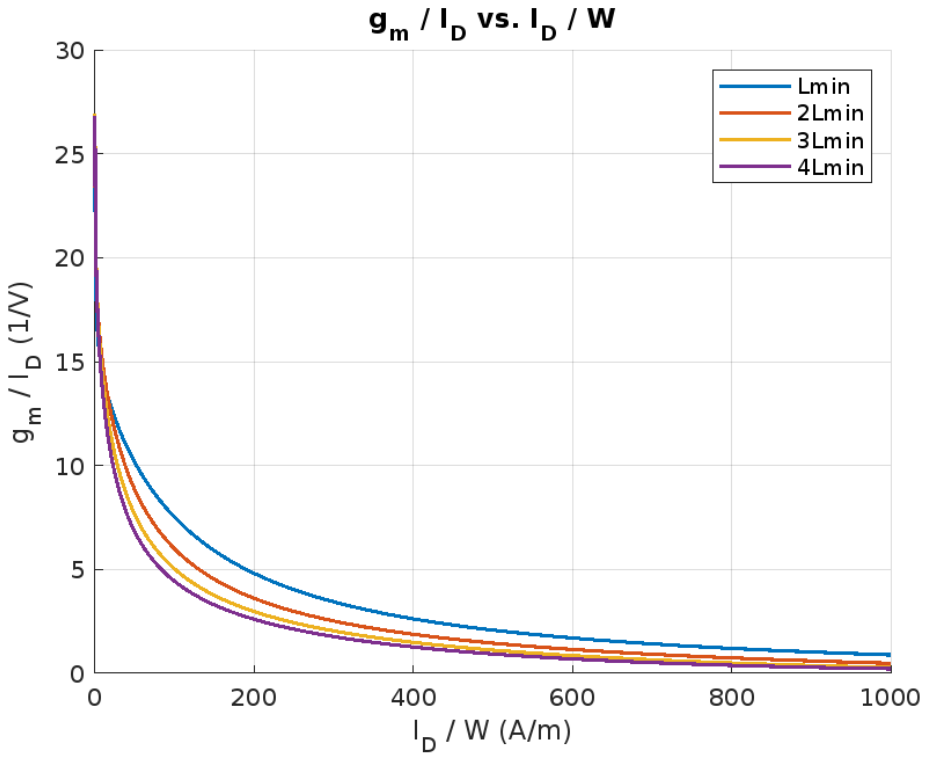

Figure 6:

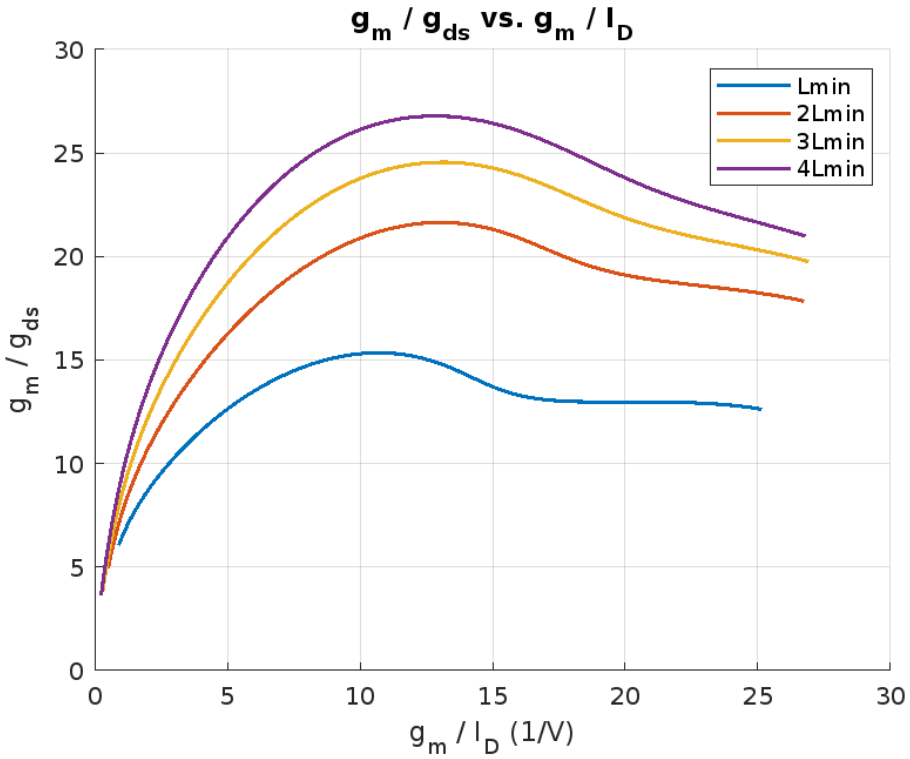

Figure 7:

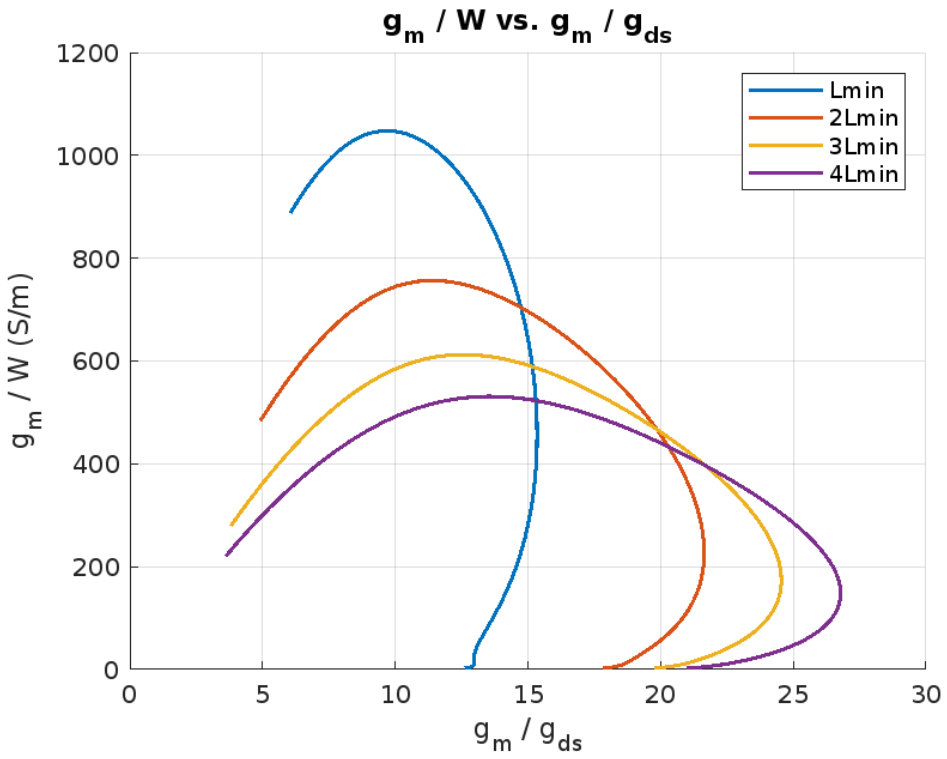

Figure 8:

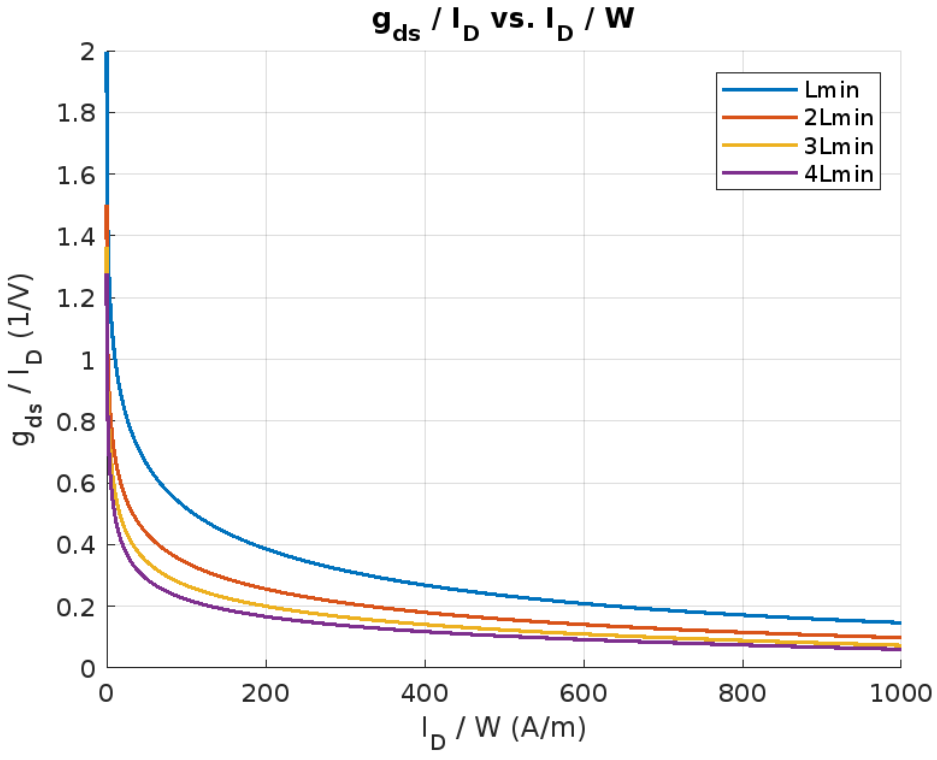

Figure 9:

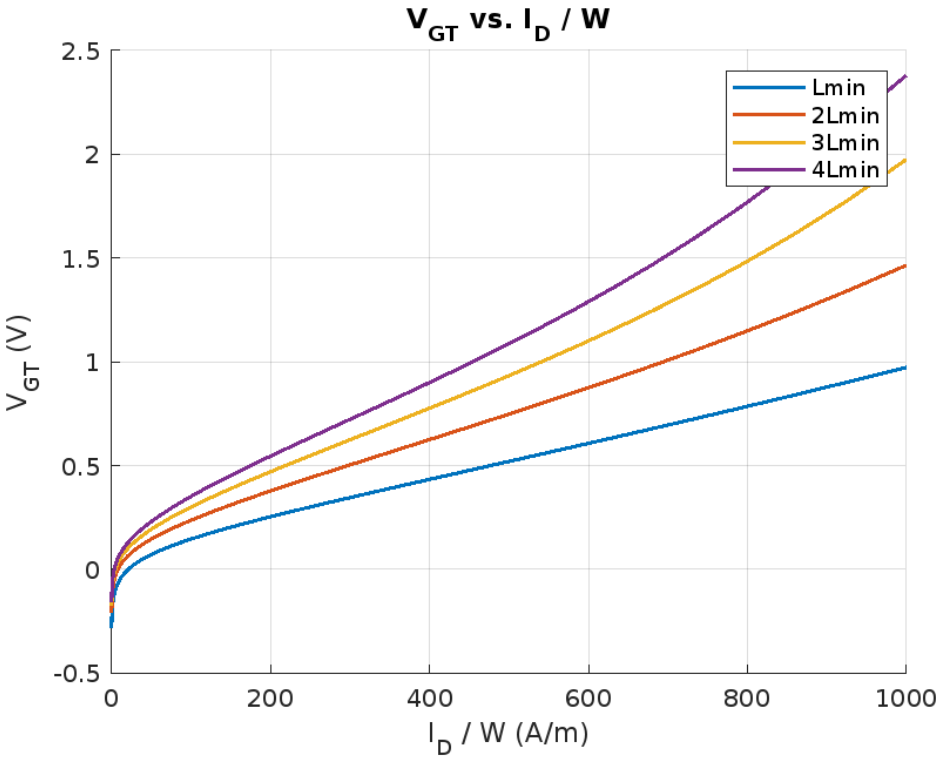

Figure 10:

For the **PMOS** also, we have the following :

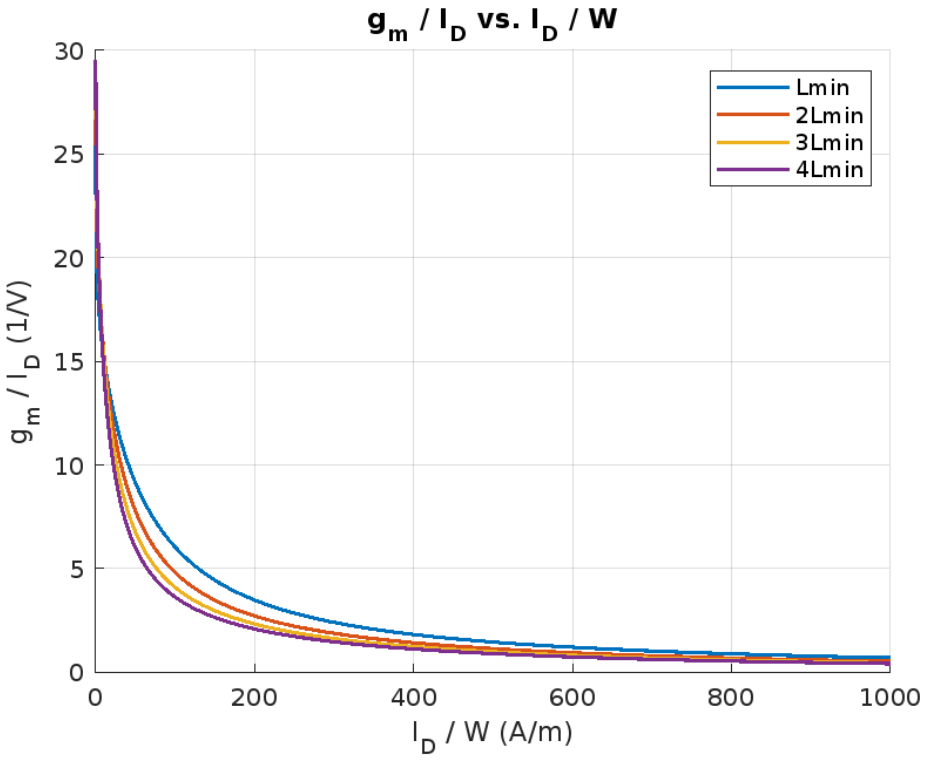

Figure 11:

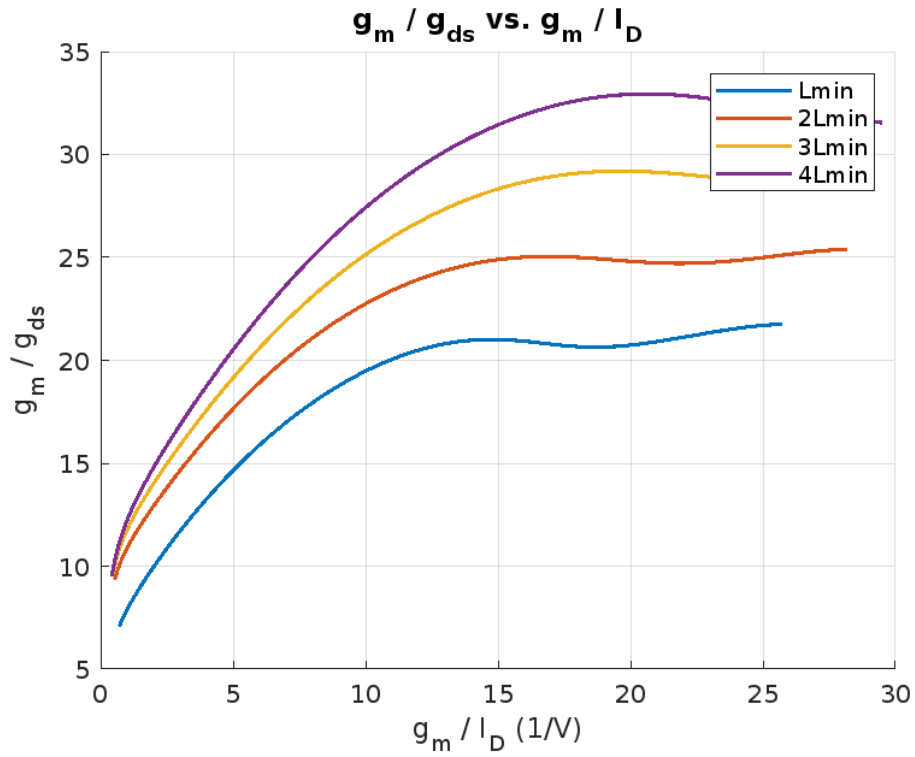

Figure 12:

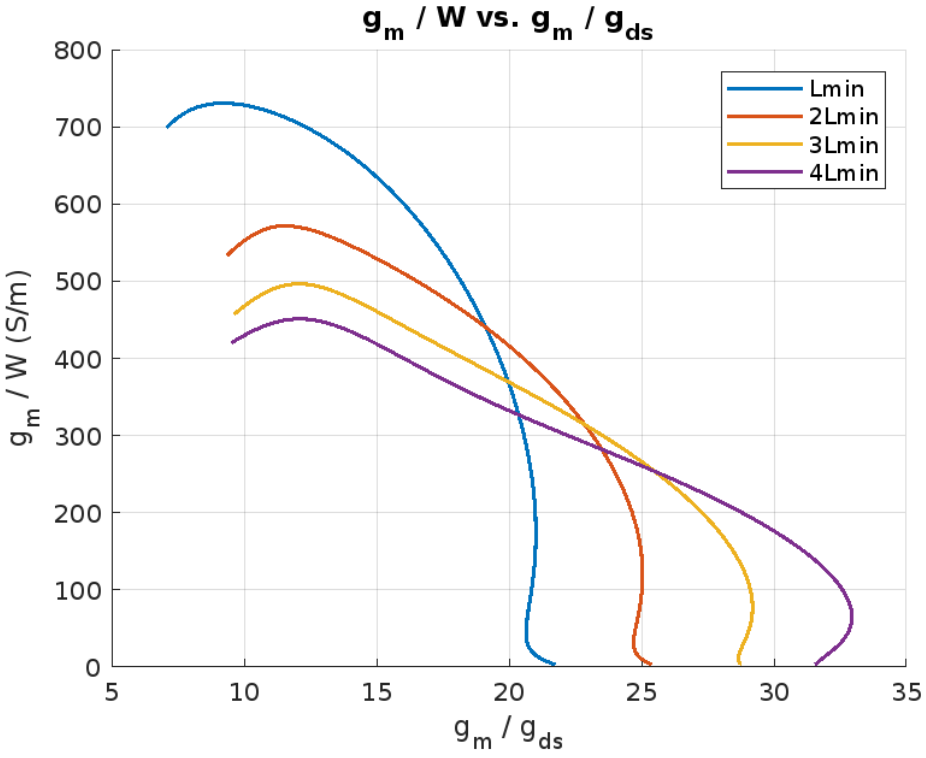

Figure 13:

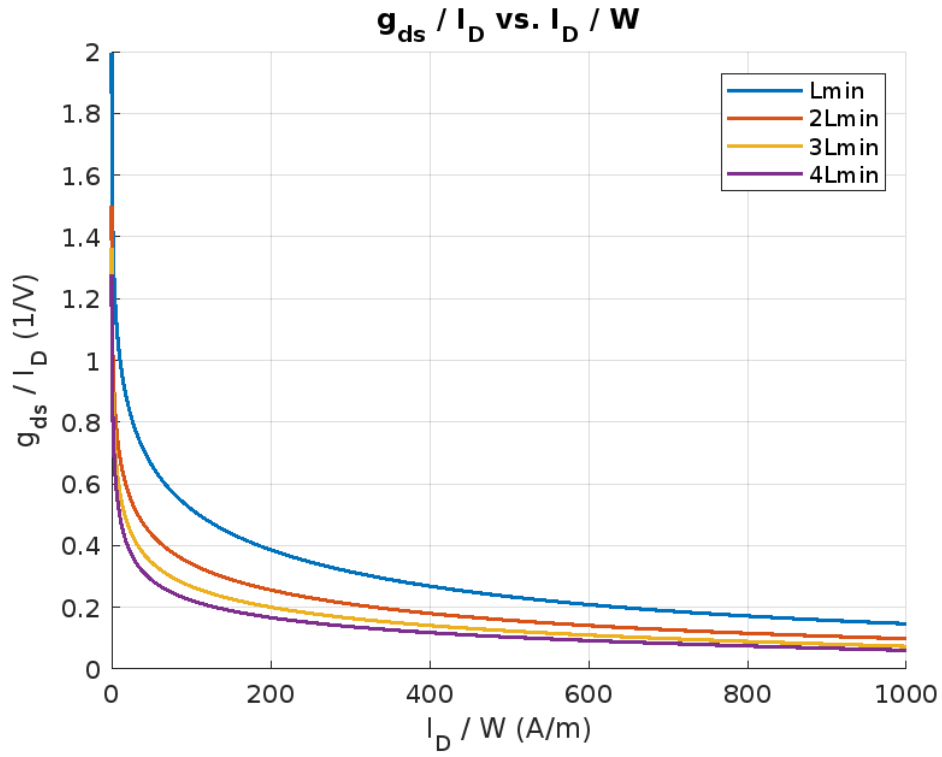

Figure 14:

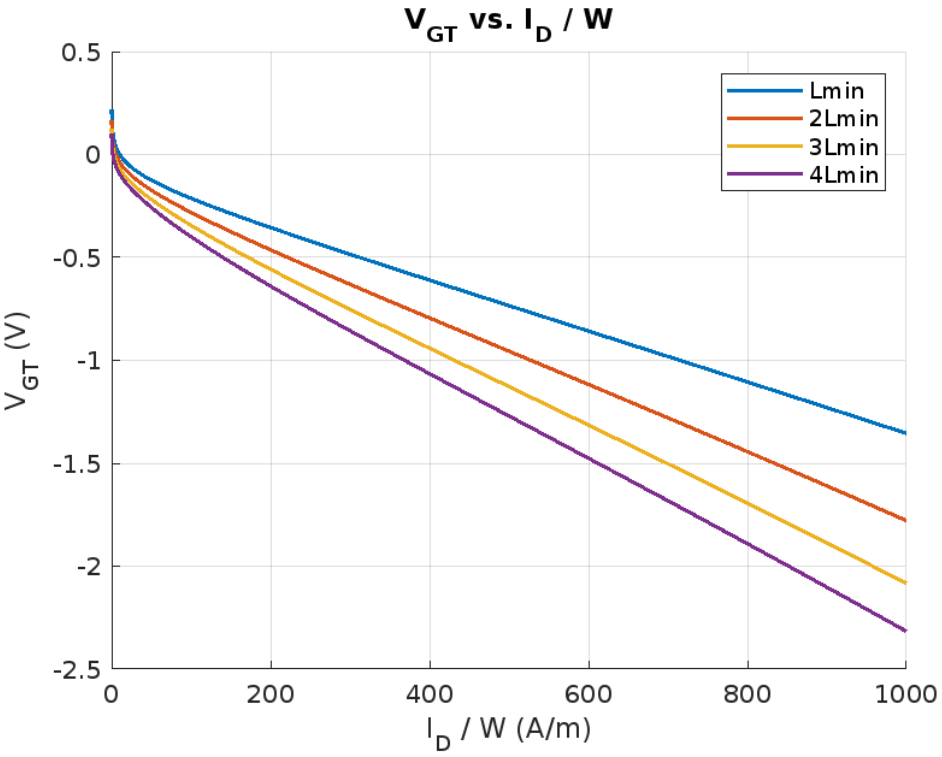

Figure 15:

Result

From our final design, we achieve the following performance metrics:

- **Loop gain at $V_{\text{bias}} = 845\,\text{mV}$: 41.405 dB**
- **Loop gain at $V_{\text{bias}} = 695\,\text{mV}$ (actual chosen V_{bias}): 41.134 dB**
- **Loop gain at $V_{\text{bias}} = 545\,\text{mV}$: 40.140 dB**
- **Open-loop Differential Mode gain: 50.81 dB**
- **Open-loop Common Mode gain: −51.64 dB**
- **Open-loop CMRR at DC: 102.45 dB**
- **Closed-loop gain: 5.94 dB**
- **Closed-loop bandwidth: 68.07 MHz**
- **Closed-loop phase margin: 60°**
- **Step response steady-state error (input: 10 mV): 0.181 mV**

Data Plots

1. Loop Gain, Bandwidth and CMRR

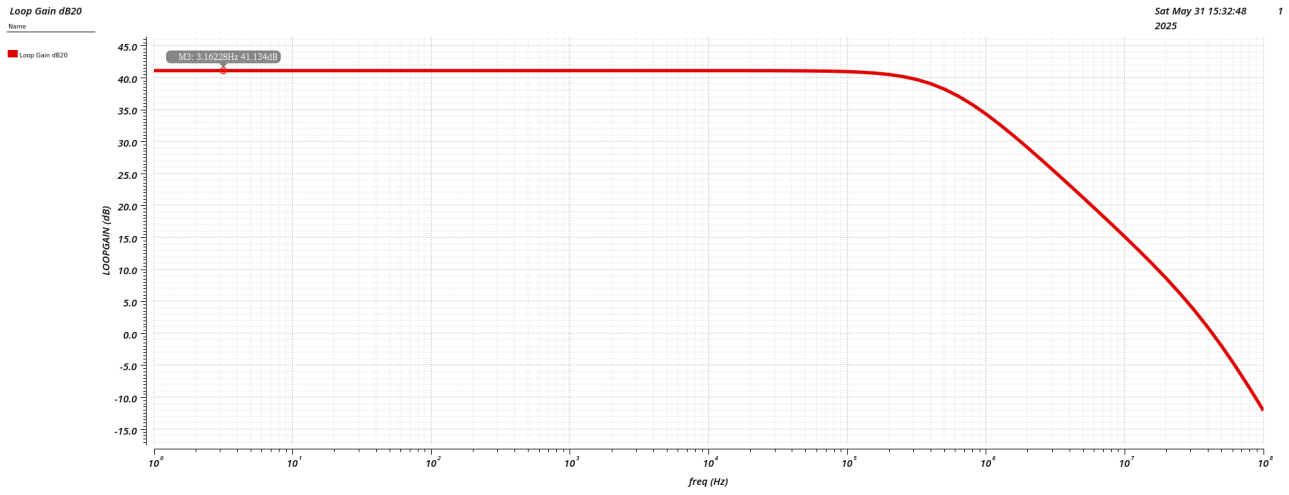

Figure 16: Loop Gain at Vbias = 695mV

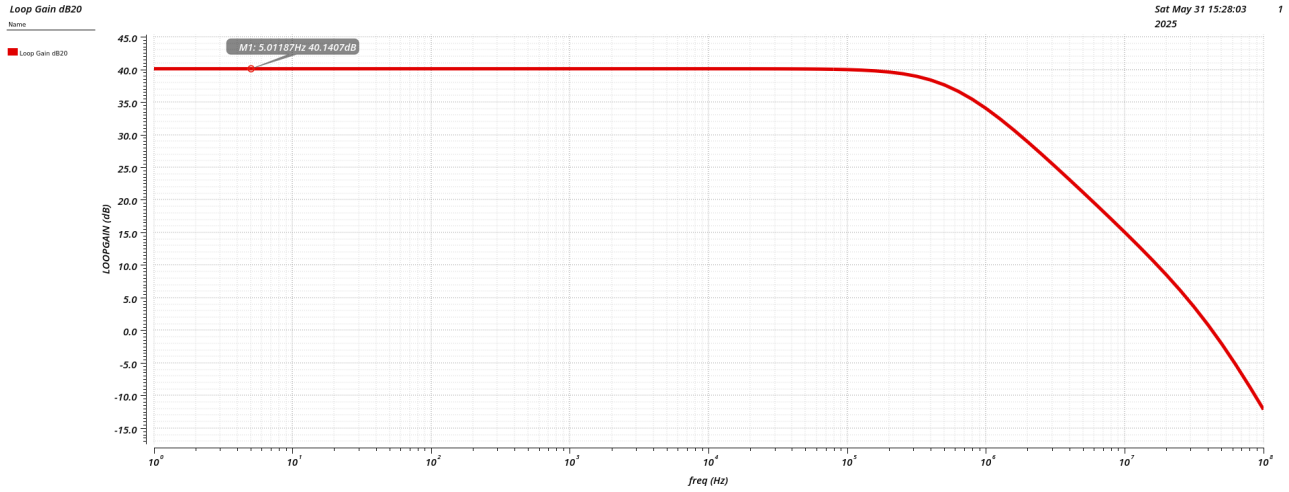

Figure 17: Loop Gain at Vbias = 545mV

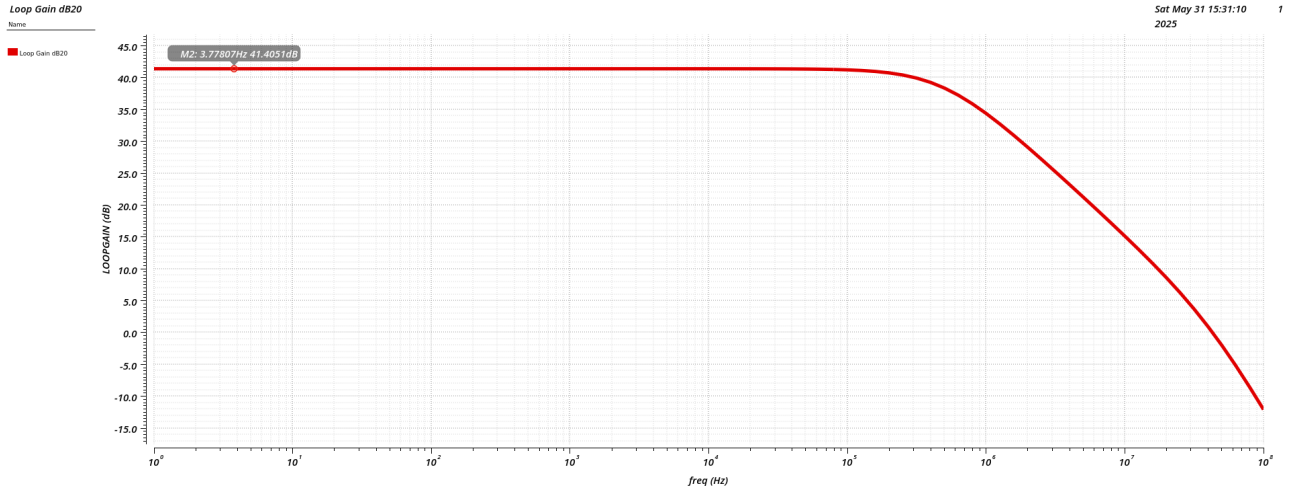

Figure 18: Loop Gain at Vbias = 845mV

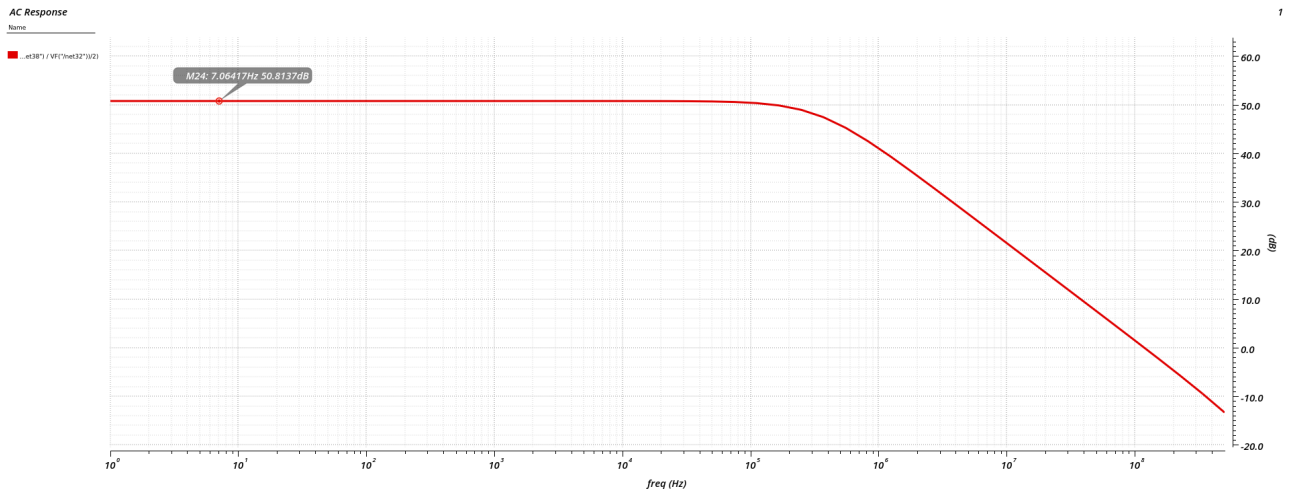

Figure 19: Open loop Deferential Mode response

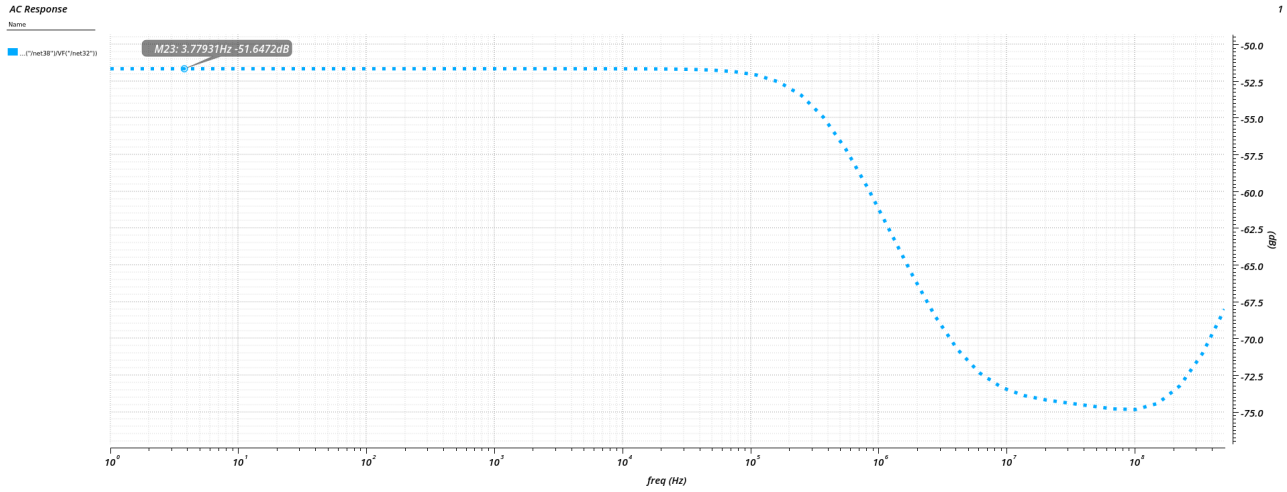

Figure 20: Open Loop Common Mode response

2. Gain and Phase

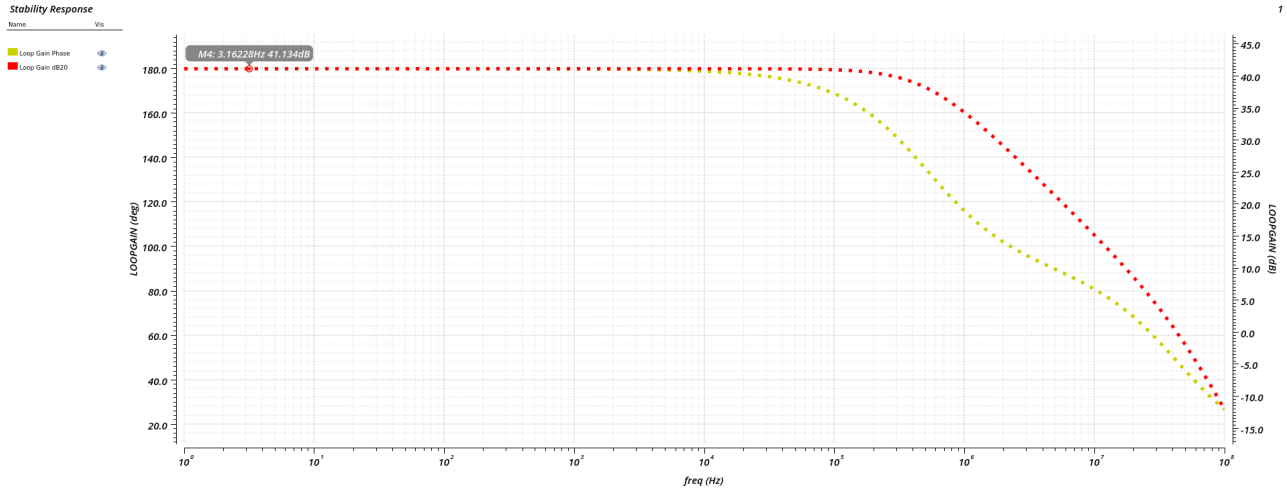

Figure 21: Open Loop Gain and phase

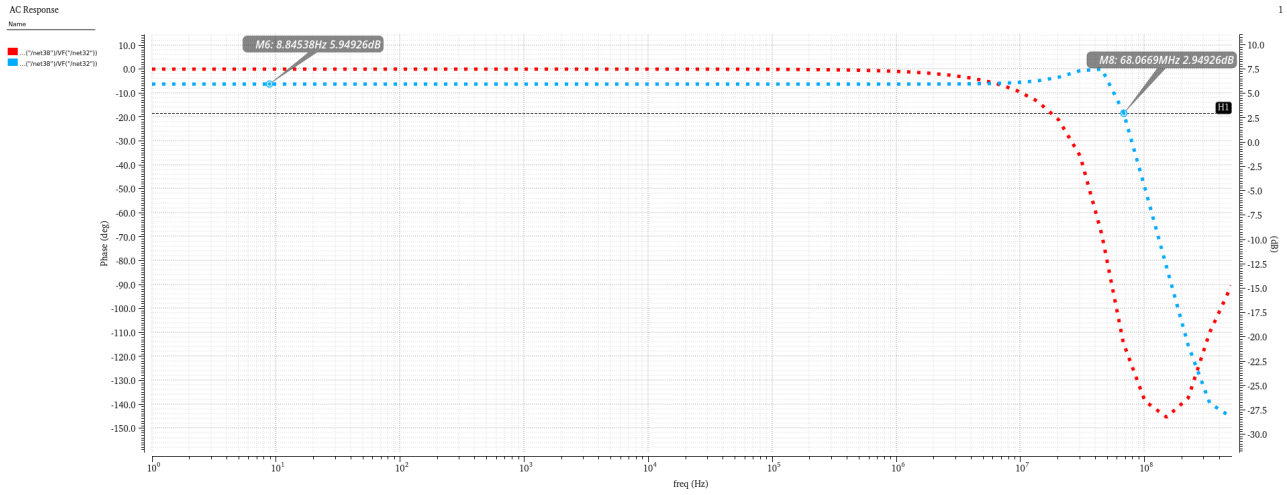

Figure 22: Closed loop Gain and Phase

3. Transient Response

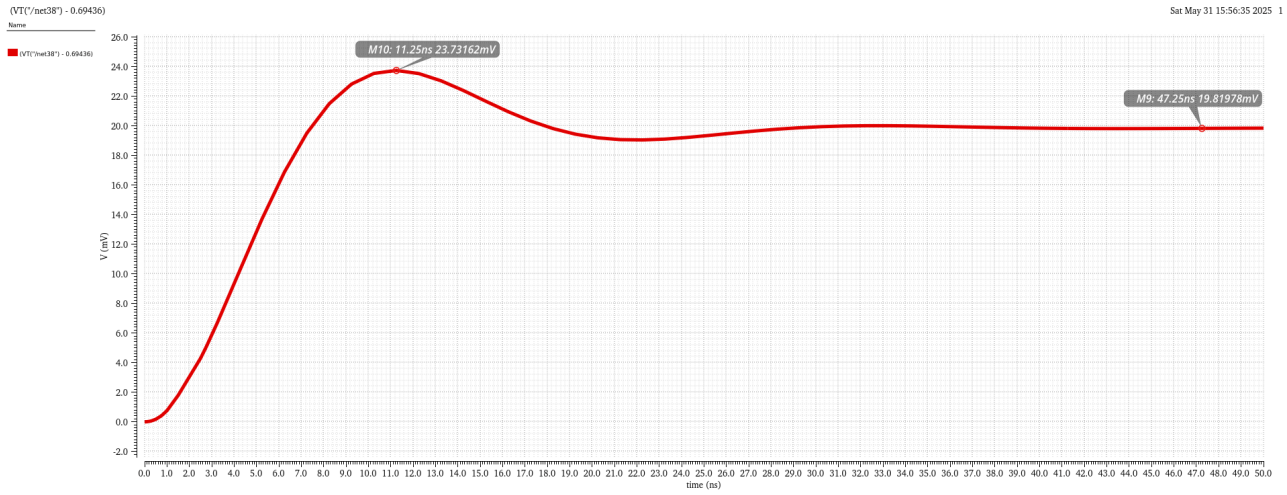

Figure 23: Step Response

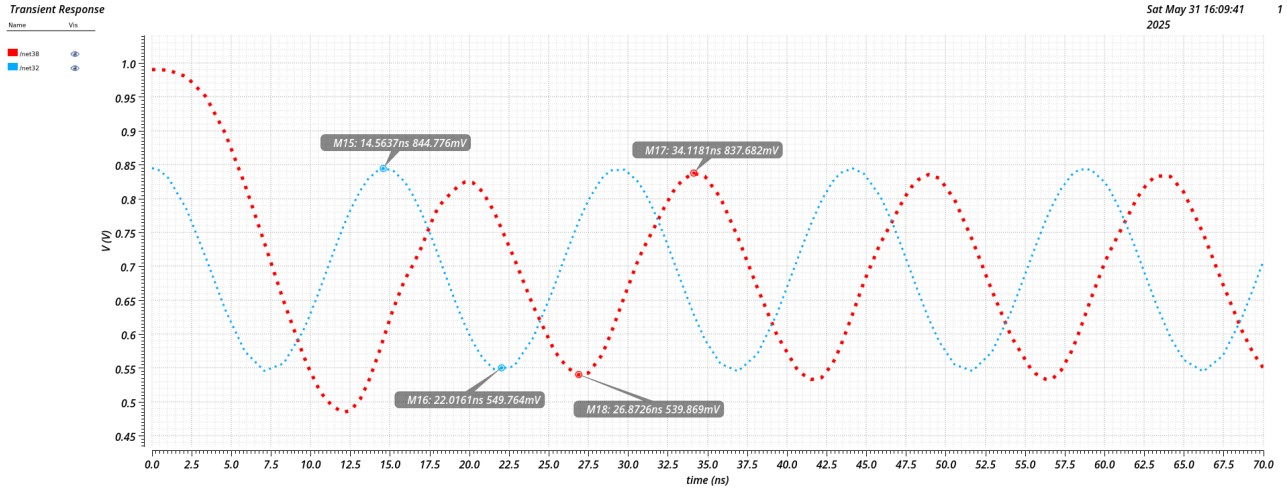

Figure 24: Sine response at frequency $\omega_{3\text{dB}}$

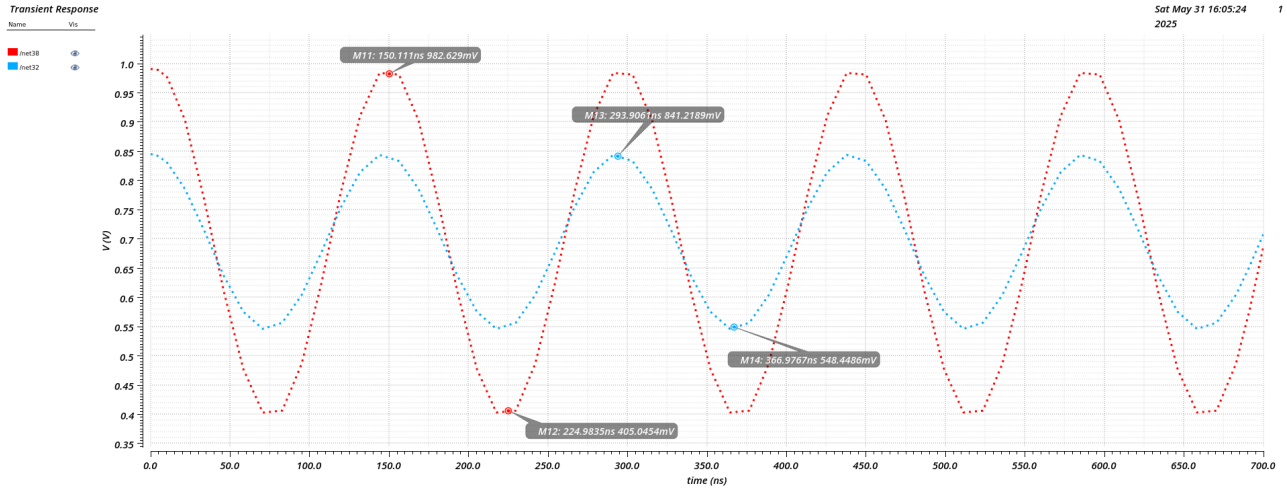

Figure 25: Sine response at frequency $\omega_{3\text{dB}}$ /10

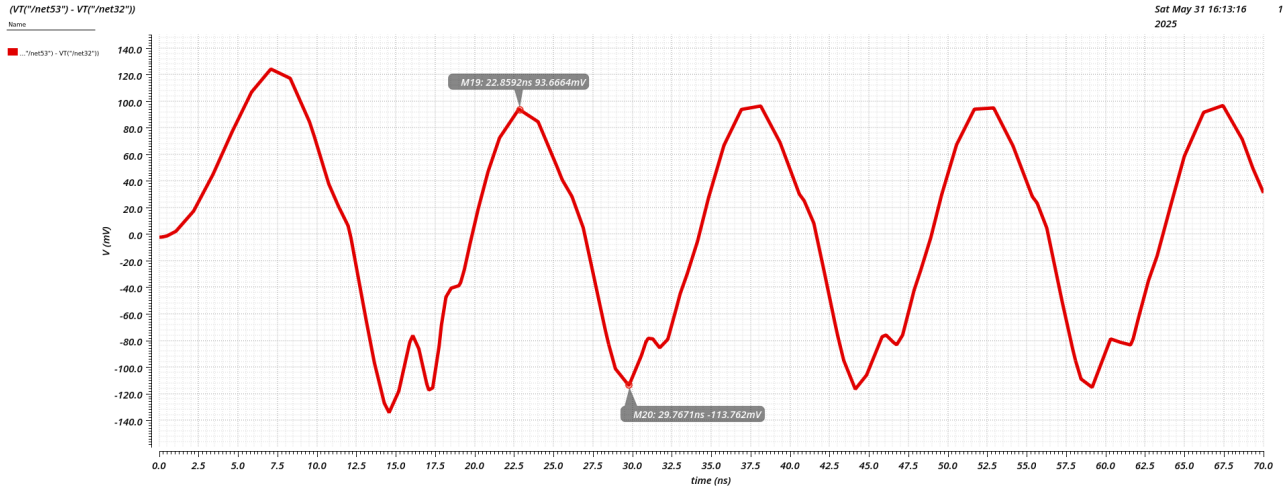

Figure 26: Difference between input voltages at freq $\omega_{3\text{dB}}$

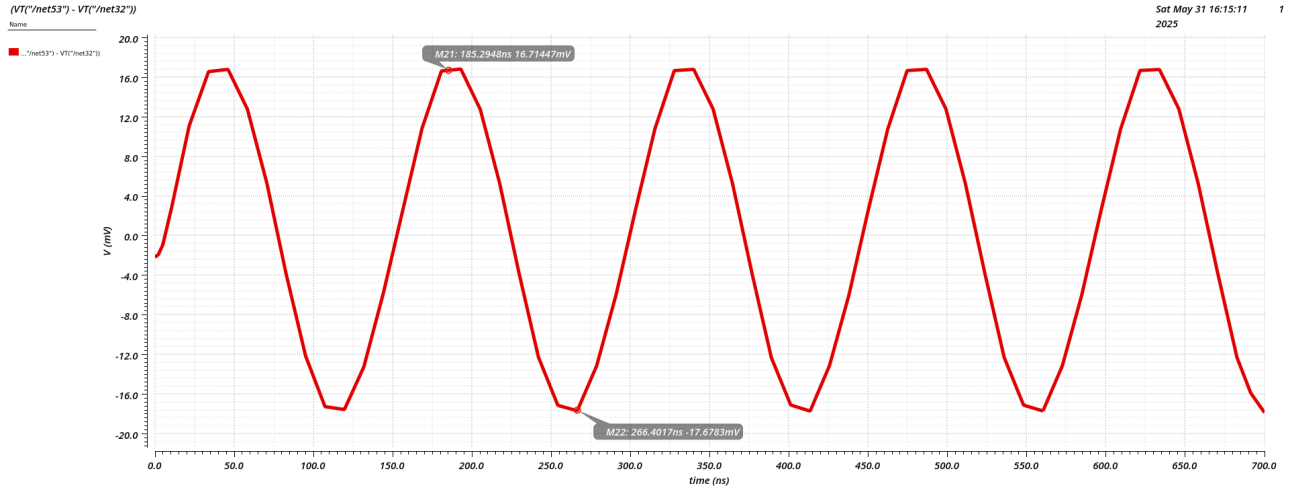

Figure 27: Difference between input voltages at freq $\omega_{3\text{dB}}$ /10

Verification with Expected Values

Open-loop Output Resistance (R_{out})

$$R_{\text{out}} = \left(\frac{7.71}{0.394 \times 0.302}\right) \parallel \left(\frac{5.93}{0.317 \times 0.204}\right) \text{k}\Omega$$

$$= \left(\frac{7.71}{0.119}\right) \parallel \left(\frac{5.93}{0.0647}\right) \text{k}\Omega = 64.79\,\text{k}\Omega \parallel 91.61\,\text{k}\Omega$$

$$R_{\text{out}} = \frac{64.79 \times 91.61}{64.79 + 91.61} = \frac{5939.1}{156.4} \approx \boxed{37.97\,\text{k}\Omega}$$

Open-loop Differential-mode Gain (A_{OL})

$$A_{\text{OL}} = g_{mp} \cdot R_{\text{out}} = 7.83 \times 37.97 = \boxed{297.28}$$

$$A_{\text{OL,dB}} = 20 \cdot \log_{10}(297.28) \approx \boxed{49.46\,\text{dB}}$$

Closed-loop Effective Output Resistance ($R_{\text{out,eff}}$)

$$R_{\text{out,eff}} = R_{\text{out}} \parallel 100\,\text{k}\Omega = \frac{37.97 \times 100}{37.97 + 100} = \frac{3797}{137.97} \approx \boxed{27.52\,\text{k}\Omega}$$

Effective Open-loop Gain in Closed-loop Configuration (A)

$$A = g_m \cdot R_{\text{out,eff}} = 7.83 \times 27.52 \approx \boxed{215.39}$$

Loop Gain at Feedback Factor $\beta = 0.5$

$$T = \beta \cdot A = 0.5 \times 215.39 = \boxed{107.695}$$

$$\text{Loop gain in dB} = 20 \cdot \log_{10}(107.695) \approx \boxed{40.64\,\text{dB}}$$

—

Steady-state Error for 10 mV Input Step

$$e_{\text{ss}} = \left(10 - \frac{A}{1 + \beta \cdot A} \cdot 10\right) \text{mV} = \left(10 - \frac{215.39}{1 + 0.5 \cdot 215.39} \cdot 10\right) \text{mV}$$

$$= \left(10 - \frac{215.39}{108.695} \cdot 10\right) = (10 - 1.982 \cdot 10) = \boxed{0.18\,\text{mV}}$$

—

Common-mode Gain Approximation

$$A_{\text{CM}} \approx \frac{g_{mp}}{g_{mn} \cdot (1 + 2 g_{mp} R_{\text{CM}})} \quad \text{where } R_{\text{CM}} = \frac{11.32}{0.506 \times 0.580} = \frac{11.32}{0.2935} \approx \boxed{38.57\,\text{k}\Omega}$$

$$A_{\text{CM}} \approx \frac{7.83}{4.03 \cdot (1 + 2 \cdot 7.83 \cdot 38.57)} = \frac{7.83}{4.03 \cdot (1 + 604.43)} = \frac{7.83}{4.03 \cdot 605.43} = \frac{7.83}{2441.89} \approx \boxed{0.00321}$$

$$A_{\text{CM,dB}} = 20 \cdot \log_{10}(0.00321) \approx \boxed{-49.87\,\text{dB}}$$

—

CMRR (Common-Mode Rejection Ratio)

$$\text{CMRR} = \frac{A_{\text{OL}}}{A_{\text{CM}}} = \frac{297.28}{0.00321} \approx 92600$$

$$\text{CMRR}_{\text{dB}} = 20 \cdot \log_{10}(92600) \approx \boxed{99.34\,\text{dB}}$$

—

Input Voltage Difference Analysis

We know that in a negative feedback system:

$$A(V_{in+} - V_{in-}) = V_{out}$$

So, for the closed-loop case:

$$V_{\text{diff}} = \frac{V_{\text{out}}}{A} = \frac{695\,\text{mV}}{215.39} \approx 3.23\,\text{mV}$$

However, from the simulation waveform, it is clear that the actual differential voltage is significantly higher. Let's consider the case when the input frequency is $\omega_{3\,\text{dB}}/10$. At this frequency, the gain remains nearly equal to the DC gain (i.e., 215), but the phase deviates slightly—specifically, by:

$$\phi \approx \tan^{-1}(0.1) \approx 5.7^\circ$$

This phase shift is the key reason why the amplitude of $V_{in+} - V_{in-}$ appears significantly larger than the expected 3–4 mV.

To understand this, consider subtracting two sine waves of equal amplitude A, but with a phase difference ϕ. The result is a sine wave of amplitude:

$$V_{\text{diff, peak}} = 2A \cdot \sin\left(\frac{\phi}{2}\right)$$

From the plots, the measured phase difference between V_{in+} and V_{in-} is approximately 6.5°. Assuming each has an amplitude of 150 mV:

$$V_{\text{diff, peak}} = 2 \cdot 150 \cdot \sin\left(\frac{6.5^\circ}{2}\right) \approx 2 \cdot 150 \cdot \sin(3.25^\circ) \approx 17\,\text{mV}$$

This matches well with the amplitude seen in the simulation and explains why the observed $V_{in+} - V_{in-}$ waveform has a much larger magnitude than the ideal calculated value.

Now, let us consider what happens at the actual 3 dB bandwidth point ($\omega = \omega_{3\,\text{dB}}$). At this frequency:

$$|A(j\omega)| = \frac{A_0}{\sqrt{2}} \approx \frac{215}{\sqrt{2}} \approx 152.01$$

So, using:

$$V_{\text{diff}} = \frac{695\,\text{mV}}{152.01} \approx 4.57\,\text{mV}$$

Also, the phase shift at this frequency is:

$$\phi = \tan^{-1}(1) = 45^\circ$$

Now, the two input signals are no longer in perfect phase. Suppose:
- $V_{in+} = 150\,\text{mV}$ - $V_{in-} = 154\,\text{mV}$ - Phase difference $\phi = 45^\circ$
The magnitude of their difference is:

$$V_{\text{diff, peak}} = \sqrt{V_{in+}^2 + V_{in-}^2 - 2V_{in+}V_{in-}\cos(\phi)}$$

$$= \sqrt{(150)^2 + (154)^2 - 2 \cdot 150 \cdot 154 \cdot \cos(45^\circ)}$$

$$= \sqrt{22500 + 23716 - 46200 \cdot 0.7071} \approx \sqrt{46216 - 32676} \approx \sqrt{13540} \approx 116.4\,\text{mV}$$

This value represents the peak amplitude of the differential signal when considering both amplitude mismatch and phase difference at the 3 dB point, and is pretty close to what we get from the graph actually too.

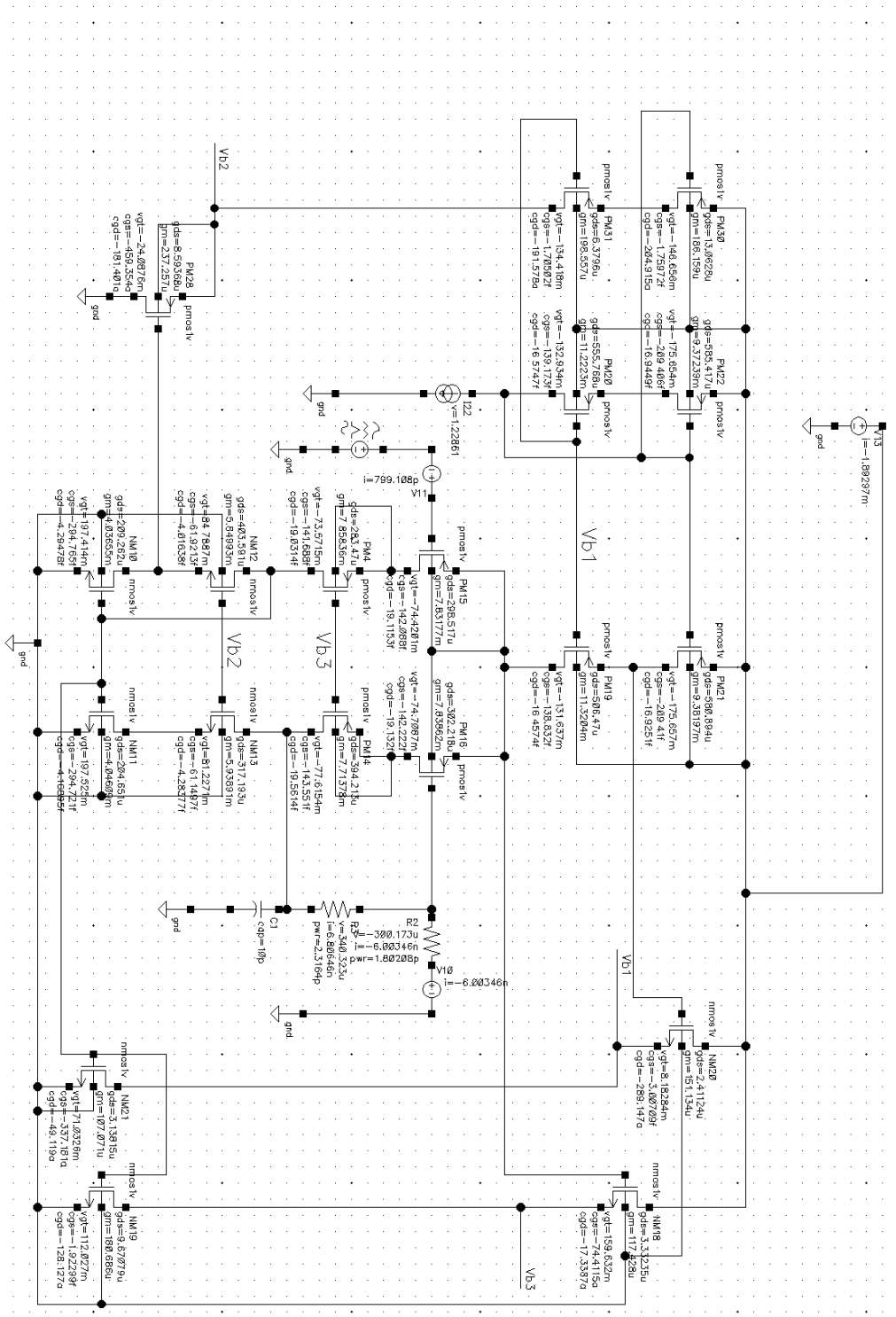

Figure 28: Full Circuit

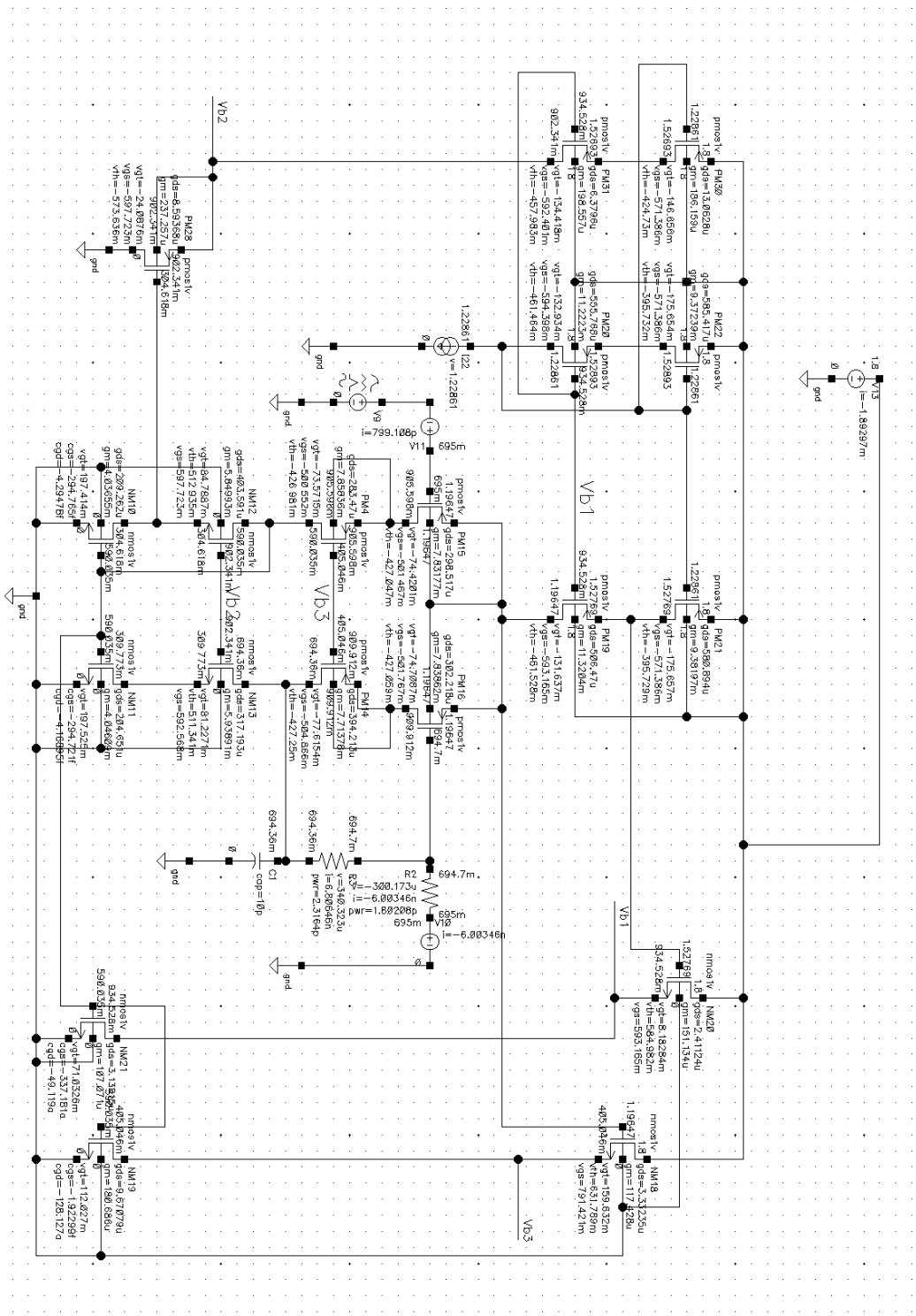

Figure 29: Full Circuit with vgs, vth and node voltages

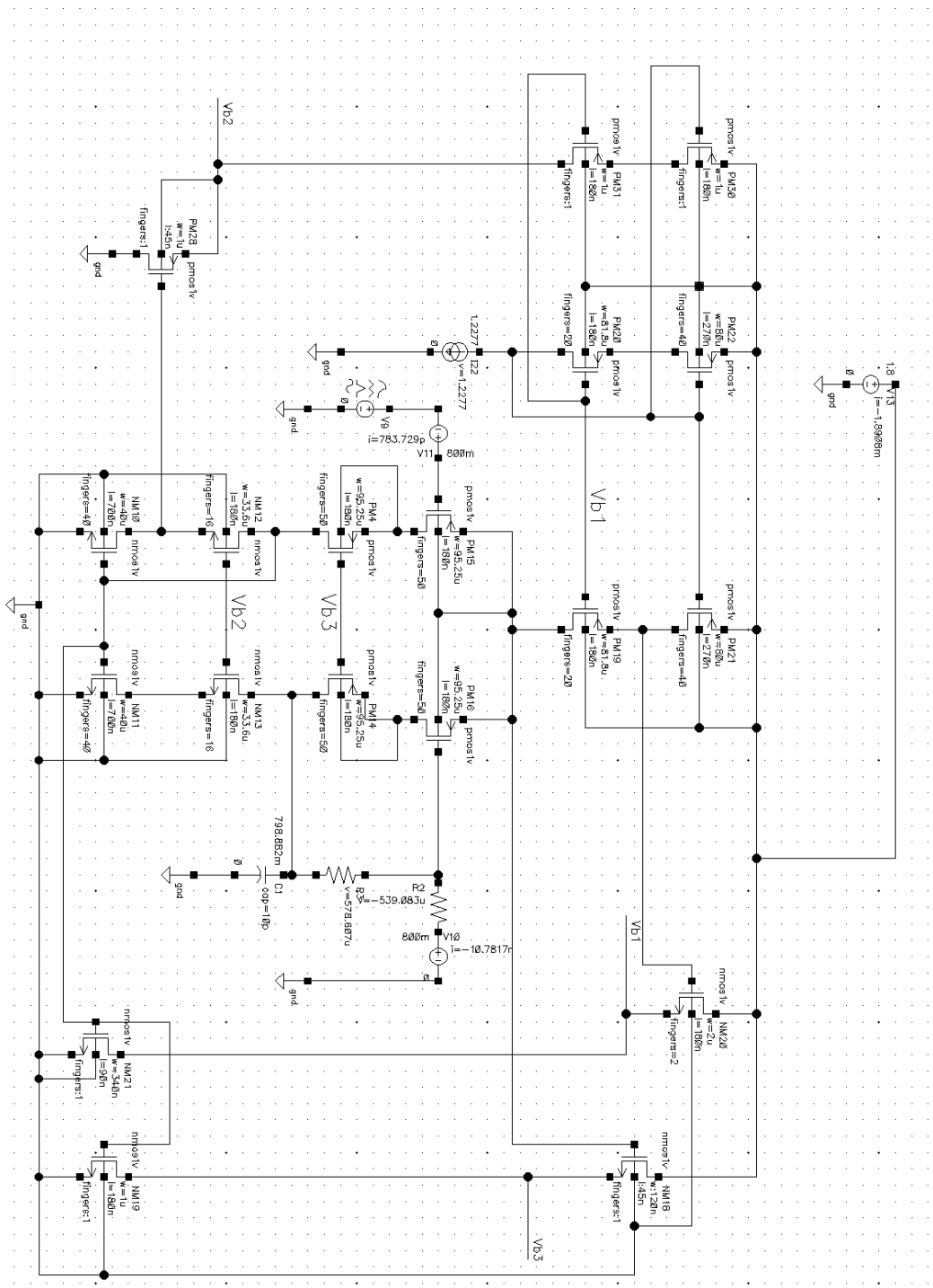

Figure 30: Full Circuit with sizes