CHAPTER

4

BASIC MIPS IMPLEMENT

TRUONG DAI HOC KHOA HOC TU NHIEN
KHTN
TP. HO CHI MINH

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KHOA CÔNG NGHỆ THÔNG TIN
TRƯỜNG ĐẠI HỌC KHOA HỌC TỰ NHIÊN

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PREREQUITES

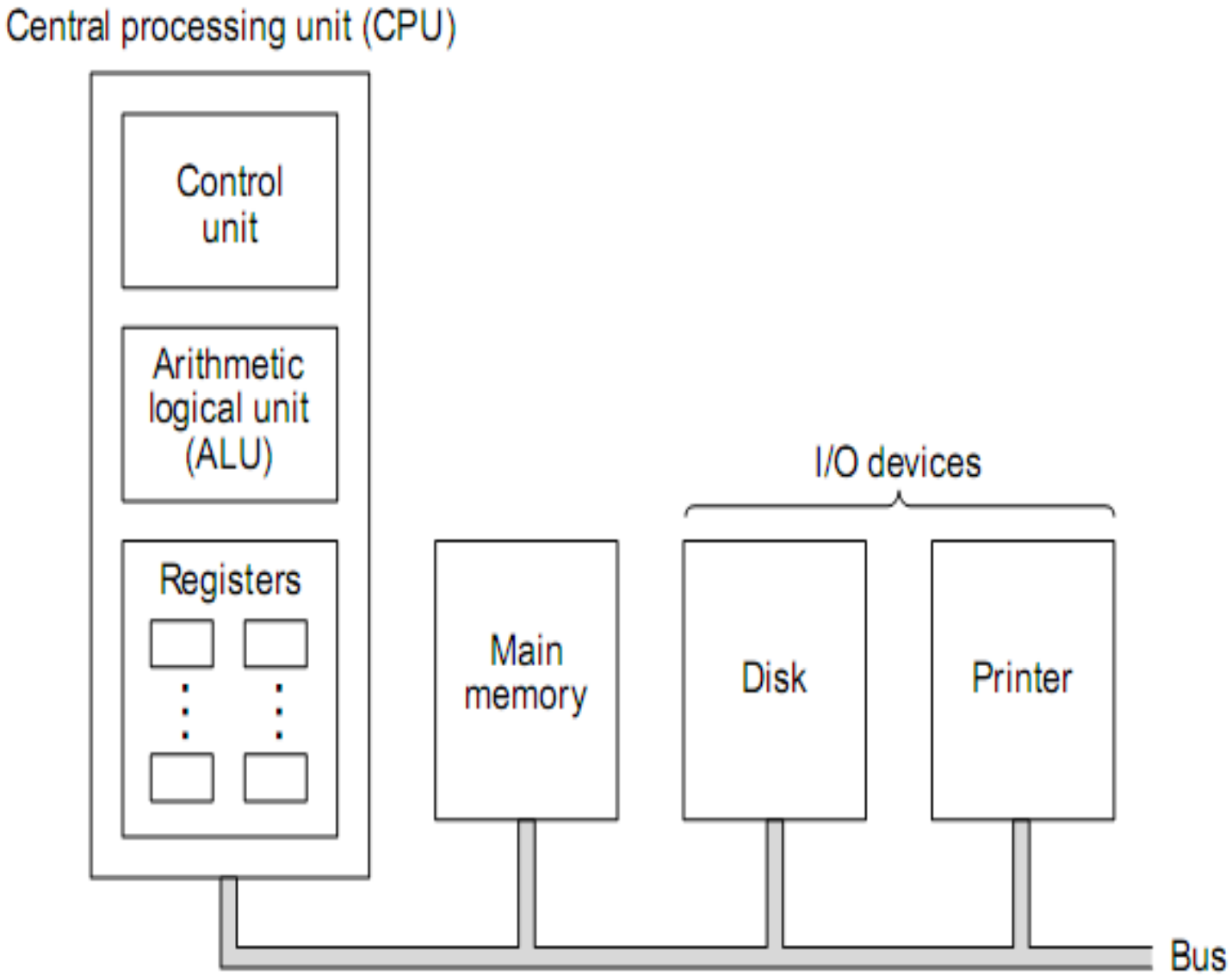
- Install Procsim software already

REMIND

- Inside a CPU
- MIPS-32 bits operations

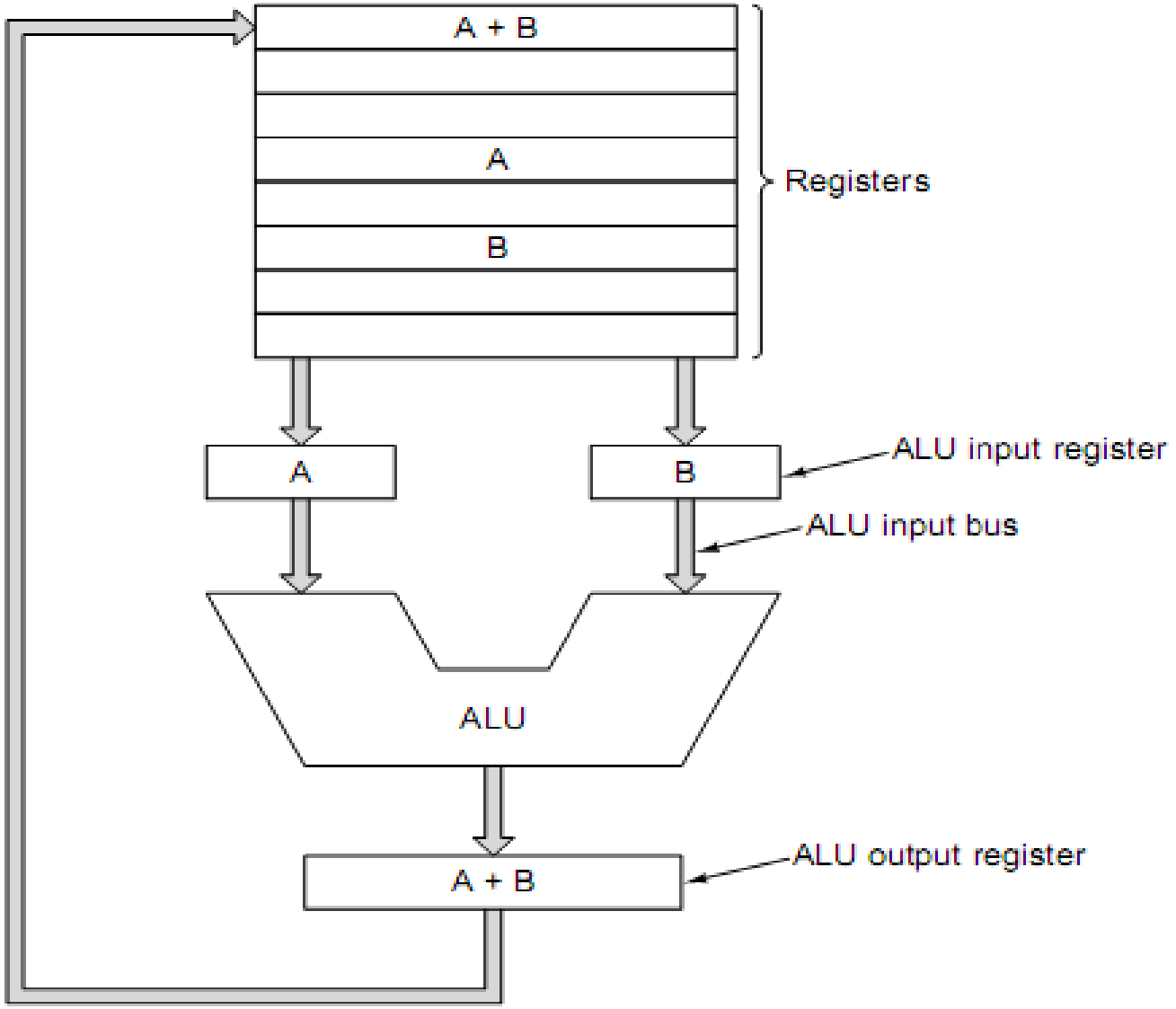
REMIND

- Control Unit
- Datapath
  - ALU (Arithmetic Logical Unit)
  - Registers



REMIND

- ALU read operand from register or load from memory
- ALU executes the operation which the CU directed
- Store the result in memory or write back to the register



The data path of a typical Von Neumann machine

What will you learn?

- Processor Implementation Styles
- Abstract view of MIPS subset
- Building Datapath
- ALU Control
- Control Unit

- Design Main Control Unit
- Multi-cycle approach
- Pipelined approach (additional)

Processor Implementation Styles

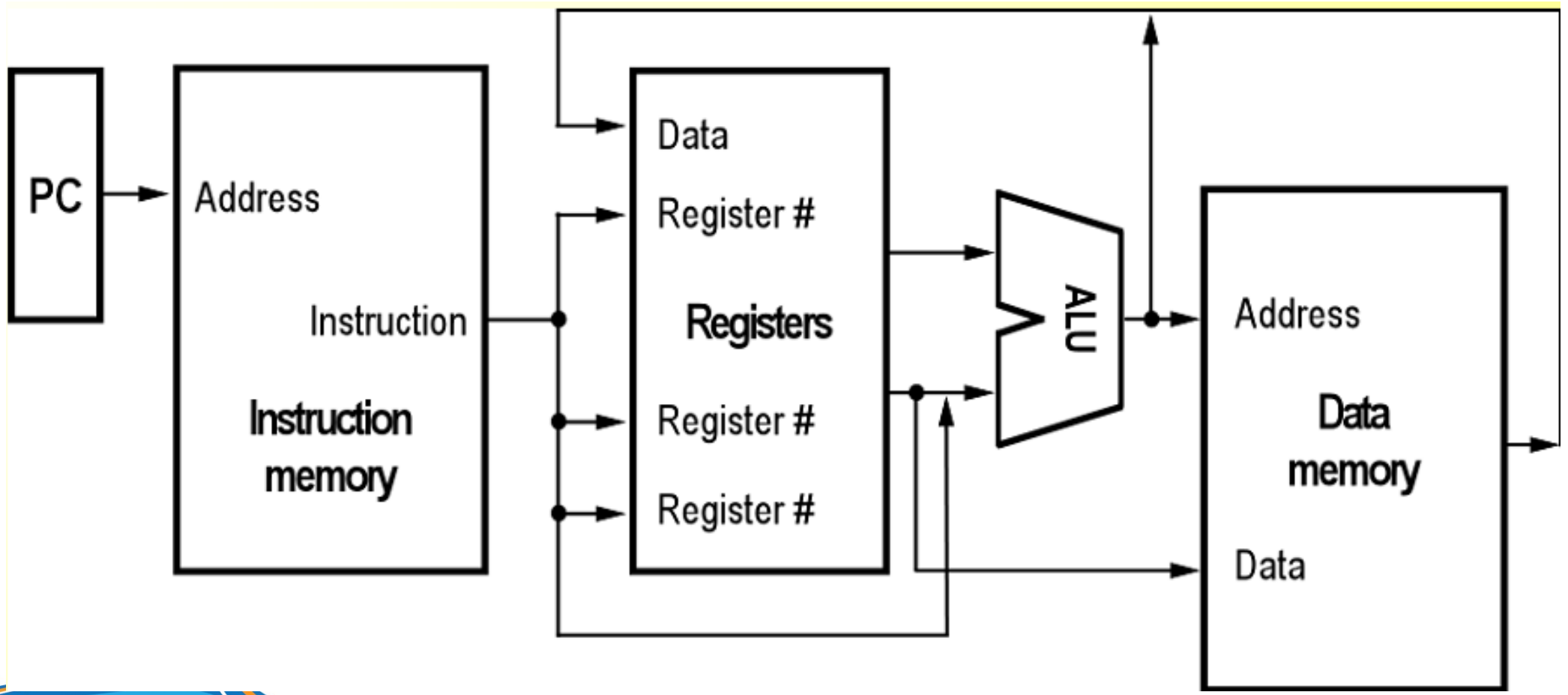
- Single Cycle
- Multi-cycle
- Pipelining

Single Cycle approach

- Execute each instruction in 1 clock cycle
- The clock cycle must have the same length for every instruction
- Therefore, the clock cycle equal to the longest possible path in the processor

→ Inefficient

Abstract view of MIPS subset



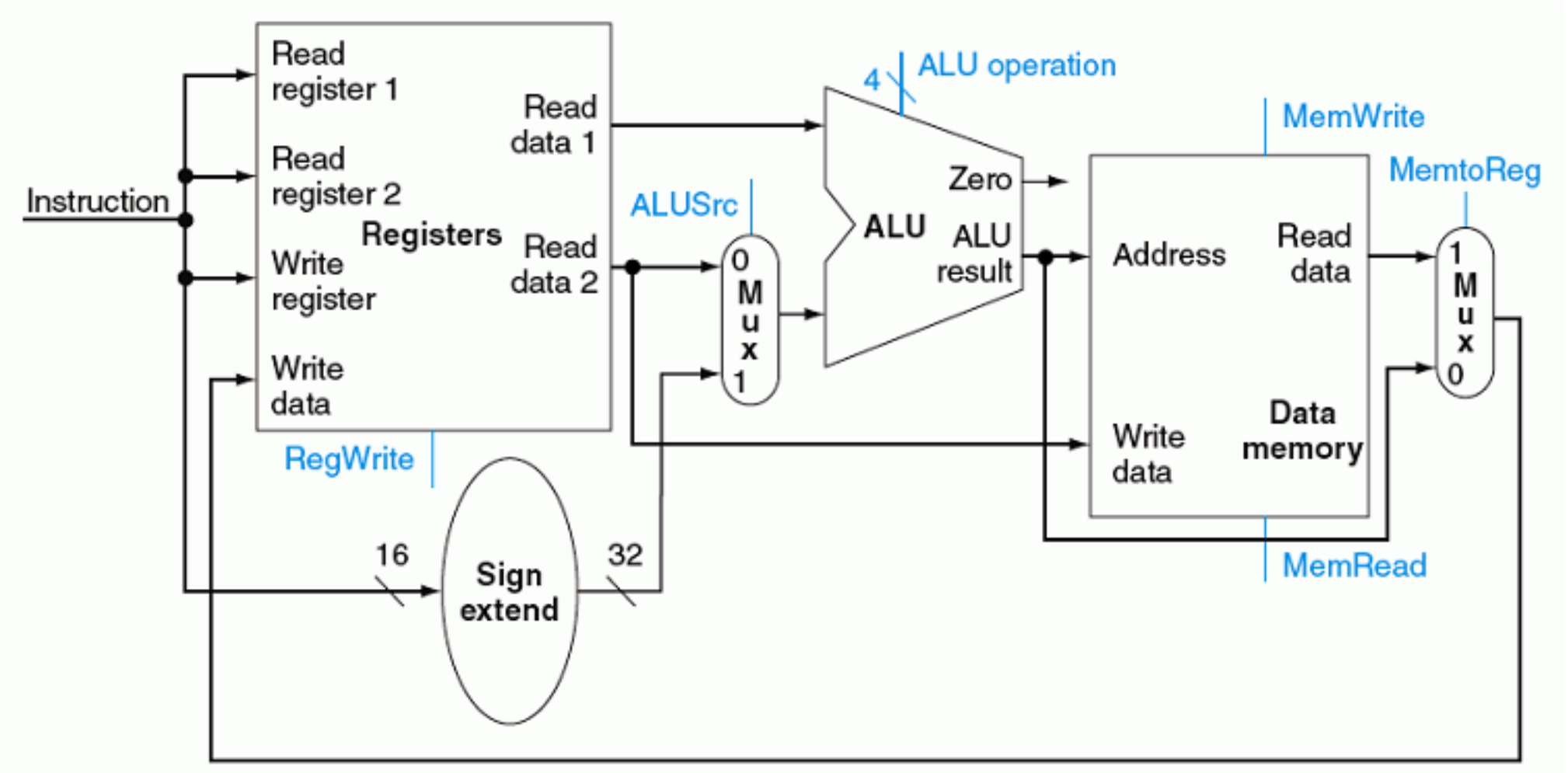
MIPS Instructions Format

Name	Fields						Comments
Filed size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instruction 32 bits
R-format	op	rs	rt	rd	sham t	funct	Arithmetic instruction format
I-format	op	rs	rt	Address/ immediate			Transfer, branch, immediate format
J-format	op	Target address					Jump instruction format

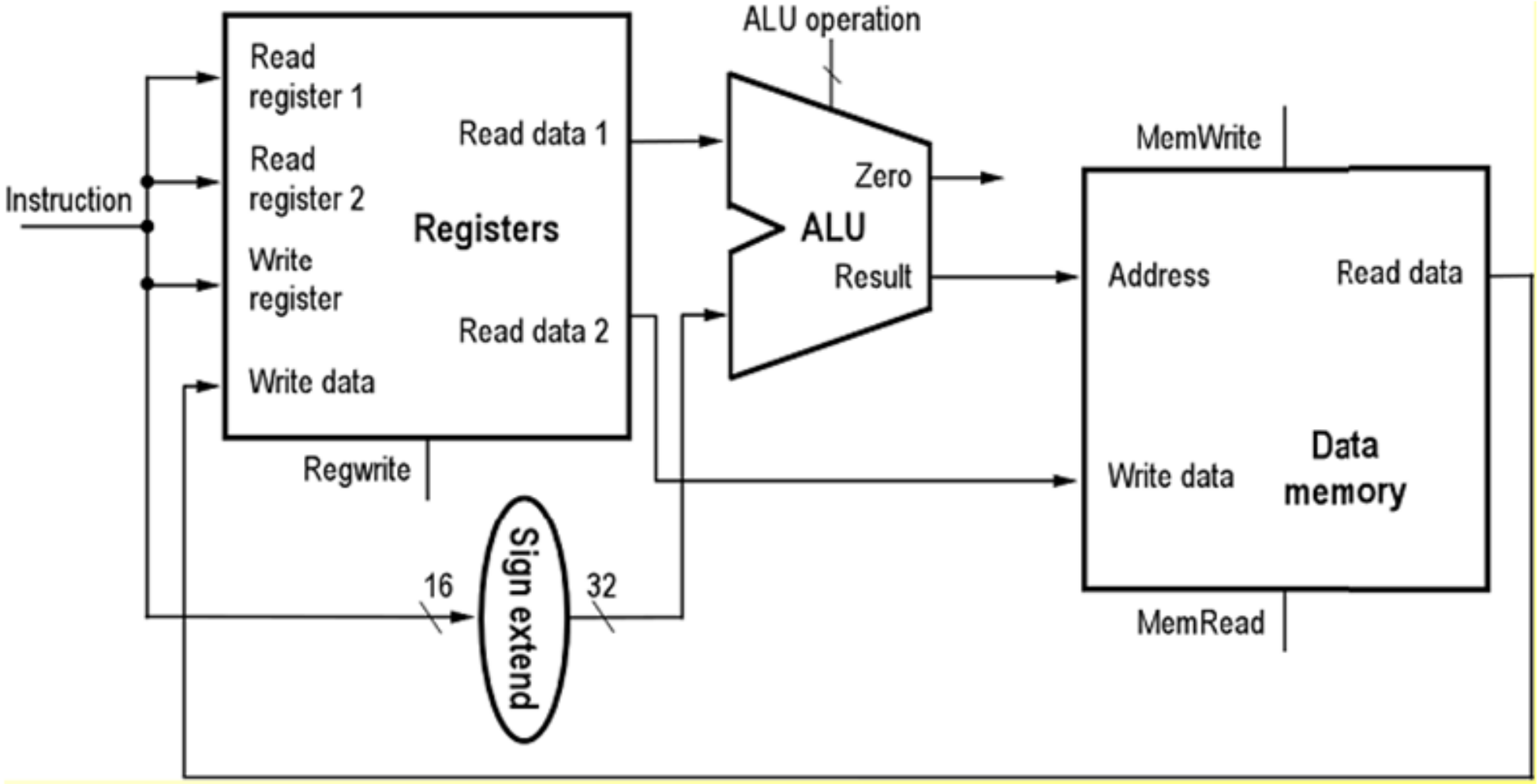
Building Datapath

- A unit used to operate or hold data in the processor
- In the MIPS implementation, the Datapath includes the instruction and data memories, the register files, the ALU, and the adders

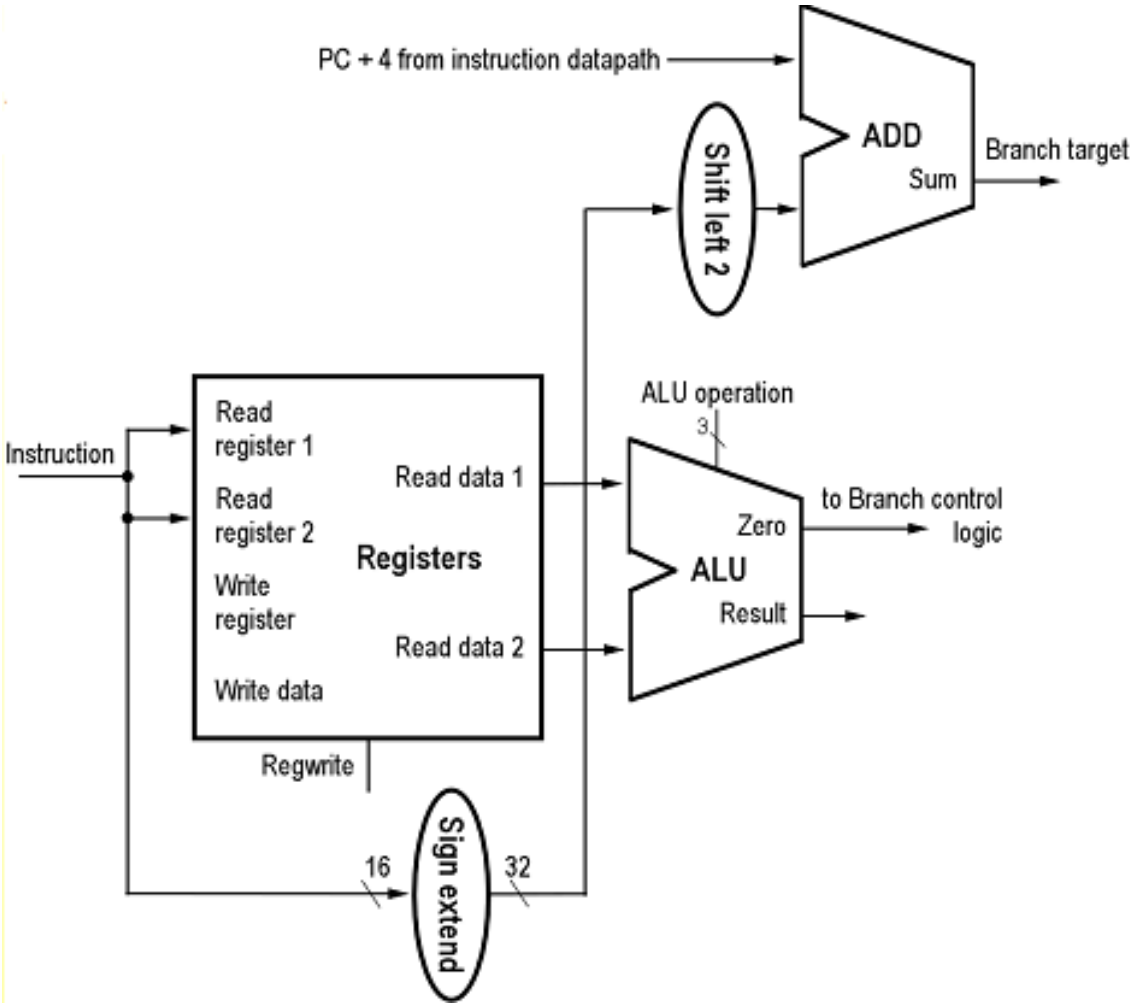
Building Datapath: R-format



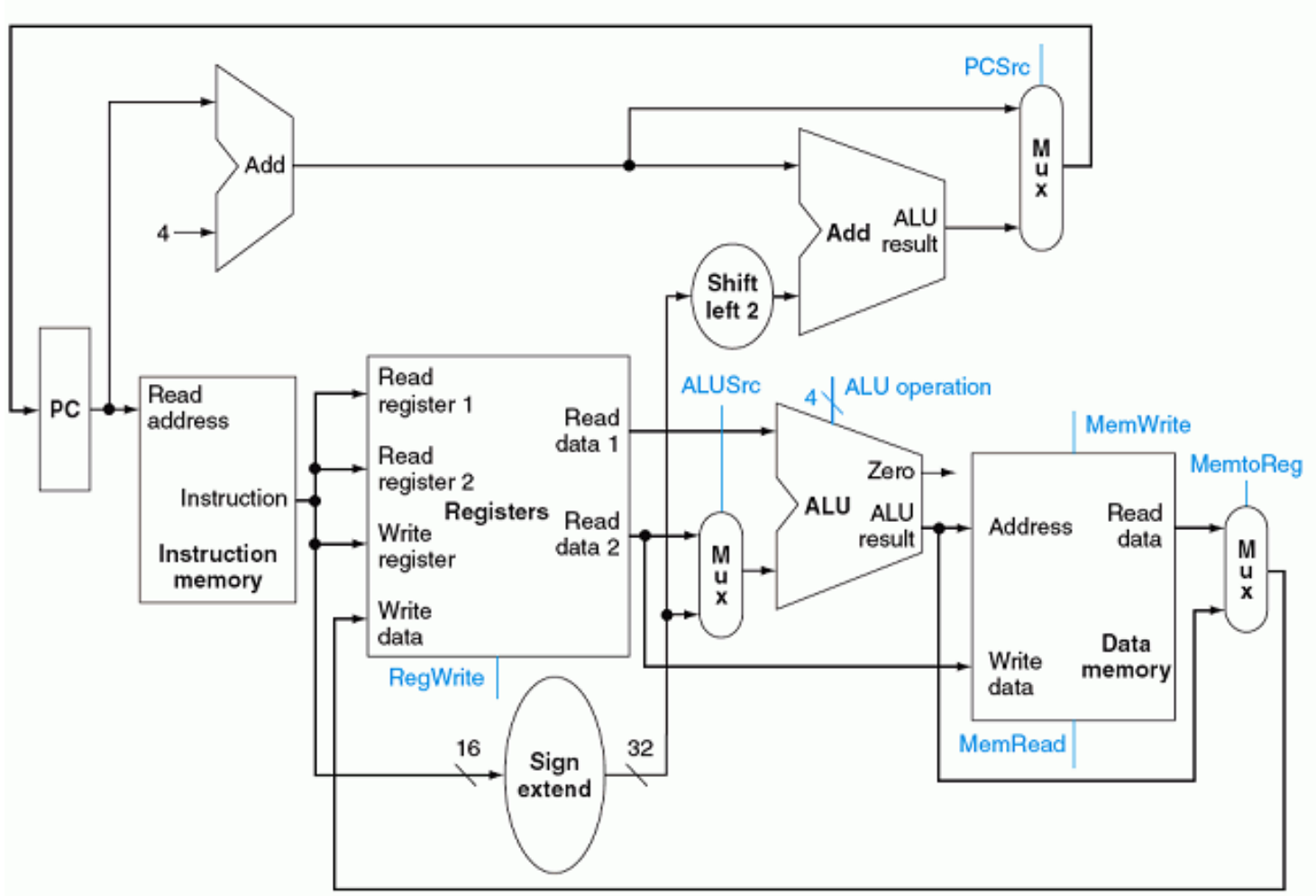
Building Datapath: I-format: lw, sw



Building Datapath: I,J-format: beq, j

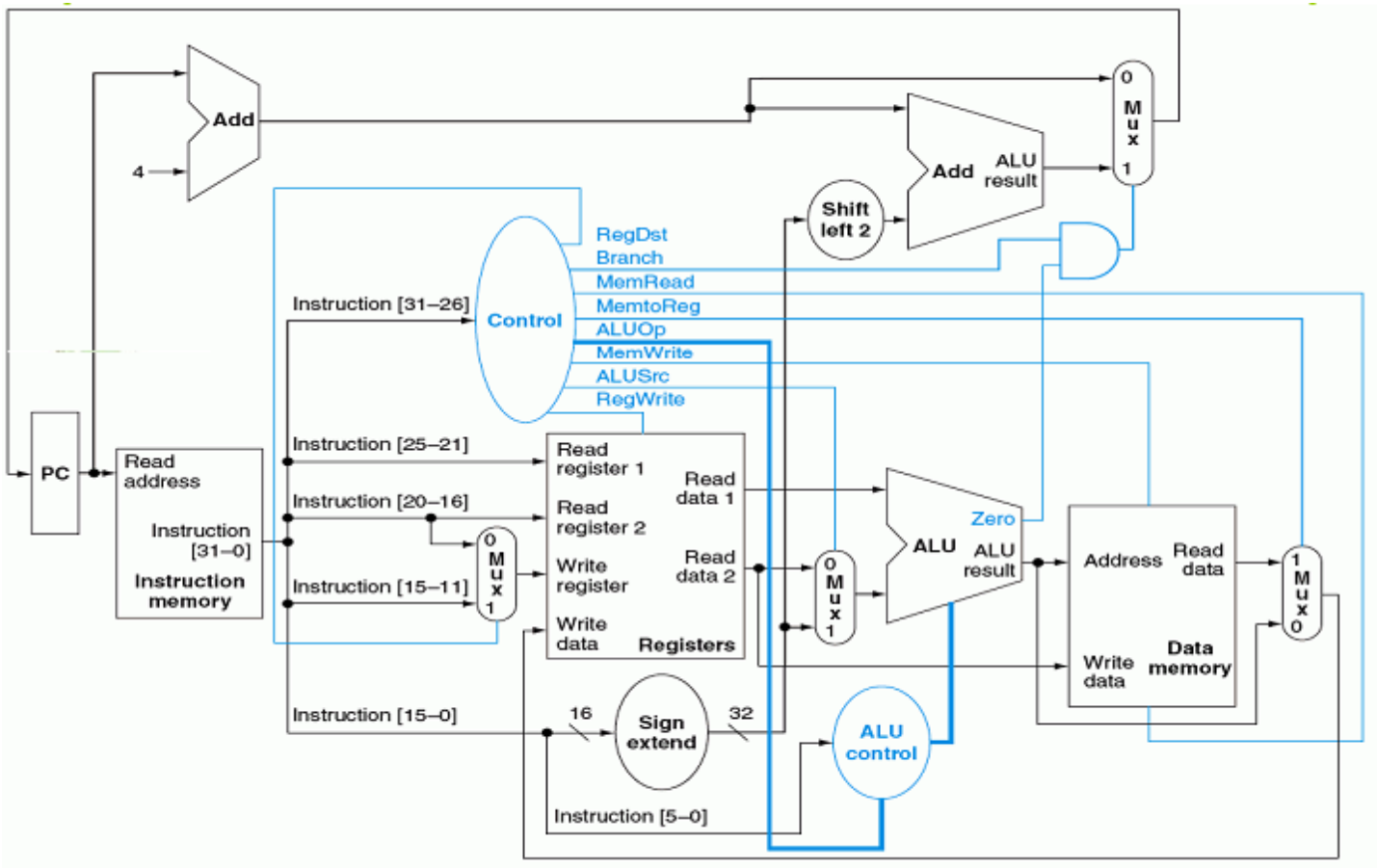


Building Datapath: R,I,J-format



Control Unit

ALU receives the directives from the control unit (ALU Control)



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Control Unit: Control Signal

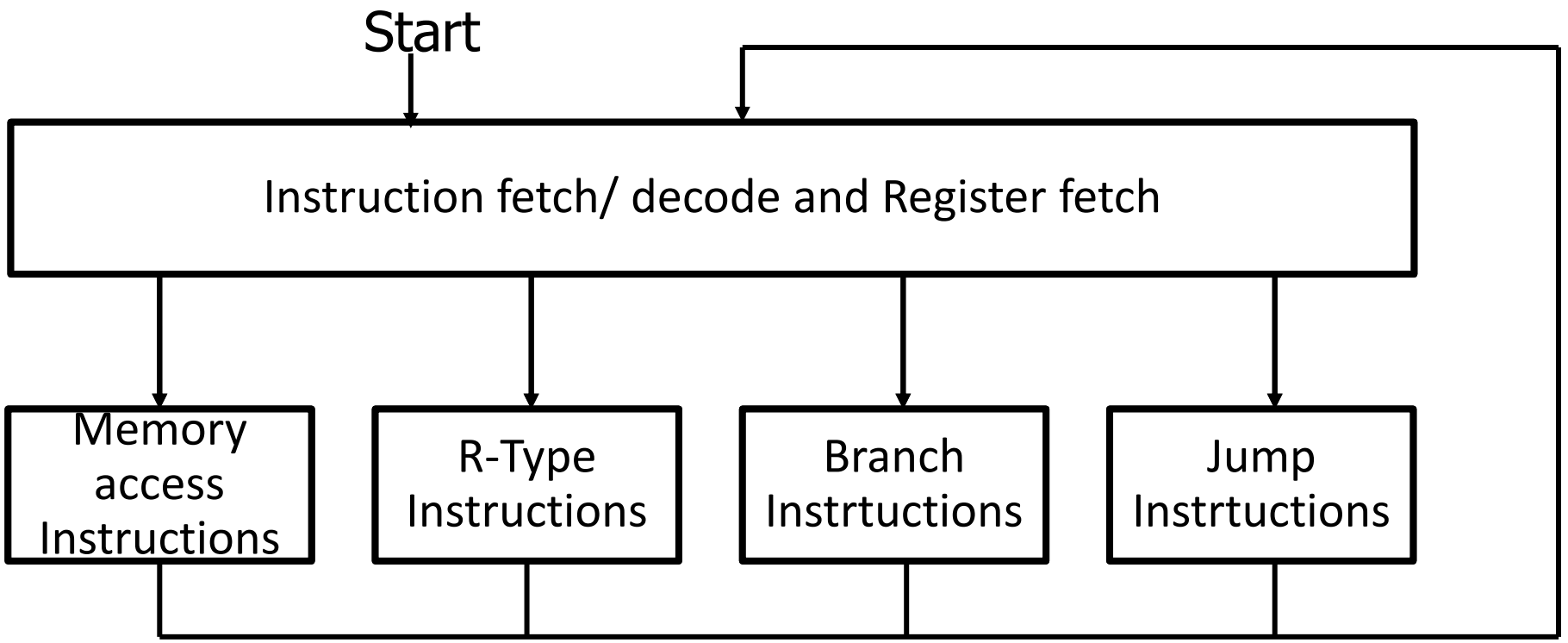
Signal Name	Effect when desserted	Effect when asserted
RegDst	The register destination number for the Write-register comes from the rt field (bits 20-16)	The register destination number for the Write register comes from the rd field (bits 15-11)
RegWrite	None	
AlLUSrc	The second ALU operand comes from the second register file output (Read data 2)	The second ALU operand is the sign-extended, lower 16 bits of the instruction
PCSrc	The PC is replaced by the output of the adder that computes the value of PC + 4	The PC is replaced by the output of the adder that compute the branch target
MemRead	None	Data memory contents designated by the address input are put on the first Read-data output
MemWrite	None	Data memory contents designated by the address input are replaced by the value of the Write-data input
MemtoReg	The value fed to the register Write data input comes from the ALU	The value fed to the register Write-data input comes from the data memory

Multi-cycle Approach

- Break up the instruction cycle to multiple step (perform 1 step/ clock cycle)
- Allow different instructions to be executed in different number of cycles
- Reuse expensive hardware on multiple cycles (ALU, memory)

→ Only one instruction can be executed at the same time

Multi-cycle Approach: Execute FSM



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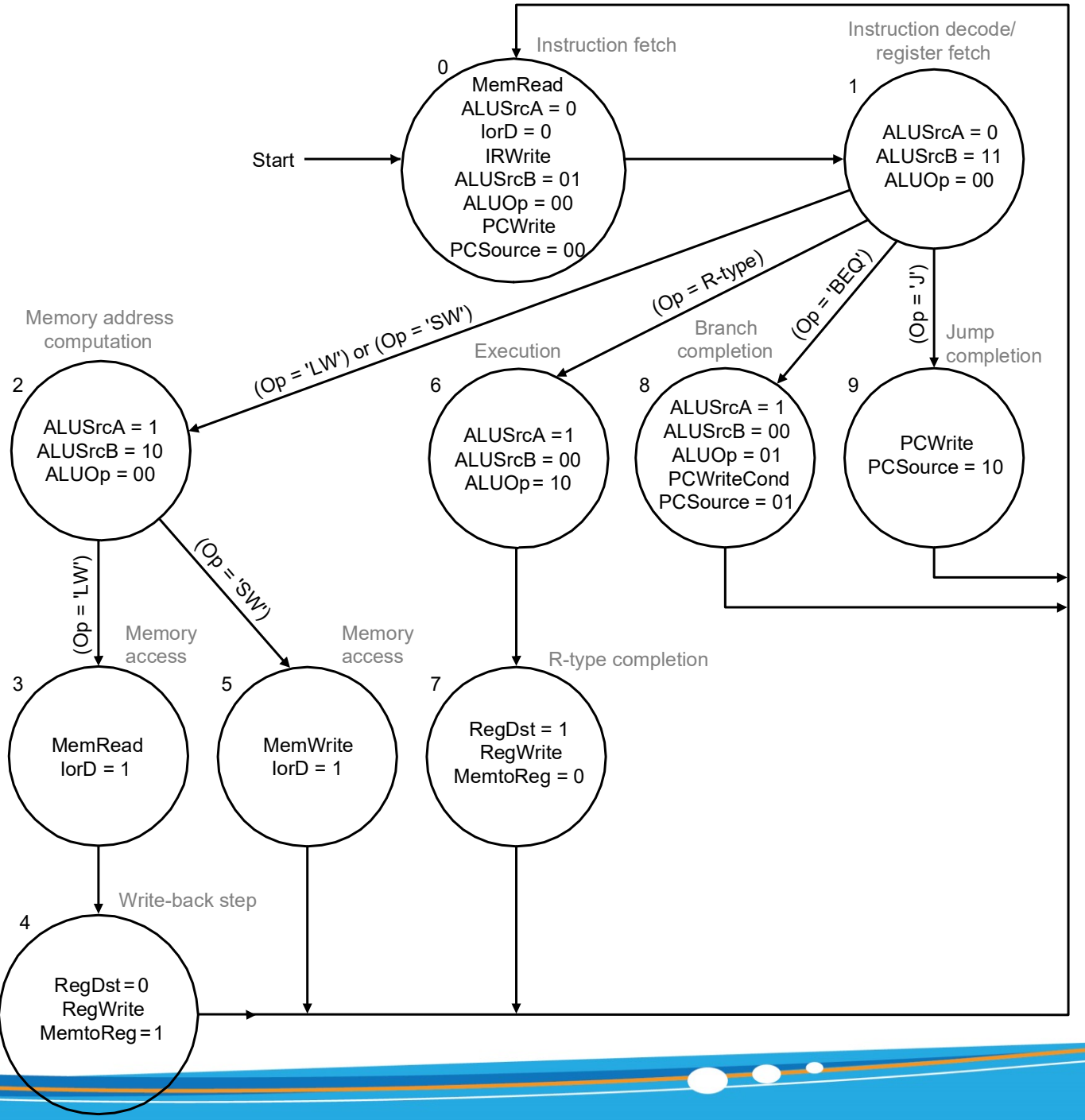
Multi-cycle: Complete Controller FSM

Execute

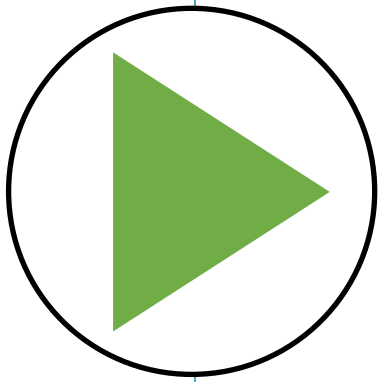
Memory access

Write Back



SIMULATE MIPS R2000 PROCESSOR

- Please watch the video besides



Pipelining: (modern approach)

- Multiple instructions are overlapped in execution
- Fixed the number of clock cycles/ instruction
- Advantage
  - The cycle time of the processor is reduced.
  - It increases the throughput of the system
  - It makes the system reliable.
- Disadvantage
  - The design of pipelined processor is complex and costly to manufacture.
  - The instruction latency is more