THE IMAGINATION UNIVERSITY PROGRAMME

Overview of the RVfpga Materials

Custom Edition

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Purpose of this Custom Update

This update is intended to broaden the scope of the RVfpga course materials to align with the University of Sheffield's curriculum and teaching requirements. It includes support for the Nexys Video FPGA board. In addition, the adaptation process for this board is presented as a key case study, allowing students to learn how an RVfpga design can be migrated to any FPGA board. The case also illustrates how to configure and debug not only the HDL design but also the surrounding tools, providing practical insight into potential issues and their solutions.

The update also introduces enhancements to the learning framework. Students are guided on how to use Git and GitHub, how to extend the RVfpga platform, and how to address common challenges that may arise during development. Furthermore, in the Nexys Video documentation, adjustments have been made to account for differences caused by updates to external tool versions compared with the original release.

All updates are highlighted with this special background.

Update History:

- Version 1.0 (Released November 2020):
  - Original release of the RVfpga course.

- Version 1.1 (Released June 2021):
  - Added description of Labs 11-20 in Lab 0.
  - Updated SweRVolf version to 0.7.3 and Verilator version to 4.106.
  - Added Boot ROM initialization program.
  - Added new Figure 1 and Table 1 in the GSG describing the RVfpga System
  - Added a UART exercise to Lab 10.
  - Fixed some typos.

- Version 2.0 (Released November 2021):
  - Added Labs 11-20: documents, figures, software sources, exercises and solutions.
  - Extended the slides with the new labs.
  - Added some minor things in the GSG and Labs 0-10, and fixed some typos.

- Version 2.1 (Released February 2022):
  - Renumbered Labs 1-5: moved Lab 1 to Lab 5 and renumbered Labs 2-5 as 1-4.

- Version 2.2 (Released May 2022):
  - Added *Workshop_Guide* document, which gives a guideline of a one-day workshop on RVfpga.
  - Added sources (such as some PlatformIO projects and Verilator binaries) required for the one-day workshop.
  - Added *ReadmeFirst* document (the one that you are reading right now), which enables ease of use for everyone. Removed Lab 0; most of this material is moved to the *ReadmeFirst* document.
  - Factored all the documents (GSG, slides, the IUP brochure, license agreement, and workshop guide) into a Documents folder.
  - Updated IUP brochure and license agreement.
  - Modifications in the slides.
  - Added some minor things in the GSG and Labs 1-20, and fixed some typos.

- Version 3.0 (Released Dec 2023):
  - Added support for VeeR EL2, which is smaller than the VeeR EH1 core. (The course materials based on the VeeR EH1 core and VeeRwolf SoC are also provided in this package)
  - Added support for low-cost boards, such as Real Digital's Boolean board and Digilent's Basys 3 board.

  - Added support for new simulation tools: RVfpga-ViDBo and RVfpga-Pipeline.
  - Added new documents (GSG and Labs) for each of the new configurations supported: Basys3 and Boolean boards, as well as the original Nexys A7 board (with and without DDR memory being used).
  - Added support for Catapult SDK (only for VeeR EL2).
  - Added Ubuntu 22.04 Virtual Machine with all the tools installed and ready to use.

- Custom Branch 3.1 (University of Sheffield, Released Oct 2025):
  - Added support for Nexys Video board, including updated lab content.
  - Added tutorial on adapting RVfpgaEL2 to new devices.
  - Guide to Using Git and GitHub

0. PREFACE

This RVfpga Course in Computer Architecture provides hands-on understanding of a commercial RISC-V processor, RISC-V SoC, and the RISC-V ecosystem. Professor David Patterson, who shared the ACM Turing Award with John Hennessy for their contribution to RISC, says:

"RISC-V is transforming processor design and software/hardware co-design. RISC-V is an open architecture, which enables open-source hardware implementations. This new option means that software development can occur alongside hardware development, accelerating the design path. The RVfpga course enhances the understanding of not only RISC-V processors but also the RISC-V ecosystem and RISC-V SoCs. This course provides a deep understanding of an industrial-strength processor architecture and system of increasing popularity, which will prove useful throughout their academic and industry careers."

This 3.0 version of RVfpga (RVfpga v3.0) includes materials that use the VeeR EL2 core and SoC. It also includes the previous materials from RVfpga v2.2 (renamed RVfpgaEH1 in this package), that targeted the VeeR EH1 processor. RVfpga v3.0 is an extension of the following courses:

- RVfpga v2.2, released in May 2022, and
- EdX RVfpga course, released on Aug 2023 (https://www.edx.org/es/learn/computer-programming/the-linux-foundation-computer-architecture-with-an-industrial-risc-v-core)

Specifically, the RVfpga v3.0 course shows how to target a VeeR EL2 based system-on-chip (SoC) to low-cost FPGA boards, such as the Basys 3 board and the Boolean Board, as well as the Nexys A7 FPGA board that was used in RVfpga v2.2. The course can also be completed only in simulation; for that purpose, several simulation tools are provided which enable the user to simulate the system at different levels: from a Boolean/Nexys A7/Basys 3 virtual board down to the VeeR EH1/EL2 pipeline.

This RVfpga package includes materials that target either VeeR EL2, called RVfpgaEL2, or Veer EH1, called RVfpgaEH1 in this package (originally called RVfpga v2.2). If you are new to RVfpga, it is recommended that you start with RVfpgaEL2. We provide RVfpgaEH1 for continuity with RVfpga v2.2 and to show how the RVfpga system can use the VeeR EH1 core and SoC.

Table 1 shows the software and hardware used in RVfpgaEH1 (originally called RVfpga v2.2) and RVfpgaEL2.

Table 1. RVfpga Software and Hardware

RVfpga			**EH1**	**EL2**
Feature		**Description**		
Core	VeeR EH1	9-stage, superscalar RISC-V core.	X	
	VeeR EL2	5-stage, scalar RISC-V core. This is a smaller core than VeeR EH1.		X
SoC	VeeRwolf EH1	SoC based on the VeeR EH1 core.	X	
	VeeRwolf EL2	SoC based on the VeeR EL2 core.		X
Supported FPGA boards (these are optional)	Nexys A7	FPGA board from Digilent, Inc. The materials show how to target this board either using the onboard DDR memory or not.	X	X
	Nexys 4 DDR	FPGA board from Digilent, Inc. that is compatible with the Nexys A7 board.	X	X
	Basys 3	Lower-cost FPGA board from Digilent, Inc.		X
	Boolean	Lower-cost FPGA board from Real Digital.		X
SDK (software development kit)	Catapult SDK	Open-source RISC-V SDK developed by Imagination Technologies.		X
	Platform IO	Open-source SDK that is a Visual Studio Code extension.	X	X
Simulation tools	RVfpga-ViDBo	Simulation tool that displays a virtual board (interactive web-interface image of board) to perform a simulation of the RVfpga System and communicate with the peripherals of the simulated board.	X	X
	RVfpga-Pipeline	Simulation tool that uses a Pipeline Simulator for analysing the evolution of the instructions through the pipeline.	X	X
	RVfpga-Trace	Simulation tool that shows a waveform of the RVfpga System's internal signals.	X	X
	Whisper	RISC-V instruction-set simulator.	X	X
Virtual machine	Ubuntu 22.04	Virtual machine (VM) with all tools pre-installed. Works with usual VM software such as VMware or VirtualBox	X	X

All of the materials are free and provided with this RVfpga download package, except for the optional FPGA board(s). Because of the cores they support, we also refer to RVfpga 3.0 as RVfpgaEL2 and RVfpga 2.2 as RVfpgaEH1.

1. STRUCTURE OF THE RVfpga MATERIALS

The first step (that you should have already completed given that you are reading this document), is to request through the Imagination University Program (https://university.imgtec.com/teaching-download/) the RVfpga v3.0 package. Once you obtain the package in a compressed file, uncompress the file and copy the **RVfpga** folder to your Linux/Windows/MacOS computer.

Note that you can choose to install the tools natively in your Linux/Windows/MacOS machine or you can use a provided Ubuntu 22.04 Virtual Machine, with all the tools already installed on it (except for Vivado, which you have to install yourself if you want to use it). The VM can be obtained from:
https://drive.google.com/file/d/1KFnJYq6krB7vYt_AqTB_zTYVmxfATwJF/view?usp=sharing
as a separate download and can be executed in typical virtualization software such as VirtualBox or VMWare. In case you use the Virtual Machine, you must copy the **RVfpga** folder into it.
If you are running Windows 11, you may also use Windows Subsystem for Linux 2 (WSL 2). With WSL 2, both Windows and Linux environments share the same files. This allows performance-demanding tools such as Vivado to run natively on Windows, while development and simulation tasks can be done in WSL 2 without additional file synchronization. Installation details can be found at the following link: Windows Subsystem for Linux Documentation | Microsoft Learn

The **RVfpga** folder includes two subfolders:

- **RVfpgaEH1**
  This folder includes the same documents and sources as RVfpga v2.2, which uses the **VeeR EH1** core but with new simulation tools added: RVfpga-ViDBo, which simulates a Nexys A7 board executing the RVfpga SoC; and RVfpga-Pipeline, which simulates the pipeline of VeeR EH1.

- **RVfpgaEL2**
  This folder includes four subfolders, one for each **VeeR EL2** based configuration supported: RVfpga_Basys3, RVfpga_Boolean, RVfpga_NexysA7-DDR, RVfpga_NexysA7-NoDDR and RVfpga_NexysVideo-NoDDR.

At this point, you should go into the subfolder of the course in which you are interested, either **RVfpgaEL2** or **RVfpgaEH1** (originally called RVfpga v2.2) and continue reading the corresponding *ReadmeSecond* document that you will find in those subfolders. Again, if you are new to RVfpga, we recommend starting with RVfpgaEL2.