CP1

Progress

In this checkpoint, we implemented fetching instructions through DRAM, Cache, and a line buffer. We started with the base cache from mp_cache and implemented a cache line adapter deserializer to make the cache work with DRAM. We've also made a parameterizable queue module that is used to implement the instruction queue that instructions are fetched into.

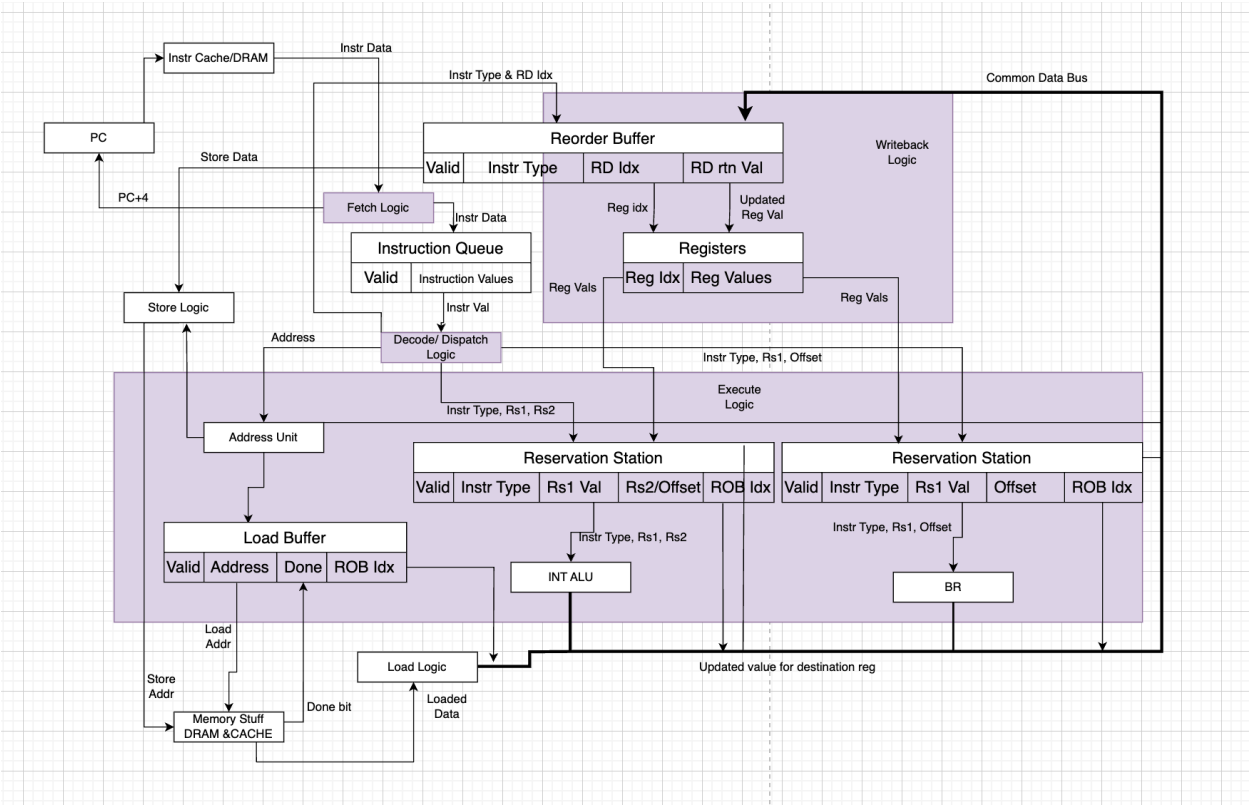
Individual Contributions

Alex- Wrote queue and cache adapter.
Erin- Made diagram and fetch
Sujin- Made diagram and fetch

Bugs

We had a bug where we held the bmem_read signals for multiple cycles, which we fixed by adding a flag.

Planned Diagram - Tomasulo's Algorithm



performance metrics

Area: 49,997.0 units
Timing: 8.145362 slack