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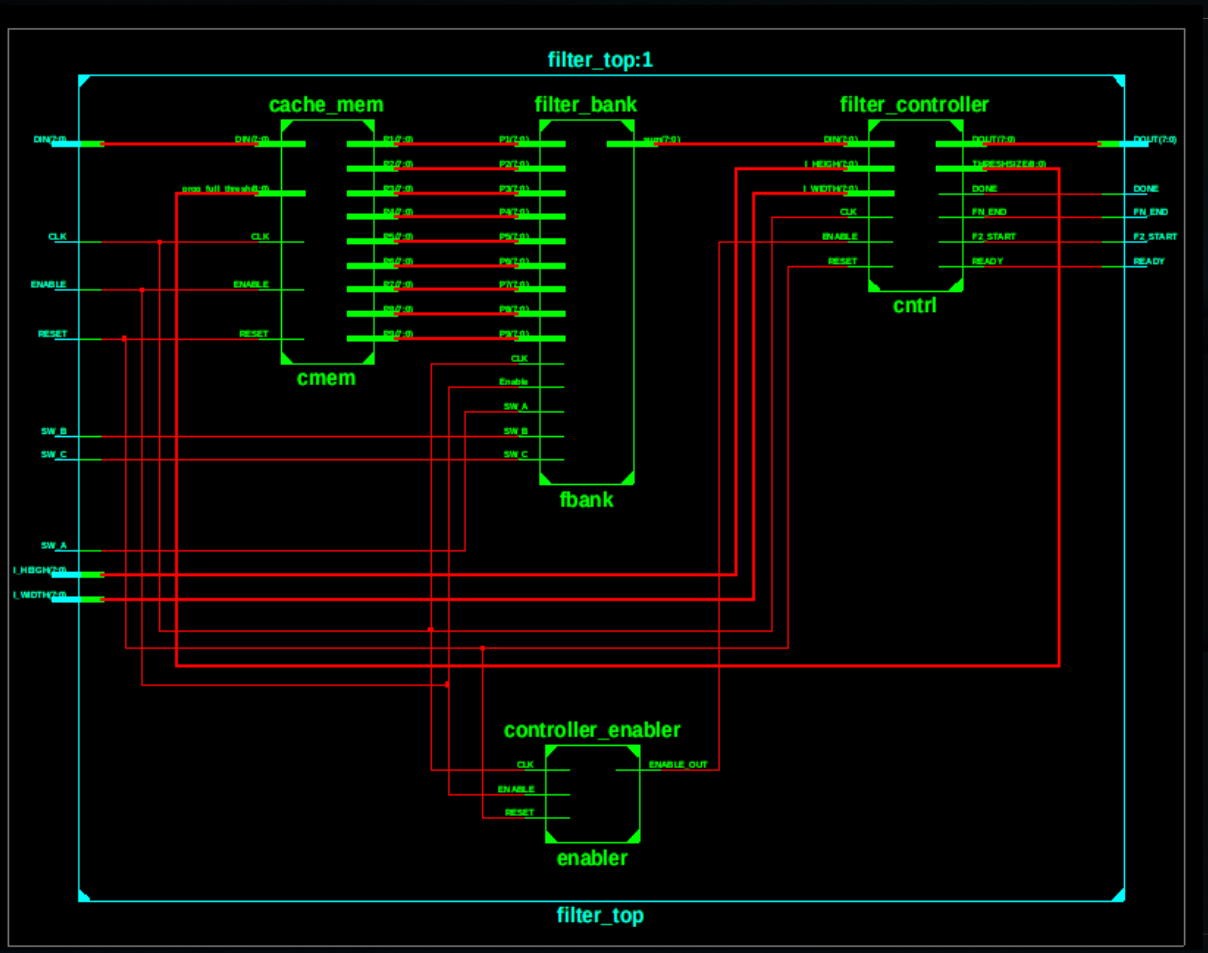
Real Time Filter Implementation On FPGA board

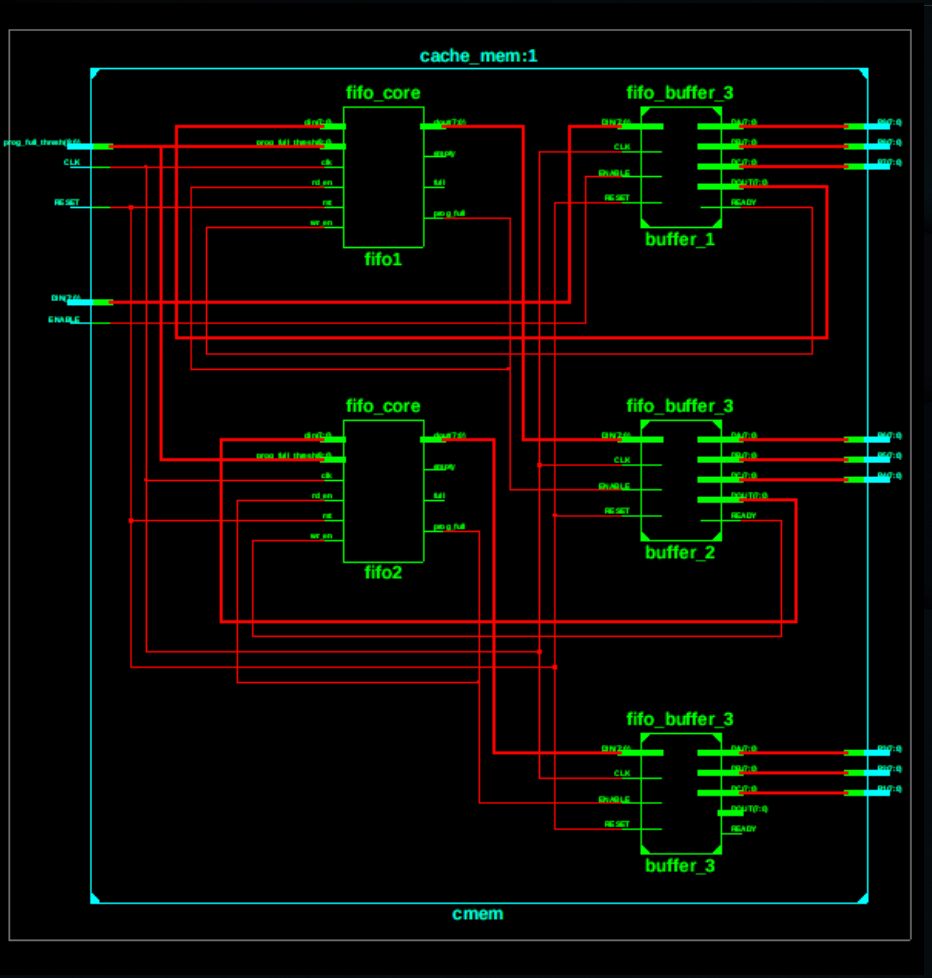
Part 1 Hardware Design

- Filter bank
  - Filter Chooser
  - Multiplier
    - Adder
  - Zipper
- Cache mem
  - Fifo_buffer_3
  - FIFO IP Core
- Filter Controller
- Controller Enable

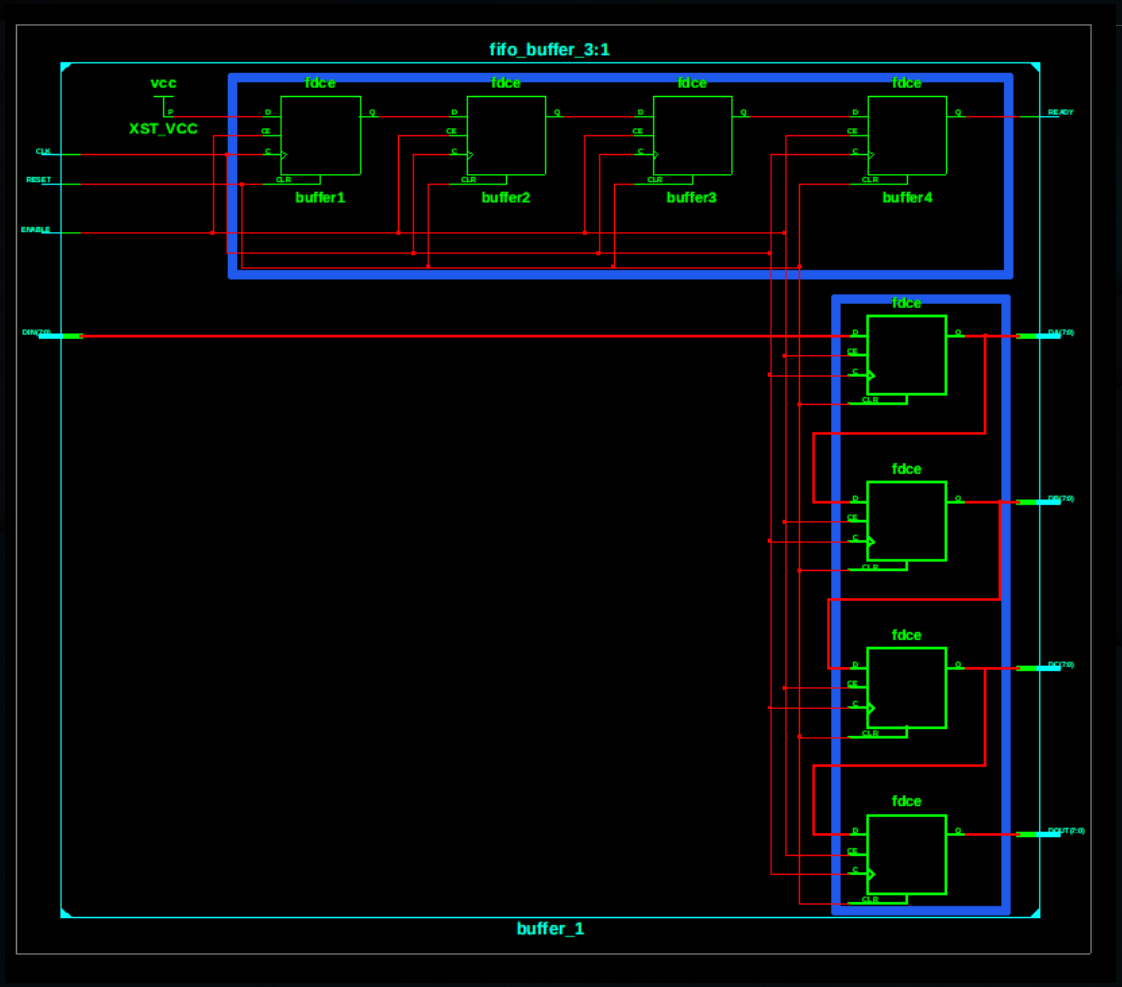
Top Level


filter_top:1
cache_mem
filter_bank
filter_controller
cmem
fbank
cntrl
controller_enabler
enabler
filter_top
DIN(7:0)
CLK
ENABLE
RESET
SW_A
SW_B
SW_C
I_HEIGH(7:0)
I_WIDTH(7:0)
DOUT(7:0)
DONE
FN_END
F2_START
READY
ENABLE_OUT

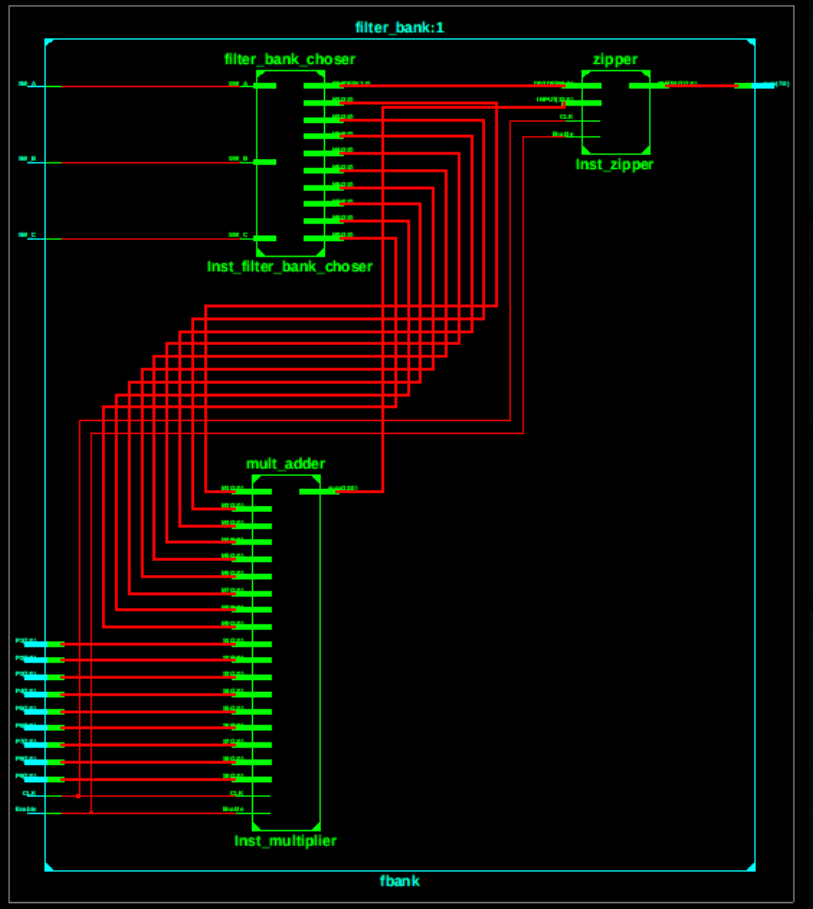
Top Level :: CacheMem

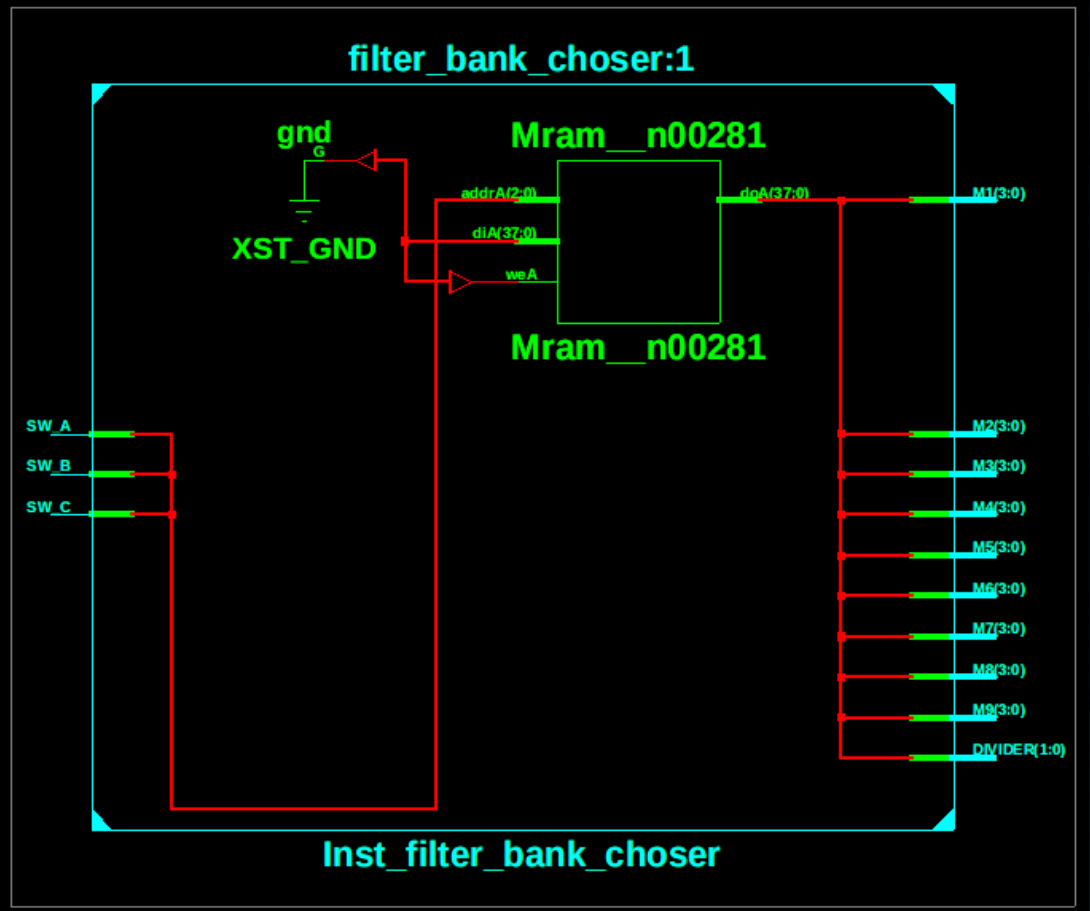


Top Level :: CacheMem :: Fifo Buffer

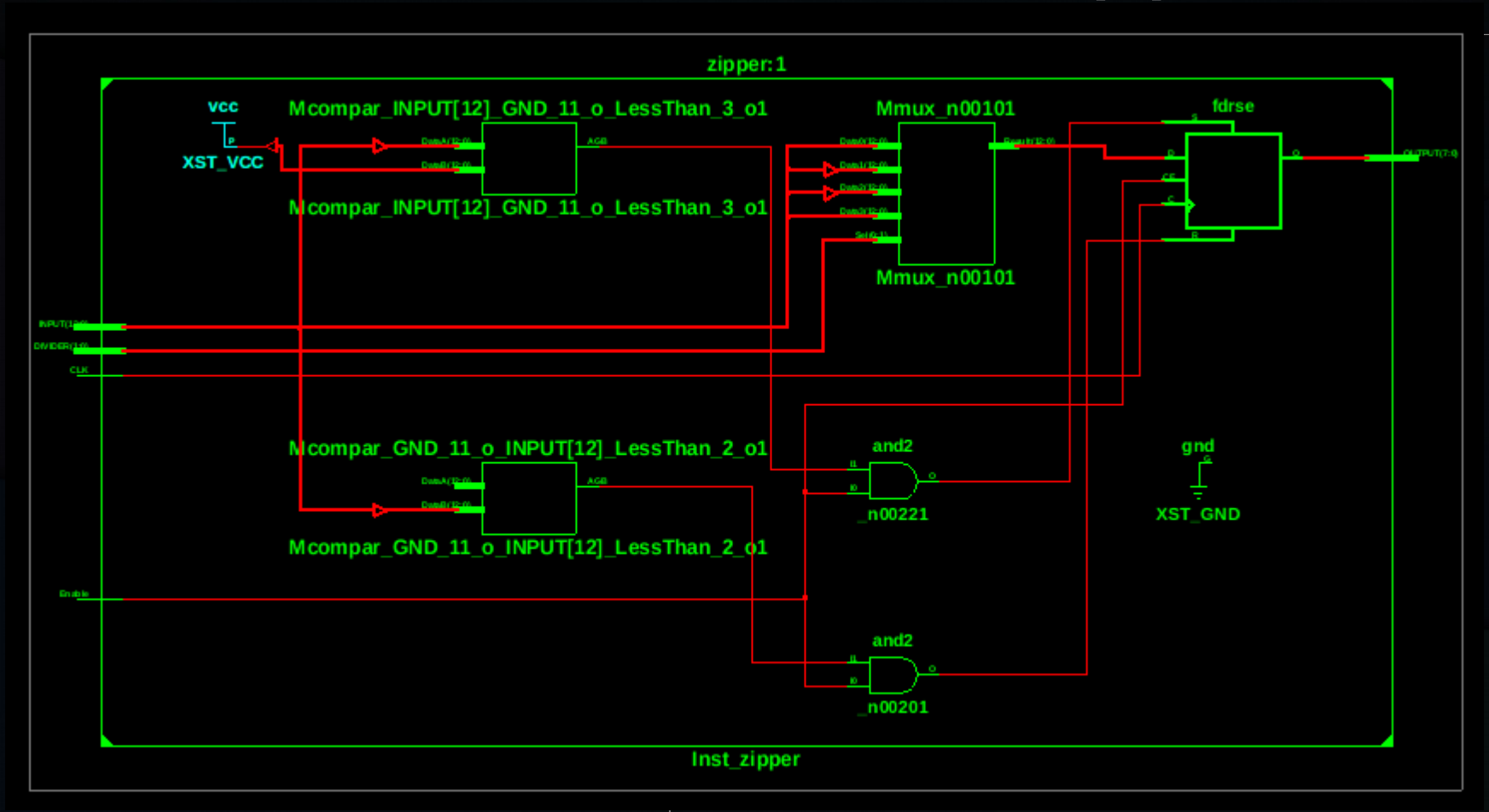


Top Level :: Filter Bank

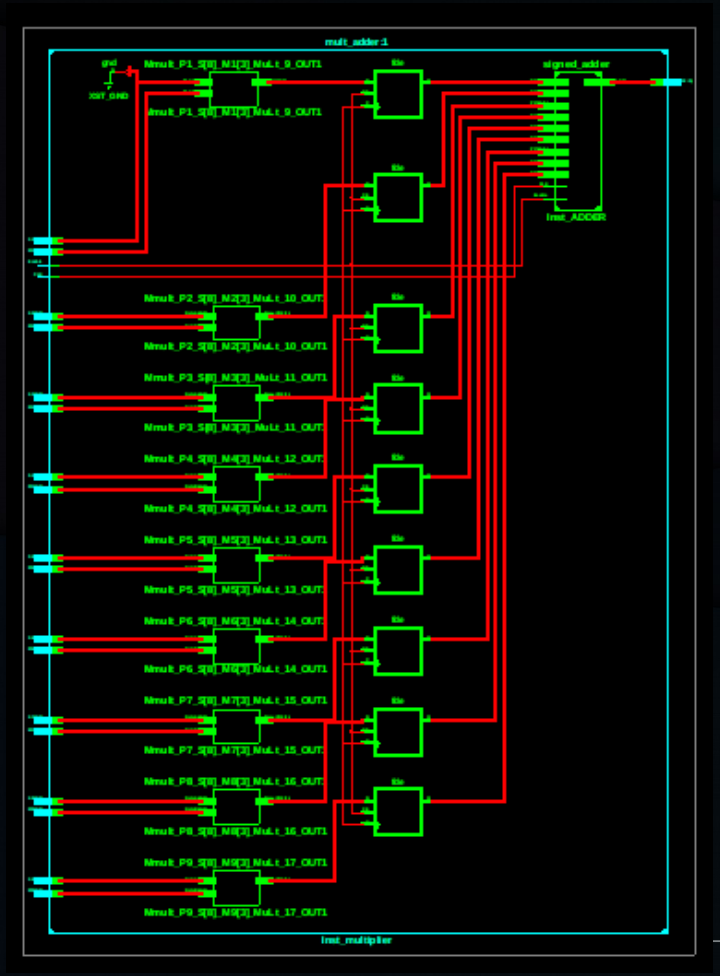




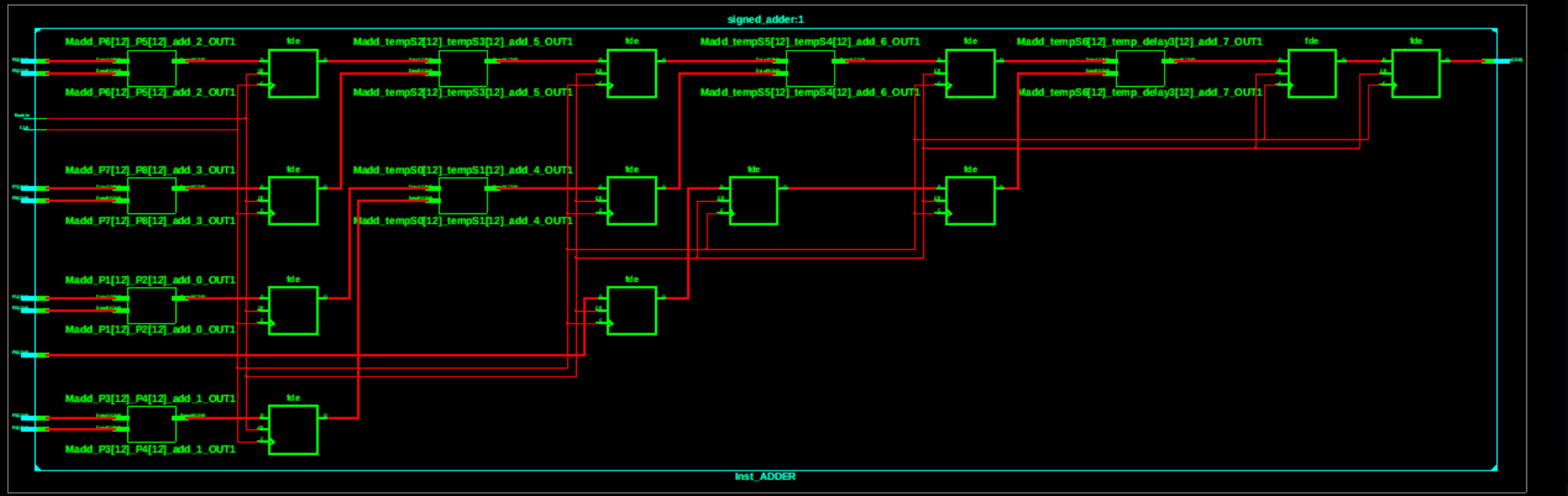
Top Level :: Filter Bank :: Zipper



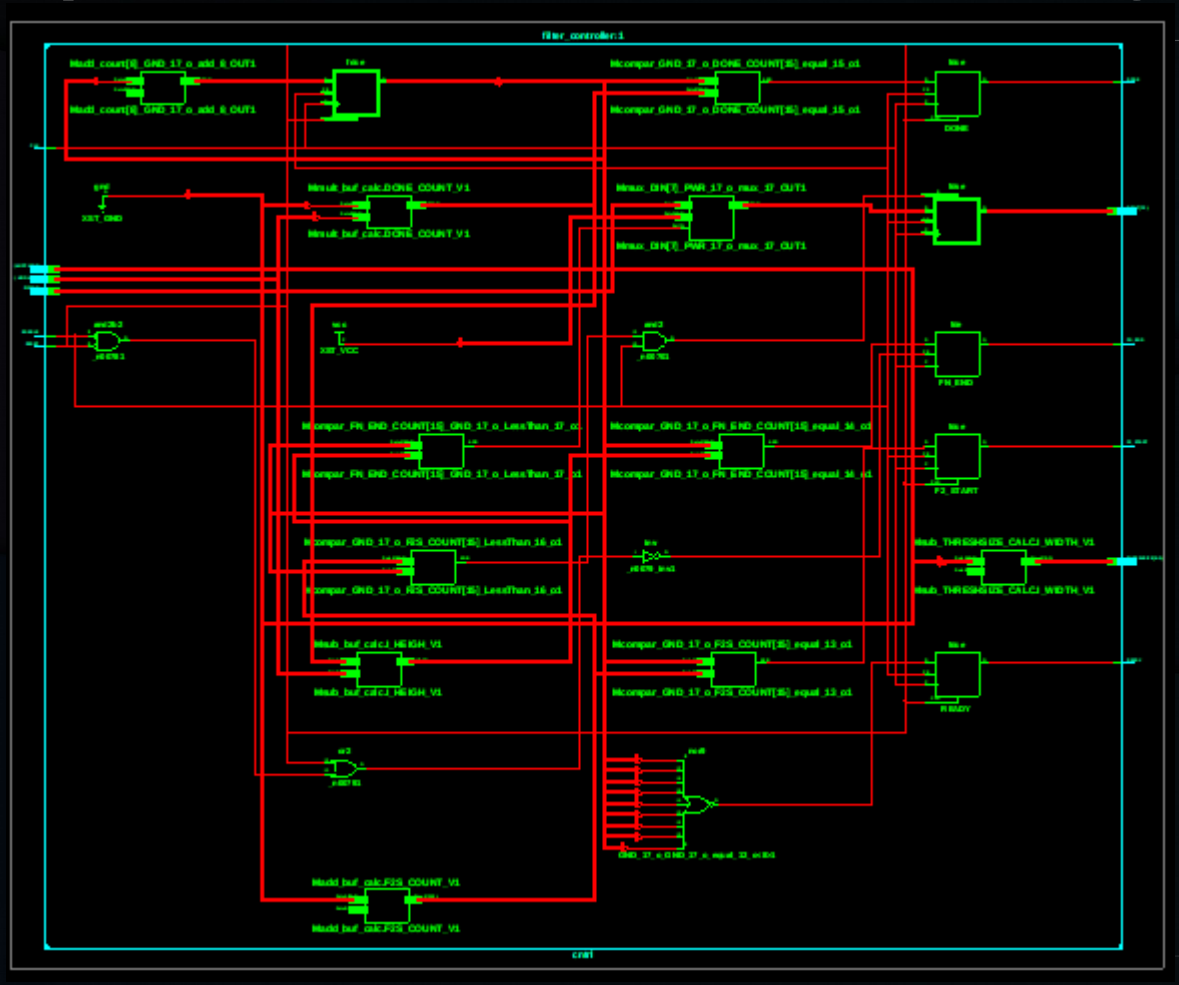
Top Level :: Filter Bank :: MADD



Top Level::Filter Bank :: MADD:: ADD



Top Level :: Control Logic



Top Level :: Control Logic

	1	2	3	4	5	6	7	8	9	10
1	0	1	2	3	4	5	6	7	8	9
2	10	11	12	13	14	15	16	17	18	19
3	20	21	22	23	24	25	26	27	28	29
4	30	31	32	33	34	35	36	37	38	39
5	40	41	42	**43**	**44**	**45**	46	47	48	49
6	50	51	52	**53**	**54**	**55**	56	57	58	59
7	60	61	62	**63**	**64**	**65**	66	67	68	69
8	70	71	72	73	74	75	76	77	78	79
9	80	81	82	83	84	85	86	87	88	89
10	90	91	92	93	94	95	96	97	98	99
11	100	101	102	103	104	105	106	107	108	109
12	110	111	112	113	114	115	116	117	118	119

SIGNALS	
0	READY
11	F2_START
108	FN_END
119	DONE