# Real Time Imaging

## State Machine on NEXYS 4

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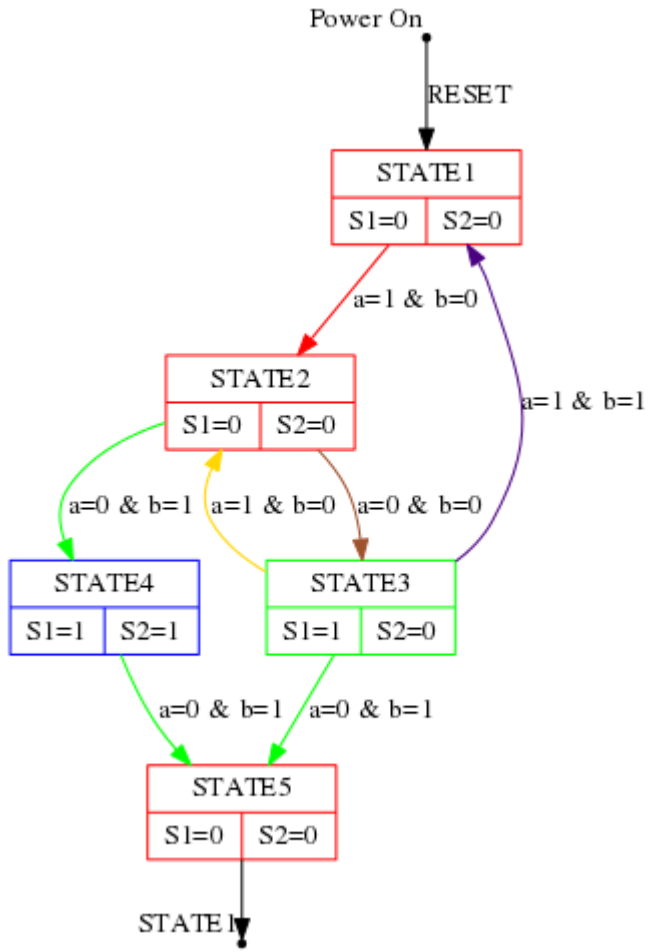
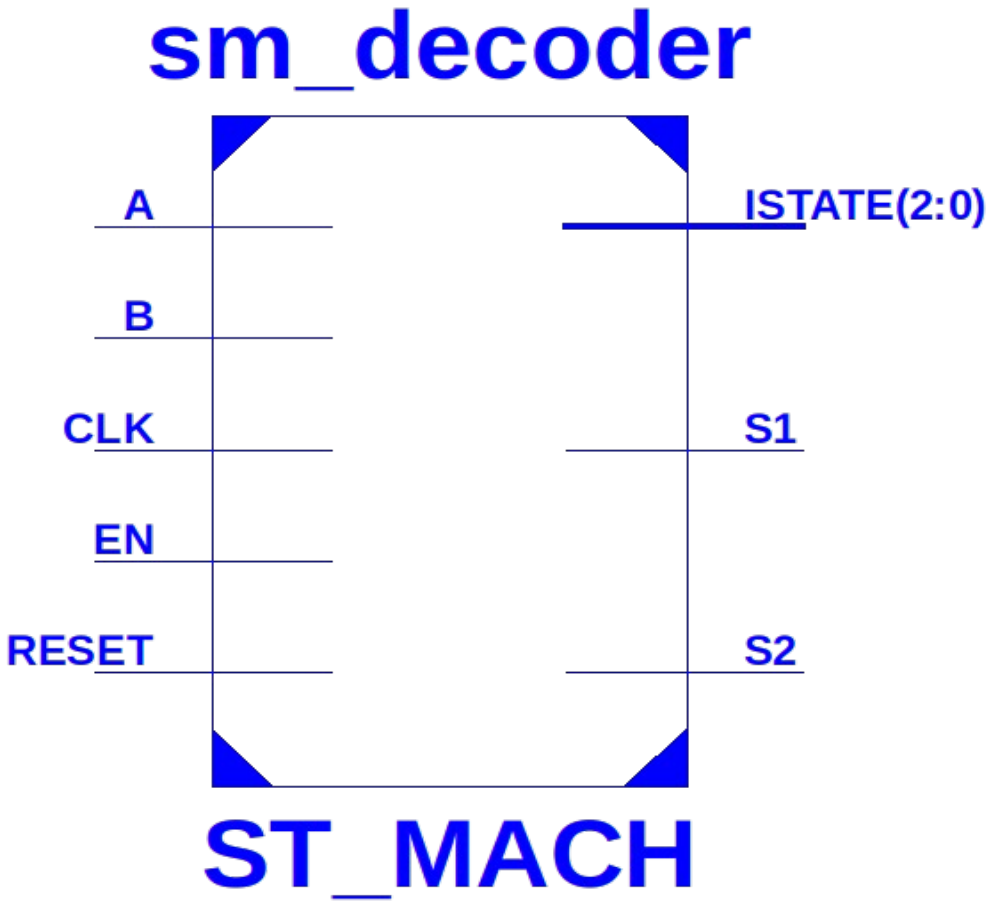
# The state machine



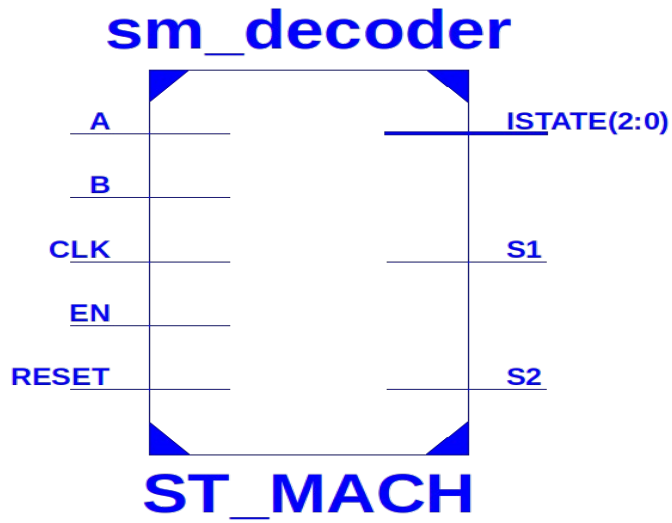



# State Machine Encoding

```
architecture sm_decoder_impl of sm_decoder is

   -- STATE ENCODINGS
   constant STATE1 : std_logic_vector(4 downto 0) := "001" & "00";
   constant STATE2 : std_logic_vector(4 downto 0) := "010" & "00";
   constant STATE3 : std_logic_vector(4 downto 0) := "011" & "01";
   constant STATE4 : std_logic_vector(4 downto 0) := "100" & "11";
   constant STATE5 : std_logic_vector(4 downto 0) := "101" & "00";

   signal CUR_STATE : std_logic_vector(4 downto 0);
begin

-- Hard wires
S1 <= CUR_STATE(0);
S2 <= CUR_STATE(1);
ISTATE <= CUR_STATE(4 downto 2);
```

ISTATE

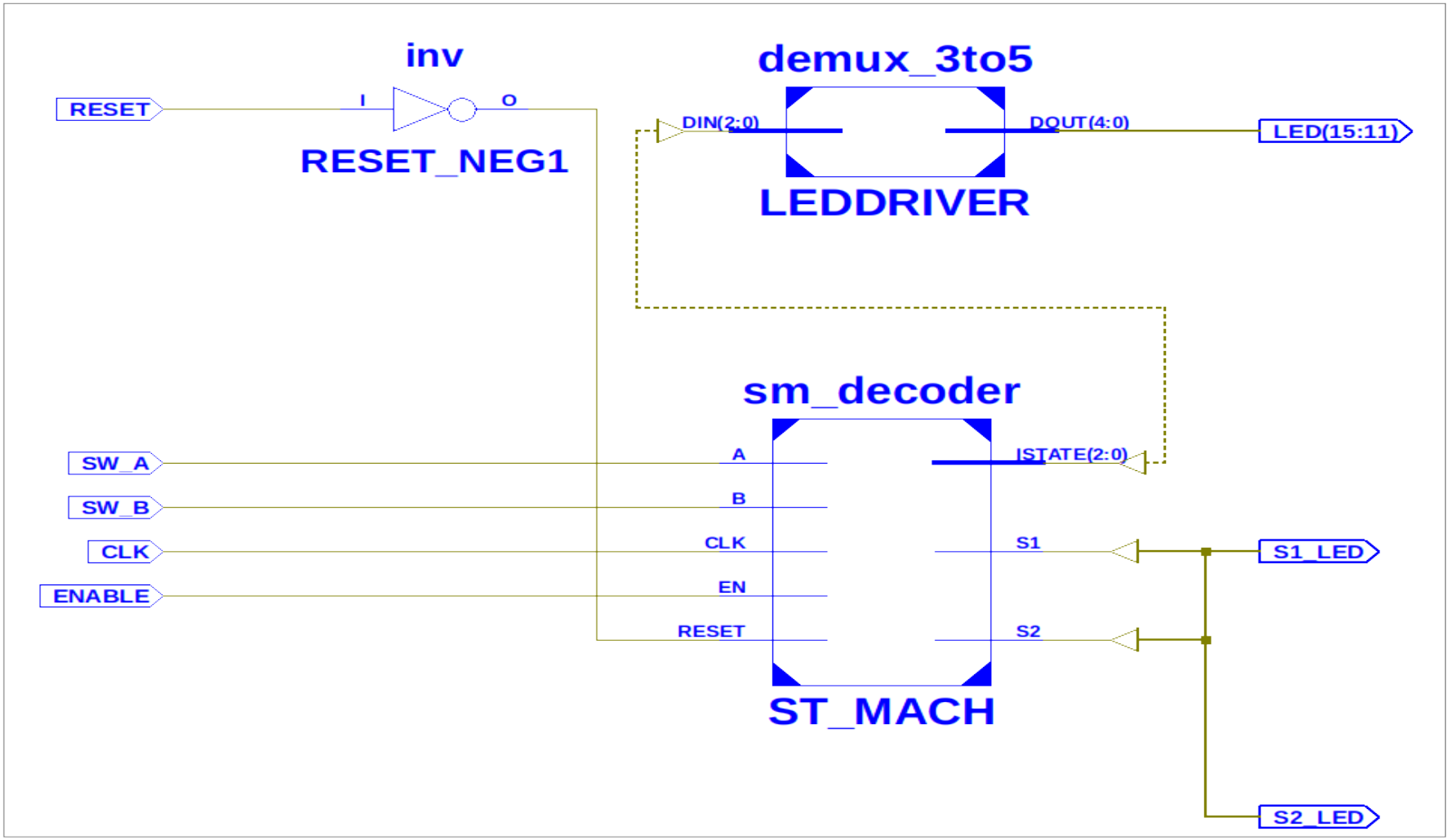
S2 S1



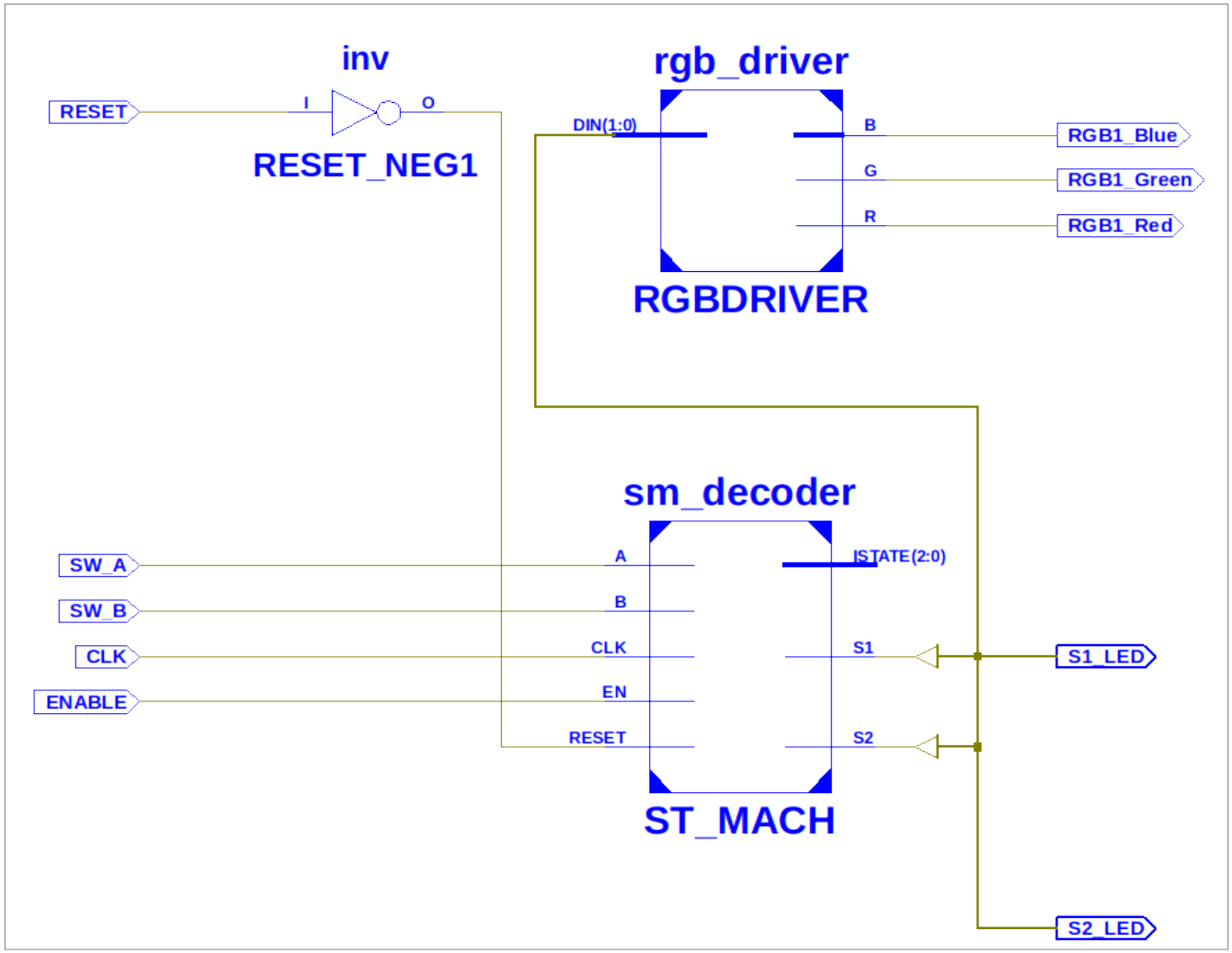
# Operation

- Input
  - Switch A
  - Switch B
  - RESET
  - ENABLE Btn
- Output
  - S1 & S2
    - 2 right leds
    - 3color led
  - Internal State
    - 5 left leds
    - 7 Segment disp.

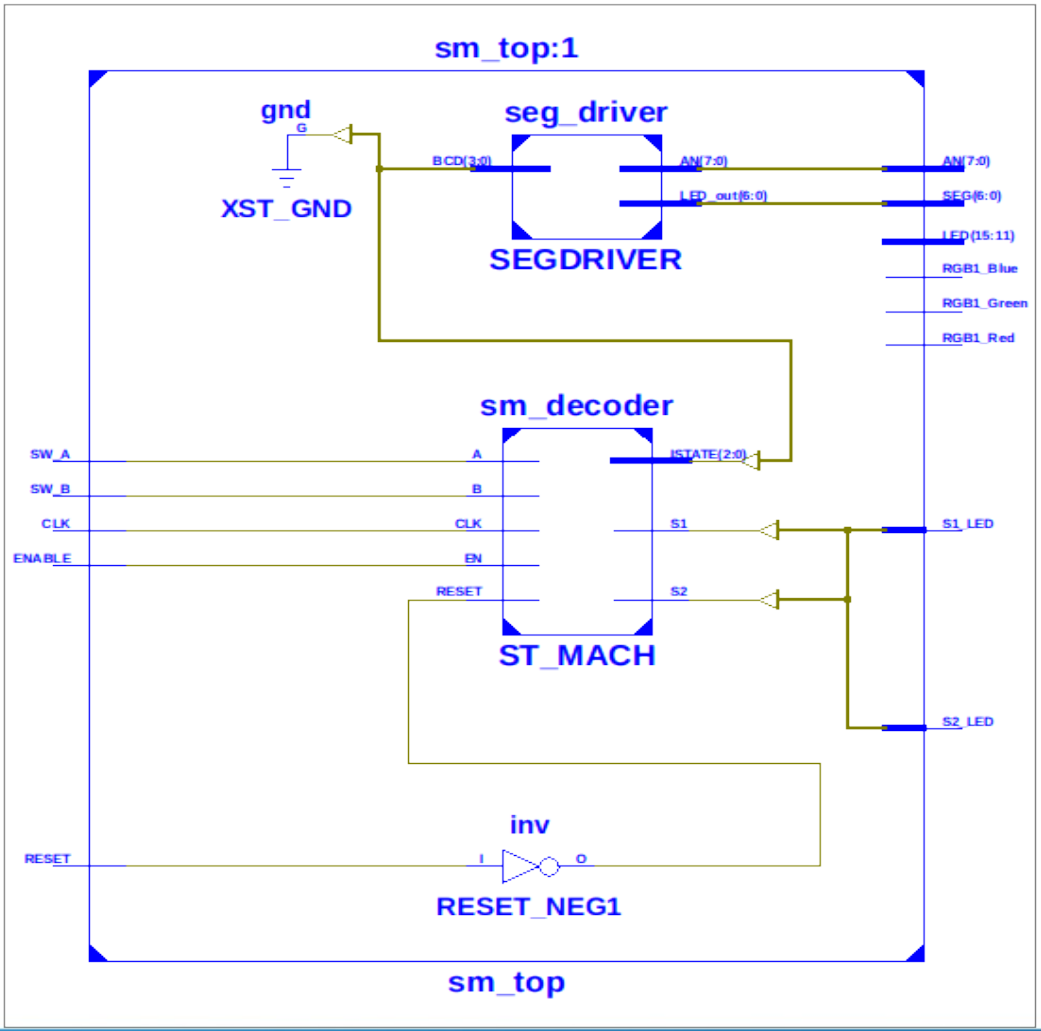
# The Output Leds Driver



# The RGB Led Driver



# The & Segment Driver



# Demo Time

Code on Github

https://github.com/jtsagata/nexys4_sm_lab