Real Time Imaging

State Machine on NEXYS 4

The state machine

Power On

RESET

STATE1	
S1=0	S2=0

a=1 & b=0

a=1 & b=1

STATE2	
S1=0	S2=0

a=0 & b=1   a=1 & b=0   a=0 & b=0

STATE4	
S1=1	S2=1

STATE3	
S1=1	S2=0

a=0 & b=1   a=0 & b=1

STATE5	
S1=0	S2=0

STATE 1
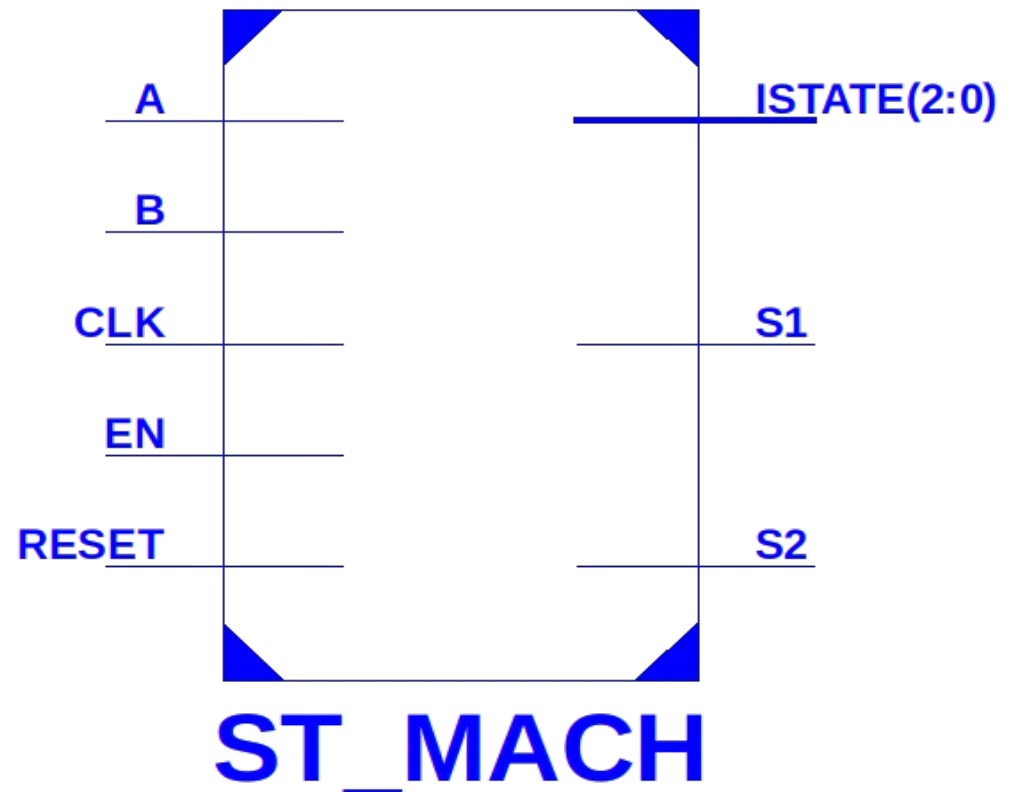
sm_decoder

A   ISTATE(2:0)

B

CLK   S1

EN

RESET   S2

ST_MACH
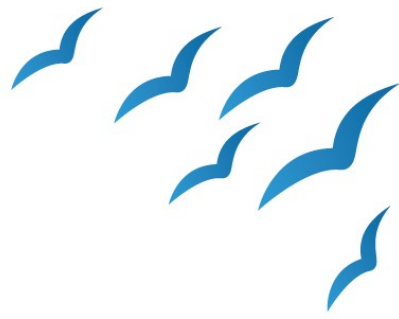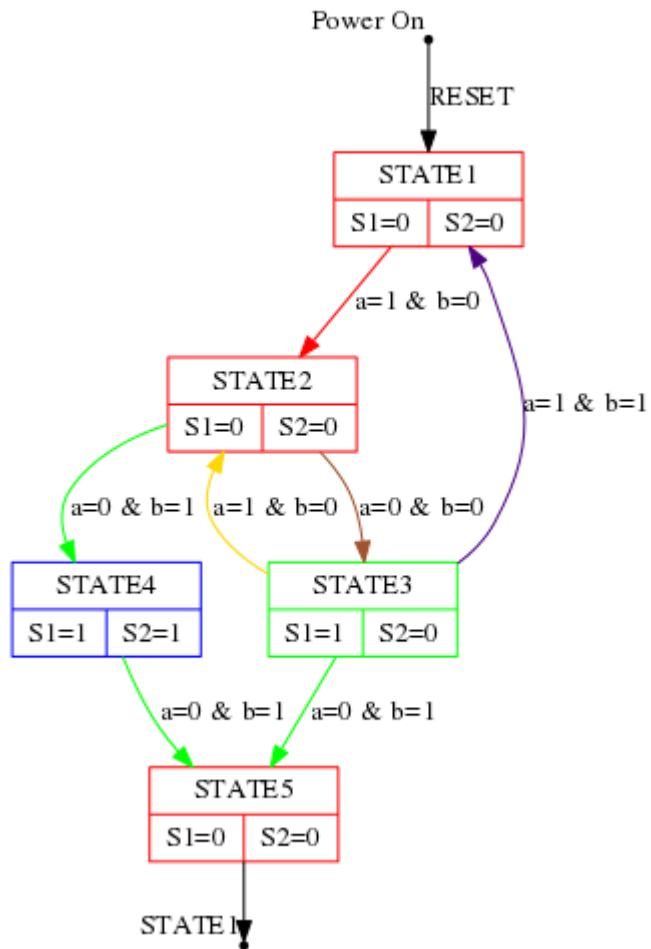
State Machine Encoding

```vhdl
architecture sm_decoder_impl of sm_decoder is

    -- STATE ENCODINGS
    constant STATE1 : std_logic_vector(4 downto 0) := "001" & "00";
    constant STATE2 : std_logic_vector(4 downto 0) := "010" & "00";
    constant STATE3 : std_logic_vector(4 downto 0) := "011" & "01";
    constant STATE4 : std_logic_vector(4 downto 0) := "100" & "11";
    constant STATE5 : std_logic_vector(4 downto 0) := "101" & "00";

    signal CUR_STATE : std_logic_vector(4 downto 0);
begin

-- Hard wires
S1 <= CUR_STATE(0);
S2 <= CUR_STATE(1);
ISTATE <= CUR_STATE(4 downto 2);
```
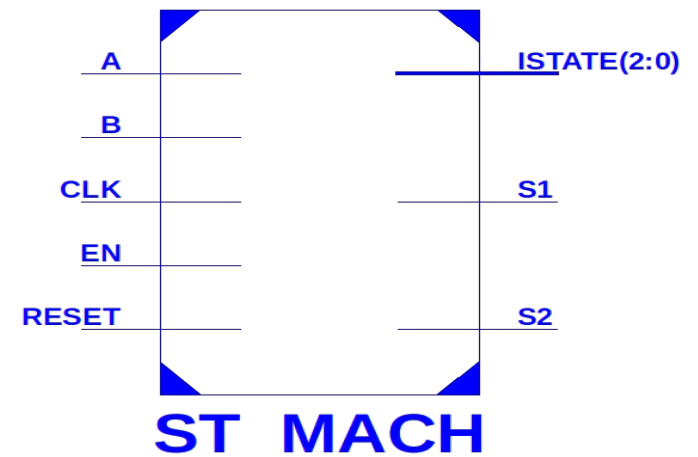
ISTATE

S2 S1

sm_decoder

A   ISTATE(2:0)

B

CLK   S1

EN

RESET   S2

ST_MACH
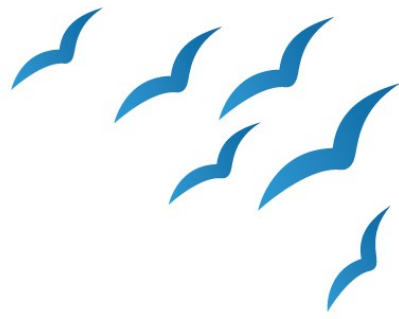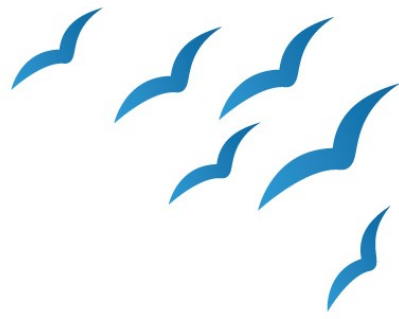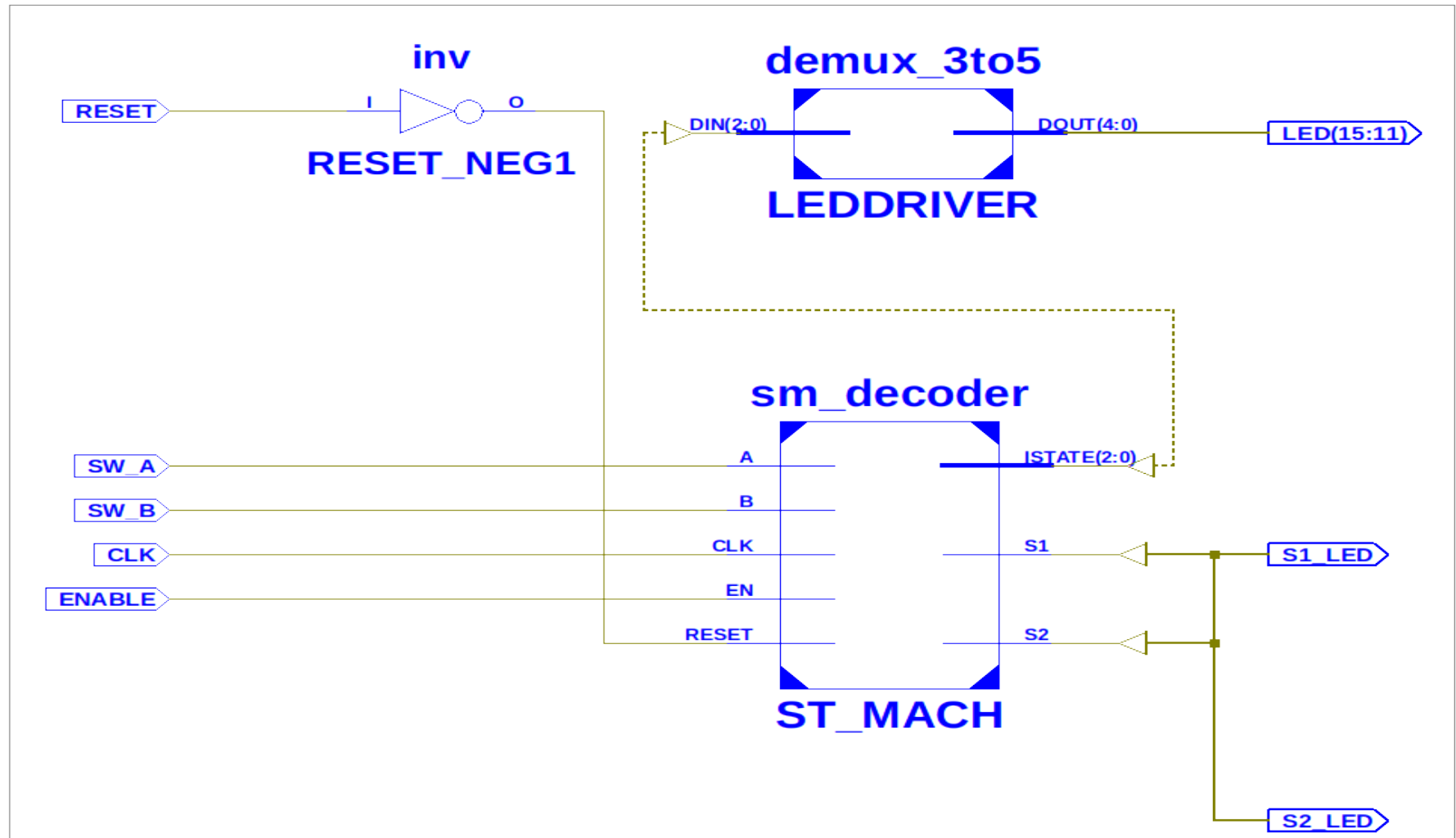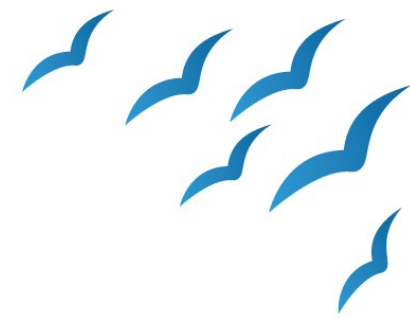
Operation

- Input
  - Switch A
  - Switch B
  - RESET
  - ENABLE Btn

- Output
  - S1 & S2
    - 2 right leds
    - 3color led
  - Internal State
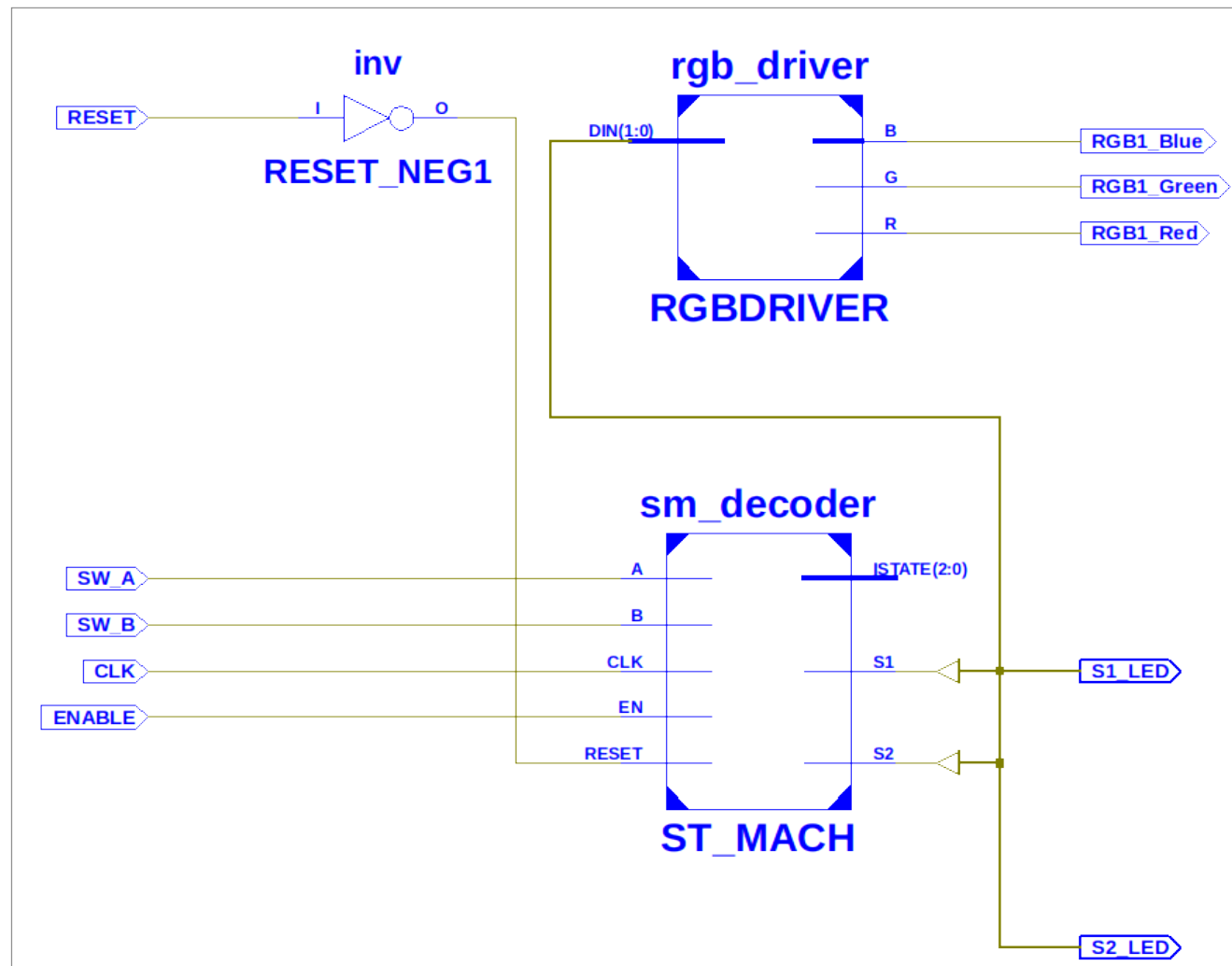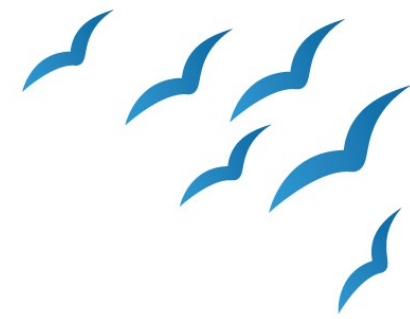   - 5 left leds
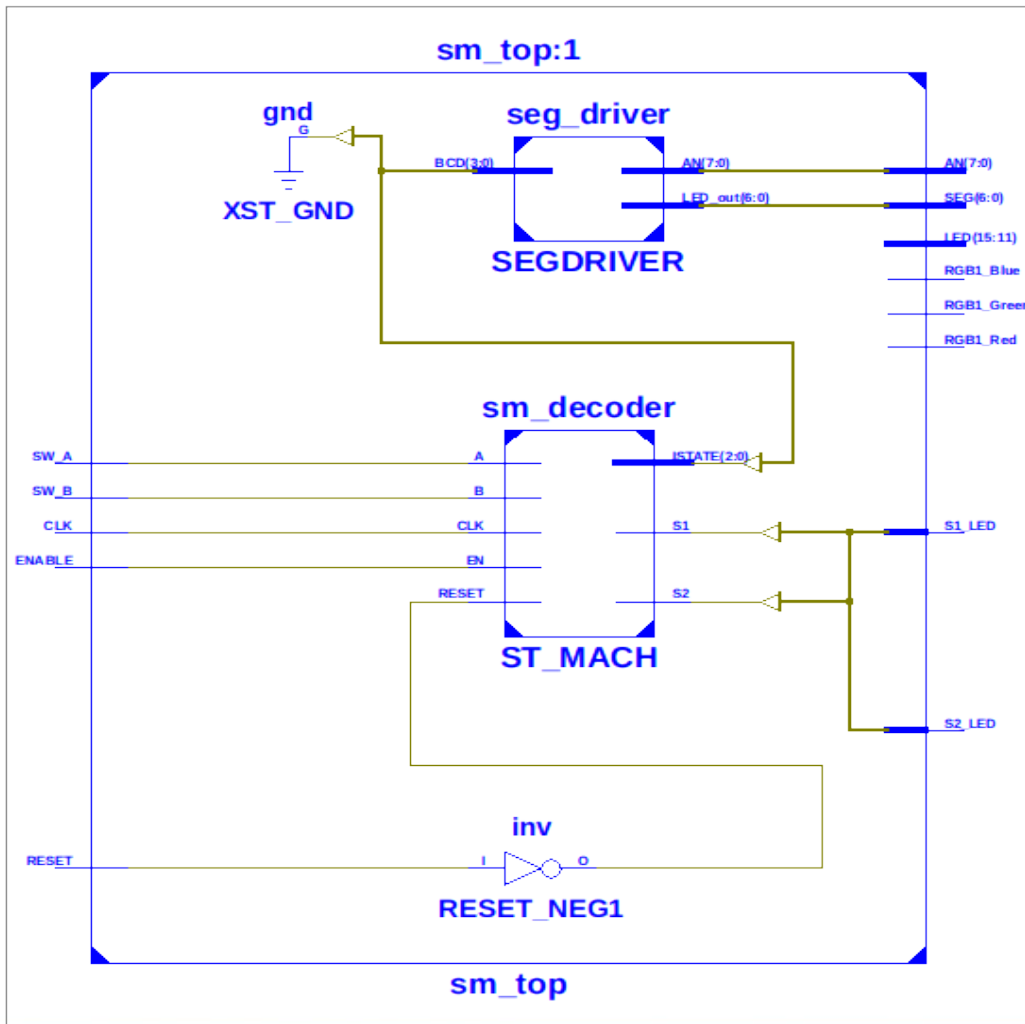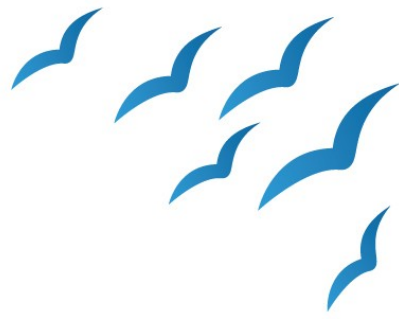   - 7 Segment disp.

The Output Leds Driver

The RGB Led Driver

The & Segment Driver

Demo Time

Code on Github

https://github.com/jtsagata/nexys4_sm_lab