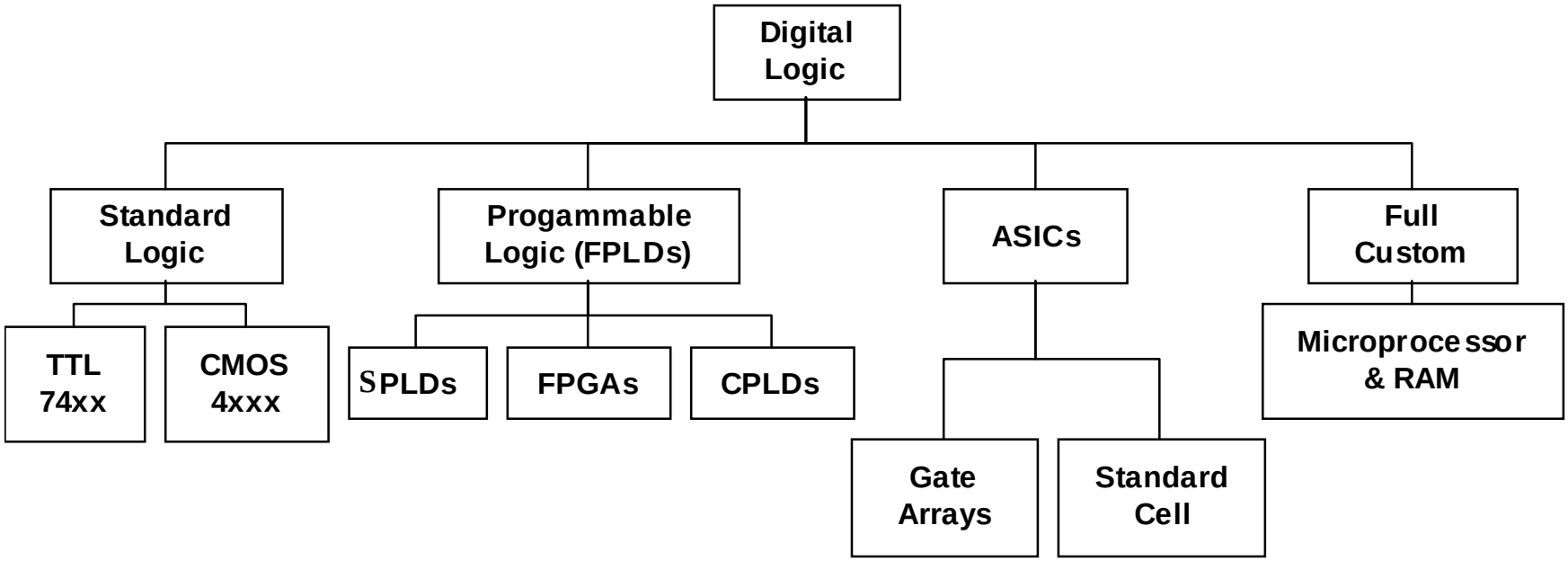
تراشه‌های منطقی برنامه‌پذیر

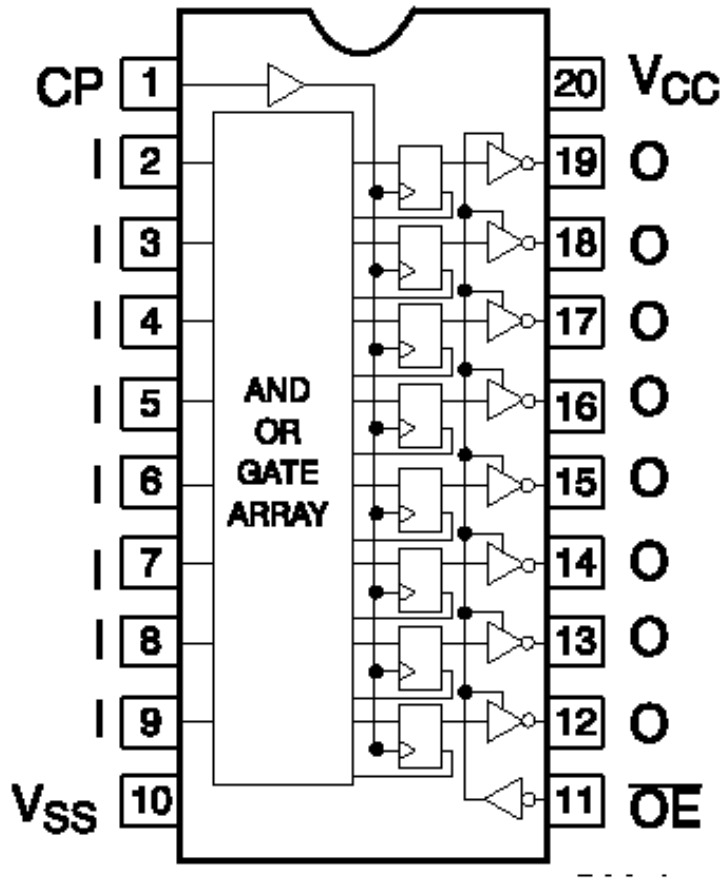
مدارهای دیجیتال



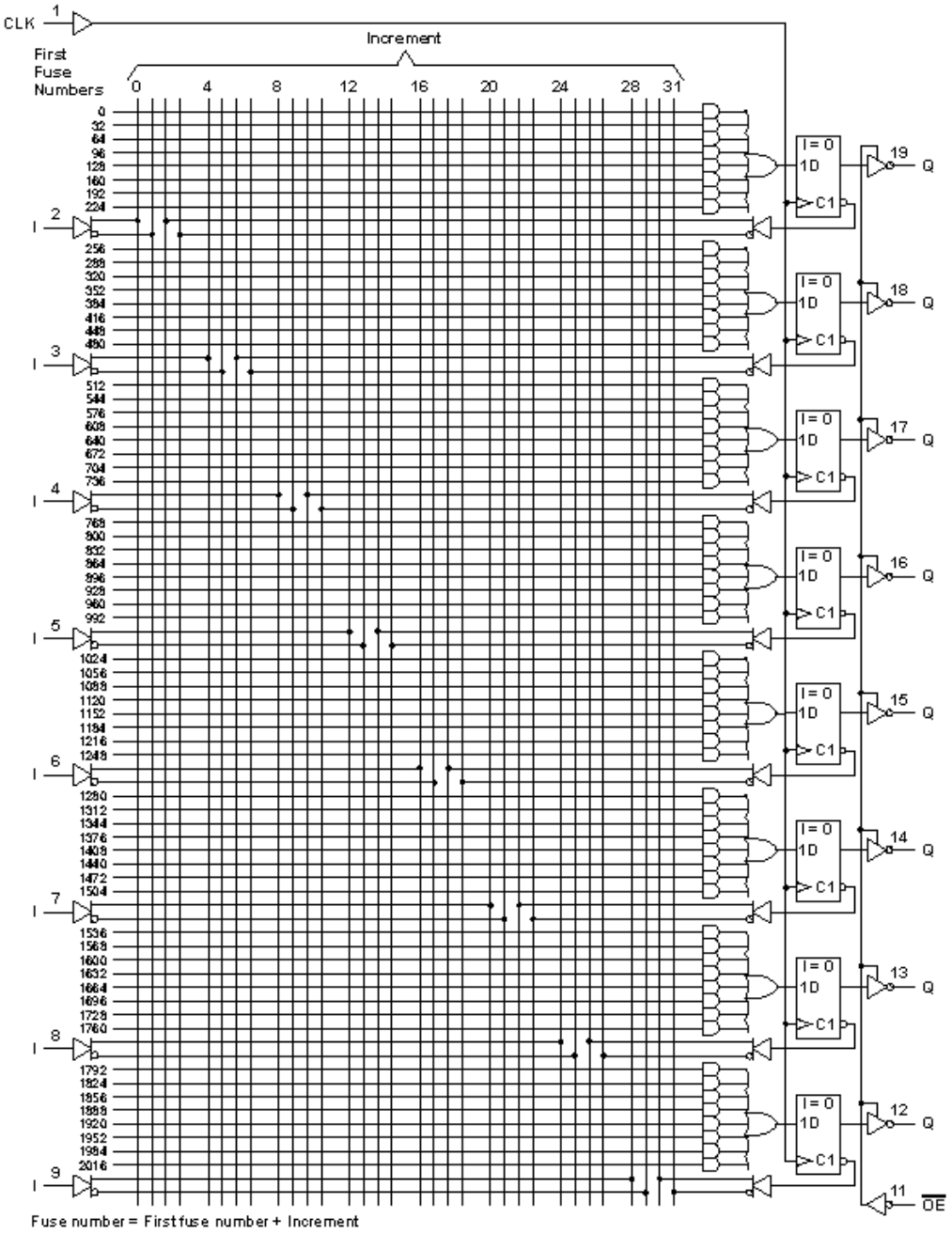
Simple PLD (SPLD)

- برای پیاده سازی مدارهای ترتیبی معمولا در خروجی، FF قرار دارد.

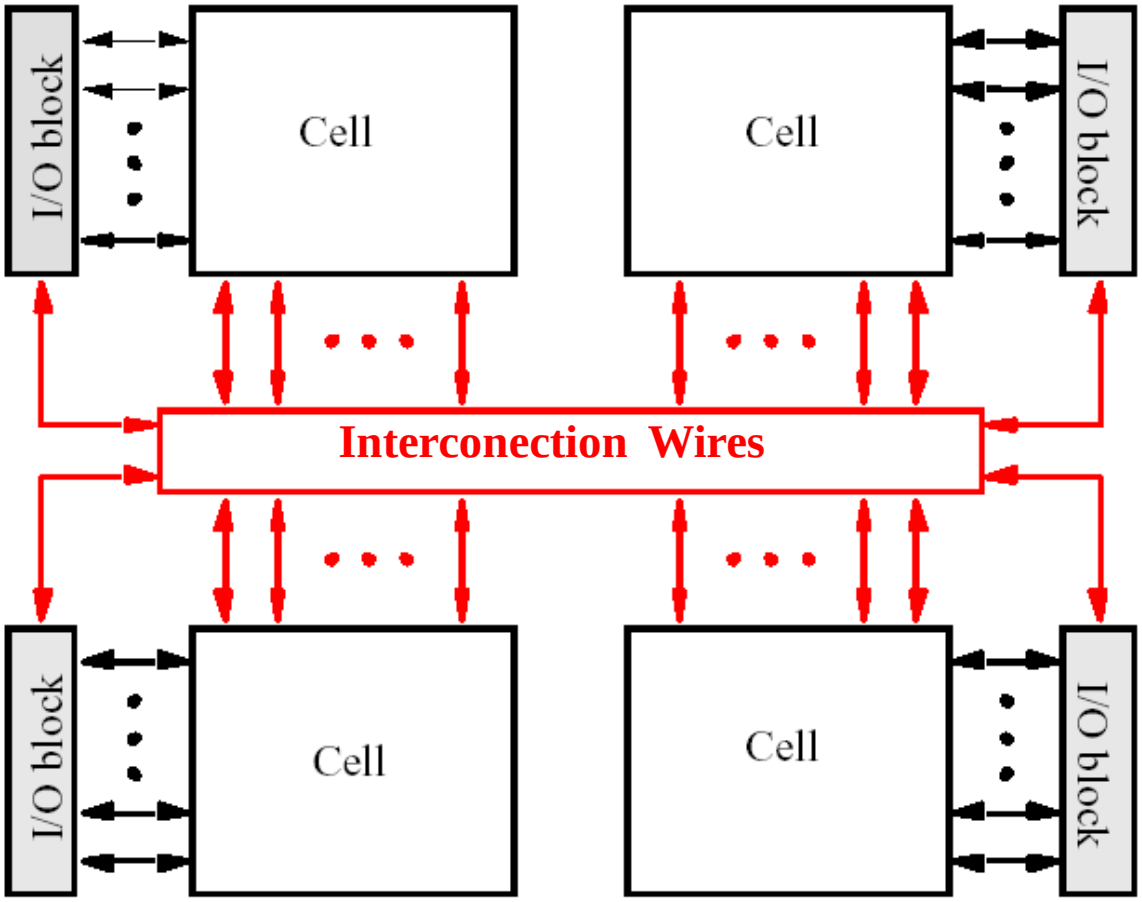
PAL16R8



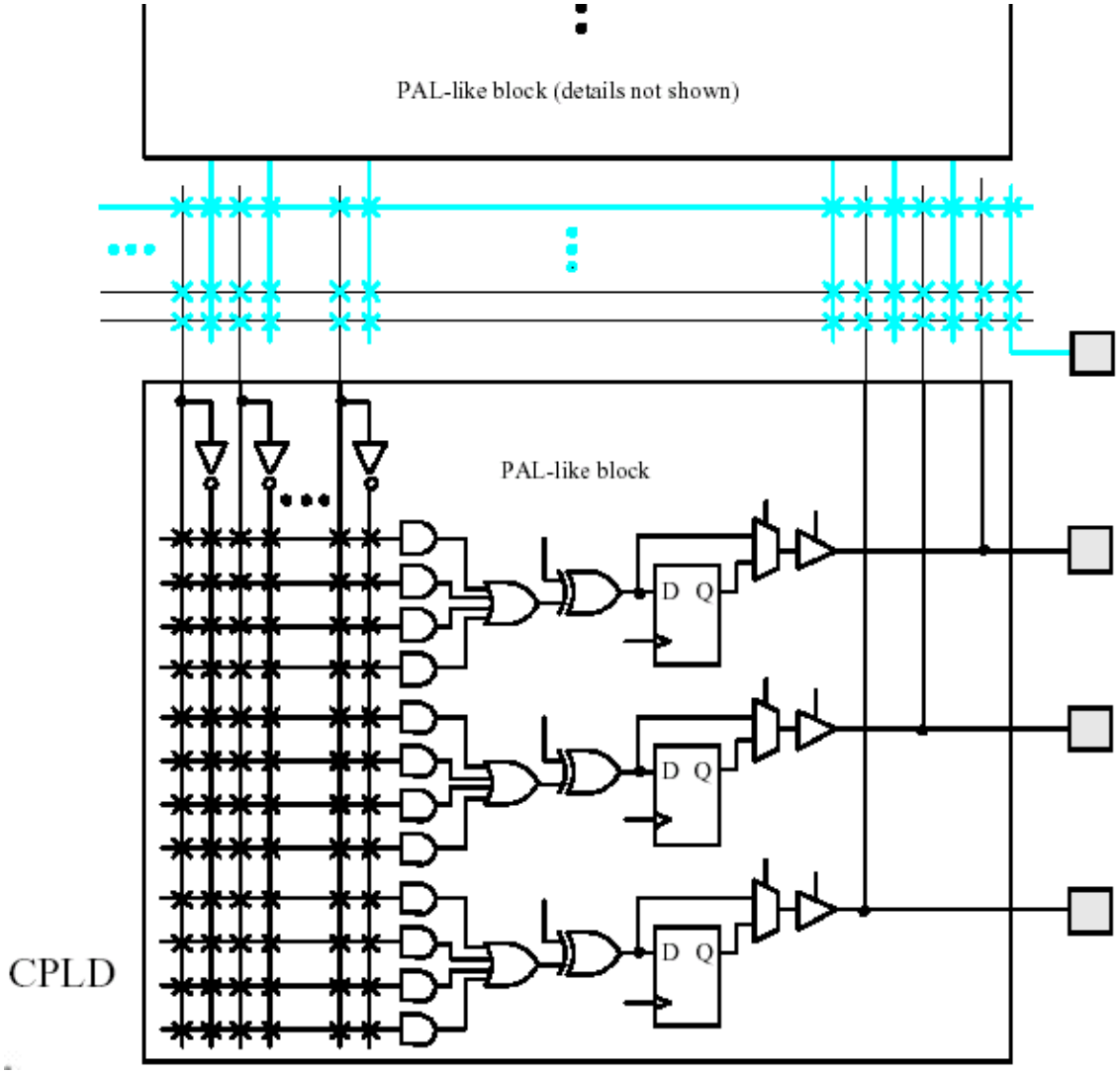
PAL 16R8


CLK
1
Increment
First
Fuse
Numbers
0
4
8
12
16
20
24
28
31
I
2
3
4
5
6
7
8
9
I = 0
1D
C1
19
18
17
16
15
14
13
12
Q
11
OE
Fuse number = First fuse number + Increment

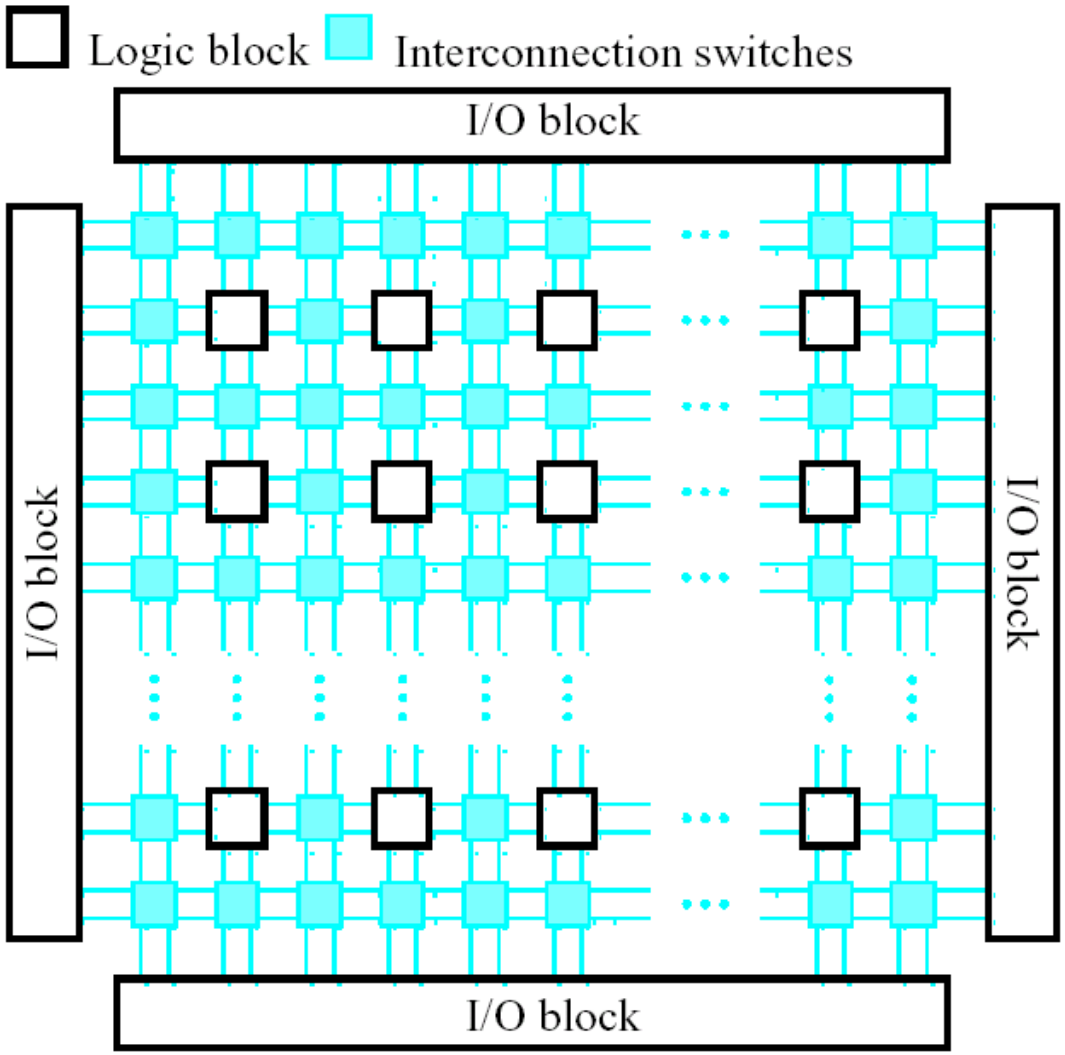
CPLD


I/O block
Cell
Cell
I/O block
Interconection Wires
I/O block
Cell
Cell
I/O block

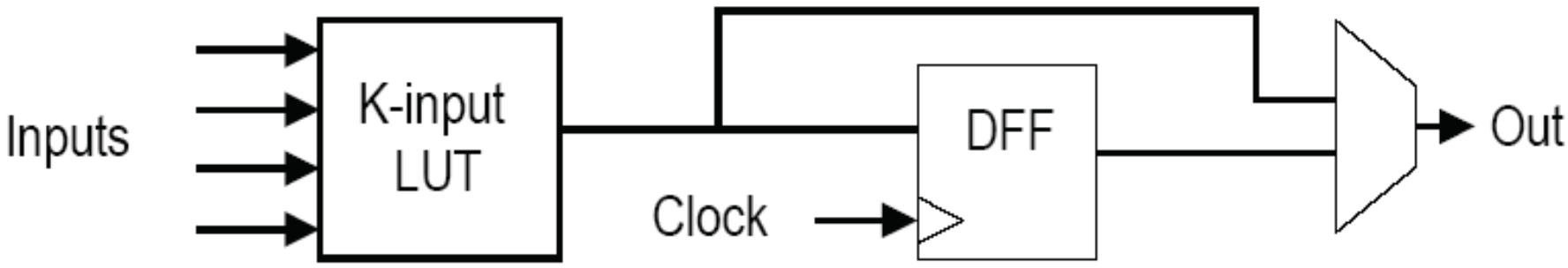
بخشی از CPLD



ساختار FPGA


Logic block
Interconnection switches
I/O block
I/O block
I/O block
I/O block

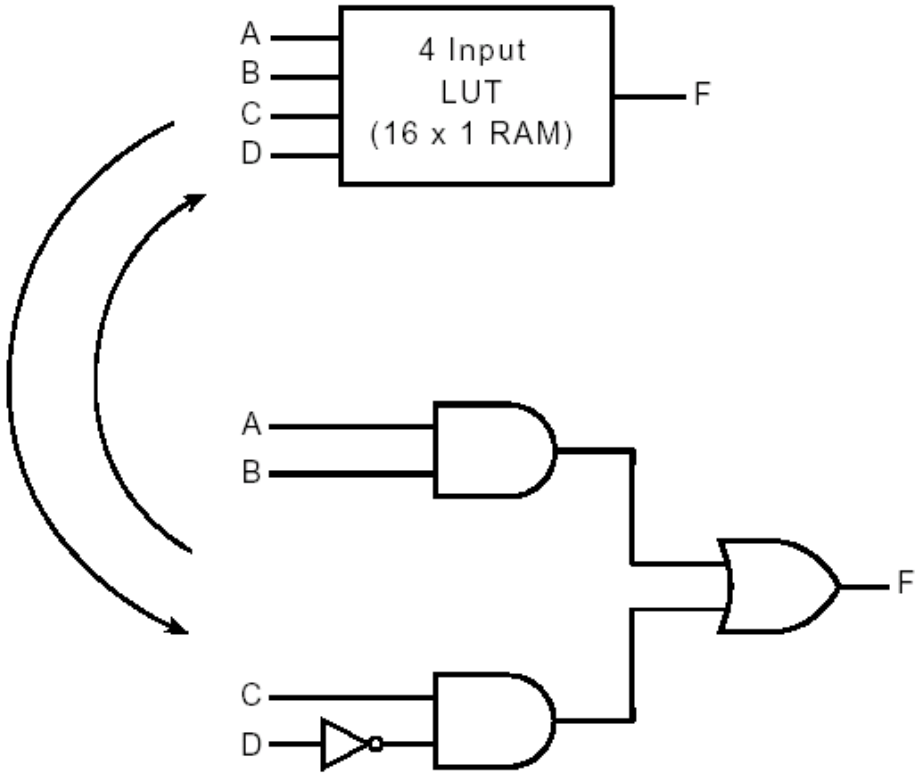
Logic Cell



LUT: Lookup Table

Flip-flop: typically DFF (in some devices programmable into D-latch or TFF)

LUT

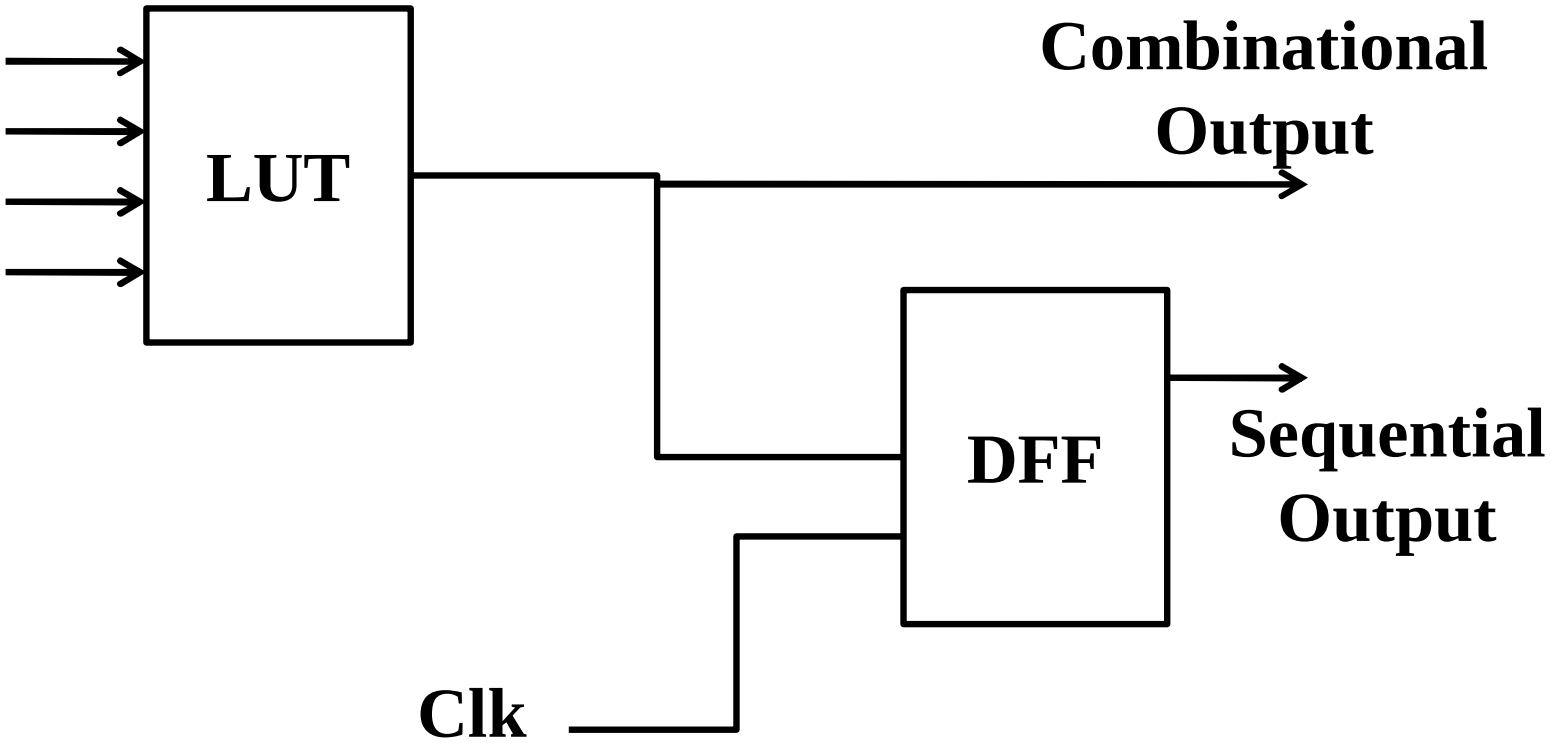


RAM Contents				
Address				Data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

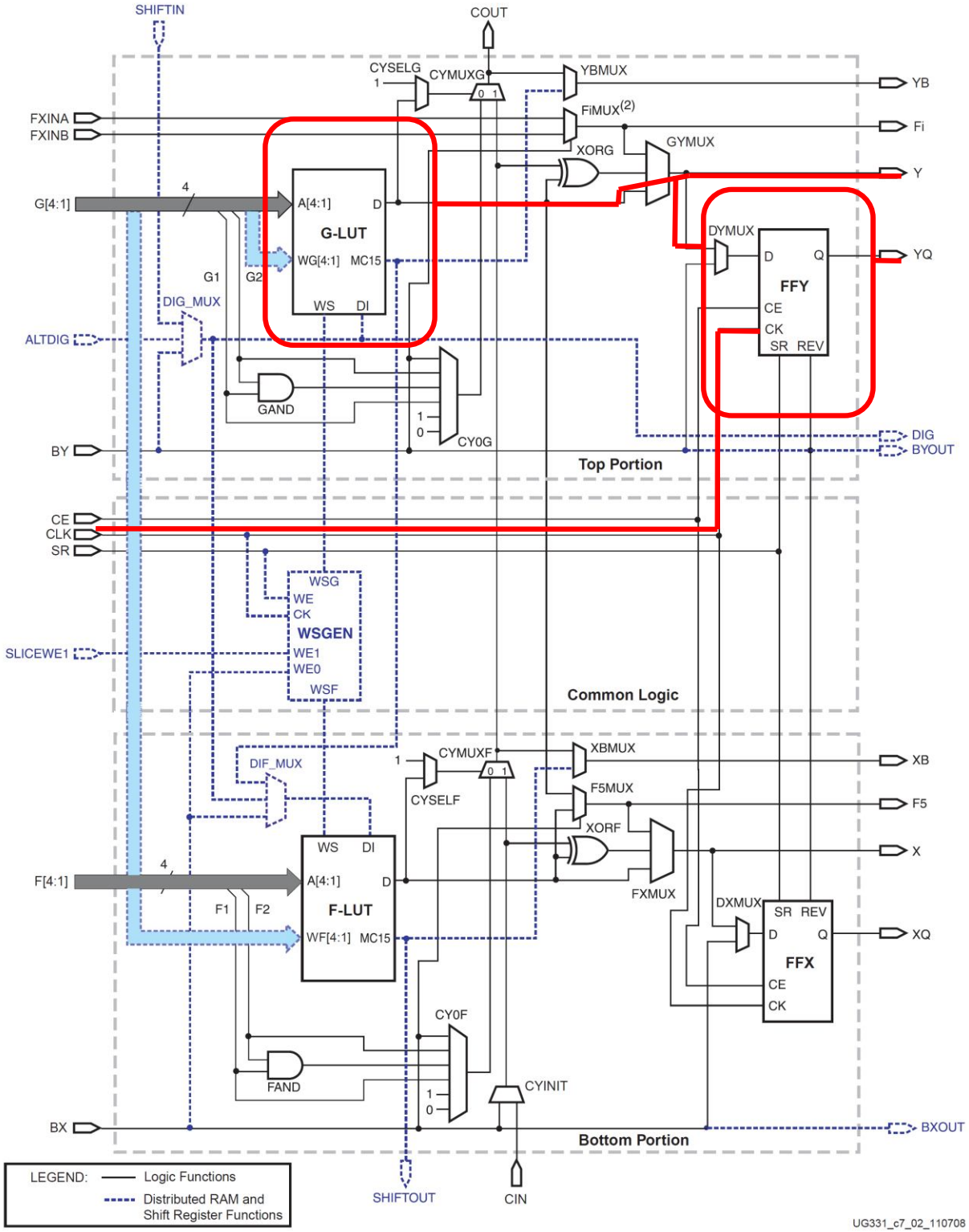
Using a lookup table (LUT) to model a gate network.

Bitstream: 0010001000101111

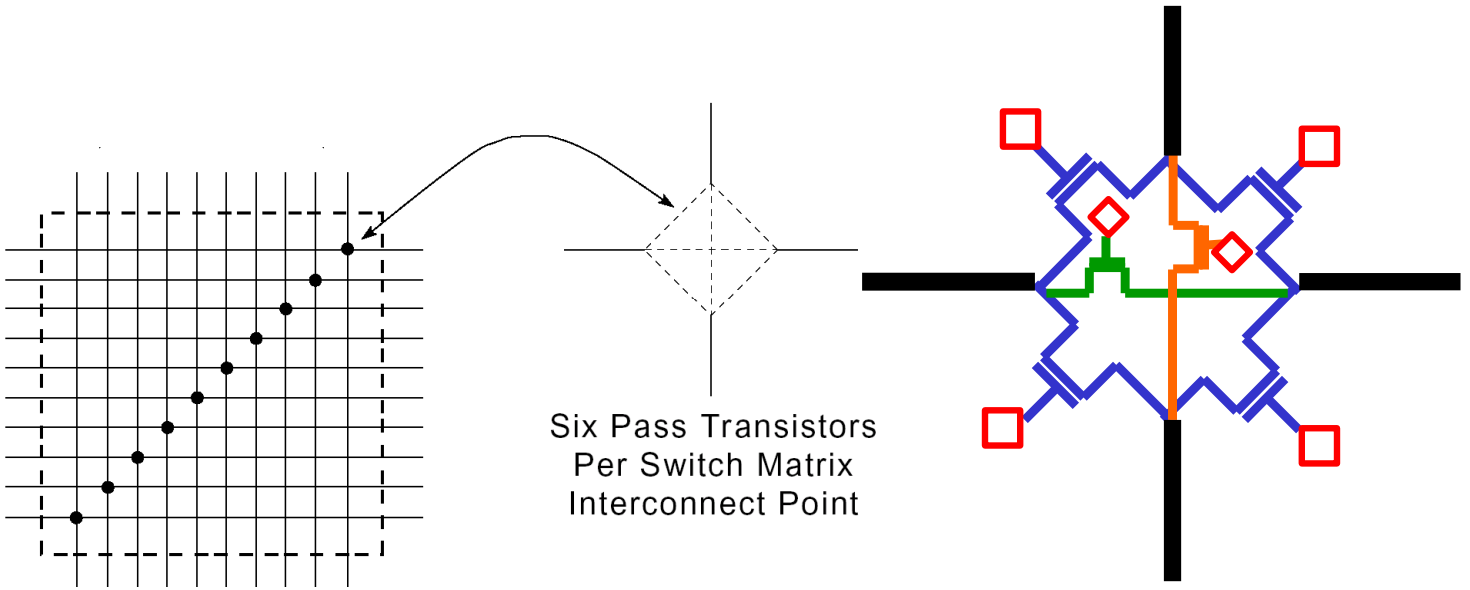
Another Type of Logic Cell



Spartan Logic Cell

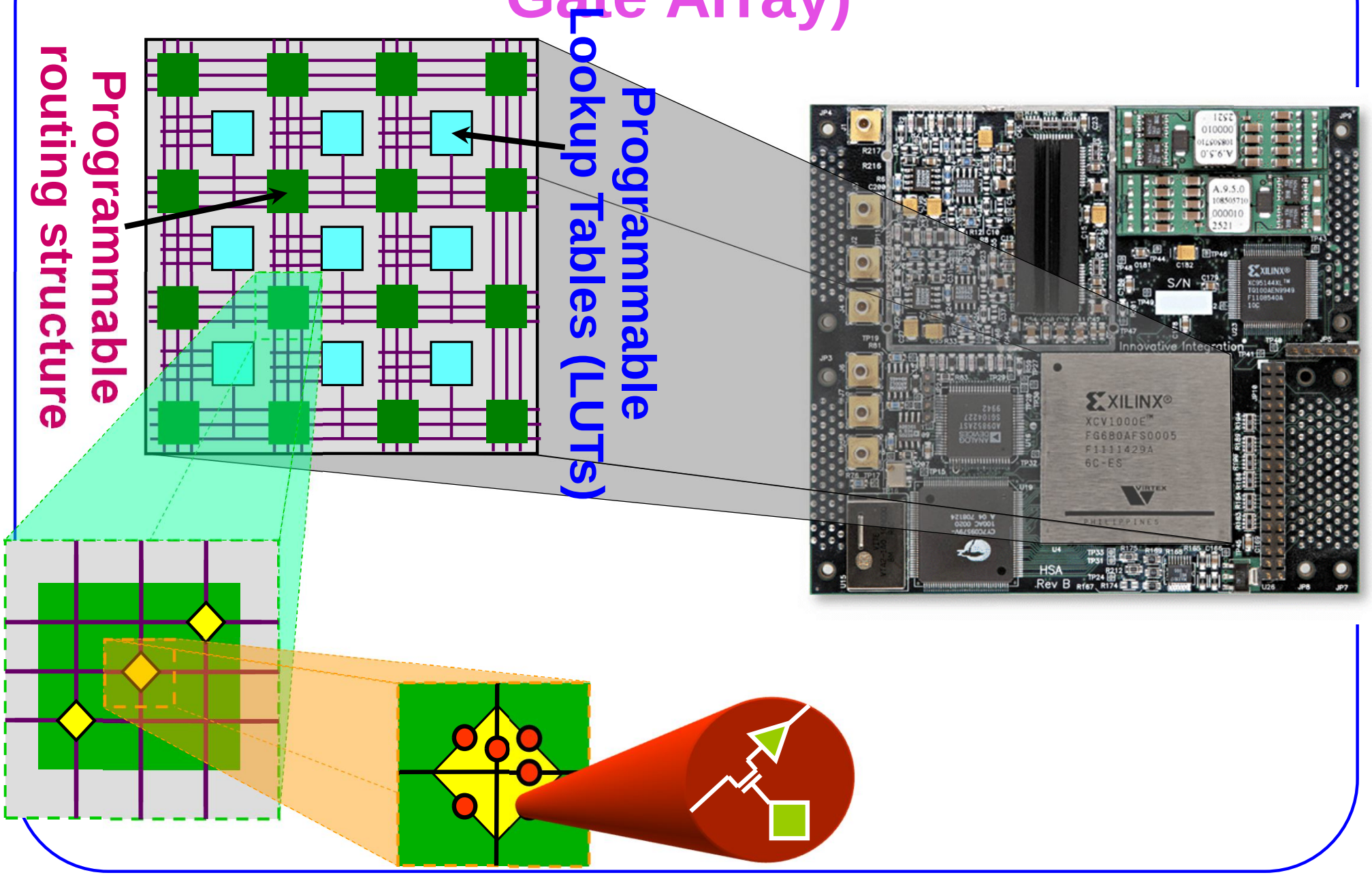


Programmable Switch Matrix (PSM)



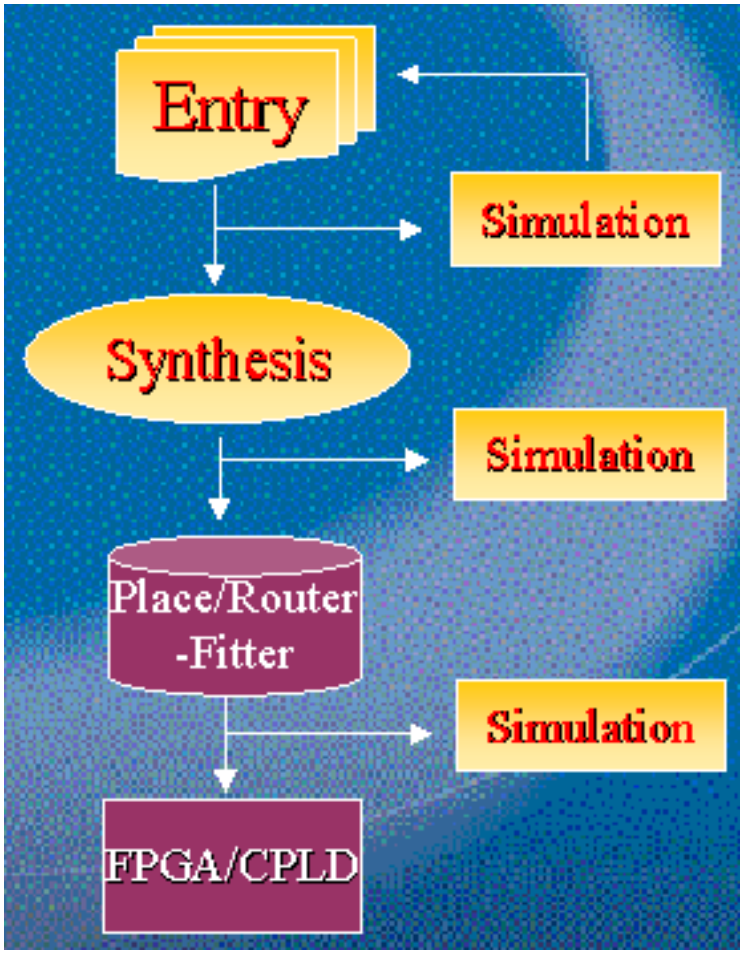
SRAM cells: contents in the bitstream

SRAM-Based FPGA (Field Programmable Gate Array)

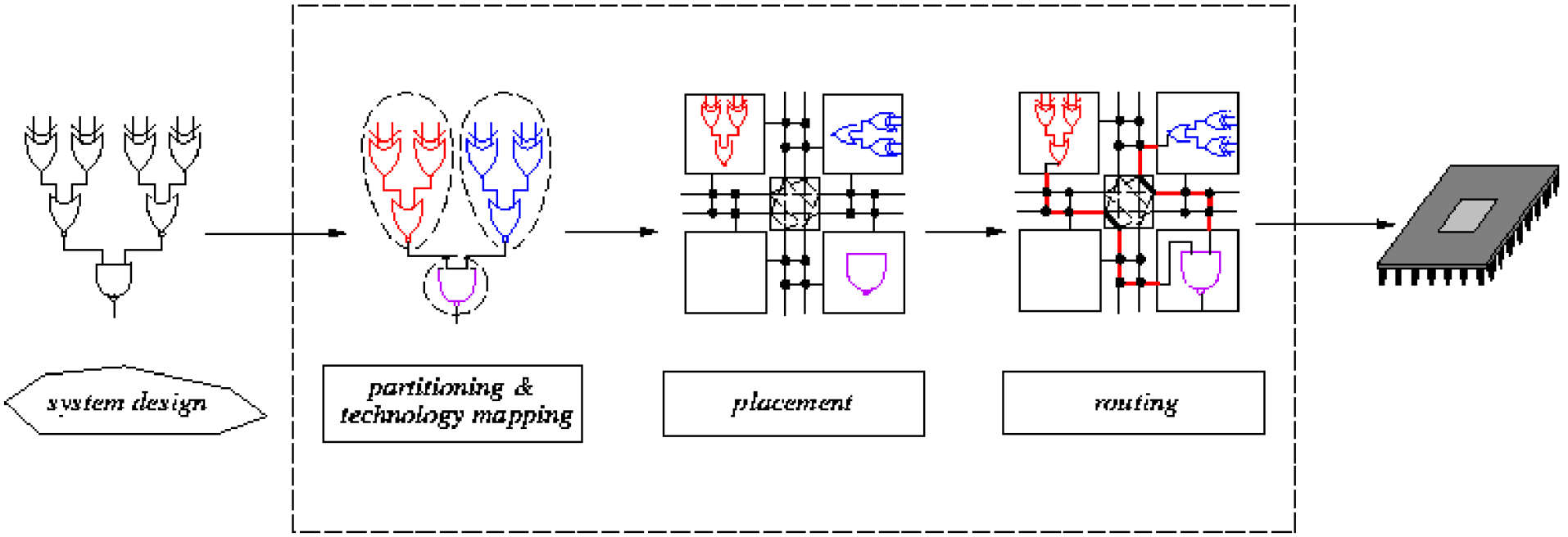


[Entegra]

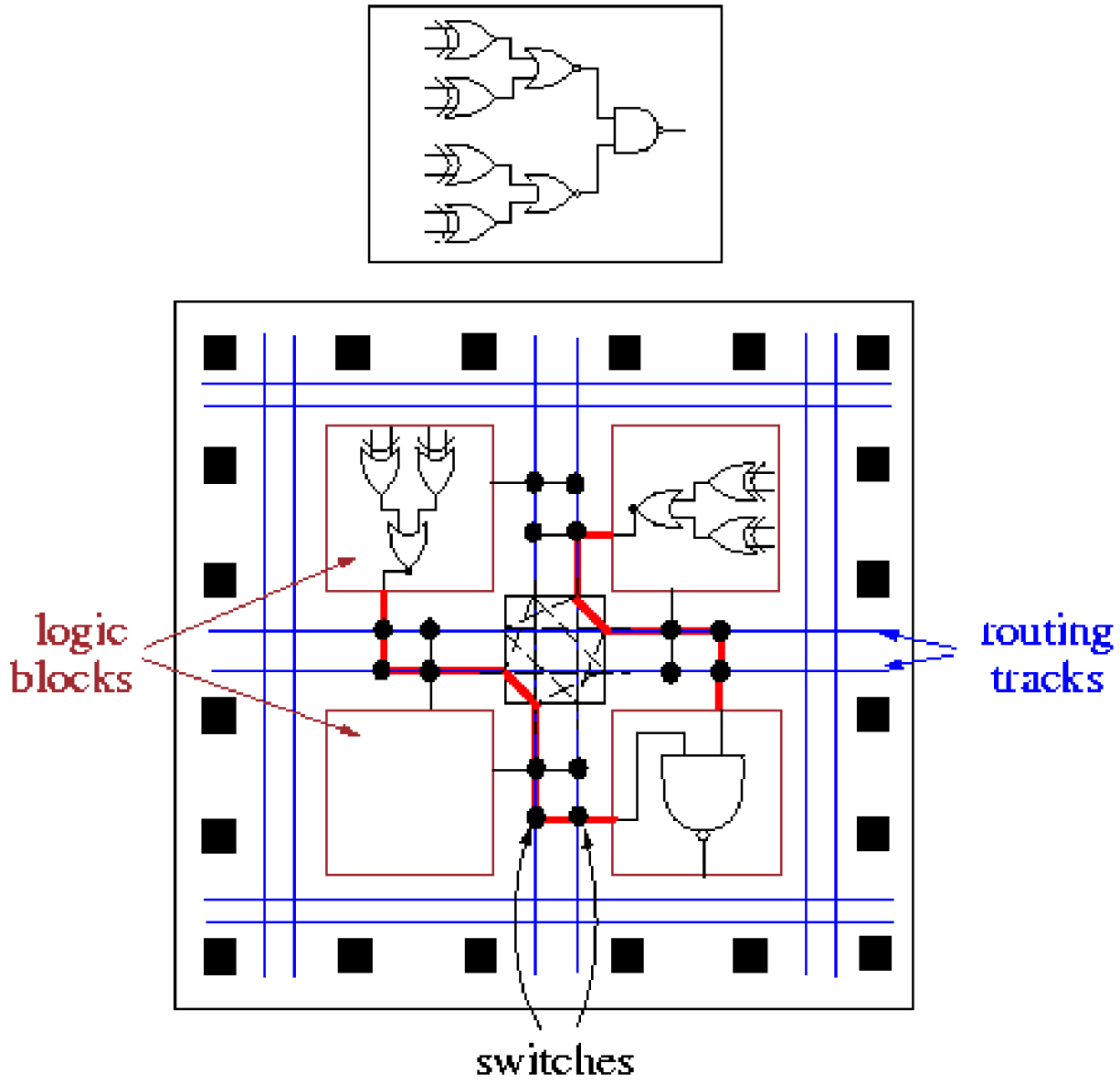
Design Cycle for FPGAs



FPGA Placement & Routing



FPGA Placement & Routing



Modern FPGA Architecture