# This is the title of the document

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## 0. Introduction

Before using this template consider using the file from Lab 6 or Final project as this template is not as refined as those!

This is a template. Note: The LATEX code is open source, github link.

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### 1. Section on inserting

This task was a introductory task...

#### 1.0. Code

```
library ieee;
                                                                                          VHDL
    use ieee.std_logic_1164.all;
 3
    -- This is an example of VHDL
 4
 5
    entity Example is
         port(SW : in std_logic_vector(9 downto 0);
 6
               LEDR : out std_logic_vector(0 to 9));
 7
 8
    end Example;
 9
    architecture structural of Example is
10
11
         signal a : std_logic;
12
         signal b : std_logic;
13
         a \leftarrow ((SW(9) \text{ or } SW(8)) \text{ and } (SW(8) \text{ or } SW(7)));
14
         b \leftarrow ((SW(9) \text{ and } SW(6)) \text{ or } (SW(6) \text{ and } SW(7)));
15
         LEDR(0) <= ((a \text{ and } b) \text{ and } SW(0));
16
17
         LEDR(1) <= ((a or b) and SW(1));
18
         LEDR(2) \leftarrow ((a nand b) and SW(2));
19
         LEDR(3) <= ((a nor b) and SW(3));
20
         LEDR(4) <= ((a \times b) \text{ and } SW(4));
21
         LEDR(5) <= ((a \times b) \text{ and } SW(5));
22
         LEDR(6 to 8) <= "000";
23
         LEDR(9) <= '1'; --This LED signifies power on
    end structural;
```

Code 1.0: Example of code inserting

```
library ieee;
                                                                 Example Code
   use ieee.std_logic_1164.all;
   -- This is another example of VHDL
 4
 5
   entity simple is
       port(SW : in std_logic_vector(9 downto 0);
 6
7
             LEDR : out std_logic_vector(0 down 9));
8
   end simple;
9
10
   architecture structural of simple is
11
12
        LEDR <= SW; -- LED signifies power on for each switch
13
   end structural;
```

Code 1.1: Without optional argument

## 1.1. Simulation results

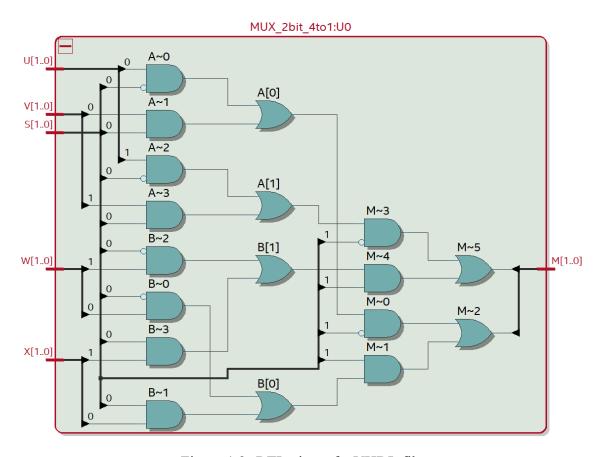
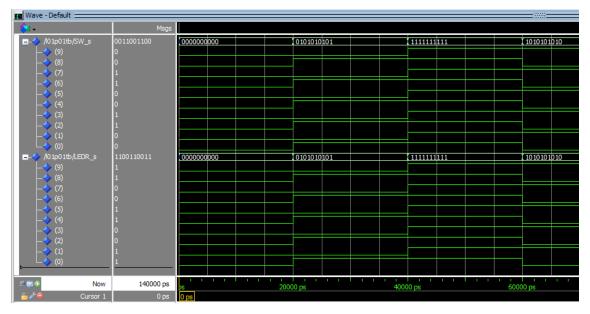
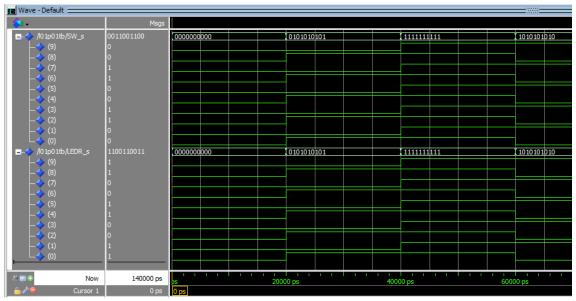


Figure 1.2: RTL view of a VHDL file

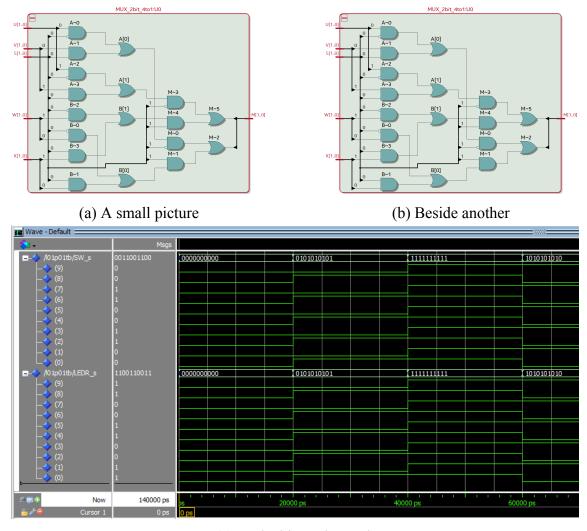


(a) First subfigure, simulation



(b) Second subfigure, yes the same picture

Figure 1.3: Simulation results, doubled up



(c) And a big underneath

Figure 1.4: All results combined together

## 2. Referencing

In this section we will reference the figures in this code and linking them.

#### 2.0. In document linking

To start with you can reference the figures like Code: 1.0 or Figure: 1.2. This will also link them so you can click on the pdf/render and it will jump to the figure.

Note, figures work well, with this as clicking the link brings you to the top of the figure, for codes you get to the bottom/caption instead. This is due to the way captions is added to the code blocks to keep them working for multipage blocks.

#### 2.1. websites

For referencing external link like a URL. there are two ways www.example.com makes all of it visible, best for printing, if you want an embedded link in text do like this. You can see by clicking it both should lead to the same website.