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Semester : 5 subject : Microprocessor
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Pg No: 1/5 of Q.3 Sign : ICG Karan

A). Timing diagram for write operation in minimum mode is as described below :-

i. When processor is ready to initiate the bus cycle it applies a pulse to ALE during T1. Before the falling edge of ALE, the address, BHE, M/IO, DEN, and DT/R must be stable i.e DEN = High and DT/R = 0 for input or DT/R = 1 for output.
ii. At ~~latching~~ trailing edge of ALE, ICs 74LS373 or 8282 latches the address.
iii. During T2 the address signals are disabled and S3-S7 are available on AD16/S3-AD19/S6 and BHE/S7. Also DEN is lowered to enable transceiver.
iv. Incase of input operation, RD is activated during T2 and AD to AD15 go in High impedance preparing for input.
v. If memory or I/O interface can perform the transfer immediately there are no wait states and data is output on bus during T3.

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vi. After the data is accepted by processor RD is raised high at beginning of T4.
vii. Upon detecting this transition during T4 the memory or I/O device will disable its data signals.
viii. For an output operation, processor applies WR=0 and then the data on data bus during T2.
ix. In T4, WR is raised high and data signals are disabled
x. For either input or output operation, DEN is raised during T4 to disable the transceiver. Also M/IO is set according to next transfer at this time or during next T1 state. Thus length of bus cycle in 8086 is four clock cycle. If the bus is to be inactive after completion of bus cycle, then the gap between successive cycles is filled by ideal state clock cycles

When memory or I/O device is not able to respond quickly during transfer, wait states (TW) are inserted between T3 and T4 by disabling the ready input of 8086. The bus activity during wait state is same as during T3

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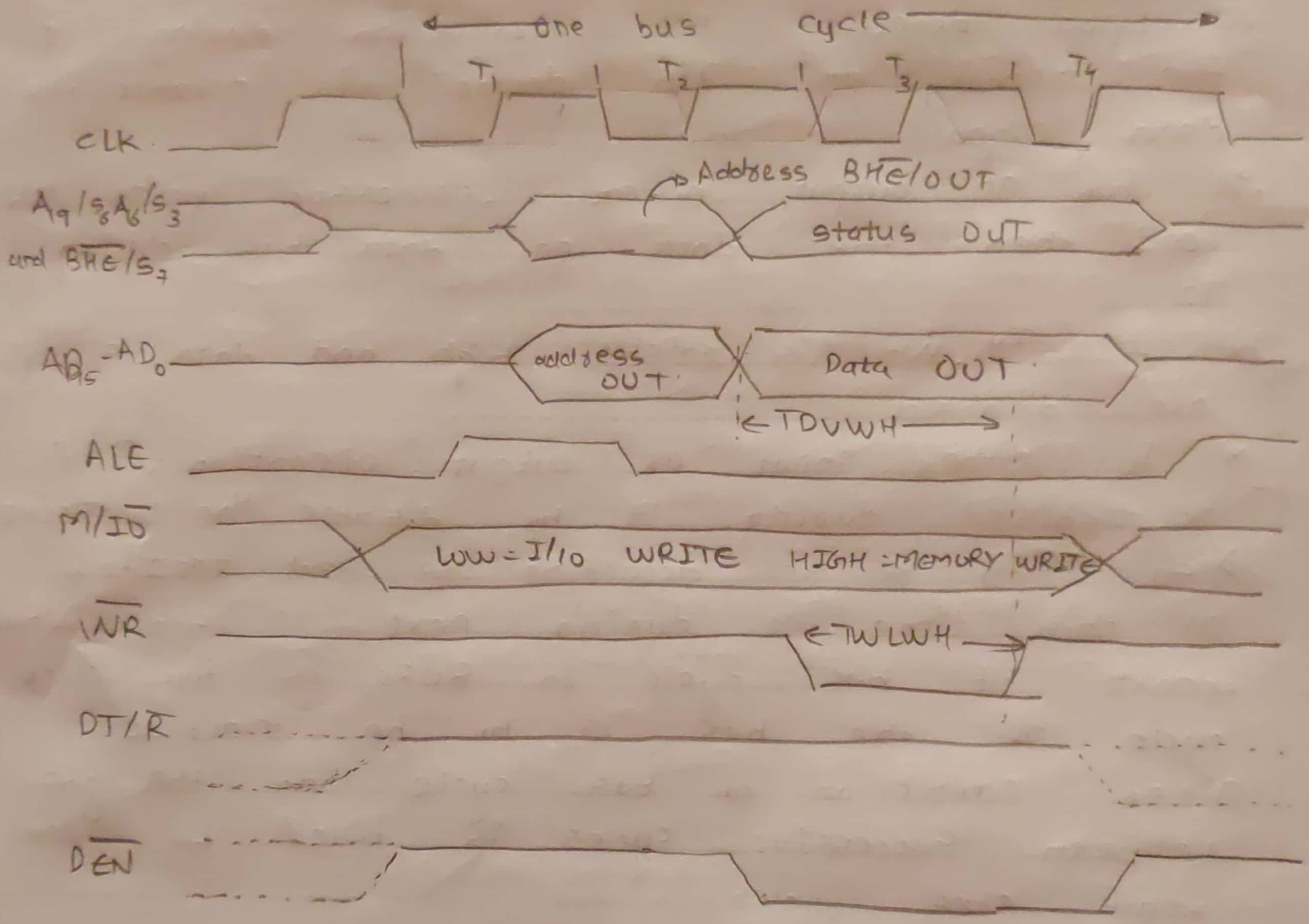

Write operation

Timing diagram for write operation in minimum mode of 8086

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B). Algorithm Assembly language program.

```
Data        SEGMENT:
            Block   DB  'ABCDEEDCBA'
            Pal     DB  00H.
Data        ENDS.
EXTRA       SEGMENT:
Code        SEG Block2  DB  Dup(?)
EXTRA       ENDS.

Code        SEGMENT
            ASSUME  CS: Code, DS: Data, ES: Extra
            MOV     AX, Data
            MOV     DS, AX.
            MOV     AX, Extra
            MOV     ES, AX
            LEA     SI, Block1
            LEA     DI, Block2 + 9
            MOV     CX, 000AH.
Back:       CLD
            LODSB
            STD
            STOSB
            LOOP    Back.
            LEA     SI, Block1
            LEA     DI, Block2
            MOV     CX, 000AH.
            CLD
```

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```
REPz    CMPSB.
        JNZ     SKIP
        MOV     Al, 01H
SKIP :  INT3.

code    ENDS
        END.
```