ELEC 5280 Homework 2

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Problem 1

Using the **TSMC 22nm CMOS PDK (Cadence library name: tsmcN45)** provided (*see **[Tutorial]02 Homework 2 TSMC 22nm CMOS Characterization with Cadence**), simulate the NMOS model named "**nmos_rf_lvt_nw**" with W = 1 μm, L = 30 nm and number of fingers = 4, i.e., the total width = 4 μm, in Cadence. For 22nm process, you can use ideal inductors and capacitors to bias the device to set Vgs = 0.4 V and Vds = 0.5V. Perform a S-parameter simulation from **200 MHz to 200 GHz**.

a) Plot the six equivalent circuit model components listed in Table 1 over the specified frequency range. For the capacitance, you will need to use the derivative function in the Calculator in Spectre.
b) Plot minimum noise figure (in dB) over the specified frequency range.
c) Determine f_T from the simulation result (|h21|). (You may need to broaden the sweep range to, e.g., **800GHz**)
d) Determine f_{max} by extrapolating the maximum power gain (G_{max}). (You may need to broaden the sweep range to, e.g., **800GHz**)

Problem 2

In this problem, you will design a standard common-source Low Noise Amplifier (LNA) with source degeneration shown below using the **TSMC 22-nm CMOS process (tsmcN22)**. You are tasked with the design of the differential LNA begin by adapting the provided single-ended common-source LNA topology into a differential configuration. Next, you will evaluate two noise reduction techniques. The first method introduces C_d to decouple the input resonant circuit Q and Cgs. The second method reduces the noise contribution from the cascode device (M2) by increasing the impedance at node X at the center frequency. For transistors, use the RF transistor model 'nmos_rf_lvt_nw' of 'tsmcN22'. For capacitors, resistors and inductors, use either ideal inductors of 'analogLib' named 'ind'.

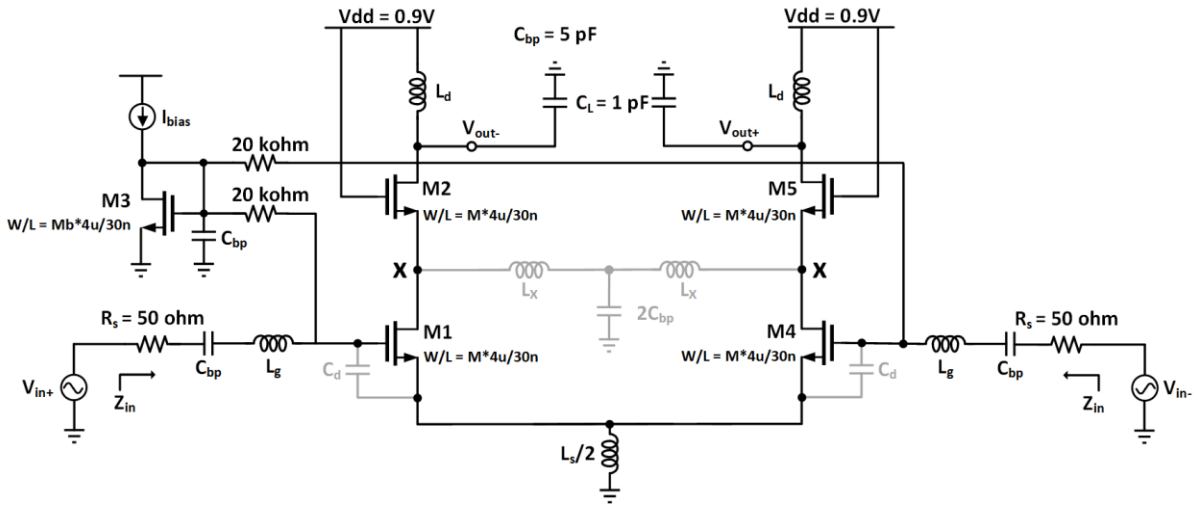

Figure. Schematic of the corresponding differential LNA.

Specifications:

1. Input impedance matching: |S11| < -12 dB
2. Center frequency f0 = 28 GHz
3. Voltage gain > 12 dB at f0
4. Power consumption < 30 mW (the lower, the better) with Vdd =0.9 V
5. Noise figure < 5 dB
6. IIP3 > -15 dBm

Questions:

a) Simulate the single transistor M1. Plot gm vs. Iden1 (current density) and fT vs. Iden1 by sweeping Ids, M1 with a fixed width, e.g., 4μm.
b) Determine Ibias and M (Multiplier of M1 and M2) that gives the optimal fT and gm for minimizing NF. What is resulting input resonant circuit Q? (For the size of transistor M3, Mb is typically very smaller than M, e.g., Mb=10%M)
c) Determine Lg and Ls using Cgs and fT to provide the required input matching. Assume Ls and Lg have a Q of 15 at f0, compute the series resistance value and include it in the simulation (use 'ind' and 'res' from 'analogLib').
d) Determine Ld such that the output node is tuned at f0. Assume Ld have a Q of 15 at f0, compute the series resistance value and include it in the simulation (use 'ind' and 'res' from 'analogLib').
e) Plot the gain (Vout/Vin), noise figure (NF) and input impedance (Zin) vs. frequency from 0.1 to 50 GHz.
f) Perform a PSS analysis at f0 to determine the 1-dB compression of this LNA by sweeping the input port power.
g) Using PSS analysis, perform a two-tone test to determine the IIP3 of the LNA using signals at f0 and f0+800MHz. (Optional: You can use hb and PAC analysis to simulate the IIP3 again and compare results for **bonus credits**).
h) Using sp analysis, plot the K factor vs. frequency from 0.1 to 50 GHz. Comment on the stability of your designed LNA based on the simulation result.
i) Using sp analysis, plot noise circles with noise ranges from 1 dB to 10 dB and gain circles with gain ranges from 10 dB to 20 dB, both at f0. Comment on the trade-off between gain and noise based on the circles.
j) Now, add Cd between the gate and source terminal of M1, plot NF at f0 vs. Cd, make sure that you adjust Lg and Ls for each value of Cd to maintain the input matching at f0. How much is the improvement in NF? What happened to the amplifier gain?
k) With the Cd and the Lg, perform a sweep of the input device width, is there a new optimal width that gives lower NF? If so, what is it and what is the NF?
l) Now, add Lx at the cascode node by first estimating the parasitic capacitance at node X. How much is the improvement in NF? What happened to the amplifier gain?

Contents

ELEC 5280 Homework 2 Answers

Problem 1

a) Plot the six equivalent circuit model components listed in Table 1 over the specified frequency range. For the capacitance, you will need to use the derivative function in the Calculator in Spectre.

According to the test bench for an NMOS device given in Problem 1, I build the circuit in Cadence as shown in Figure 1.

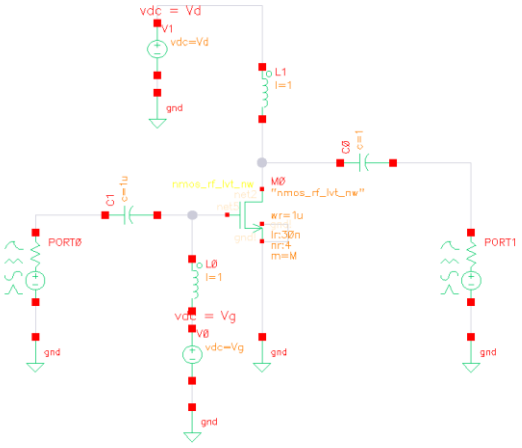

Figure 1. Circuit for Problem 1

Using the equations listed in Table 'equivalent circuit model components based on Y-parameters', I did dc and sp simulation to calculate all the values. The components value over frequency range are shown below.

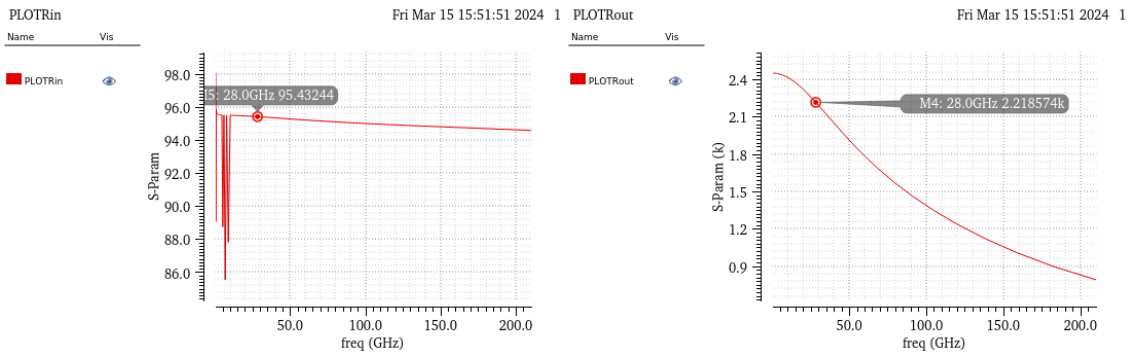

Figure 2. Input and output resistance

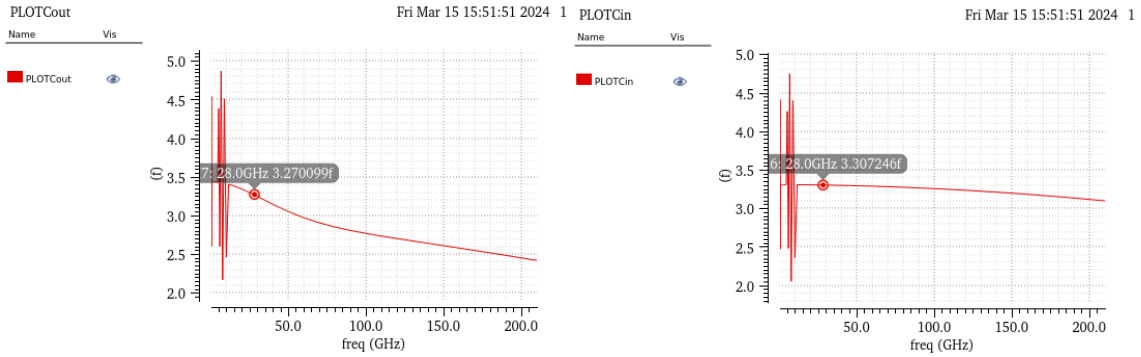

Figure 3. Input and output capacitance

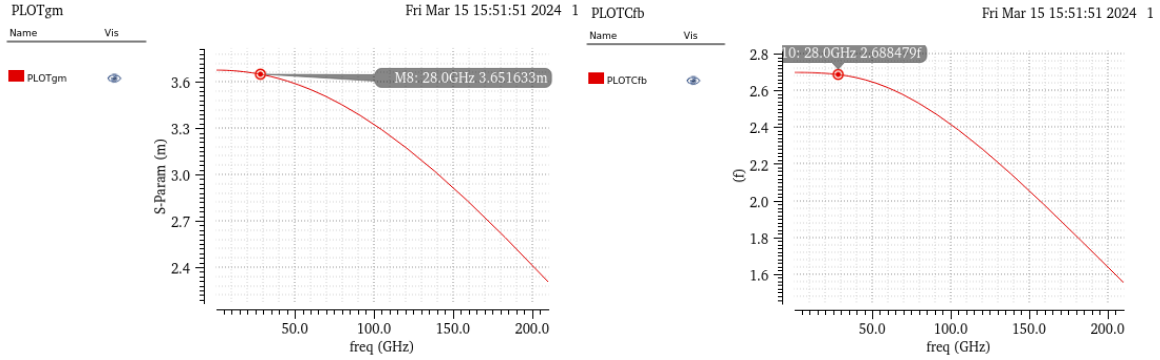

Figure 4. Transconductance and Feedback Capacitance

Referring to the second question on frequency point selection, I listed the individual component values at 28 GHz.

R_{in}	95.4 Ω
R_{out}	2.21k Ω
C_{in}	3.27fF
C_{out}	3.31fF
g_m	3.65mS
$C_{feedback}$	2.69fF

b) Plot minimum noise figure (in dB) over the specified frequency range.

The minimum noise figure of the circuit is shown in Figure 5 from 200MHz to 200GHz, where the value at 28GHz is highlighted.

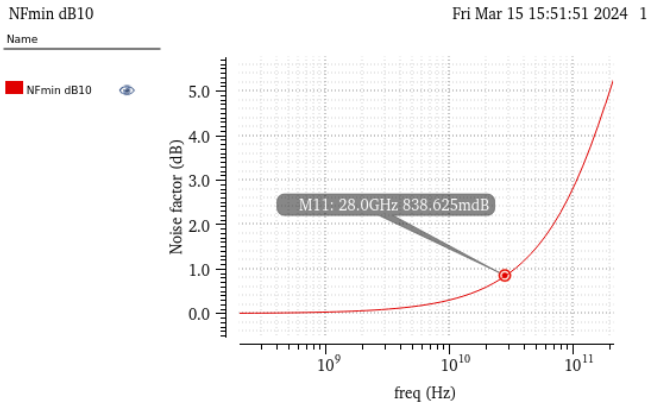

Figure 5. NF_{min} over frequency range

c) *Determine f_T from the simulation result (|h21|). (You may need to broaden the sweep range to, e.g., **800GHz**)*

The value of h21 represents the ratio of output current to input current. The frequency corresponding to when the value of this ratio decreases to 1 is the cutoff frequency of the circuit, which corresponds to the point at which the dB value decreases to 0. Therefore, by applying the cross function in cadence to the hp21 curve, we can obtain f_T.

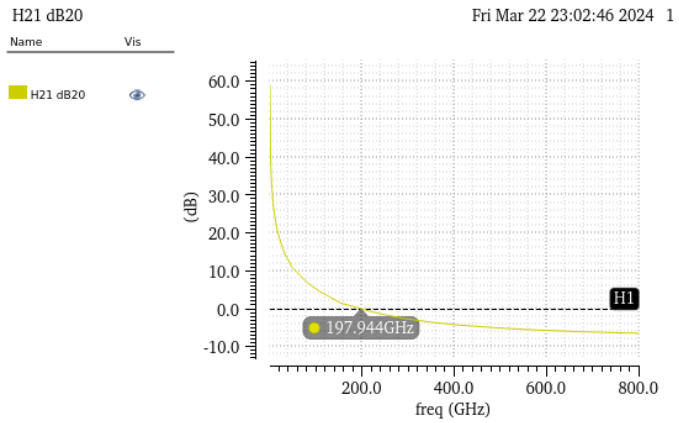

Figure 6. h21 over frequency range

After expanding the frequency range to 800Ghz, the f_T can be obtained at 197.9GHz.

d) *Determine f_{max} by extrapolating the maximum power gain (G_{max}). (You may need to broaden the sweep range to, e.g., **800GHz**)*

The f_{max} is defined when G_{max} drops to 0 dB. In Figure 7, it can be seen that f_{max} equals to 203.3GHz.

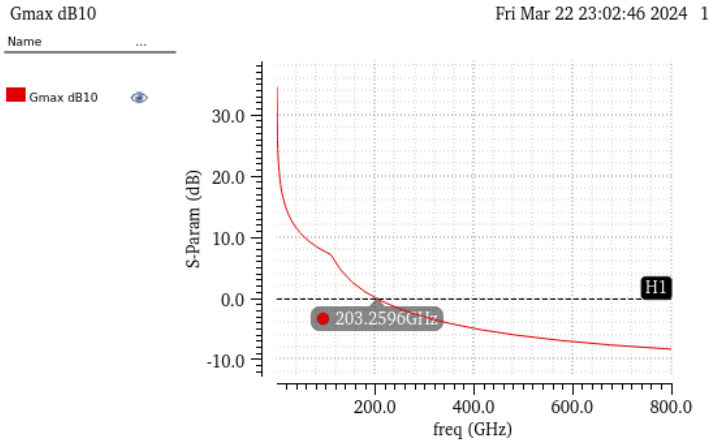

Figure 7. G_{max} over frequency range

Problem 2

a) Simulate the single transistor M1. Plot gm vs. Iden1 (current density) and fT vs. Iden1 by sweeping Ids, M1 with a fixed width, e.g., 4μm.

The simulation circuit for single transistor is the same as the circuit in problem 1. During the simulation, I swept V_g in dc simulator from 0 to 1V. After the simulation, gm, f_T anf I_{den} versus V_g are plotted in Figure 8.

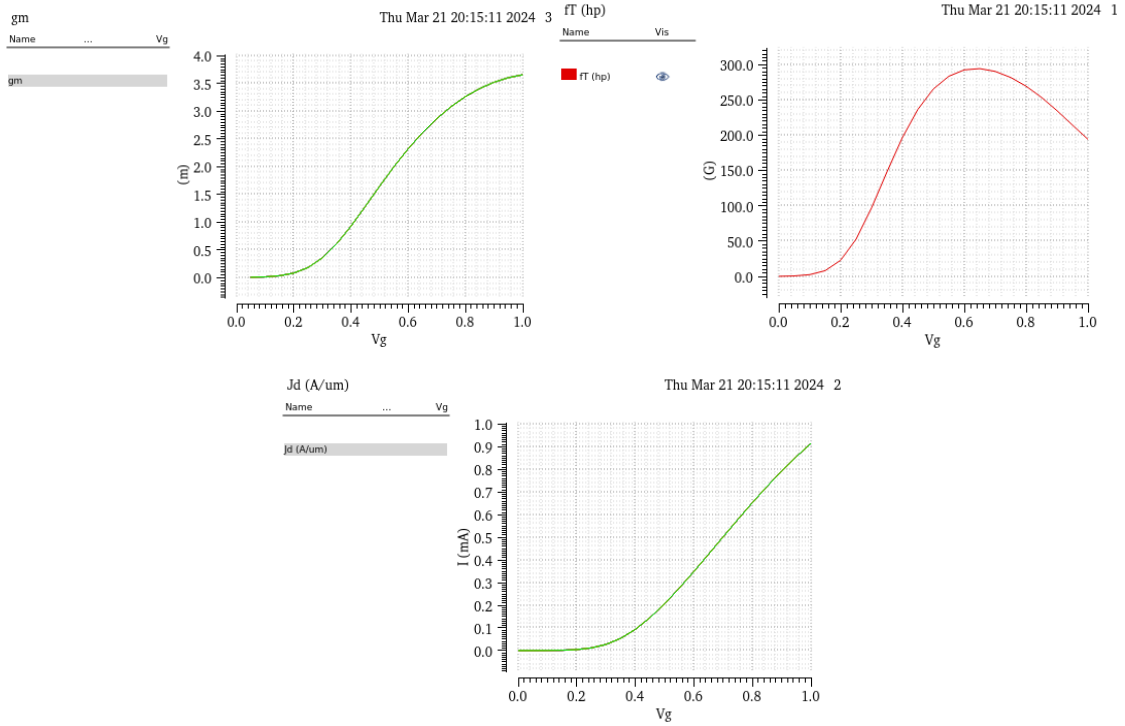

Figure 8. gm, f_T anf I_{den} of single transistor

After changing the x axis of gm and f_T to I_{den}, the required gm vs. Iden1 (current density) and fT vs. Iden1 can be plotted in Figure 9.

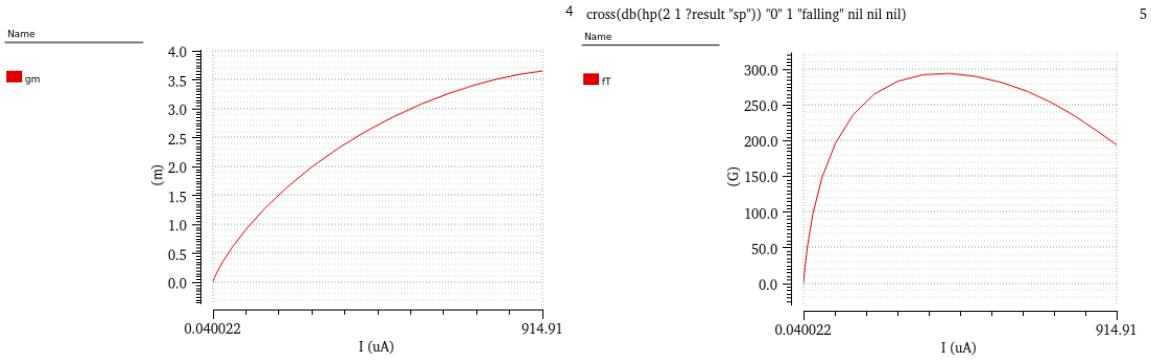

Figure 9. gm, f_T vs I_{den} of single transistor

However, in the given single-ended LNA, the gm, f_T vs I_{den} can also be obtained by sweeping I_{bias}. This is due to the topology of a current sink with M3 which serves as the bias for M1. When M1 and M3 are both in saturation region, the current flows through M1 can be determined simply by the ratio of multipliers, which is shown below:

$$\frac{I_{dsM1}}{I_{dsM3}} = \frac{M}{M_b} \tag{1}$$

Considering the power consumption specification, the drain current of single ended LNA should be less than 33mA. So I firstly set M to be 10 and Mb to be 1, and do the dc simulation by sweeping Ibias from 0 to 3mA. It is worth mentioning that since it is the current density that is being observed, the value of M takes no effect at this point.

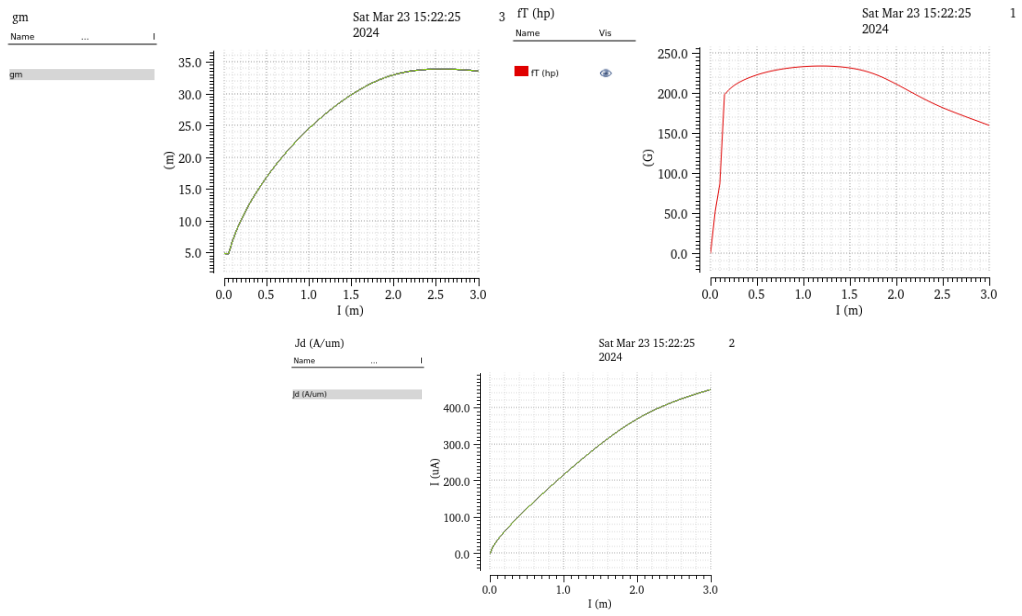

Figure 10. gm, f_T vs I_{den} of single-ended LNA

After changing the x axis of gm and f_T to I_{den}, the required gm vs. Iden1 (current density) and fT vs. Iden1 can be plotted in Figure 11.

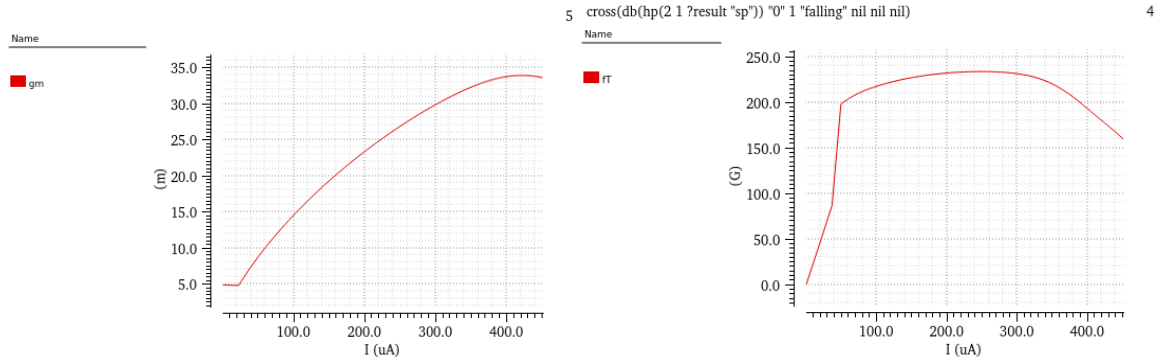

Figure 11. gm, f_T vs I_{den} of single-ended LNA

b) Determine Ibias and M (Multiplier of M1 and M2) that gives the optimal fT and gm for minimizing NF. What is resulting input resonant circuit Q? (For the size of transistor M3, Mb is typically very smaller than M, e.g., Mb=10%M)

To determine the optimal value of all three important parameters, the first step is to figure out the relationship between them.

The gm is the transconductance of the transistor. When drain current is large enough for the transistor to enter saturation region, velocity saturation takes over which leads to the saturation of gm. In order to get minimum noise figure, we choose the suitable I_{den} to make sure gm won't saturate. Thus I_{den} should be smaller than 400uA/um. The next step is to illustrate f_T and NF_{min} vs I_{den}. By setting M to be 10 and Mb to be 1, the dc simulation by sweeping Ibias is done from 0 to 3mA just the same as question (a).

What matters next is how to do sp analysis over the current sweeping range. By using parametric analysis, we can get the value of f_T and NF_{min} at different current biasing point. The required working frequency is 28GHz, so NFmin of 28GHz is extracted.

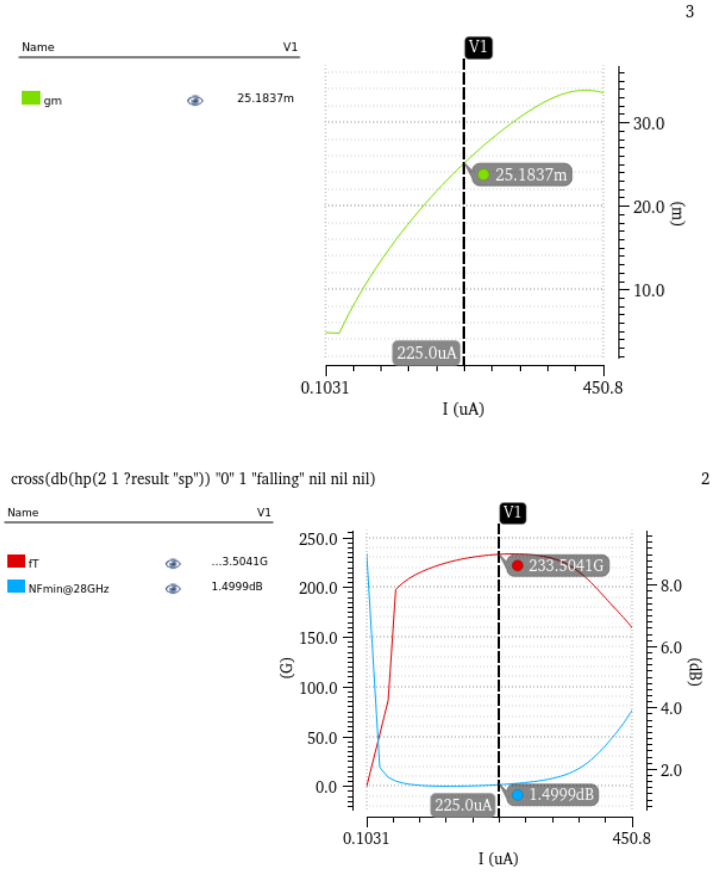

Figure 12. g_m,f_T and NF_{min} vs I_{den} of LNA

Based on the current density range determined previously from g_m, I choose 225uA/um as the current density of single transistor, which gives the optimal $\mathbf{g_m=25.2mS}$, $\mathbf{f_T=233.5GHz}$ and $\mathbf{NF_{min}=1.5dB}$ as can be seen in Figure 12. So the biasing current equals to the product of width of M3(4um) and I_{den} of 225uA/um.

Up to now, $\mathbf{I_{bias}}$ and **M** of this differential LNA is chosen to be **900uA** and **15**, fulfilling all the requirements including optimal parameters and power consumptions at same time.

The resulting input resonant circuit Q can be calculated as below:

$$C_{gs}=\frac{g_m}{2\pi f_T}=\frac{25.2\times10^{-3}}{6.28\times233.5\times10^{9}}=17.2\,fF$$
$$Q=\frac{1}{2\omega_0 C_{gs}R_0}=\frac{1}{2\times6.28\times28\times10^{9}\times17.2\times10^{-15}\times50}=3.31 \quad (2)$$

Input resonant circuit Q is 3.31, which is not quite good.

c) *Determine Lg and Ls using Cgs and fT to provide the required input matching. Assume Ls and Lg have a Q of 15 at f0, compute the series resistance value and include it in the simulation (use 'ind' and 'res' from 'analogLib').*

The topology of given single-ended LNA is source degeneration LNA. The source degeneration inductor is added for negative feedback. With L_s contributing to the real part of the input impedance, the conjugately power match can be easily achieved. However, the trade-off between better power match and lower noise figure leave much to discuss when choosing the degeneration inductance. It is still worth mentioning that L_S makes it easier to satisfy S_{11} and NF_{min} requirments. Below equation gives the calculation of single ended LNA input impedance.

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + j[\omega(L_s + L_g) - \frac{1}{\omega_0 C_{gs}}] \tag{3}$$

Basically, there are two ways to calculate the required L_s and L_g for input matching. In this work, I initially use formulas to calcula the theoretical value of them and then made some adjustments to the S_{11} based on the input Smith Chart. The calculation of series resistance is also shown below.

$$\begin{aligned} L_s &= \frac{R_0}{2\pi f_T} \\ \omega_0 &= \sqrt{\frac{1}{(L_s + L_g)C_{gs}}} \\ R &= \frac{\omega L}{Q} \end{aligned} \tag{4}$$

In the second step, I use sp simulator to sweep L_s and L_g at 28GHz separately. Then, the conjugately matched S_{11} is plotted in Figure 13. However, this is only the perfect match without considering the output part of the circuit. After trying to tune the output node at 28GHz in (d), S_{11} will inevitably deviate from the initial value. At this point, L_s and L_g are chosen to be 95pH and 500pH respectively.

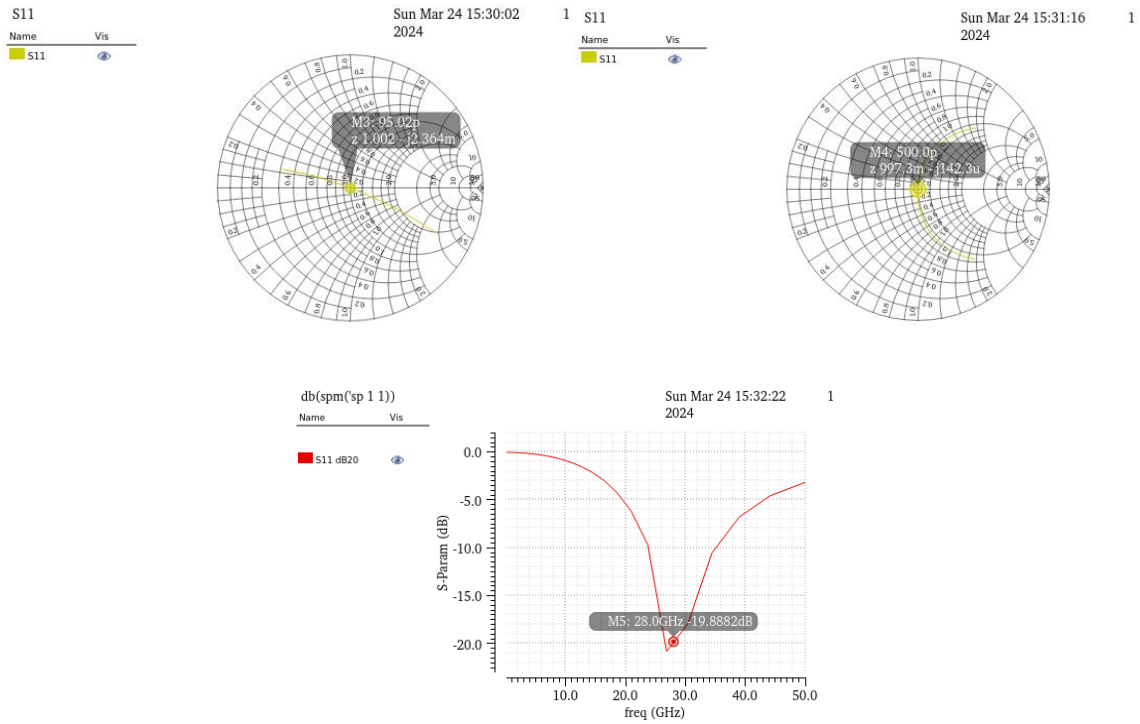

Figure 13. a)first step of sweeping L_s ;b)second step of sweeping L_g ;c)S_{11} of LNA after doing input matching

d) Determine Ld such that the output node is tuned at f0. Assume Ld have a Q of 15 at f0, compute the series resistance value and include it in the simulation (use 'ind' and 'res' from 'analogLib').

In order to tune the output node at f_0, I need to select output inductance, such that it resonates with the transistor output capacitance at 28GHz. The output inductance can be approximately estimated through C_{gd}. The L_d can be calculated as below.

$$L_d = \frac{1}{\omega^2 C_{gd}} \tag{5}$$

After calculation, smith chart of S11 is used for further tuning. Thus, L_d is chosen to be 33.6pH. However, after deciding the drain inductance of LNA, the whole circuit seen from input port is different. In order to get required impedance match and S parameters, all the three inductance should be tuned again to maximize the satisfaction of the indicators. During the adjustments of L_s, L_g and L_d, it is obvious that S_{11} is much more easier to be tuned while S_{22} can hardly change to lower than -12dB. So the only way to meet the requirements of output tuning is to sacrifice S_{11} to some extent. The final results of tuning are shown in Figure 14 at **L_s=74pH, L_g=500pH and L_d=32.5pH**.

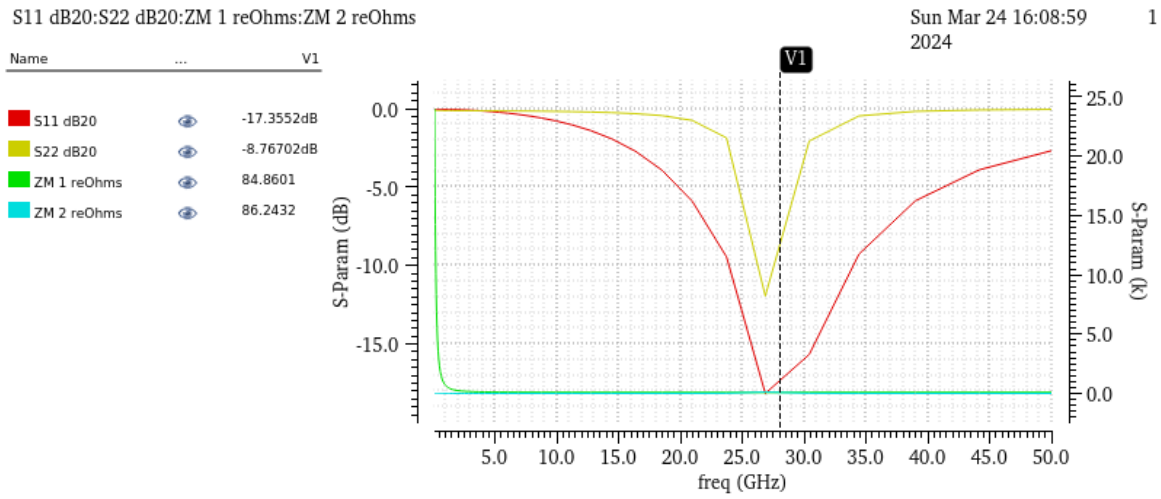

Figure 14. Final results of S_{11}, S_{22} and impedance after input and output tuning

e) *Plot the gain (Vout/Vin), noise figure (NF) and input impedance (Zin) vs. frequency from 0.1 to 50 GHz.*

Up to now, the circuit is determined with certain values of components. The whole circuit is shown in Figure 15. After creating symbol based on the differential LNA, Voltage gain, NF and Z_{in} are plotted separately in Figure 16 and 17.

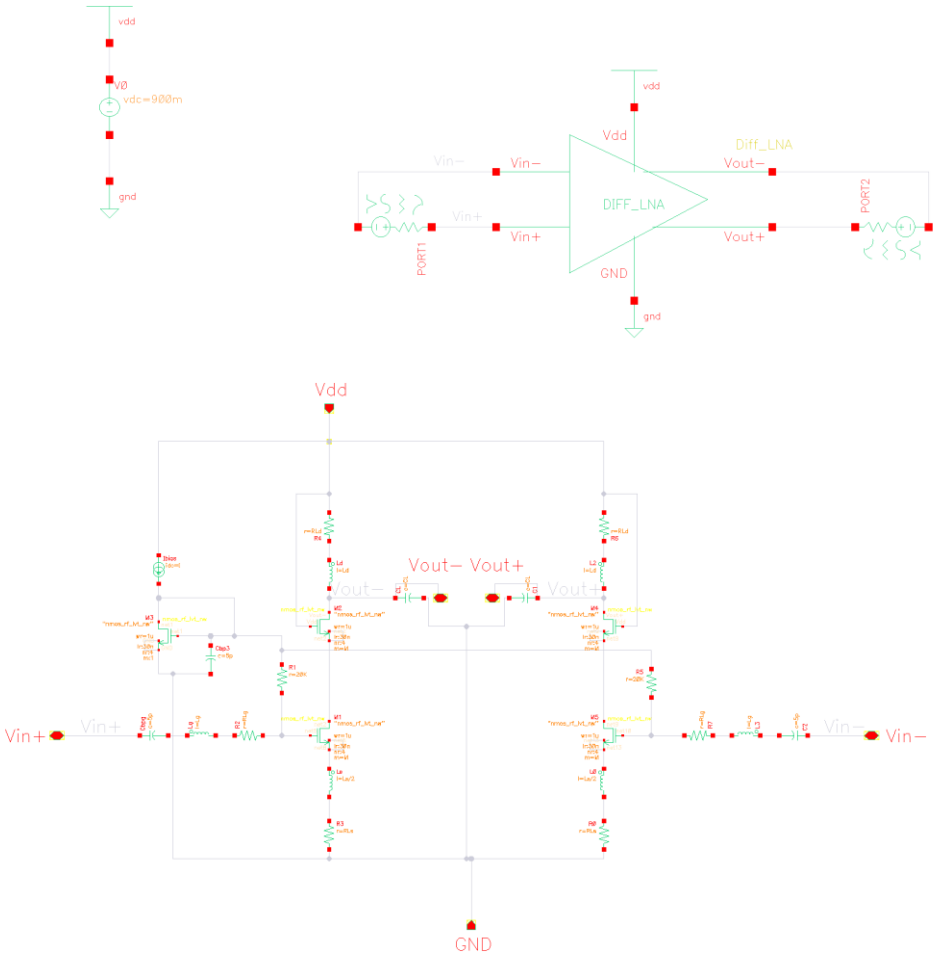

Figure 15. The whole simulation circuit: top part and symbol part

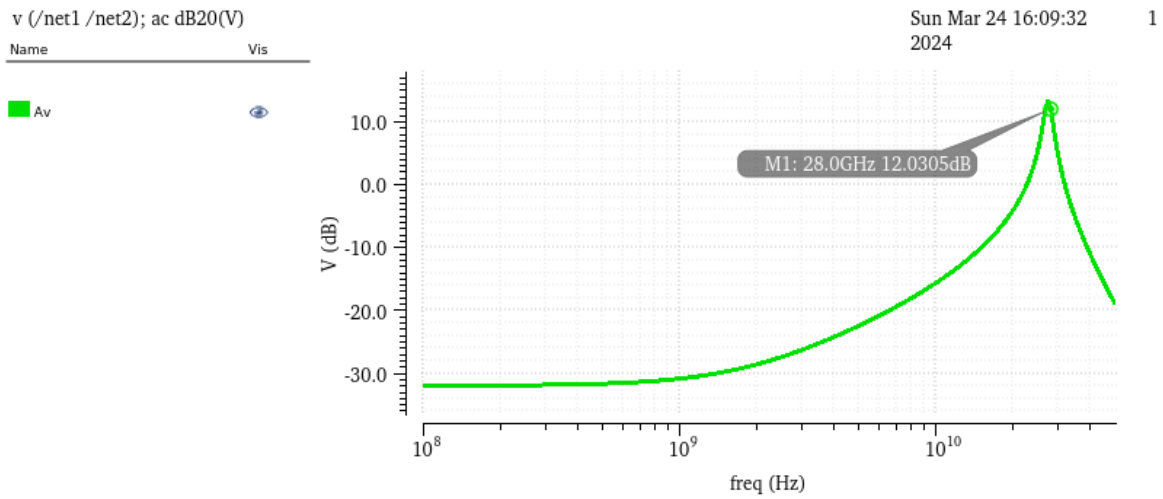

Figure 16. Voltage gain of the circuit

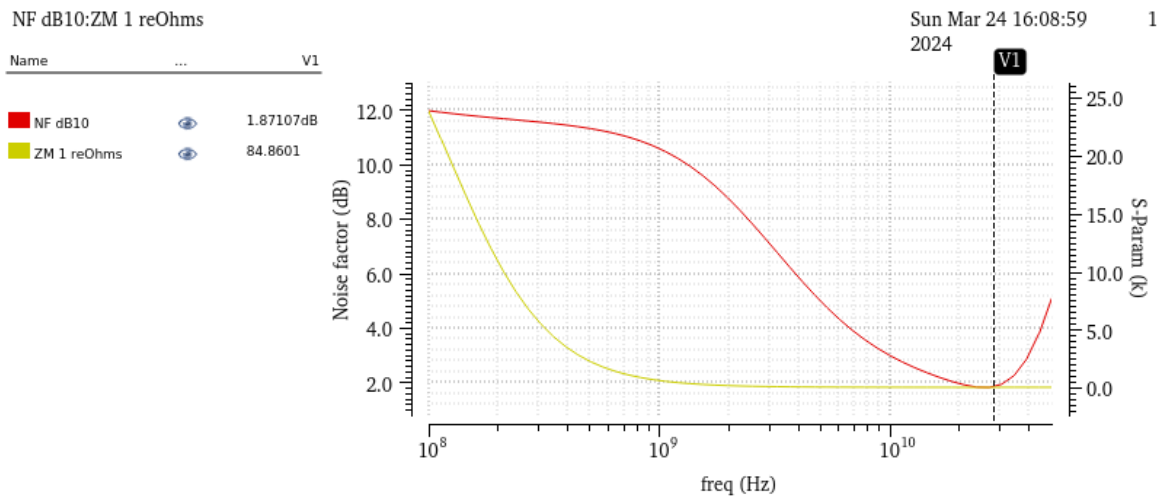

Figure 17. NF and Z_{in} of the circuit over the frequency range

f) *Perform a PSS analysis at f0 to determine the 1-dB compression of this LNA by sweeping the input port power.*

The 1-dB compression characteristic of differential LNA is a large signal parameter. It tells LNA's ability of handling weak input signal without output distortion. The 1dB compression point of LNA is the input power level at which the output power of the amplifier is compressed by 1dB, where non-linearity of the circuit takes in charge. By sweeping input power of port 1 from -50dBm to 10dBm, P_{1dB} of -6.59dBm can easily be extracted as shown in Figure 18, which is quite outstanding.

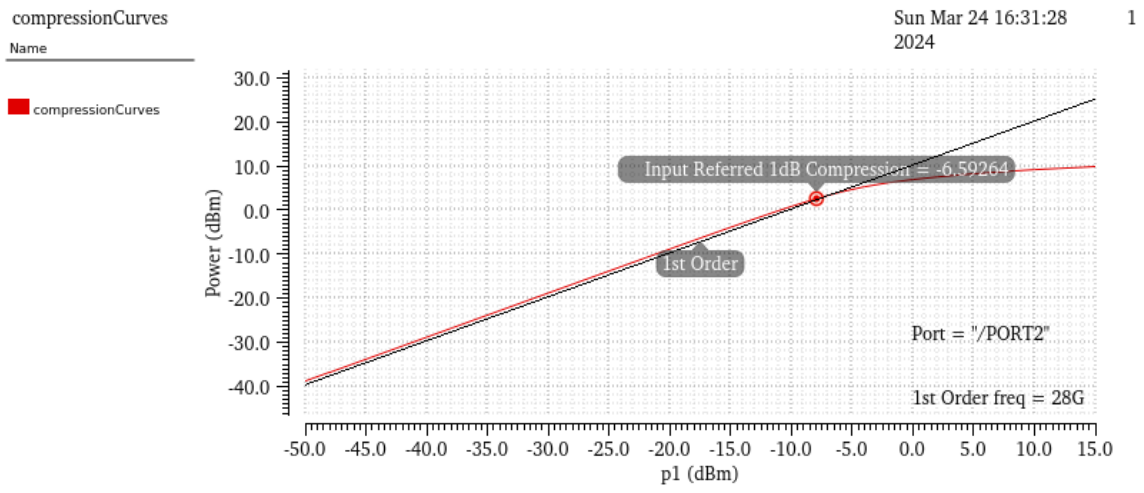

Figure 18. 1-dB compression point of the designed LNA

g) *Using PSS analysis, perform a two-tone test to determine the IIP3 of the LNA using signals at f0 and f0+800MHz. (Optional: You can use hb and PAC analysis to simulate the IIP3 again and compare results for* ***bonus credits****).*

IIP3 is a measure of the linearity of the amplifier, indicating how well it can handle strong input signals without introducing distortion.

Firstly, I use PSS and PAC analysis to perform two-tone test. The first frequency is set to be 28GHz while the second one is 28.8GHz. The second frequency is one interferer for the working frequency. In this kind of analysis, the second frequency is added through PAC, causing the possible distortion at the output port. The PSS and PAC analysis settings are shown in Figure 19, and the obtained IIP3 is 3.98dBm as shown in Figure 20.

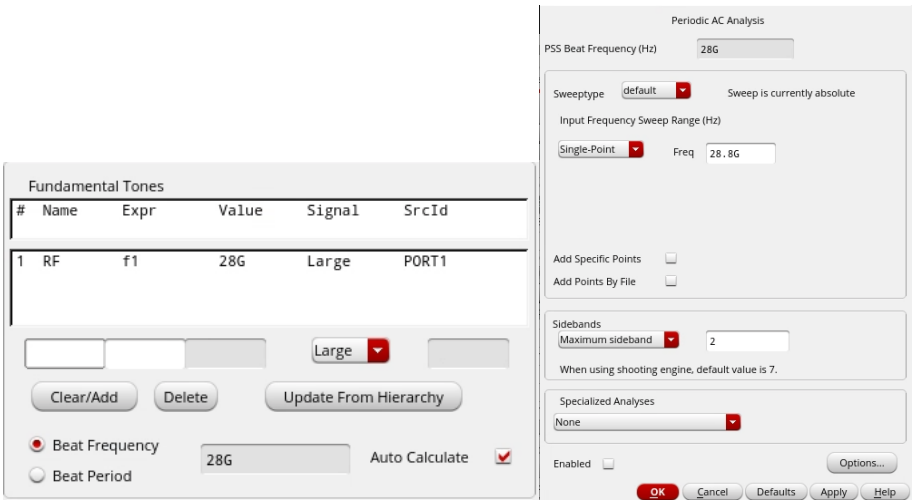

Figure 19. PSS and PAC analysis settings

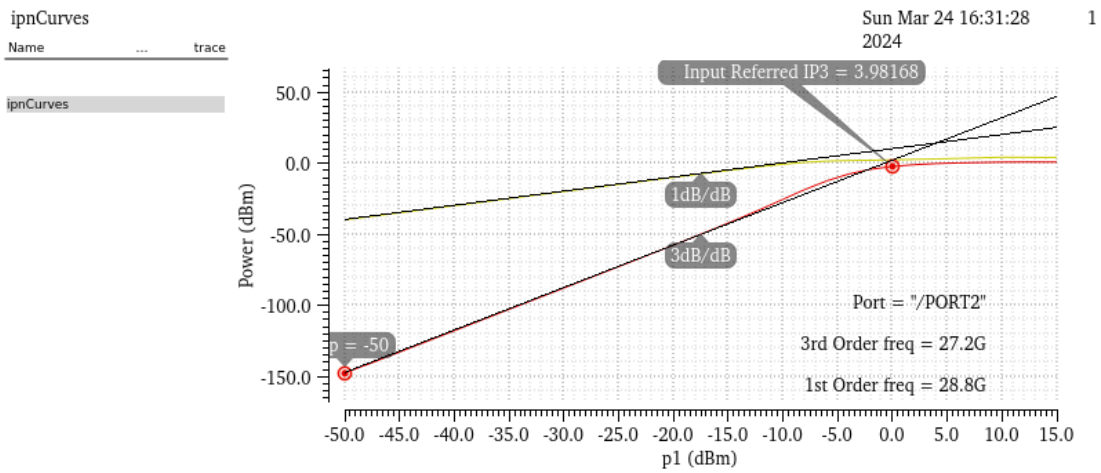

Figure 20. IIP3 with PSS and PAC analysis

Secondly, by conducting HB(harmonic balance) analysis alone, IIP3 can also be easily obtained. The different part is that I need to add another sinusoidal signal at 28.8GHz in port 1 of the circuit. Thus, two-tone simulation will be performed in the circuit. HB settings and IIP3 in this simulation are shown in Figure 21. The results of IIP3 are completely the same.

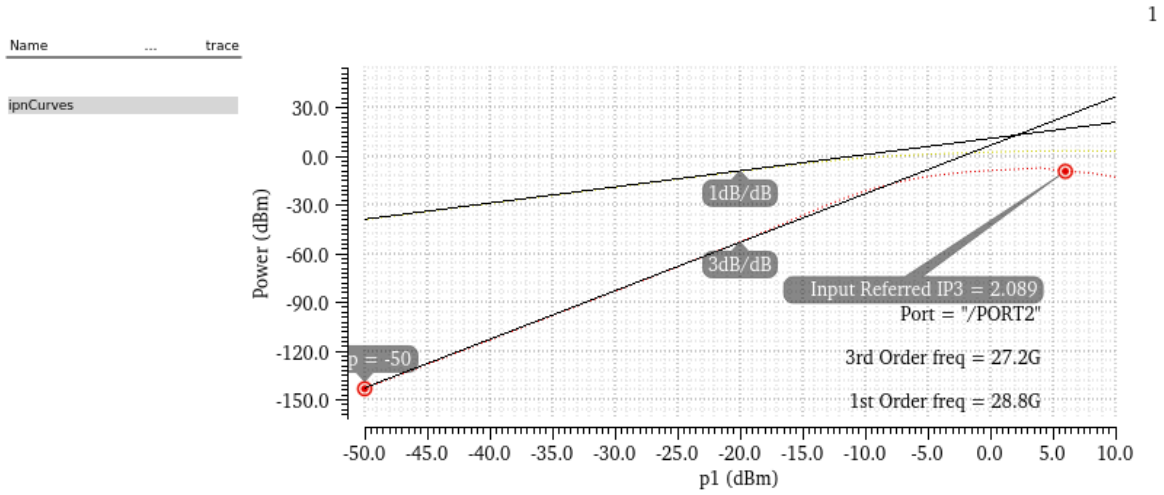

Figure 21. IIP3 with HB analysis

h) Using sp analysis, plot the K factor vs. frequency from 0.1 to 50 GHz. Comment on the stability of your designed LNA based on the simulation result.

It is known that when $|K_f|>1$, the system is stable. In Figure 222, we can know that the system is always free from oscillation and distortion from 0.1GHz to 50GHz, which shows extraordinary stability. Also, as the frequency increase more, the negative feedback may cause oscillation at some point.

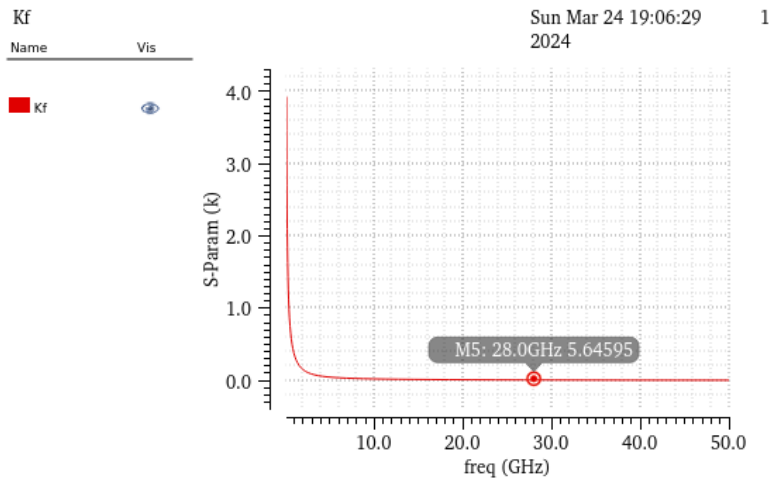

Figure 22. K_f over the frequency range

i) *Using sp analysis, plot noise circles with noise ranges from 1 dB to 10 dB and gain circles with gain ranges from 10 dB to 20 dB, both at f0. Comment on the trade-off between gain and noise based on the circles.*

For noise and gain circles, the center of each circle represents the ideal noise figure or gain, and the radius of each circle represents the deviation from the ideal. As the gain of the amplifier increases, the gain circle expands, and the noise circle also expands due to the increase in noise figure. Thus the noise and gain of the system show an inverse relation. Using the noise and gain circles, the trade-off can be easily achieved by choosing the intercept points and tuning along the circles. Theoretically, perfect power match won't give good noise figure. So trade-off between noise and gain should be at the cost of mismatch.

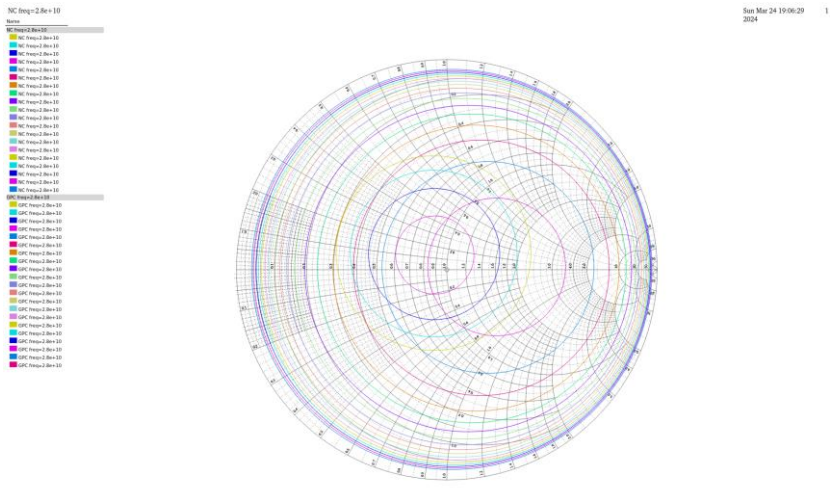

Figure 23. Noise and gain circles

j) *Now, add Cd between the gate and source terminal of M1, plot NF at f0 vs. Cd, make sure that you adjust Lg and Ls for each value of Cd to maintain the input matching at f0. How much is the improvement in NF? What happened to the amplifier gain?*

Adding C_d between gate and source in parallel with Cgs is an effective way to improve noise figure. After sweeping C_d in sp analysis, the change of NF can be seen from Figure 24, where 3.2fF C_d stands out when considering NF improvement. The NF changes from 1.856dB to 1.846dB by 0.54%.

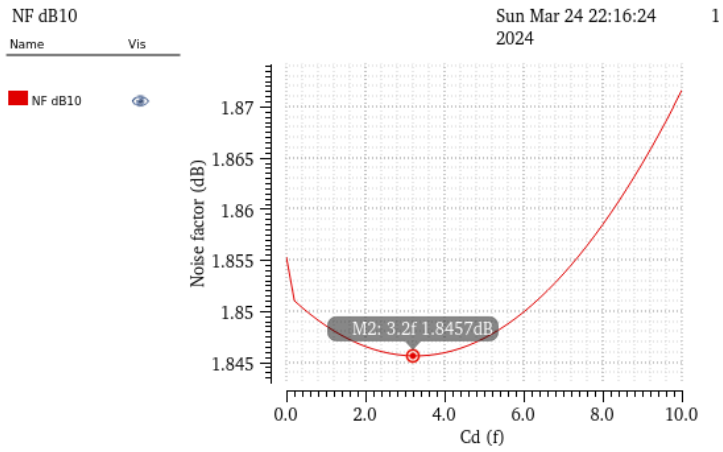

Figure 24. Noise Figure improvement

In the meantime, the amplifier gain goes through decrease. This is due to the inverse relation between noise and gain. Voltage gain decreases from 12.036dB to 11.815dB by 1.84%.

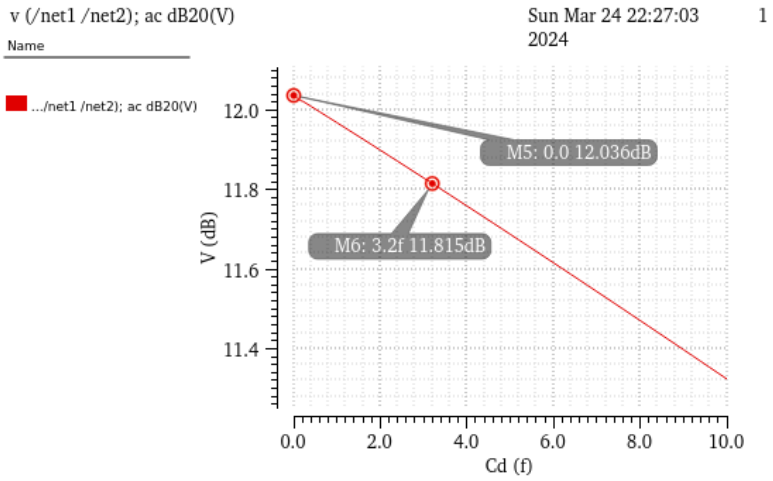

Figure 25. Amplifier gain variations

k) *With the Cd and the Lg, perform a sweep of the input device width, is there a new optimal width that gives lower NF? If so, what is it and what is the NF?*

In the question, I choose to sweep multiplier of M1, which is initially 15. Figure 26 shows that M=16 gives a better NF. In this case, the total width of input device is 64um. NF changes from 1.867dB to 1.859dB, improved by 0.43%.

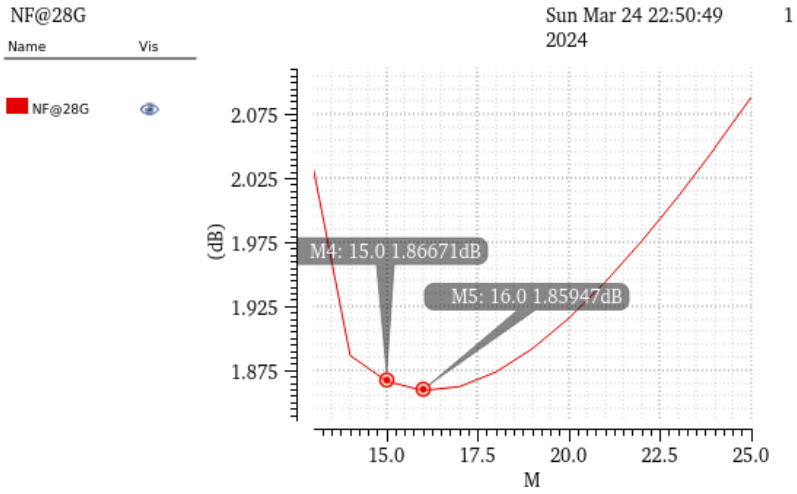

Figure 26. NF with sweeping width

l) *Now, add Lx at the cascode node by first estimating the parasitic capacitance at node X. How much is the improvement in NF? What happened to the amplifier gain?*

Firstly estimating L_x based on the parallel parasitic capacitance, I choose the sweep range of L_x to be from 50pH to 1nH. Theoretically, L_x will eliminate the influence of parasitic capacitance on input impedance. However, the NF improvements is not obvious in my design.

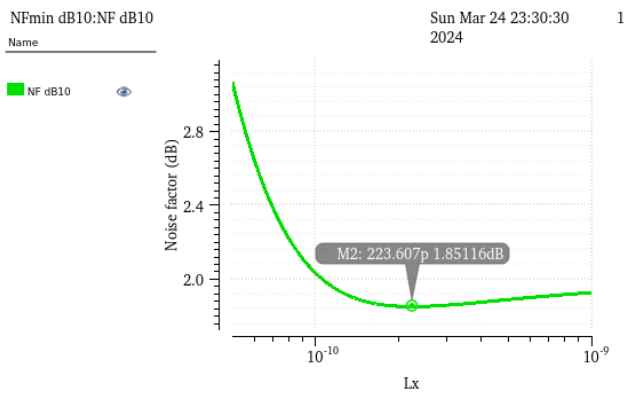

Figure 27. NF with sweeping Lx

It can be seen that NF improves from 1.859dB to 1.851dB by 0.4% when choosing Ls to be 223.6pH. At the same time, voltage gain improves from 11.815dB to 12.667dB by 7.2%, which is significant.

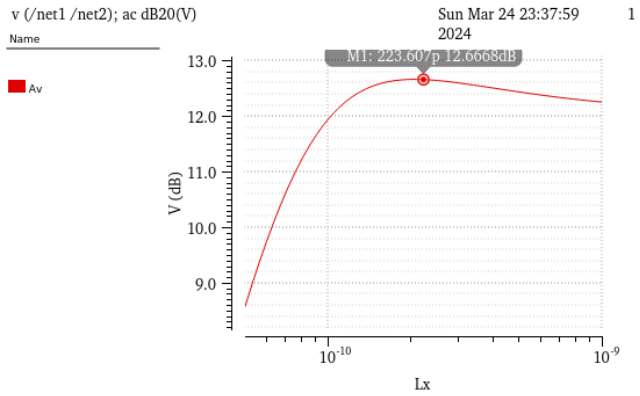

Figure 28. NF with sweeping Lx

Homework 2 finishes at this moment, while the exploration of High Frequency Circuits has just begun.