ELEC 5280 Final Project – A 27.2 GHz Receiver Design Based on TSMC 28nm CMOS Process

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***Abstract*—In this work, we present a heterodyne RF 27.2-GHz receiver using the TSMC 28nm CMOS process. The receiver is composed of a differential Low Noise Amplifier (LNA), two differential mixers, and two Intermediate Frequency (IF) amplifiers. The simulation manages to achieve conversion gain, noise figure, IIP, and power consumption of 26.7 dB, 4.0 dB, -17.4 dBm and 28.8 mW respectively from a 0.9-V supply.**

***Keywords*—Heterodyne RF receiver, LNA, mixer, amplifier.**

I. Introduction

Millimeter-wave systems are used in an increasing number of commercial, defense, and security-related applications, such as high-speed wireless communication and millimeter-wave imaging. Among them, the receiver, as the core part of the wireless communication system, needs to consider key characteristics such as selectivity and sensitivity when designing. When designing RF receivers with heterodyne architecture, the gain, noise figure, and linearity of the receiver need to be optimized to improve the sensitivity of the receiver.

In this work, we present a 27.2 GHz RF receiver system design with heterodyne topology in the TSMC 28 nm CMOS process. The system specifications, architectures of individual parts, and simulation results using Cadence and ADS will be discussed.

II. Receiver Specification and Architecture

The architecture of the receiver is shown in Fig. 1. This system contains a two-stage differential LNA, two mixers, and two baseband amplifiers, where the voltage-controlled oscillator (VCO) is replaced by an ideal clock. The input signal of the system comes from the antenna and the output signal goes straight to the analog-to-digital converter, and these two parts will not be analyzed in this design. According to the design specifications, the system achieves a power consumption of less than 30mW at a power supply voltage of 0.9V. To meet the overall power consumption requirements, the consideration of energy consumption when designing

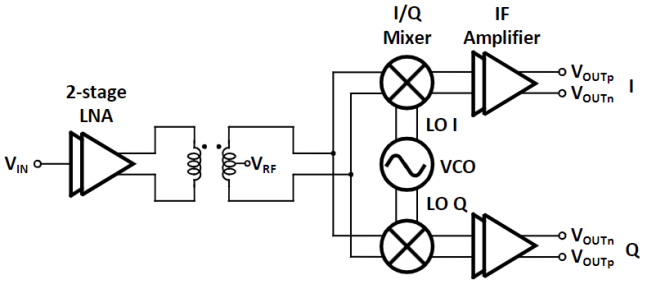

Fig. 1. Architecture of the receiver system.

Table I. Specifications distribution of the receiver

Building Block	NF (dB)	IIP3 (dBm)	Gain (dB)	Power (mW)	S_{11} (dB)
LNA	2.9	-5	12.9	19.7	-
Mixer	9.8	2.5	-1.9	6.75	-
IF Amplifier	6.6	-5.1	14.6	1.76	-
Receiver	4	-17.4	26.7	28.2	-22.5

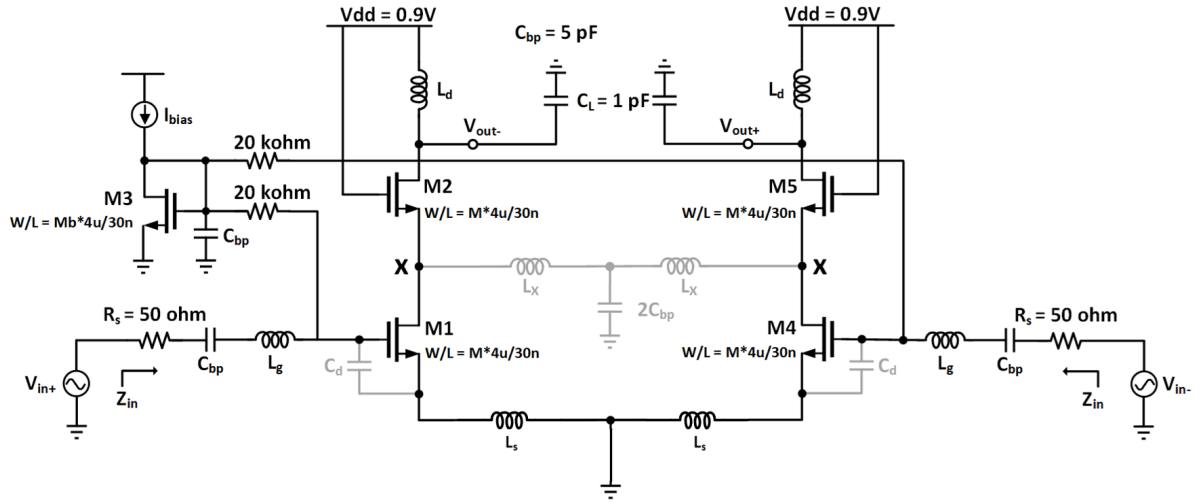

Fig. 2. The schematic of a single stage differential LNA.

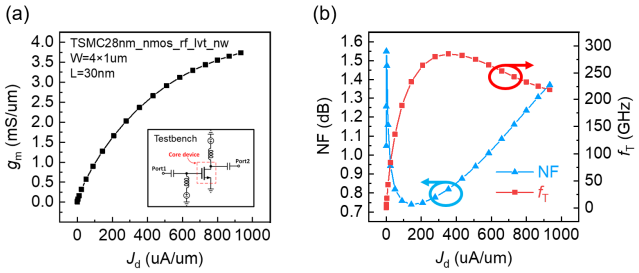

Fig. 3. The DC characteristics of TSMC 28nm transistors. (a) transconductance with the inset of the testbench circuit, (b) noise figure and cutoff frequency.

individual blocks is extremely important and will be addressed in the subsequent sections. In this work, the discrete block design is first done in Cadence and then the receiver system is simulated in ADS. The performance of the receiver system is shown in Table I.

III. Individual Block Design

A. LNA

Fig. 2 shows a single-stage differential LNA designed in this work. Before proceeding with the LNA design for this work, we first completed the characterization extraction of the TSMC 28nm transistor. The transconductance g_m, noise figure NF, and cutoff frequency f_T characteristic curves of the transistor are shown in Fig. 3 respectively. The DC operating point is selected to increase the device gm to obtain sufficient gain. To avoid the excessive effect of channel Thermal Noise and Drain Current noise, the device is biased at a lower current density point of NF.

The LNA is based on a common source structure with source degeneration, and the load consists of an active load of M2 to increase the system gain. A current-mirror structure provides the gate bias voltage of the LNA input pair. The source degeneration inductor L_s is used to resonate with the transistor intrinsic C_{gs} to achieve input impedance matching, and the gate inductance L_g is adjusted to match the input at 27.2 GHz as shown in Equation (1). Similarly, the output matching is achieved by the inductive loads L_d and C_L at the output. Meanwhile, this LNA incorporates two additional designs. The shunt capacitance C_d between the gate and source of input transistor M1 is used to reduce C_{gs} to minimize the gate-induced current noise. Shunt inductor L_x at point X is used to counteract the effect of the parasitic capacitance at point X to reduce the noise contribution from the active load transistor of M2 [1]. The influence of C_d and L_x are shown in Fig. 4. With a C_{gg} of 11.8fF, the transistor gate to source intrinsic capacitor can be effectively decoupled from the LNA input quality factor at C_d of 11.8fF, thus the noise figure is 10% lower as for L_x, an inductor larger than 500pH can steadily reduce NF, by nullifying parasitic capacitance at node X.

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + s(L_s + L_g + \frac{1}{C_{gs}}) \quad (1)$$

where Z_{in} denotes the input impedance of LNA.

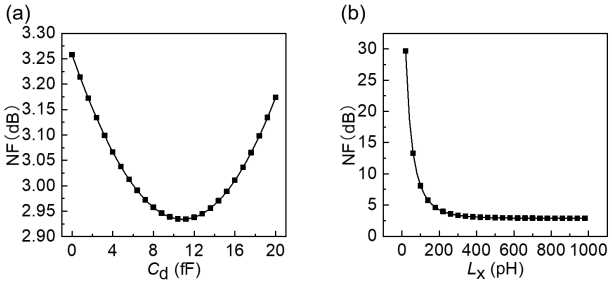

Fig. 4. The influence of C_d and L_x on NF.

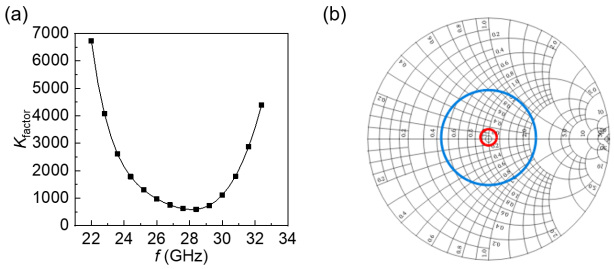

Fig. 5. The stability and noise performance of 2-stage LNA: (a) k factor; (b) noise circles(red and blue circles represent NF = 3dB and 3.5dB respectively)

With a two-stage amp, the noise performance and amplification performance of the LNA are guaranteed. In a cascaded system, the noise figure of the first stage LNA needs to be low enough to minimize the system noise figure. At the cost of this, the first-stage LNA may not be able to obtain sufficient gain, and we design the second-stage LNA where the transistors in it have a larger W/L ratio and larger transconductance. As a result, the NF and gain characteristics of this LNA are satisfied. However, it is still worth considering what level of gain to design. A larger gain LNA will be beneficial to suppress the noise figure of later stages and improve the total noise figure of the receiver while deteriorating the IIP3 of later stages in the meantime, which is according to (2) and (3). Taking all these considerations into account, our 2-stage LNA gain is designed at 10-15 dB.

$$NF_{tot} = NF_{LNA} + \frac{NF_{MIXER} - 1}{A_{P_{LNA}}} \quad (2)$$

$$\frac{1}{IP_{3,tot}^2} = \frac{1}{IP_{3,LNA}^2} + \frac{\alpha_{LNA}^2}{IP_{3,MIXER}^2} \quad (3)$$

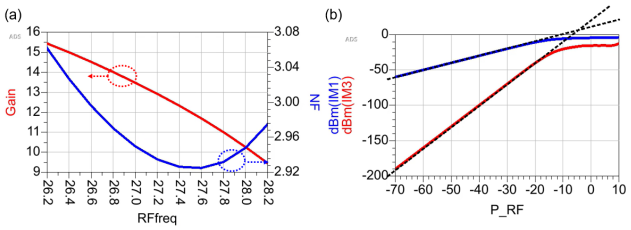

Fig. 6. LNA simulation results.

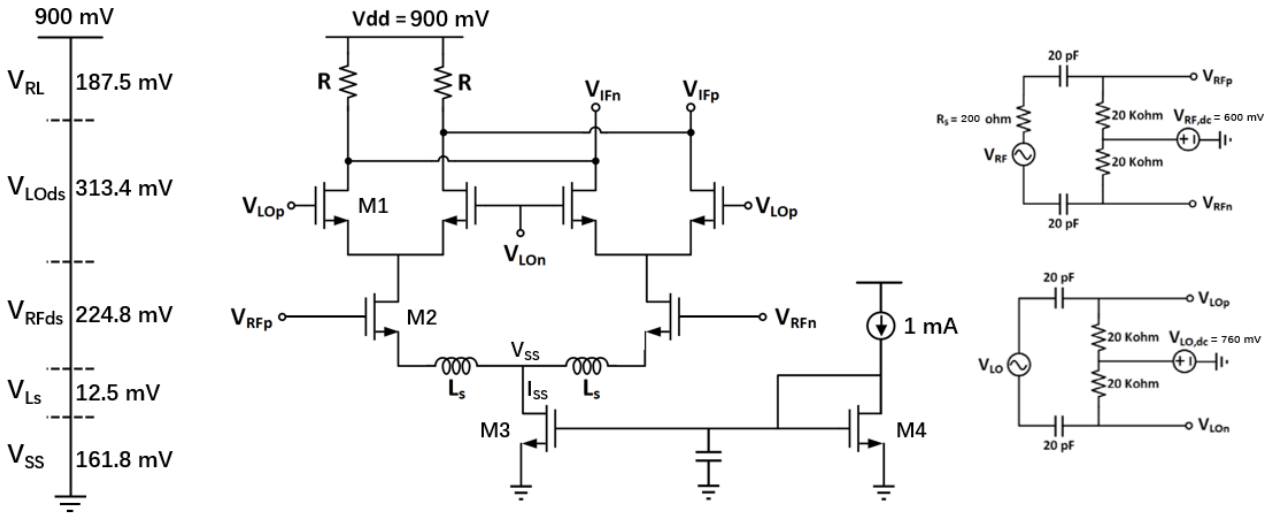

Fig. 7. The schematic of the designed Gilbert cell mixer with voltage distribution from V_{DD} to ground.

where A_{PLNA} denotes the power gain of LNA, and α_{LNA} denotes the voltage gain of LNA.

Fig. 5 illustrates the stability and noise characteristics of the designed LNA. With a K f actor larger than one at all the required frequency bands, the stability of the 2-stage LNA is guaranteed. Fig. 5(b) demonstrates an excellent noise figure of 3 dB with the center of the noise circle matched near 50ohms. Fig. 6 shows the simulation results of the designed LNA. In ADS simulation, the minimum value of NF is achieved near the RF signal frequency of 27.2 GHz. The simulation results show that the maximum gain value is not near 27.2 GHz, and it may be due to the LNA output port impedance mismatch at 27.2 GHz. According to Fig. 6(b), IIP3 of LNA is around -5 dBm, while the 1 dB compression point occurs around -15 dBm, showing good linearity.

B. Mixer

The mixer input is connected to the output of LNA with a suitable transformer, while the output of the mixer is further connected to the IF amplifier. The mixer design follows the design of the Gilbert Cell, as depicted in Fig. 7. It produces output IF signals that are proportional to the product of two input RF and LO signals. Such circuits are widely used for frequency conversion in RF systems. The Gilbert Cell balanced operation cancels out many unwanted mixing products, resulting in a "cleaner" IF output.

The linearity of the Gilbert cell can be controlled in both the transconductance stage and switching stages. IIP3 is directly proportional to the overdrive voltage shown in (4) [2]. Based

$$IIP_3 = 4\sqrt{\frac{2}{3}}(V_{gs} - V_t) \tag{4}$$

$$NF = 10\log\left(2 + \frac{4\gamma}{g_m R_s} + \frac{\pi^2}{2g_m^2 R R_s}\right) \tag{5}$$

$$Gain = 20\log\left(\frac{2}{\pi} g_m R\right) \tag{6}$$

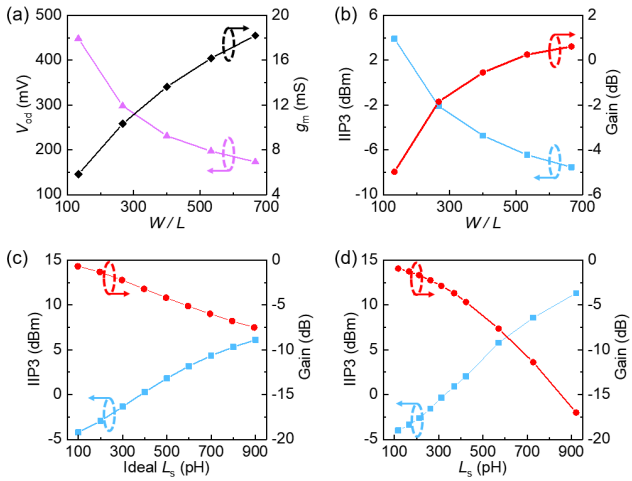

Fig. 8. (a) The overdrive voltage and transconductance vs. W/L of RF transistor with fixed I_{SS} = 4 mA. (b) The IIP3 and voltage gain vs. W/L of RF transistor with fixed I_{SS} = 4 mA. (c) The IIP3 and voltage gain of mixer after ideal L_S loading and (d) TSMC's PDK inductor L_S loading.

on the calculation and equations of gain and noise figure in equations (5) and (6), the voltage conversion gain of the mixer is designed to reach a better noise figure with a good IIP3 performance. There is a trade-off between IIP3 and NF and Gain. A larger overdrive voltage is obtained at the cost of a smaller W/L value. Then, referring to equations (5) and (6), the NF will increase, and the gain will decrease as the g_m is smaller.

In this project, the major factor to consider for the mixer is power. Since the LNA and IF amplifier already take up most of the power (21 mW / 30 mW), the mixer power design is limited to less than 4 mW. The system supply voltage is fixed at 0.9 V for TSMC 28 nm PDK. Hence, the current I_{SS} is selected as 4 mA. The resistance of output is chosen to be 100 Ω for high gain. The W/L of the current source transistor M3 needs to be carefully considered for gain and IIP3. As is shown in Fig. 8(a), the overdrive voltage will be decreased and transconductance will be increased by increasing W/L of the RF transistor with the fixed I_{SS} = 4 mA (without L_S loading). As a result, the IIP3

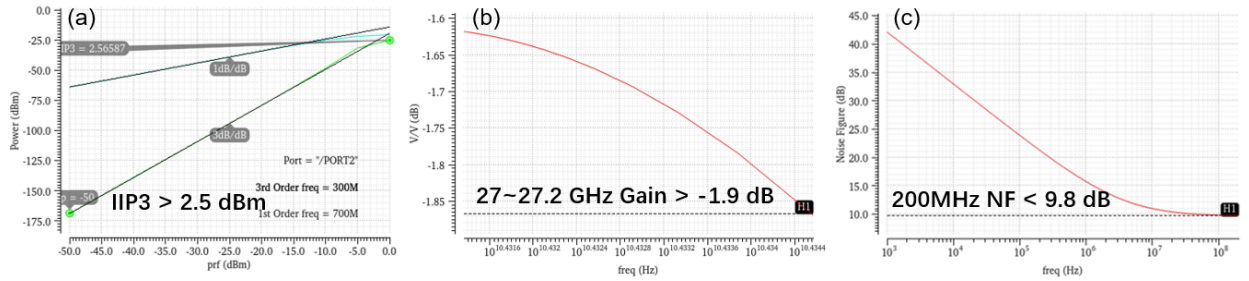

Fig. 9. The schematic of the designed Gilbert cell mixer with voltage distribution from V_{DD} to ground.

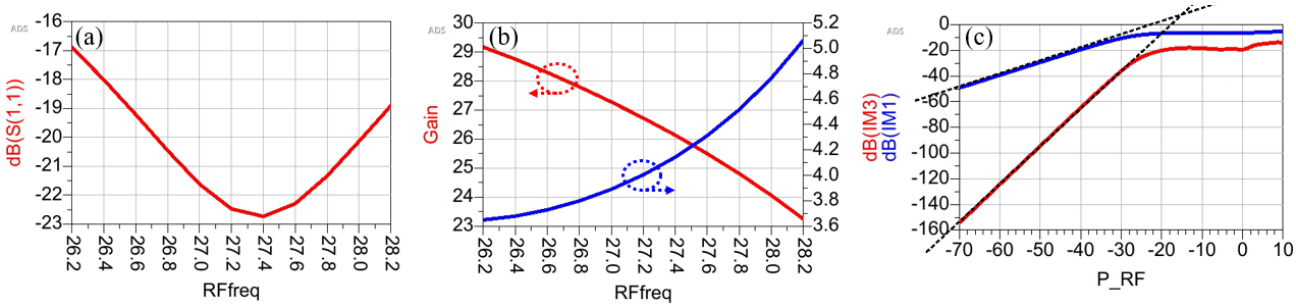

Fig. 10. The simulated (a) return loss, (b) gain and NF, and (c) intercept point of the designed receiver.

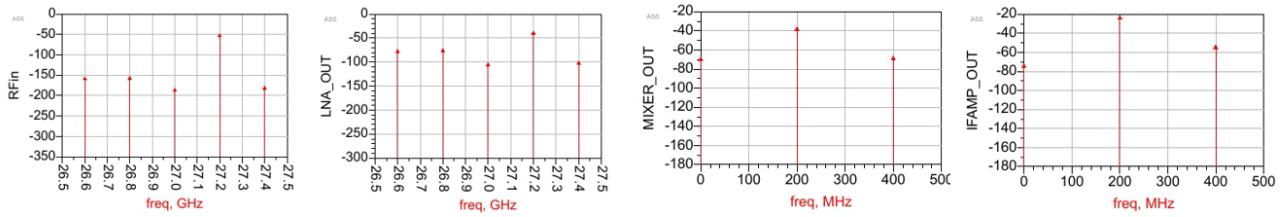

Fig. 11. Receiver output spectrum at each block.

will be decreased from 4 dBm to -7 dBm and gain will be increased from -5 dB to 0.7 dB in Fig. 8(b). Based on these results, the W/L needs to be selected around 500 to achieve positive IIP3 with a gain larger than -5 dB. As is shown in Fig. 8(c), an ideal L_S is inserted with an inductance range from 100 pH to 900 pH. The IIP3 will be increased to larger than 0 dBm easily, and the gain will be decreased a little. However, after inserting the same value of L_S from the TSMC 28nm library, the IIP3 will be increased fatly while the gain will drop dramatically in Fig. 8(d). Finally, the L_S is chosen as a value of 424 pH with a coil width of 5 microns, a turn number of one, an inner radius of 90 microns, a coil spacing of 2 microns, and a guard ring distance of 29 microns. Fig. 9 shows the simulation results with an IIP3 > 2.5 dBm, a gain > -1.9 dB, and an NF < 9.8 dB of the designed mixer. The W/L = 20μm / 30nm is chosen for LO and RF transistors with dc voltage = 760 and 600 mV, respectively.

C. IF Amplifier

The amplifier immediately following the mixer is used to amplify the baseband signal. The main design consideration for this amplifier is to meet the maximum gain. A single-stage differential amplifier structure with a common source structure is used to achieve low noise while maintaining a 15dB gain and good linearity of the IF amplifier.

IV. Receiver Simulation

The performance of each block is shown in Table I. All performances have met the design specifications. Fig.10 shows the simulated receiver performance. The return loss is smaller than -21 dB at the operation band. The gain is 26.7 dB with power consumption 28.2 mW. The NF is smaller than 4.0 dB at 27.2 GHz. The IIP3 is -17.4 dBm. All parameters meet the design requirements in Table I. As is shown in Fig. 11, the receiver works well for demodulation of 27.2 GHz RF signal and 27 GHz LO signal.

V. Conclusion

In this report, a millimeter wave RF receiver based on TSMC 28nm PDK is designed and simulated. The designed receiver comprises a two-stage cascode common source stage differential LNA with inductive degeneration, two Gilbert cell mixers, two baseband amplifiers, and an ideal VCO. The designed receiver works well with a frequency range from 27 to 27.2 GHz with a return loss of -22.5dB, a gain of 26.7 dB, an IIP3 of -17.4 dBm, an NF of 4.0 dB, and a power consumption of 28.2 mW, which meet all the design specifications.

References

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