ELEC5280 Final Project Presentation

XU Jiashuai, LIU Yichen

03/06/2024

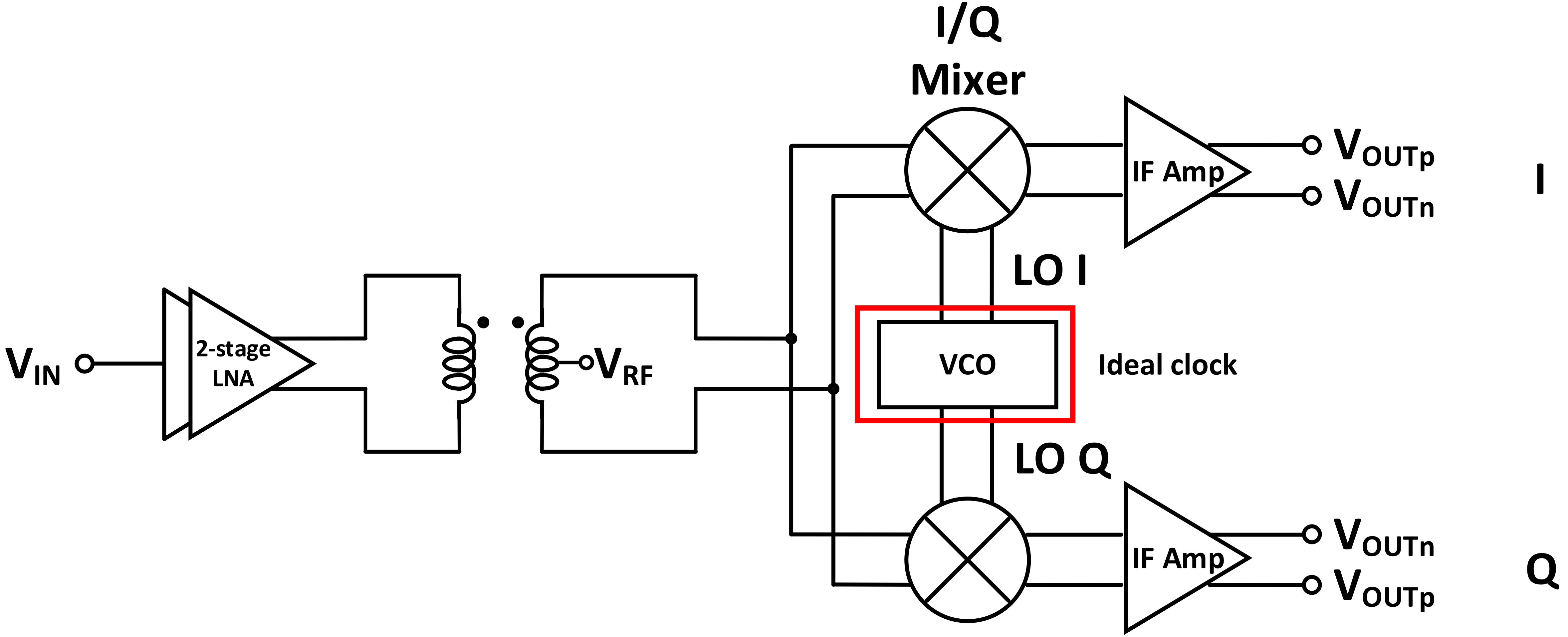
Outline

- **Architecture of the Receiver**
- **Workload Distribution**
- **Design of Building Blocks**
  1. LNA
  2. Mixer
  3. IF Amplifier
  4. Receiver System
- **Conclusion**

Outline

- **Architecture of the Receiver**
- **Workload Distribution**
- **Design of Building Blocks**
  i. LNA
  ii. Mixer
  iii. IF Amplifier
  iv. Receiver System
- **Conclusion**

Architecture of the Receiver



Outline

- Architecture of the Receiver
- **Workload Distribution**
- Design of Building Blocks
  i. LNA
  ii. Mixer
  iii. IF Amplifier
  iv. Receiver System
- Conclusion

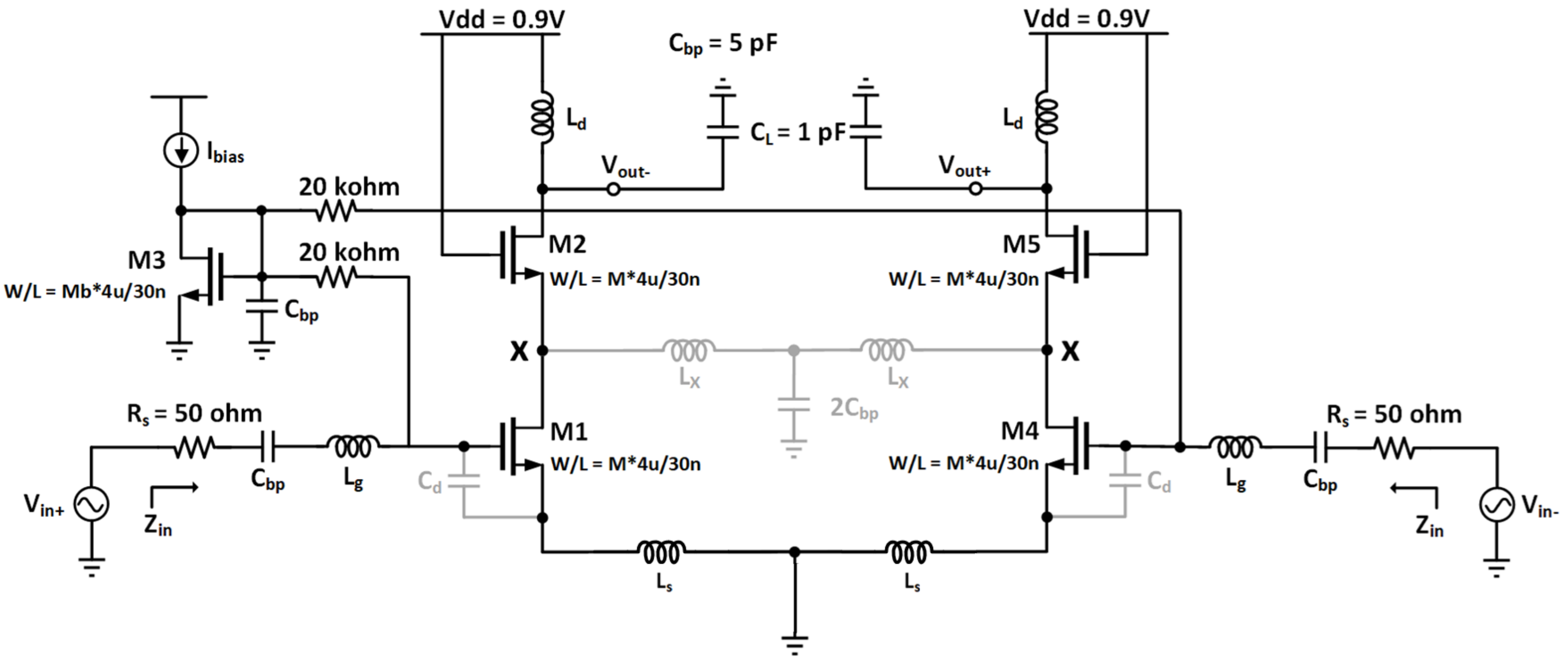
Workload Distribution (Specifications)

Task	LNA	Mixer	IF Amplifier	Report + System Simulation	Specifications
Person in charge	Yichen	Jiashuai	TA	ALL	/
Noise Figure (dB)	2.9 (<5)	9.8 (<20)	5.1 (<10)	4.0	< 7
Gain (dB)	12.9 (>9)	-1.9 (>-5)	14.6 (>20)	26.7	> 25
IIP3 (dBm)	-5 (>-20)	2.5 (>0)	-5.1 (>-10)	-17.4	> -20
Power Consumption (mW)	19.7 (<20)	6.75 (<15)	1.76 (<10)	28.2	< 30
S11 (dB)	/	/	/	-22.5	< -12
EVM	/	/	/	on-going	< 15%

Outline

- Architecture of the Receiver
- Workload Distribution
- **Design of Building Blocks**
  1. LNA
  2. Mixer
  3. IF Amplifier
  4. Receiver System
- Conclusion

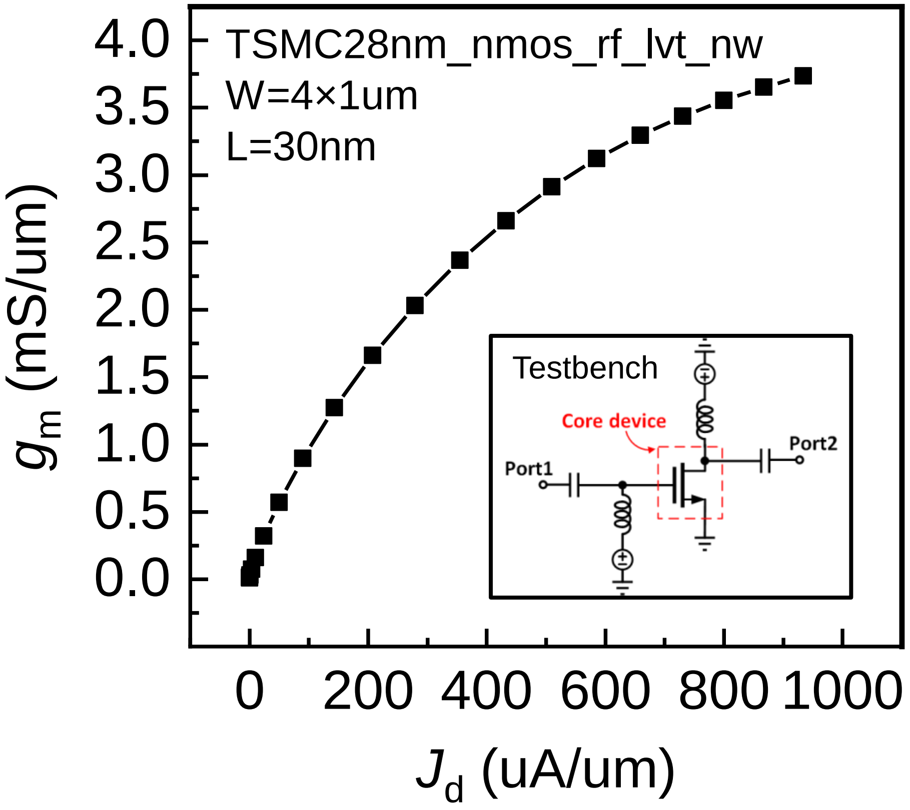
i. LNA: schematic

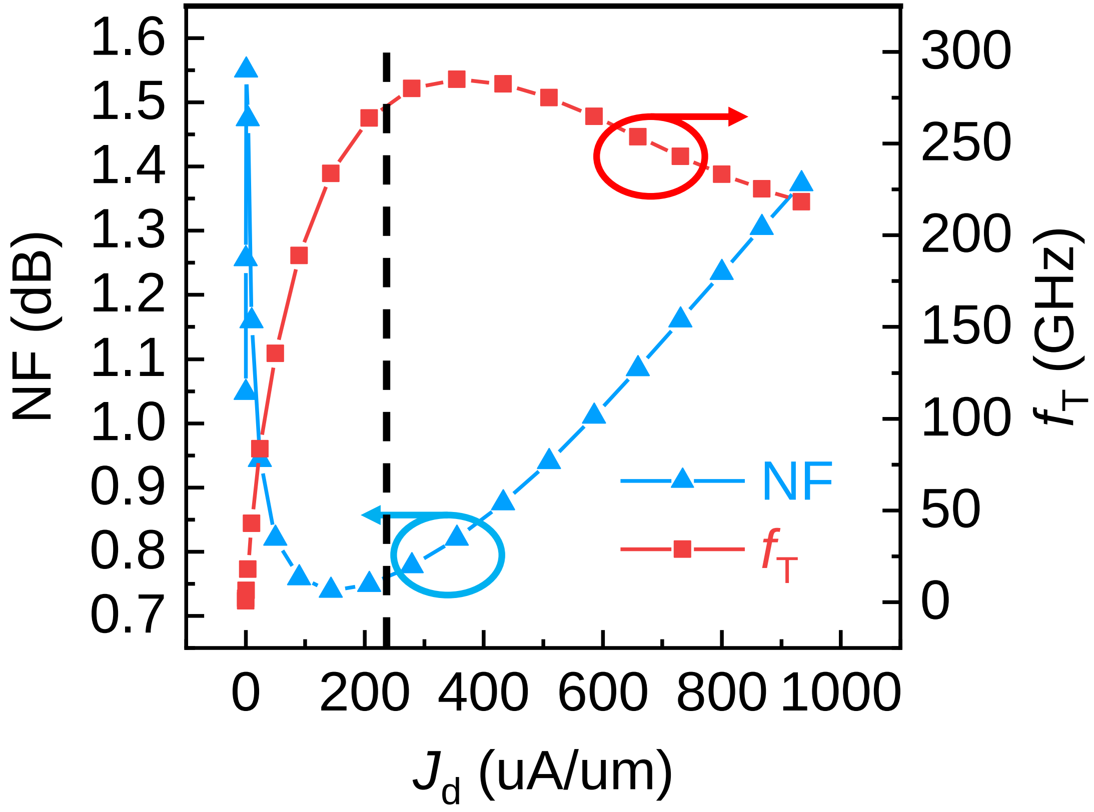


- One standard differential low noise amplifier with inductive load
- Impedance matching: L_s and L_g
- C_d: decoupling Q from C_{gs} → gate induced current noise ↓
- L_x: reduce the influence of parasitic C_x → noise of M2 relatively decrease↓

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + s\left(L_s + L_g + \frac{1}{C_{gs}}\right)$$

i. LNA: design considerations



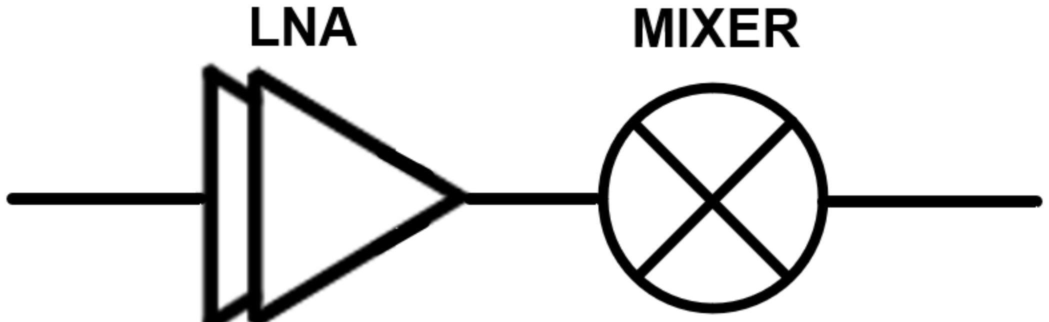


- DC operating point selection: trade-off between Gain and NF
- Gain: larger with larger g_m
- NF: trade off between thermal noise and drain current noise
- Better linearity when g_m saturates

i. LNA: design considerations

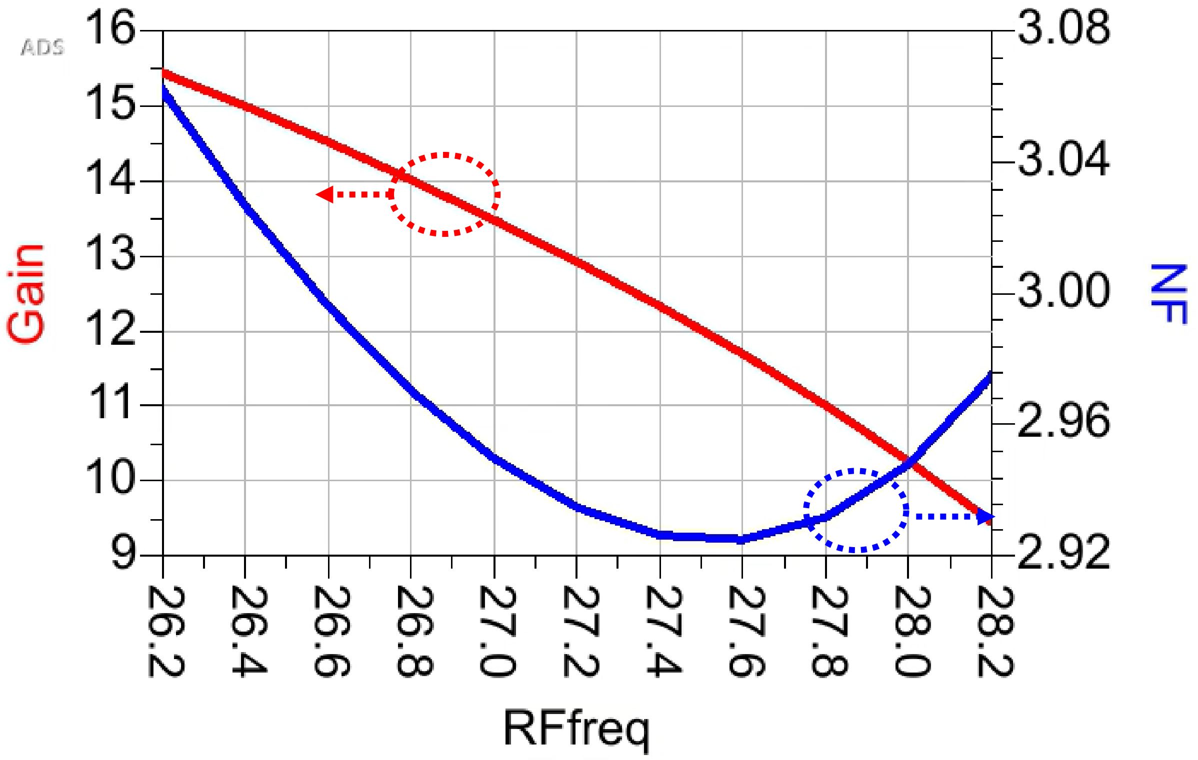
$$NF_{tot} = NF_{LNA} + \frac{NF_{MIXER} - 1}{A_{P_{LNA}}}$$

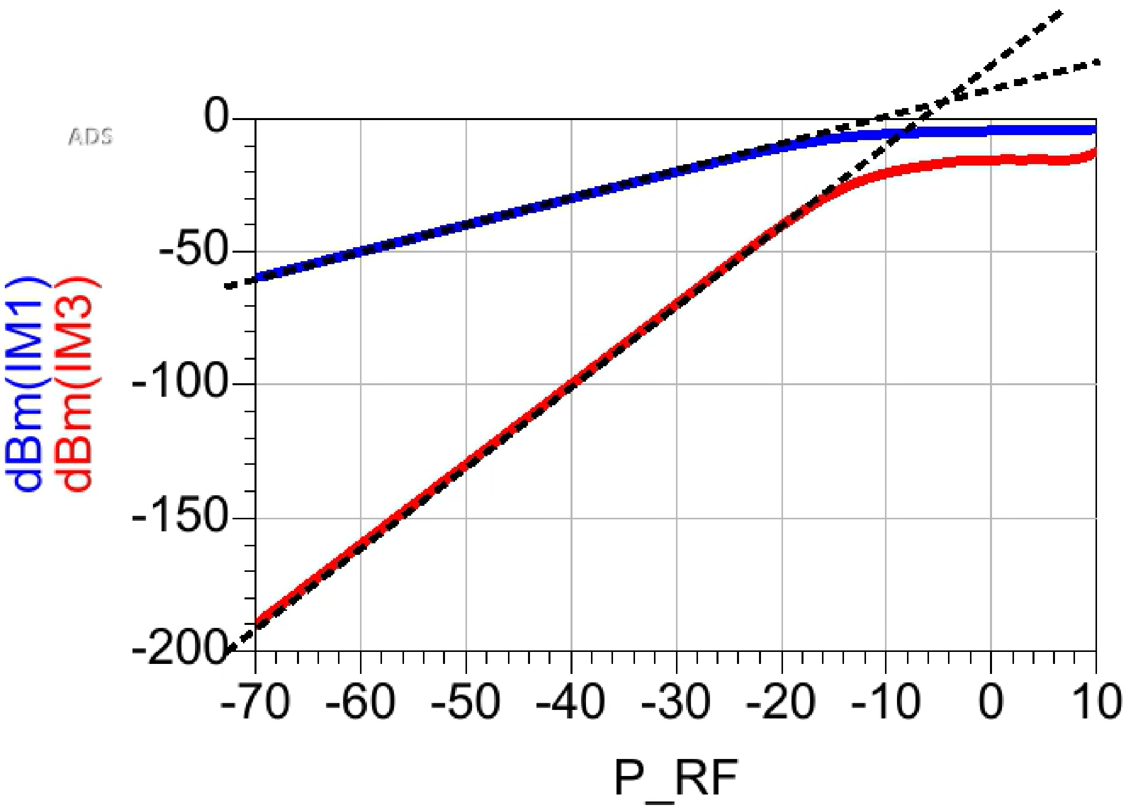
$$\frac{1}{IP_{3,tot}^2} = \frac{1}{IP_{3,LNA}^2} + \frac{\alpha_{LNA}^2}{IP_{3,MIXER}^2}$$



- System Gain: sum of all blocks
- System NF: mainly determined by LNA
- System IIP3: mainly determined by MIXER due to nearly 13dB gain of LNA

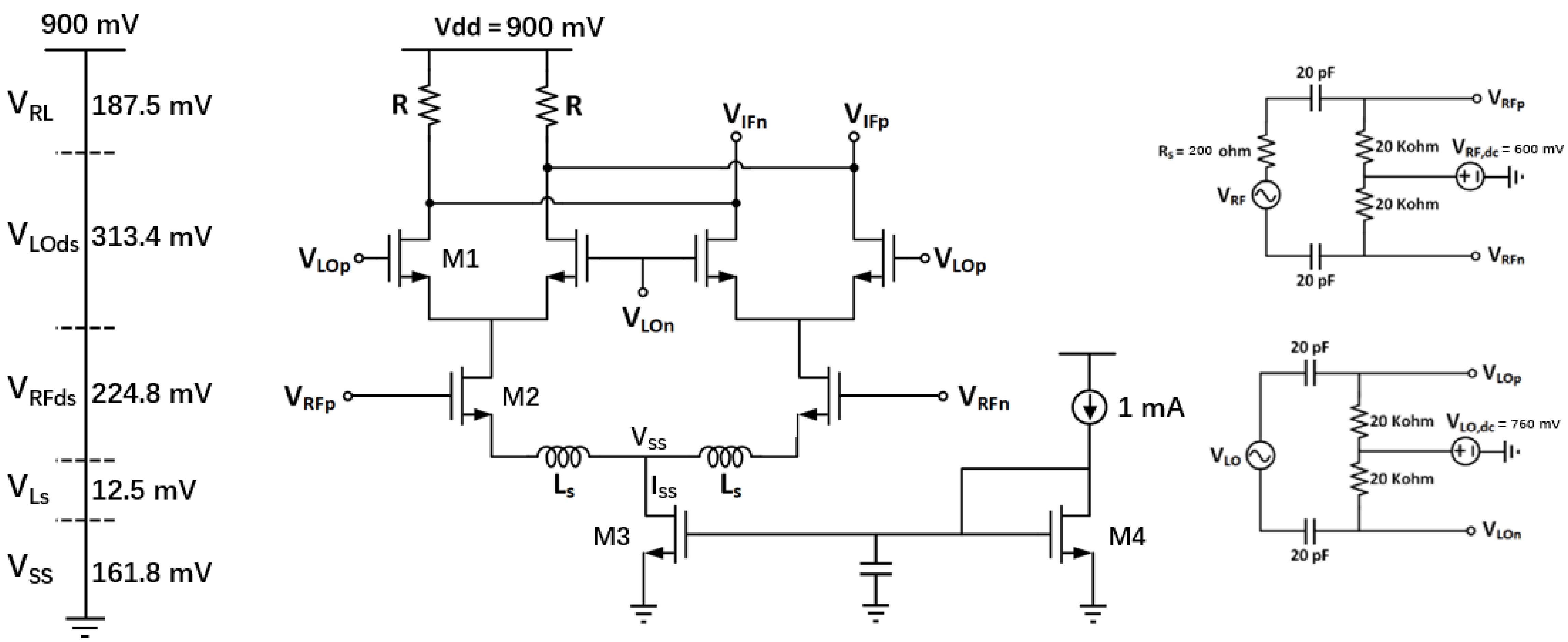
i. LNA: simulation results





Part	Noise Figure (dB)	Gain (dB)	IIP3 (dBm)	Power Consumption (mW)
LNA	2.9(<5)	12.9 (>9)	-5.0 (>-20)	19.7 (<20)

ii. Mixer: schematic



ii. Mixer: design considerations

$$I_{ds} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{gs} - V_{TH})^2$$

$$g_m = \mu_n C_{ox}\frac{W}{L'}(V_{gs} - V_{TH})$$

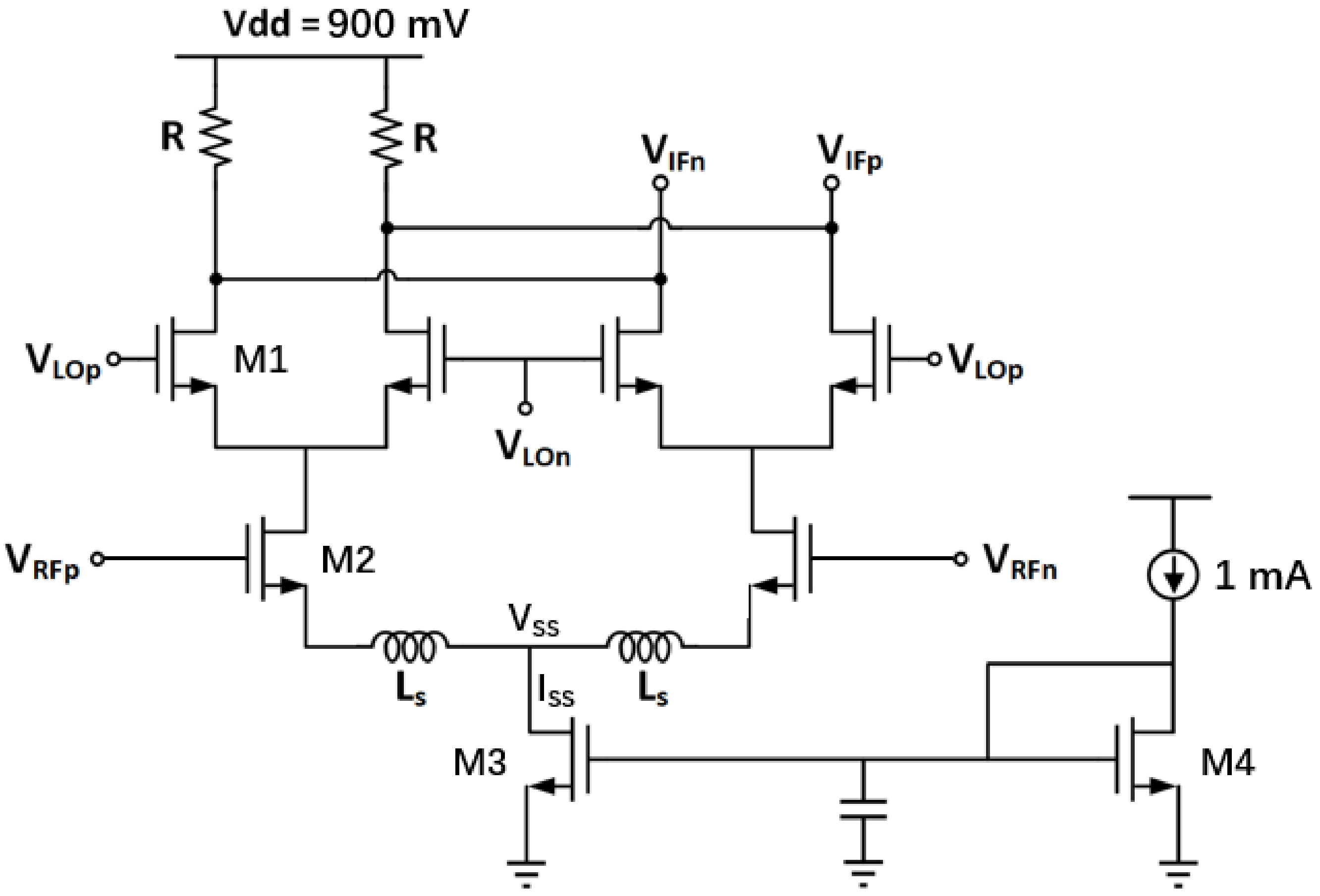
$$g_m = \frac{2I_{ds}}{V_{gs} - V_{TH}}$$

$$Gain = \frac{2}{\pi} g_{mRF} R_L$$

IIP3 is directly proportional to both the drive current and the overdrive voltage:

$$IIP3 = 4\sqrt{\frac{2}{3}\frac{I_{dsRF}}{\mu_n C_{ox}}}$$

$$IIP3 = 4\sqrt{\frac{2}{3}(V_{gs} - V_{TH})}$$



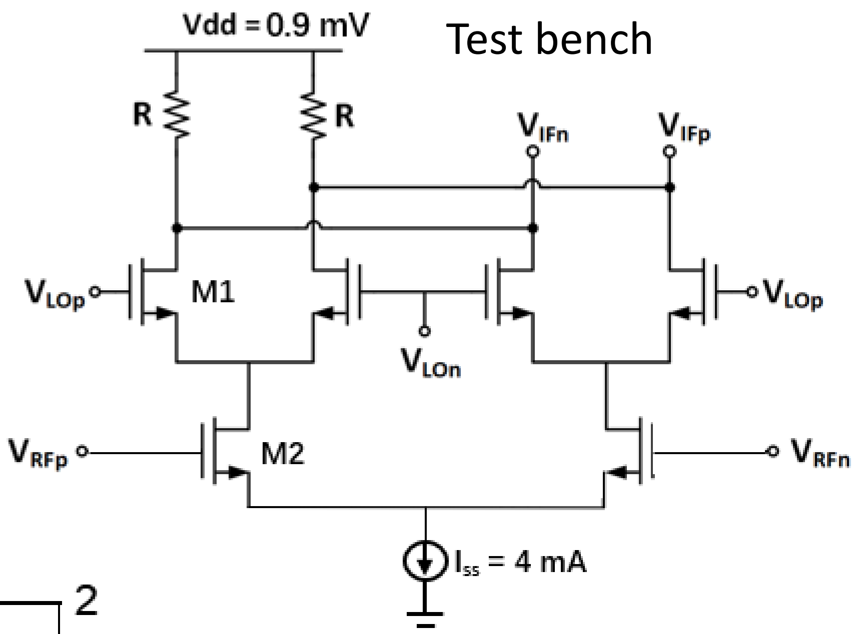
$$NF = 10\log\left(2 + \frac{4\gamma}{g_m R_s} + \frac{\pi^2}{2g_m^2 R R_s}\right)$$

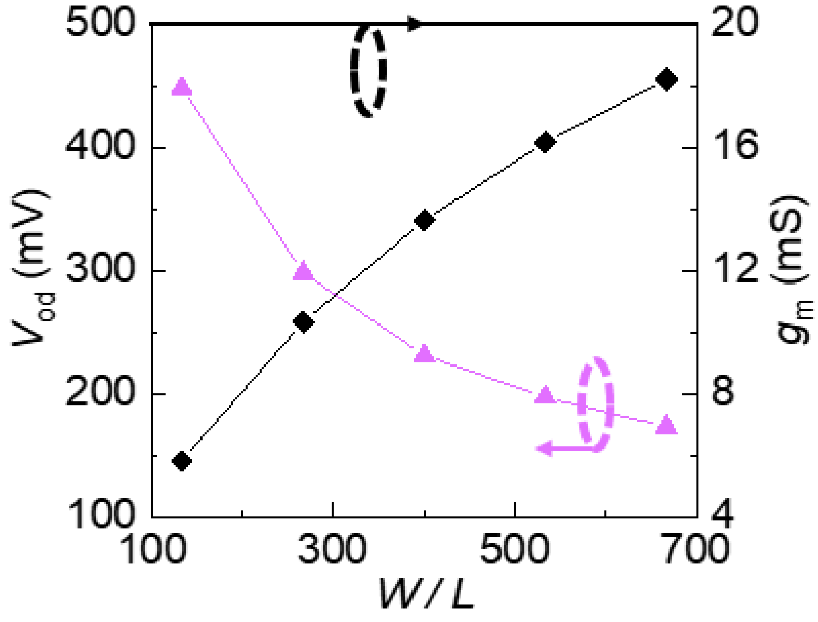
ii. Mixer: design process

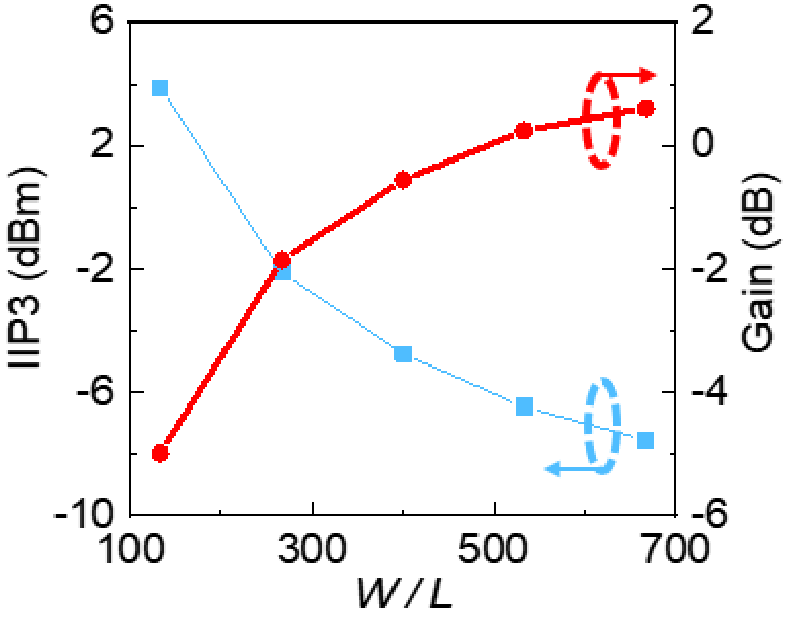
Total power requirement: 30mW
LNA power: 20mW
IF amplifier power: 2mW (two)
Mixer power: 8mW (<4mW per one)

Power = $V_{DD}I_{SS}$ $I_{SS} < 4.4mA$

Test bench



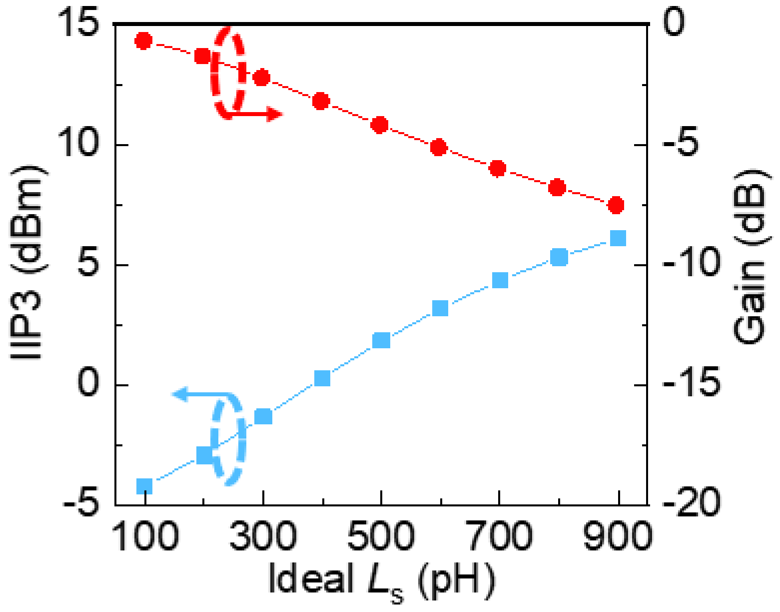


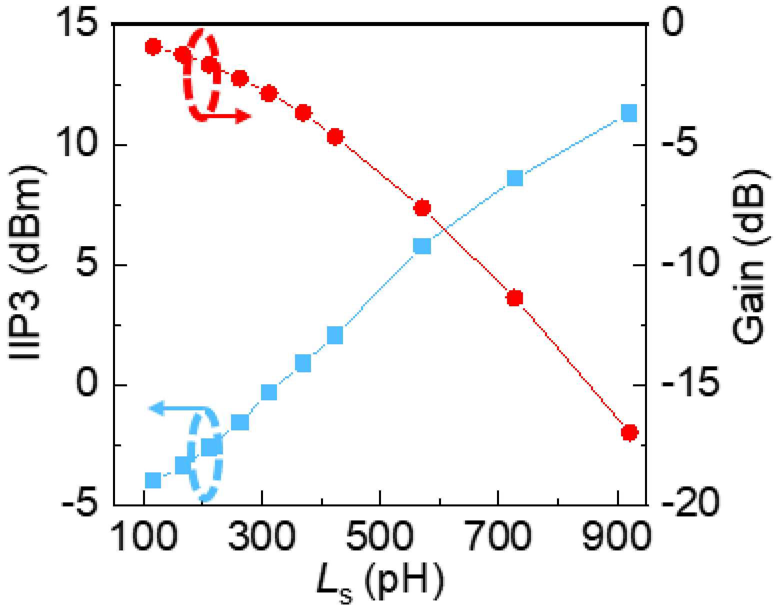


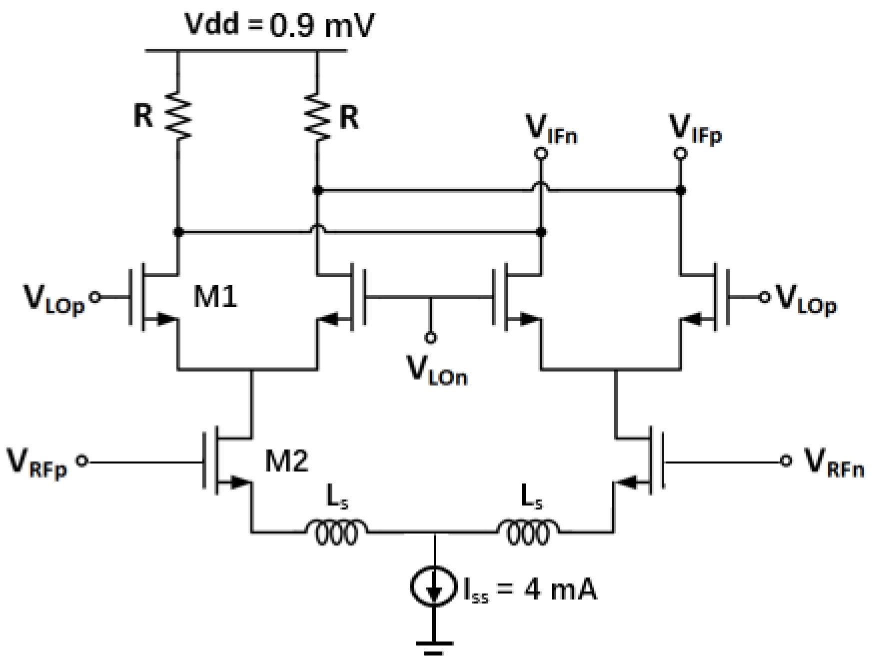
- W/L of M2 is chosen around 500 with fixed I_{SS} = 4 mA.

- Gain ~ 0 dB
- IIP3 ~ -6 dBm
- gm ~ 16 mS
- Vod ~ 200 mV

ii. Mixer: design process







Test bench

- L_S can be inserted for high IIP3.
- Ideal L_S and TSMC's inductors are different.
- 426 pH is chosen for mixer design.
  - Gain ~ 0 dB → -1.9 dB
  - IIP3 ~ -6 dBm → 2.5 dB

ii. Mixer: design process

1. Set I_{SS} = 4mA → power < 4mW

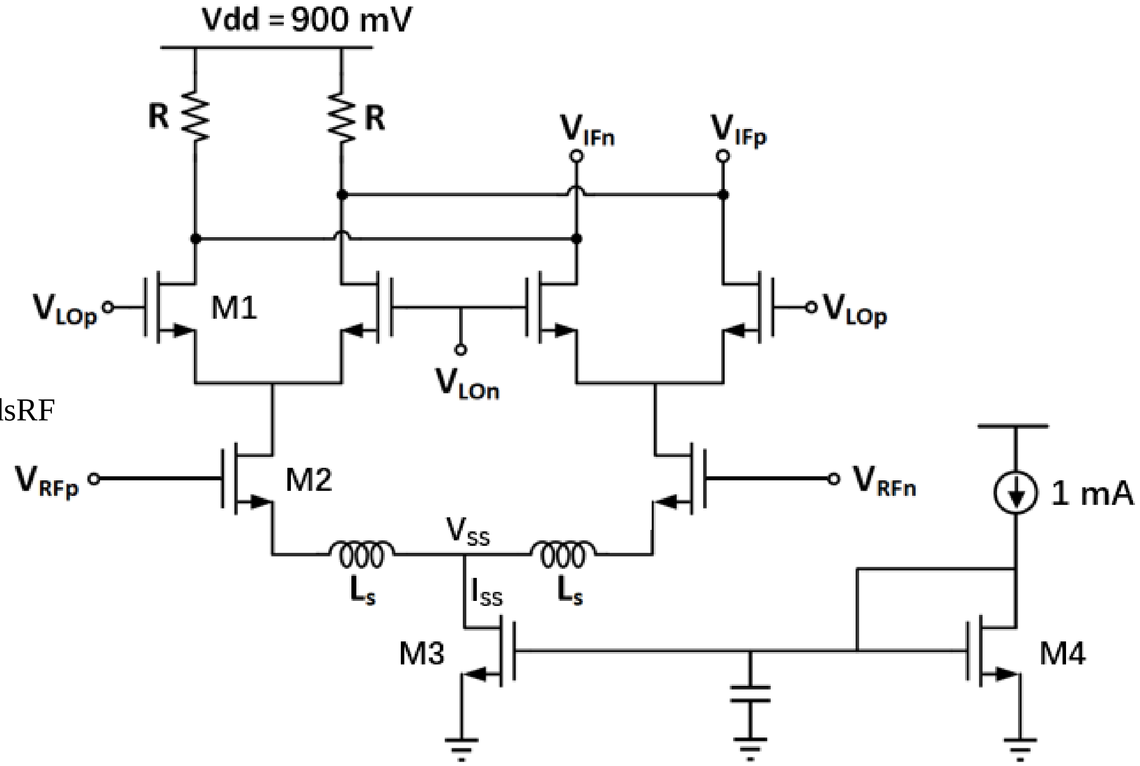
2. Select suitable $\frac{W}{L'}$ for M3 with suitable g_m → headroom

3. Set R_L = 100Ω → headroom

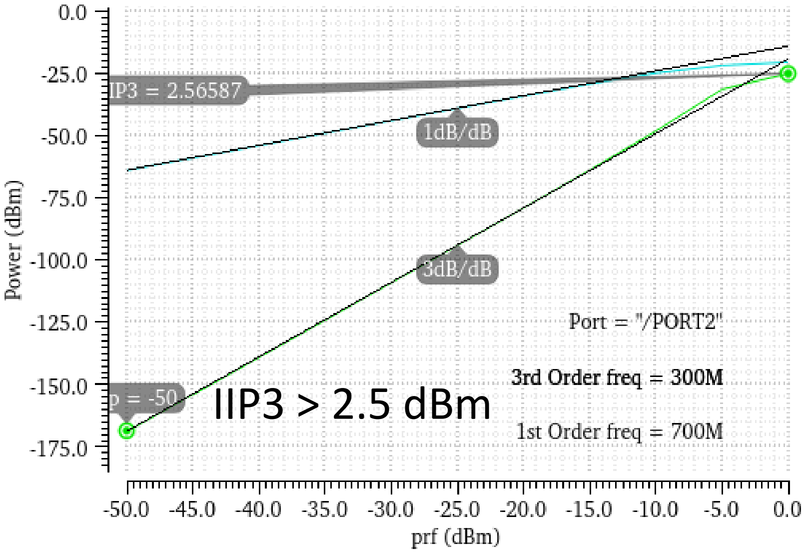
4. Select initial $\frac{W}{L'}$ for M2 with suitable g_{mRF} → IIP3, gain, and V_{dsRF}

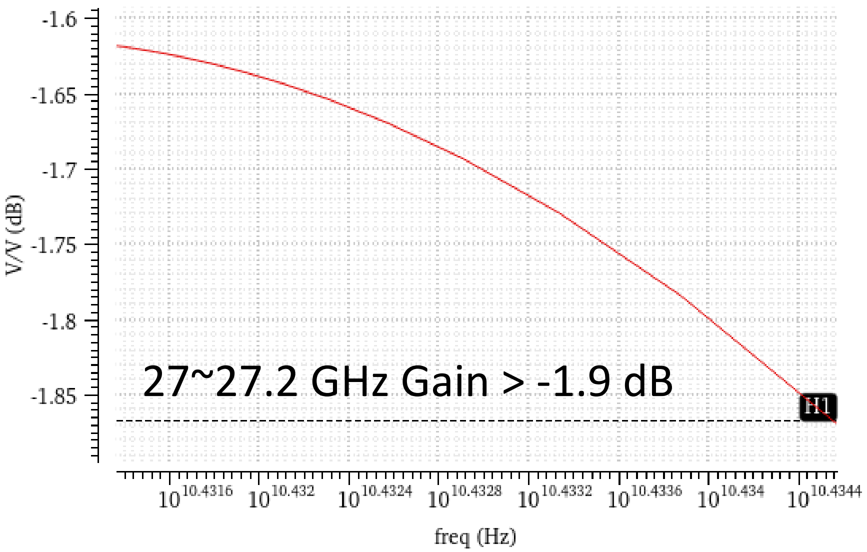
5. Select initial $\frac{W}{L'}$ for M1 with suitable g_{mLO} → V_{dsLO}

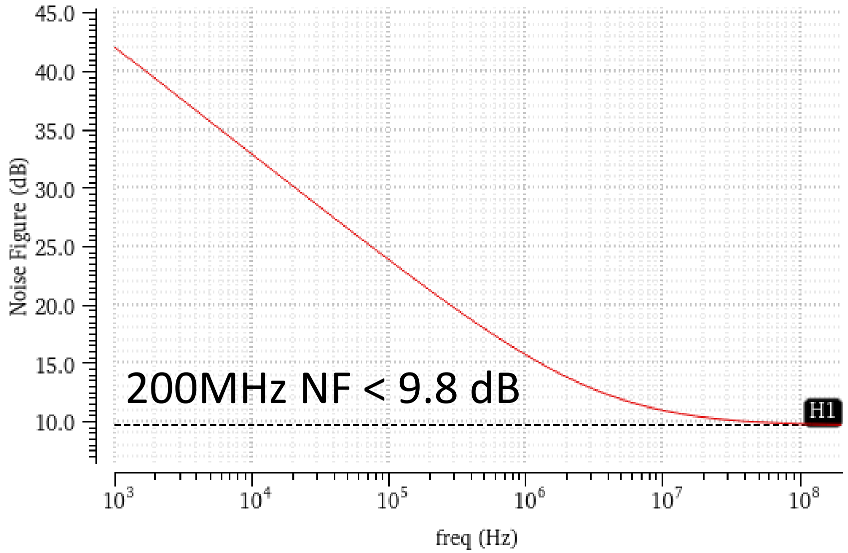
6. Optimize L_s until IIP3 and gain are big.



ii. Mixer: simulation results

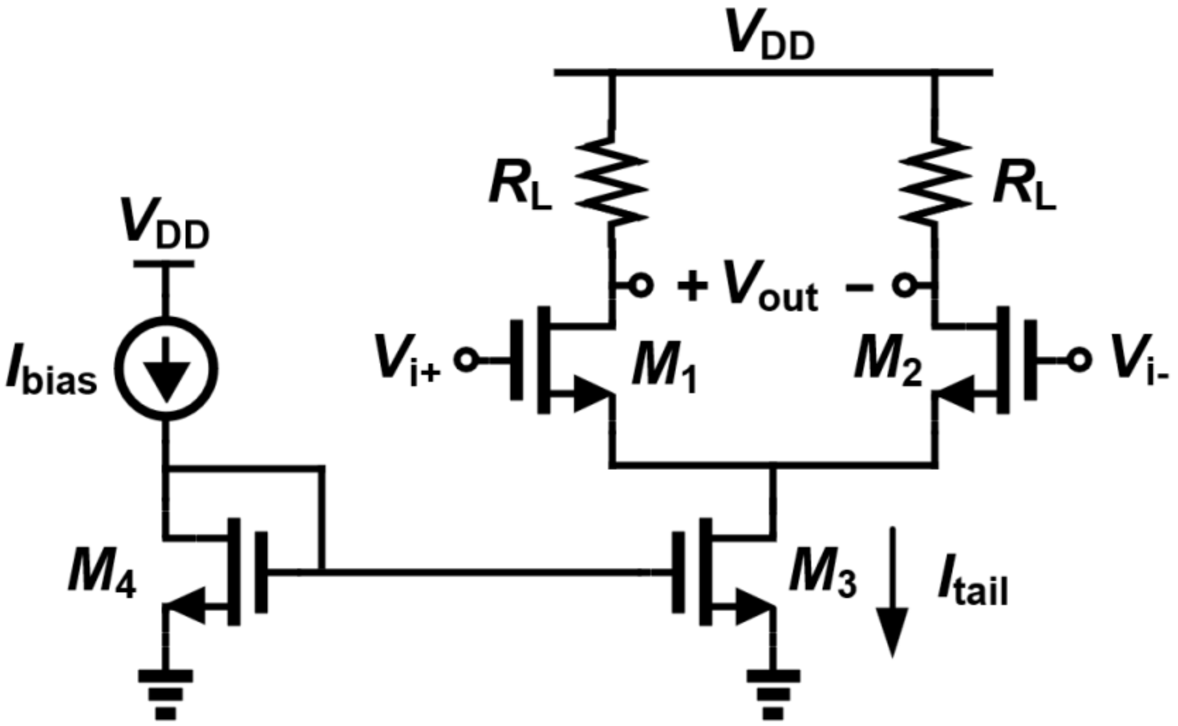






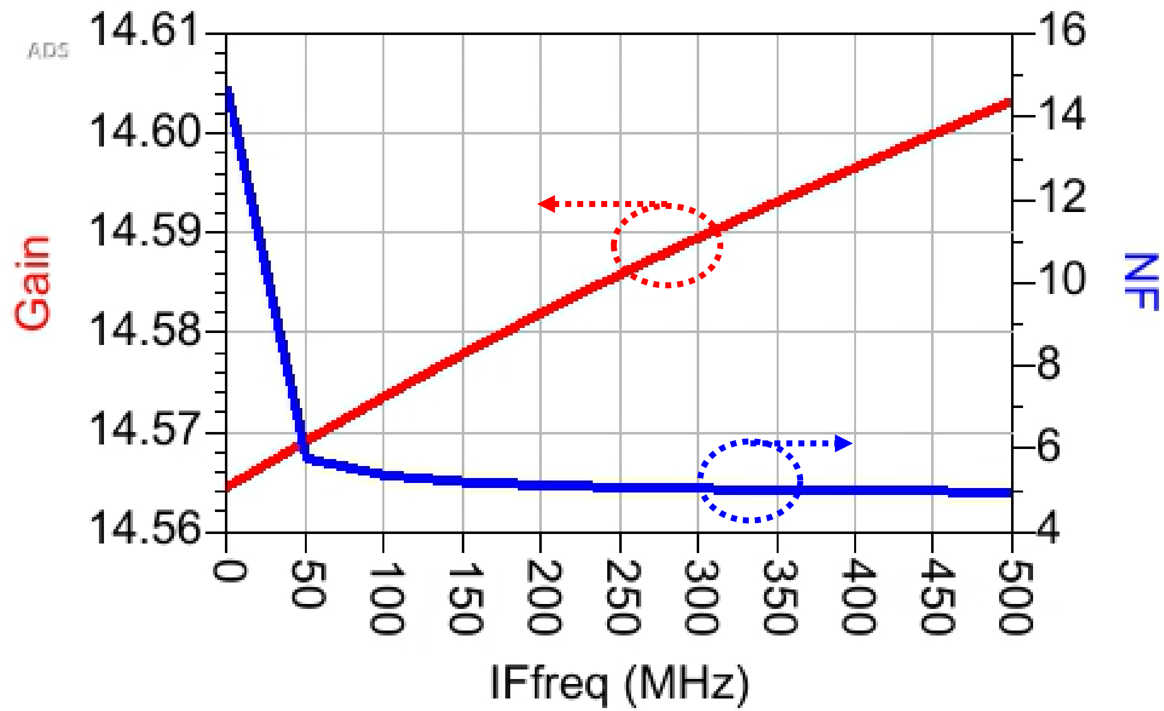
Part	Noise Figure (dB)	Gain (dB)	IIP3 (dBm)	Power Consumption (mW)
Mixer	9.8 (<10)	-1.9 (>-5)	2.5 (>0)	6.75

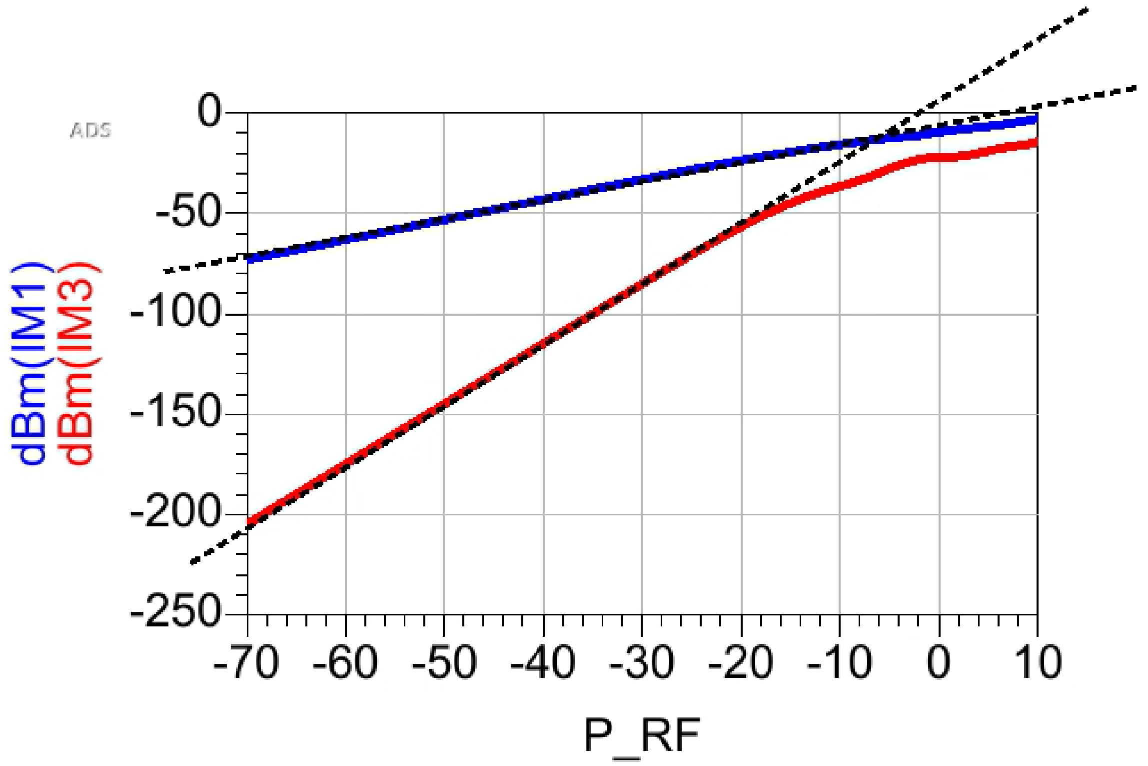
iii. IF Amplifier (given by TA) : schematic



- ➢ Simple resistor load differential structure
- ➢ Focus on large gain design to amplify the BB signal

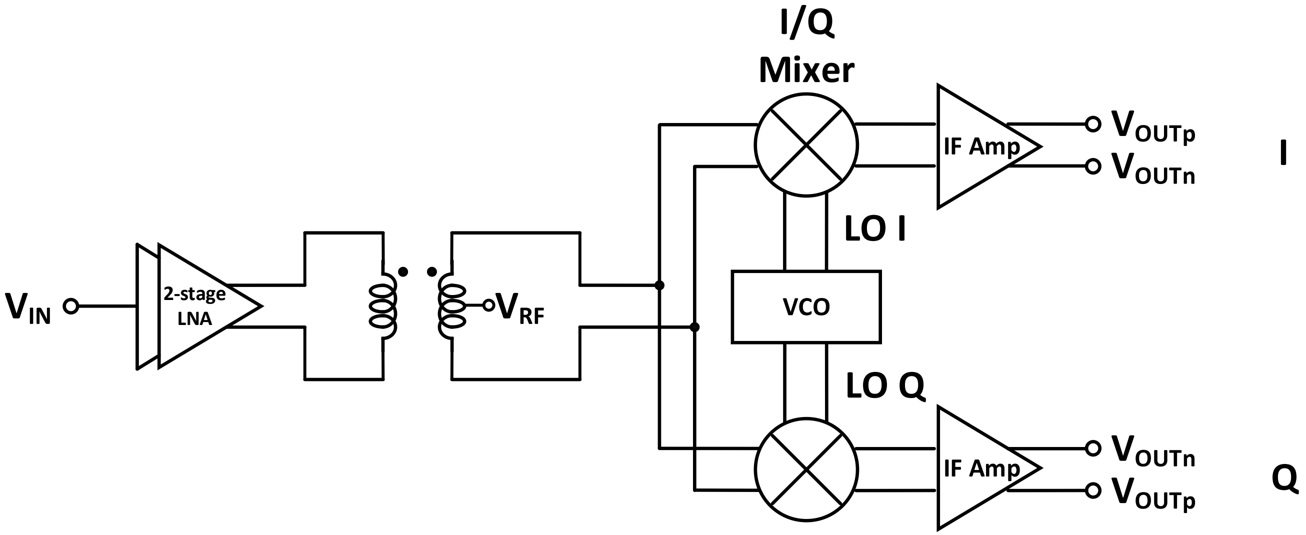
iii. IF Amplifier (given by TA) : simulation results

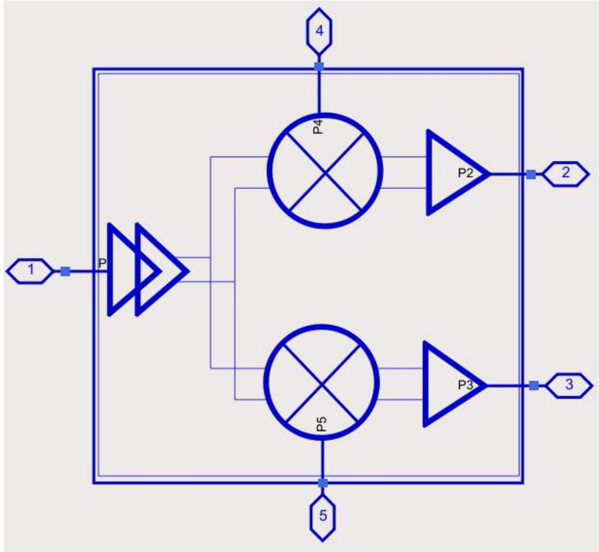




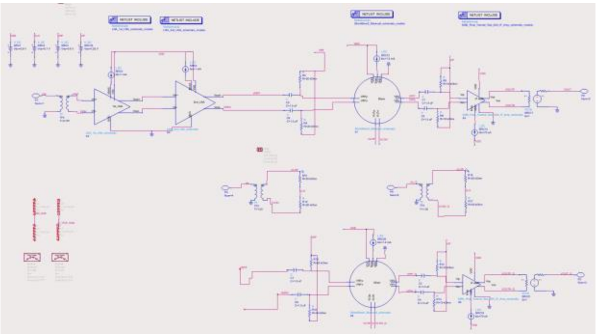
Part	Noise Figure (dB)	Gain (dB)	IIP3 (dBm)	Power Consumption (mW)
IF_Amplifier	5.1 (<10)	14.6 (>20)	-5.1 (>-10)	1.76 (<10)

iv. Receiver system

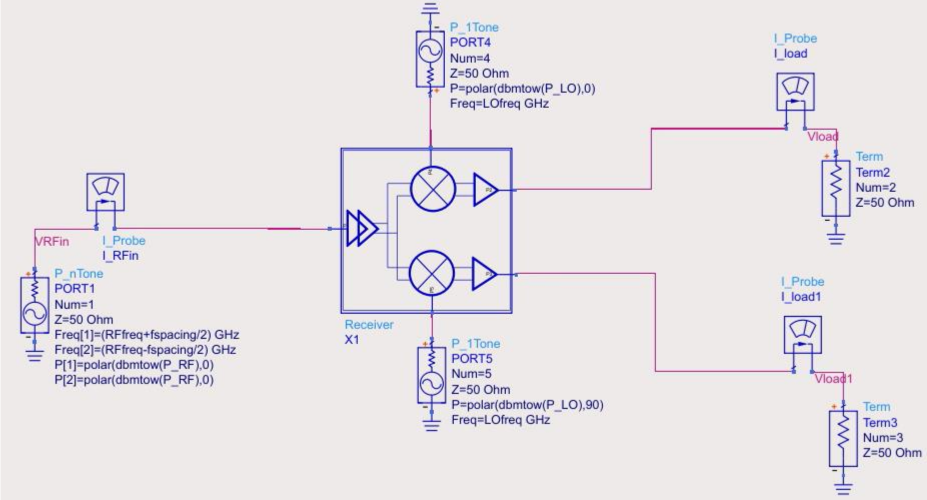




ADS Symbol

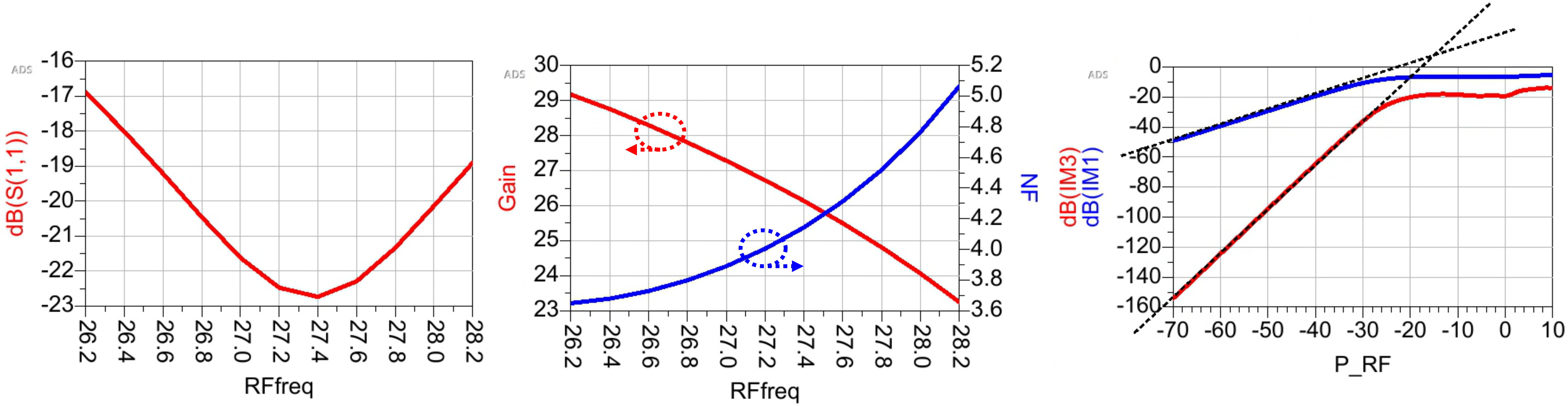


ADS circuit



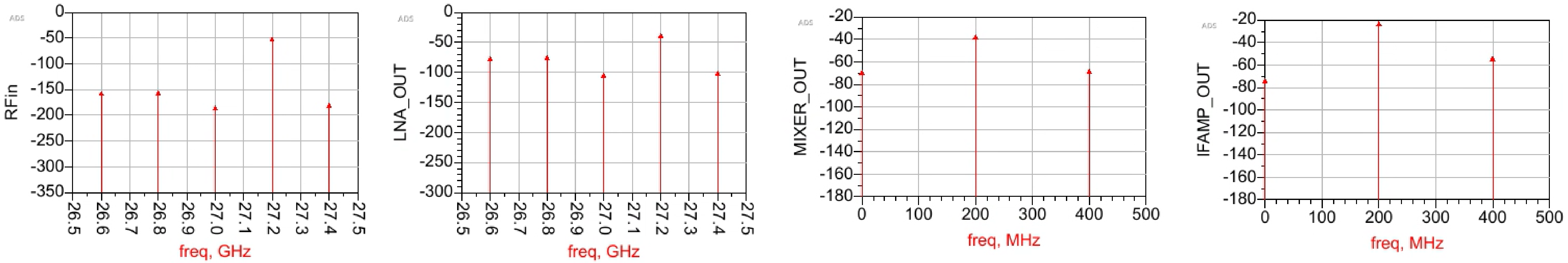
ADS test bench

iv. Receiver system: simulation results



Part	S11(dB)	Noise Figure (dB)	Gain (dB)	IIP3 (dBm)	Power Consumption (mW)
Receiver	-22.5 (<-12)	4.0 (<10)	26.7 (>25)	-17.4 (>-20)	28.2 (<30)

iv. Receiver system: simulation results - Spectrum



Part	S11(dB)	Noise Figure (dB)	Gain (dB)	IIP3 (dBm)	Power Consumption (mW)
Receiver	-22.5 (<-12)	4.0 (<10)	26.7 (>25)	-17.4 (>-20)	28.2 (<30)

Outline

- Architecture of the Receiver
- Workload Distribution
- Schematic of Building Blocks
  i. LNA
  ii. Mixer
  iii. IF Amplifier
- Simulation Results
  i. LNA
  ii. Mixer
  iii. IF Amplifier
  iv. Receiver System
- **Conclusion**

Conclusion

Parameters	Specifications	Simulations
Noise Figure (dB)	< 7	4.0
Conversion Voltage Gain (dB)	> 25	26.7
S11 (dB)	< -12	-22.5
IIP3 (dBm)	> -20	-17.4
Power Consumption (mW)	< 30	28.2
EVM	< 15%	On-going

Acknowledgement

We would like to thank Sarah, Shawn, and Elise for their help of software operation and debug, and Oscar for useful discussions.