



1. Description

1.1. Project

Project Name	KLST_PANDA-STM32H723ZGT-BSP
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	03/01/2024

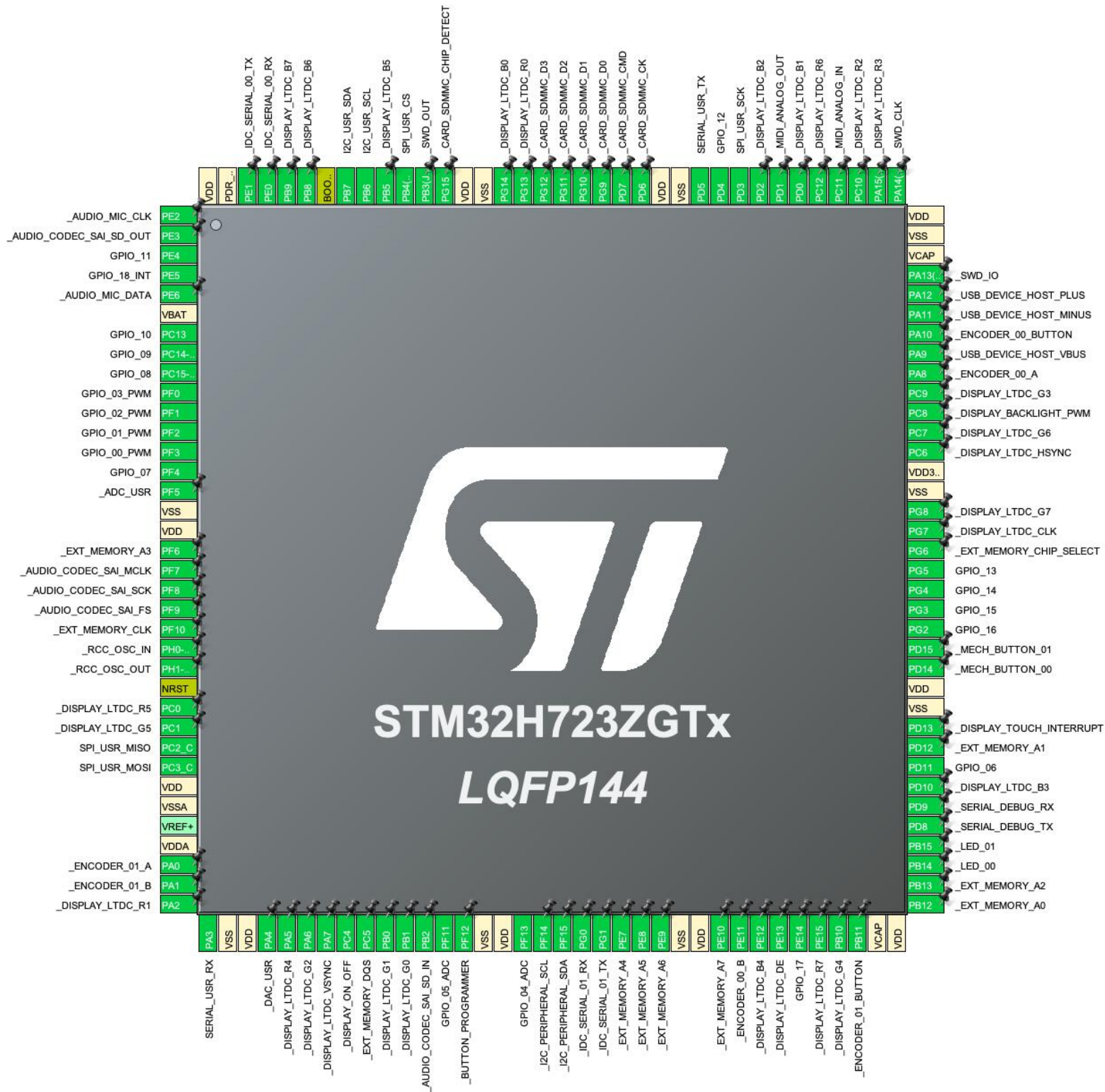
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SAI4_CK1	_AUDIO_MIC_CLK
2	PE3	I/O	SAI1_SD_B	_AUDIO_CODEC_SAI_SD_OUT
3	PE4 *	I/O	GPIO_Output	GPIO_11
4	PE5	I/O	TIM15_CH1	GPIO_18_INT
5	PE6	I/O	SAI4_D1	_AUDIO_MIC_DATA
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	GPIO_10
8	PC14-OSC32_IN *	I/O	GPIO_Output	GPIO_09
9	PC15-OSC32_OUT *	I/O	GPIO_Output	GPIO_08
10	PF0	I/O	TIM23_CH1	GPIO_03_PWM
11	PF1	I/O	TIM23_CH2	GPIO_02_PWM
12	PF2	I/O	TIM23_CH3	GPIO_01_PWM
13	PF3	I/O	TIM23_CH4	GPIO_00_PWM
14	PF4 *	I/O	GPIO_Output	GPIO_07
15	PF5	I/O	ADC3_INP4	_ADC_USR
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	OCTOSPIM_P1_IO3	_EXT_MEMORY_A3
19	PF7	I/O	SAI1_MCLK_B	_AUDIO_CODEC_SAI_MCLK
20	PF8	I/O	SAI1_SCK_B	_AUDIO_CODEC_SAI_SCK
21	PF9	I/O	SAI1_FS_B	_AUDIO_CODEC_SAI_FS
22	PF10	I/O	OCTOSPIM_P1_CLK	_EXT_MEMORY_CLK
23	PH0-OSC_IN	I/O	RCC_OSC_IN	_RCC_OSC_IN
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	_RCC_OSC_OUT
25	NRST	Reset		
26	PC0	I/O	LTDC_R5	_DISPLAY_LTDC_R5
27	PC1	I/O	LTDC_G5	_DISPLAY_LTDC_G5
28	PC2_C	I/O	SPI2_MISO	SPI_USR_MISO
29	PC3_C	I/O	SPI2_MOSI	SPI_USR_MOSI
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0	I/O	TIM2_CH1	_ENCODER_01_A
35	PA1	I/O	TIM2_CH2	_ENCODER_01_B

KLST_PANDA-STM32H723ZGT-BSP Project
Configuration Report

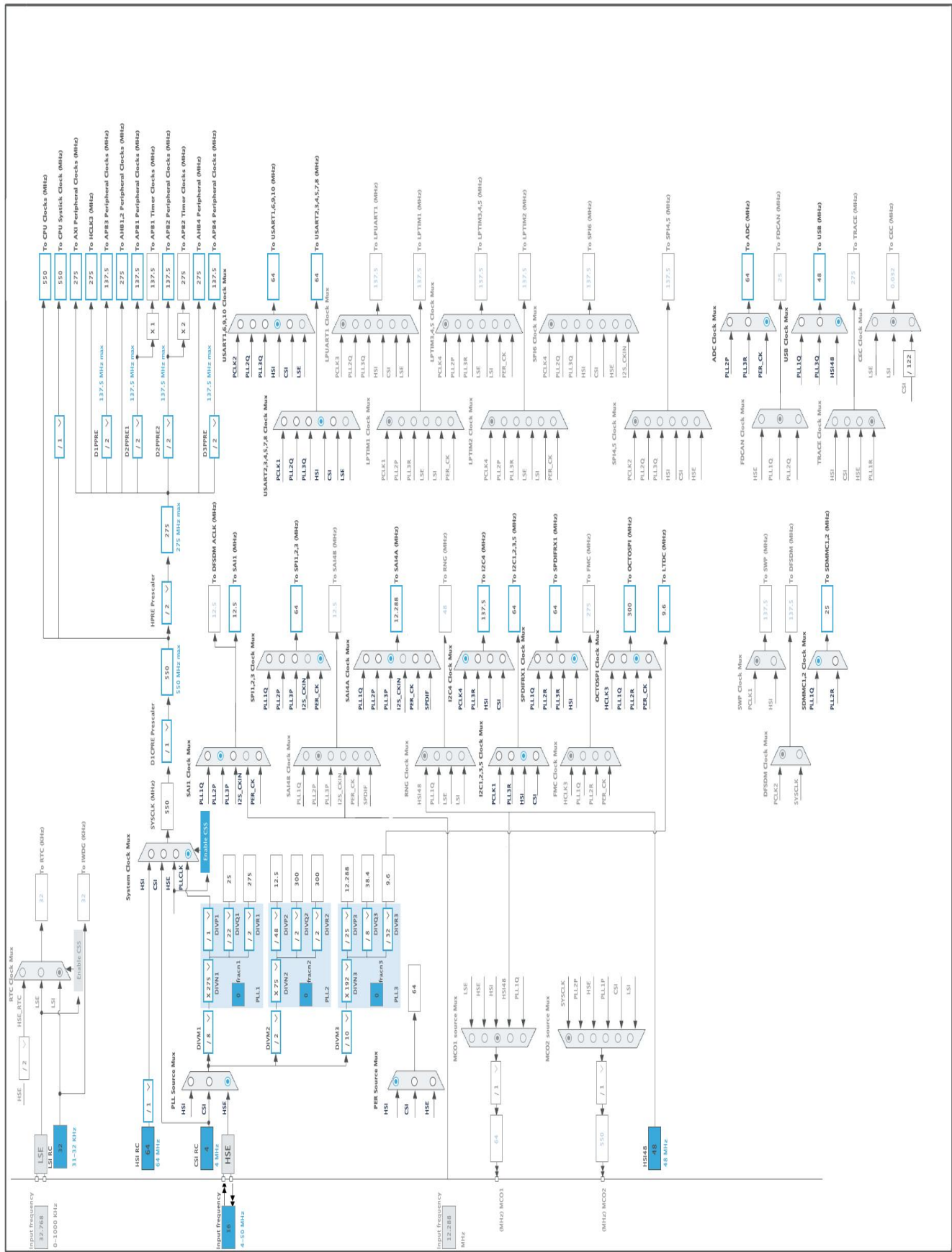
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
36	PA2	I/O	LTDC_R1	_DISPLAY_LTDC_R1
37	PA3	I/O	USART2_RX	SERIAL_USR_RX
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC1_OUT1	_DAC_USR
41	PA5	I/O	LTDC_R4	_DISPLAY_LTDC_R4
42	PA6	I/O	LTDC_G2	_DISPLAY_LTDC_G2
43	PA7	I/O	LTDC_VSYNC	_DISPLAY_LTDC_VSYNC
44	PC4 *	I/O	GPIO_Output	_DISPLAY_ON_OFF
45	PC5	I/O	OCTOSPIM_P1_DQS	_EXT_MEMORY_DQS
46	PB0	I/O	LTDC_G1	_DISPLAY_LTDC_G1
47	PB1	I/O	LTDC_G0	_DISPLAY_LTDC_G0
48	PB2	I/O	SAI1_SD_A	_AUDIO_CODEC_SAI_SD_IN
49	PF11	I/O	ADC1_INP2	GPIO_05_ADC
50	PF12	I/O	TIM24_CH2	_BUTTON_PROGRAMMER
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	ADC2_INP2	GPIO_04_ADC
54	PF14	I/O	I2C4_SCL	_I2C_PERIPHERAL_SCL
55	PF15	I/O	I2C4_SDA	_I2C_PERIPHERAL_SDA
56	PG0	I/O	UART9_RX	_IDC_SERIAL_01_RX
57	PG1	I/O	UART9_TX	_IDC_SERIAL_01_TX
58	PE7	I/O	OCTOSPIM_P1_IO4	_EXT_MEMORY_A4
59	PE8	I/O	OCTOSPIM_P1_IO5	_EXT_MEMORY_A5
60	PE9	I/O	OCTOSPIM_P1_IO6	_EXT_MEMORY_A6
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	OCTOSPIM_P1_IO7	_EXT_MEMORY_A7
64	PE11	I/O	TIM1_CH2	_ENCODER_00_B
65	PE12	I/O	LTDC_B4	_DISPLAY_LTDC_B4
66	PE13	I/O	LTDC_DE	_DISPLAY_LTDC_DE
67	PE14 *	I/O	GPIO_Output	GPIO_17
68	PE15	I/O	LTDC_R7	_DISPLAY_LTDC_R7
69	PB10	I/O	LTDC_G4	_DISPLAY_LTDC_G4
70	PB11	I/O	TIM2_CH4	_ENCODER_01_BUTTON
71	VCAP	Power		
72	VDD	Power		
73	PB12	I/O	OCTOSPIM_P1_IO0	_EXT_MEMORY_A0

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
74	PB13	I/O	OCTOSPIM_P1_IO2	_EXT_MEMORY_A2
75	PB14	I/O	TIM12_CH1	_LED_00
76	PB15	I/O	TIM12_CH2	_LED_01
77	PD8	I/O	USART3_TX	_SERIAL_DEBUG_TX
78	PD9	I/O	USART3_RX	_SERIAL_DEBUG_RX
79	PD10	I/O	LTDC_B3	_DISPLAY_LTDC_B3
80	PD11 *	I/O	GPIO_Output	GPIO_06
81	PD12	I/O	OCTOSPIM_P1_IO1	_EXT_MEMORY_A1
82	PD13	I/O	GPIO_EXTI13	_DISPLAY_TOUCH_INTER RUPT
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	GPIO_EXTI14	_MECH_BUTTON_00
86	PD15	I/O	TIM4_CH4	_MECH_BUTTON_01
87	PG2 *	I/O	GPIO_Output	GPIO_16
88	PG3 *	I/O	GPIO_Output	GPIO_15
89	PG4 *	I/O	GPIO_Output	GPIO_14
90	PG5 *	I/O	GPIO_Output	GPIO_13
91	PG6	I/O	OCTOSPIM_P1_NCS	_EXT_MEMORY_CHIP_SE LECT
92	PG7	I/O	LTDC_CLK	_DISPLAY_LTDC_CLK
93	PG8	I/O	LTDC_G7	_DISPLAY_LTDC_G7
94	VSS	Power		
95	VDD33USB	Power		
96	PC6	I/O	LTDC_HSYNC	_DISPLAY_LTDC_HSYNC
97	PC7	I/O	LTDC_G6	_DISPLAY_LTDC_G6
98	PC8	I/O	TIM3_CH3	_DISPLAY_BACKLIGHT_P WM
99	PC9	I/O	LTDC_G3	_DISPLAY_LTDC_G3
100	PA8	I/O	TIM1_CH1	_ENCODER_00_A
101	PA9	I/O	USB_OTG_HS_VBUS	_USB_DEVICE_HOST_VB US
102	PA10	I/O	TIM1_CH3	_ENCODER_00_BUTTON
103	PA11	I/O	USB_OTG_HS_DM	_USB_DEVICE_HOST_MIN US
104	PA12	I/O	USB_OTG_HS_DP	_USB_DEVICE_HOST_PLU S
105	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	_SWD_IO
106	VCAP	Power		
107	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
108	VDD	Power		
109	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	_SWD_CLK
110	PA15(JTDI)	I/O	LTDC_R3	_DISPLAY_LTDC_R3
111	PC10	I/O	LTDC_R2	_DISPLAY_LTDC_R2
112	PC11	I/O	UART4_RX	_MIDI_ANALOG_IN
113	PC12	I/O	LTDC_R6	_DISPLAY_LTDC_R6
114	PD0	I/O	LTDC_B1	_DISPLAY_LTDC_B1
115	PD1	I/O	UART4_TX	_MIDI_ANALOG_OUT
116	PD2	I/O	LTDC_B2	_DISPLAY_LTDC_B2
117	PD3	I/O	SPI2_SCK	SPI_USR_SCK
118	PD4 *	I/O	GPIO_Output	GPIO_12
119	PD5	I/O	USART2_TX	SERIAL_USR_TX
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	SDMMC2_CK	_CARD_SDMMC_CK
123	PD7	I/O	SDMMC2_CMD	_CARD_SDMMC_CMD
124	PG9	I/O	SDMMC2_D0	_CARD_SDMMC_D0
125	PG10	I/O	SDMMC2_D1	_CARD_SDMMC_D1
126	PG11	I/O	SDMMC2_D2	_CARD_SDMMC_D2
127	PG12	I/O	SDMMC2_D3	_CARD_SDMMC_D3
128	PG13	I/O	LTDC_R0	_DISPLAY_LTDC_R0
129	PG14	I/O	LTDC_B0	_DISPLAY_LTDC_B0
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Input	_CARD_SDMMC_CHIP_DETECT
133	PB3(JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	_SWD_OUT
134	PB4(NJTRST)	I/O	SPI2_NSS	SPI_USR_CS
135	PB5	I/O	LTDC_B5	_DISPLAY_LTDC_B5
136	PB6	I/O	I2C1_SCL	I2C_USR_SCL
137	PB7	I/O	I2C1_SDA	I2C_USR_SDA
138	BOOT0	Boot		
139	PB8	I/O	LTDC_B6	_DISPLAY_LTDC_B6
140	PB9	I/O	LTDC_B7	_DISPLAY_LTDC_B7
141	PE0	I/O	UART8_RX	_IDC_SERIAL_00_RX
142	PE1	I/O	UART8_TX	_IDC_SERIAL_00_TX
143	PDR_ON	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	KLST_PANDA-STM32H723ZGT-BSP
Project Folder	/Users/dennisppaul/Documents/dennisppaul/projects/klangstrom/git/klangstrom-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x400
Minimum Stack Size	0x800

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_BDMA_Init	BDMA
5	MX_I2C1_Init	I2C1
6	MX_I2C4_Init	I2C4
7	MX_TIM1_Init	TIM1
8	MX_TIM2_Init	TIM2
9	MX_USART2_UART_Init	USART2
10	MX_USART3_UART_Init	USART3
11	MX_ADC1_Init	ADC1

Rank	Function Name	Peripheral Instance Name
12	MX_ADC2_Init	ADC2
13	MX_ADC3_Init	ADC3
14	MX_SPI2_Init	SPI2
15	MX_TIM4_Init	TIM4
16	MX_TIM23_Init	TIM23
17	MX_LTDC_Init	LTDC
18	MX_DMA2D_Init	DMA2D
19	MX_TIM12_Init	TIM12
20	MX_TIM24_Init	TIM24
21	MX_UART8_Init	UART8
22	MX_SAI4_Init	SAI4
23	MX_UART9_Init	UART9
24	MX_FATFS_Init	FATFS
25	MX_SDMMC2_SD_Init	SDMMC2
26	MX_TIM3_Init	TIM3
27	MX_TIM15_Init	TIM15
28	MX_UART4_Init	UART4
29	MX_OCTOSPI1_Init	OCTOSPI1
30	MX_DAC1_Init	DAC1
31	MX_SAI1_Init	SAI1
32	MX_CRC_Init	CRC
33	MX_PDM2PCM_Init	PDM2PCM
34	MX_USB_HOST_Init	USB_HOST

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
MCU	STM32H723ZGTx
Datasheet	DS13313_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

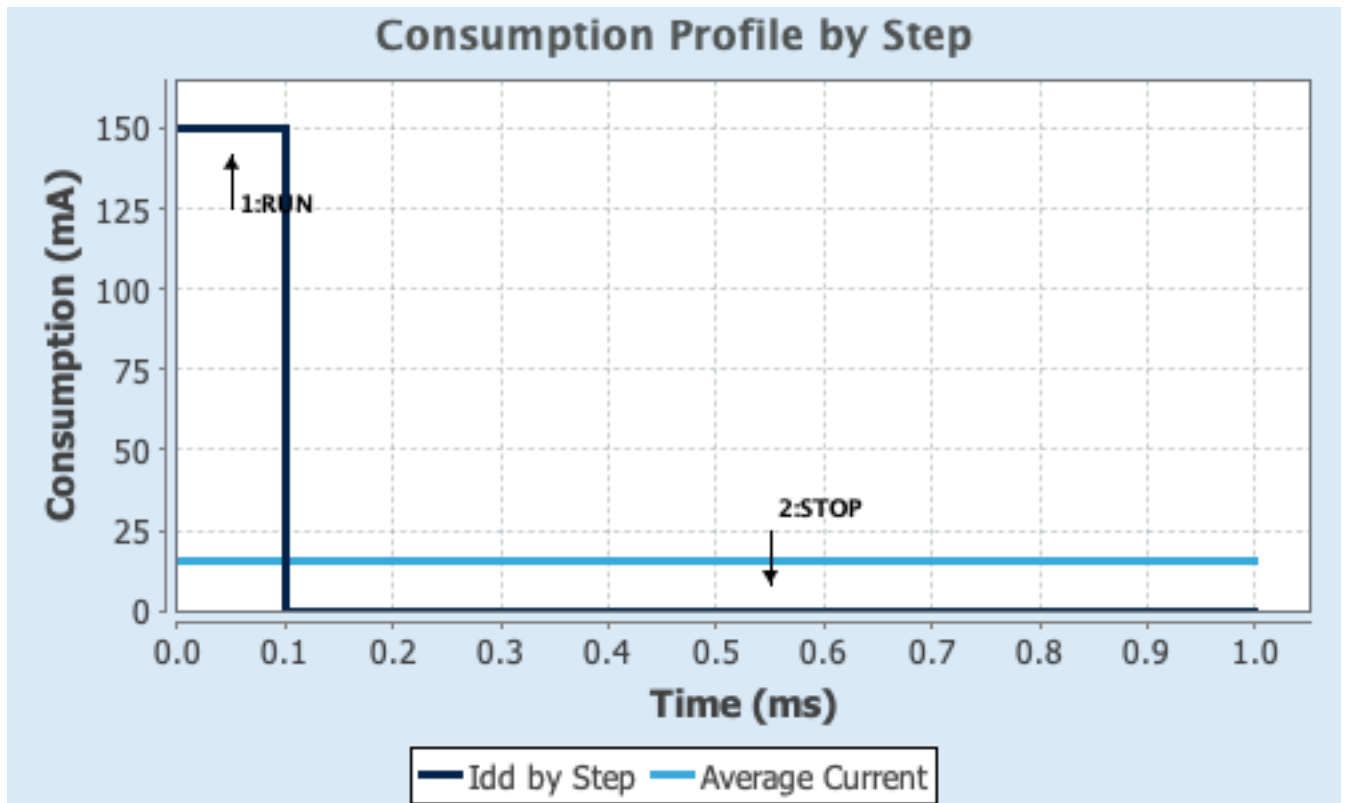
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0/Boost	SVOS5: System-Scale5
D1 Mode	DRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	SRAM1/FlashMode-ON/Cache	NA
CPU Frequency	550 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	150 mA	94.5 μ A
Duration	0.1 ms	0.9 ms
DMIPS	1177.0	0.0
Ta Max	105.2	124.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	15.09 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1

IN2: IN2 Single-ended

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler

Asynchronous clock mode divided by 4 *

Resolution

ADC 16-bit resolution

Scan Conversion Mode

Disabled

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

End Of Conversion Selection

End of single conversion

Overrun behaviour

Overrun data preserved

Left Bit Shift

No bit shift

Conversion Data Management Mode

Regular Conversion data stored in DR register only

Low Power Auto Wait

Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions

Enable

Enable Regular Oversampling

Disable

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

Rank

1

Channel

Channel 2

Sampling Time

1.5 Cycles

Offset Number

No offset

Offset Signed Saturation

Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions

Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode

false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode

false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode

false

2.2. ADC2

IN2: IN2 Single-ended

2.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler

Asynchronous clock mode divided by 4 *

Resolution

ADC 16-bit resolution

Scan Conversion Mode

Disabled

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

End Of Conversion Selection

End of single conversion

Overrun behaviour

Overrun data preserved

Left Bit Shift

No bit shift

Conversion Data Management Mode

Regular Conversion data stored in DR register only

Low Power Auto Wait

Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions

Enable

Enable Regular Oversampling

Disable

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

Rank

1

Channel

Channel 2

Sampling Time

1.5 Cycles

Offset Number

No offset

Offset Signed Saturation

Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions

Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode

false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode

false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode

false

2.3. ADC3

IN4: IN4 Single-ended

2.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Scan Conversion Mode	Disabled
Data Alignment	Right alignment
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Sampling Mode	Normal
<u>Rank</u>	1
Channel	Channel 4
Sampling Time	2.5 Cycles
Offset Number	No offset
Offset Sign	Offset Sign Negative

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable
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Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false
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Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false
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Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false
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2.4. CORTEX_M7

2.4.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode Disabled

Cortex Interface Settings:

CPU ICache Enabled *

CPU DCache Enabled *

Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers *

Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled *

MPU Region Base Address KLST_DISPLAY_FRAMEBUFFER_ADDRESS *

MPU Region Size 16MB *

MPU SubRegion Disable 0x0 *

MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED *

MPU Instruction Access DISABLE *

MPU Shareability Permission DISABLE

MPU Cacheable Permission ENABLE *

MPU Bufferable Permission DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region Enabled *

MPU Region Base Address 0x38000000 *

MPU Region Size 16KB *

MPU SubRegion Disable 0x0 *

MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED *

MPU Instruction Access DISABLE *

MPU Shareability Permission DISABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region Disabled

2.5. CRC

mode: Activated

2.5.1. Parameter Settings:

Basic Parameters:

Default Polynomial State Enable

Default Init Value State Enable

Advanced Parameters:

Input Data Inversion Mode None

Output Data Inversion Mode Disable

Input Data Format Bytes

2.6. DAC1

OUT1 connected to: only external pin

2.6.1. Parameter Settings:

DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

2.7. DEBUG

Debug: Trace Asynchronous Sw

2.8. DMA2D

mode: Activated

2.8.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)
DMA2D Chroma Sub-Sampling Mode	No chroma sub-sampling 4:4:4

2.9. I2C1

I2C: I2C

2.9.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
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I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.10. I2C4

I2C: I2C

2.10.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Fast Mode *
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Disabled *
Timing	0x00D056FC *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.11. LTDC

Display Type: RGB888 (24 bits)

2.11.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	4 *
Horizontal Back Porch	43 *
Active Width	KLST_DISPLAY_WIDTH *
Horizontal Front Porch	8 *
HSync Width	3
Accumulated Horizontal Back Porch Width	46
Accumulated Active Width	526
Total Width	534

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	12 *
Active Height	KLST_DISPLAY_HEIGHT *
Vertical Front Porch	8 *
VSynC Height	3
Accumulated Vertical Back Porch Height	15
Accumulated Active Height	287
Total Height	295

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

Red	0
Green	0
Blue	0

2.11.2. Layer Settings:

Layer Default Color:

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Number of Layers:

Number of Layers	1 layer *
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Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	KLST_DISPLAY_WIDTH *
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	KLST_DISPLAY_HEIGHT *

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
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Blending:

Layer 0 - Alpha constant for blending	255 *
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	KLST_DISPLAY_FRAMEBUFFER_ADDRESS *
Layer 0 - Color Frame Buffer Line Length (Image Width)	KLST_DISPLAY_WIDTH *
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	KLST_DISPLAY_HEIGHT *

2.12. OCTOSPI1

Mode: HyperBus(TM)

Clock: Port1 CLK

Chip Select: Port1 NCS

Data Strobe: Port1 DQS (RWDS)

Data [3:0]: Port1 IO[3:0]

Data [7:4]: Port1 IO[7:4]

2.12.1. Parameter Settings:

Generic:

Fifo Threshold	4 *
Dual Quad mode	Disable
Memory Type	HyperBus(TM)
Device Size	24 *
Device Type	RAM *
Chip Select High Time	2 *
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	

	2 *
Sample Shifting	None
Delay Hold Quarter Cycle	Enable *
Chip Select Boundary	0
Delay Block	Enable *
Maximum Transfer	23 *
Refresh Rate	799 *
HyperBus(TM):	
RW Recovery Time	4 *
Access Time	7 *
Write Access Latency	Enable *
Latency Mode	Fixed *

2.13. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.13.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	3 WS (4 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 2 and 4 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL3 input frequency range	Between 1 and 2 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL3 clock Output range	MEDIUM VCO range

2.14. SAI1

Mode: Synchronous Slave

mode: I2S/PCM Protocol

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

2.14.1. Parameter Settings:

SAI A:

Synchronization Inputs	Synchronous with other block of same SAI
Audio Mode	Slave Receive
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven

Protocol Parameters

Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Fifo Threshold	Empty
Output Drive	Disabled

SAI B:

Synchronization Inputs	Asynchronous
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven

Protocol Parameters

Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Clock Source	SAI PLL Clock
Master Clock No Divider	Enabled
Audio Frequency	48 KHz *
Real Audio Frequency	48.828 KHz *
Error between Selected	1.72 % *
Fifo Threshold	Empty
Output Drive	Disabled

2.15. SAI4

Mode: Pulse Density Modulation using MicroPhones pairs (1-2) and CK1 as clock

2.15.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous
Protocol	Free
Audio Mode	Master Receive
Frame Length	16 bits *
Data Size	8 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active High *
Frame Synchro Offset	First Bit
First Bit Offset	0
Number of Slots	2 *
Slot Active Final Value	0x0000FFFF *
Slot Active	All *
Clock Source	SAI PLL Clock
Master Clock No Divider	Enabled
Audio Frequency	48 KHz *
Real Audio Frequency	48.0 KHz *
Error between Selected	0.0 % *
Clock Strobing	Falling Edge
Fifo Threshold	Empty
Output Drive	Disabled

2.16. SDMMC2

Mode: SD 4 bits Wide bus

2.16.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock

SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

2.17. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

2.17.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	32.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

2.18. SYS

Timebase Source: SysTick

2.19. TIM1

Channel3: Input Capture direct mode

Combined Channels: Encoder Mode

2.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection	Both Edges *
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	7 *

Encoder:

Encoder Mode	Encoder Mode TI1 and TI2 *
_____ Parameters for Channel 1 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *
_____ Parameters for Channel 2 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *

2.20. TIM2

Channel4: Input Capture direct mode

Combined Channels: Encoder Mode

2.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 4:

Polarity Selection	Both Edges *
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	7 *

Encoder:

Encoder Mode	Encoder Mode TI1 and TI2 *
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *

2.21. TIM3

Channel3: PWM Generation CH3

2.21.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	32768 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
--------------------	---------

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	16383 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.22. TIM4

Channel4: Input Capture direct mode

2.22.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 4:

Polarity Selection	Both Edges *
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

2.23. TIM12

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

2.23.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
--------------------	---------

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.24. TIM15

Channel1: Input Capture direct mode

2.24.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
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IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

2.25. TIM23

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

2.25.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
--------------------	---------

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable

CH Polarity	High
PWM Generation Channel 4:	
Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.26. TIM24

Channel2: Input Capture direct mode

2.26.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

2.27. UART4

Mode: Asynchronous

2.27.1. Parameter Settings:

Basic Parameters:

Baud Rate	31250 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.28. UART8

Mode: Asynchronous

2.28.1. Parameter Settings:

Basic Parameters:

Baud Rate	31250 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.29. UART9

Mode: Asynchronous

2.29.1. Parameter Settings:

Basic Parameters:

Baud Rate	31250 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.30. USART2

Mode: Asynchronous

2.30.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1
Advanced Parameters:	
Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.31. USART3

Mode: Asynchronous

2.31.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.32. USB_OTG_HS

Internal FS Phy: Host_Only

Activate_VBUS: Activate-VBUS

2.32.1. Parameter Settings:

Host Channels	16
Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Signal start of frame	Disabled

2.33. FATFS

mode: SD Card

2.33.1. Set Defines:

Version:

FATFS version	R0.12c
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Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled

MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

2.33.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance	SDMMC2
Use dma template	Enabled *
BSP code for SD	Generic

2.33.3. Platform Settings:

Detect_SDIO	PG15
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2.34. PDM2PCM

mode: Enabled

2.34.1. Parameter Settings:

Version:

PDM2PCM version	3.5.1
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PDM2PCM:

How many channel do you use ?	1
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2.34.2. CHANNEL1:

PDM2PCM_Channel:

Initialisation

bit_order (define the bit order)	PDM_FILTER_BIT_ORDER_LSB
endianness (define the byte order)	PDM_FILTER_ENDIANNESSE_BE
high_pass_tap (the high pass filter alpha)	2104533974
in_ptr_channels (the channels number in the input PDM stream)	2
out_ptr_channels (the channels number in the output PCM stream)	2

Initial Configuration

decimation_factor (the factor to adapt PDM frequency to PCM frequency)	PDM_FILTER_DEC_FACTOR_64
output_samples_number (the number of samples by request)	16
mic_gain (the microphone gain in dB)	0

2.35. USB_HOST

Class For HS IP: Human Interface Host Class (HID)

2.35.1. Parameter Settings:

NO_SW_VBUS_DRIVE_HS false

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	2
USBH_MAX_NUM_INTERFACES (Maximum number of interfaces)	2
USBH_MAX_NUM_SUPPORTED_CLASS (Maximum number of supported class)	1
USBH_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximum size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximum size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	

3: All messages and internal debug messages are shown *

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS) Disabled

2.35.2. Platform Settings:

Drive_VBUS_HS PC8

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PF11	ADC1_INP2	Analog mode	No pull-up and no pull-down	n/a	GPIO_05_ADC
ADC2	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	GPIO_04_ADC
ADC3	PF5	ADC3_INP4	Analog mode	No pull-up and no pull-down	n/a	_ADC_USR
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	_DAC_USR
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	_SWD_IO
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	_SWD_CLK
	PB3(JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	_SWD_OUT
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	I2C_USR_SCL
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	I2C_USR_SDA
I2C4	PF14	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	_I2C_PERIPHERAL_SCL
	PF15	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	_I2C_PERIPHERAL_SDA
LTDC	PC0	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R5
	PC1	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G5
	PA2	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R1
	PA5	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R4
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G2
	PA7	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_VSYNC
	PB0	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G1
	PB1	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G0
	PE12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_B4

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IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE13	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_DE
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R7
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G4
	PD10	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_B3
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_CLK
	PG8	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G7
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_HSYNC
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G6
	PC9	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_G3
	PA15(JTDI)	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R3
	PC10	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R2
	PC12	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R6
	PD0	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_B1
	PD2	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_B2
	PG13	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_R0
	PG14	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_B0
	PB5	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_B5
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	_DISPLAY_LTDC_B6
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_DISPLAY_LTDC_B7

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Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
OCTOSPI1	PF6	OCTOSPIM_P1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A3
	PF10	OCTOSPIM_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_CLK
	PC5	OCTOSPIM_P1_DQS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_DQS
	PE7	OCTOSPIM_P1_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A4
	PE8	OCTOSPIM_P1_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A5
	PE9	OCTOSPIM_P1_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A6
	PE10	OCTOSPIM_P1_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A7
	PB12	OCTOSPIM_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A0
	PB13	OCTOSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A2
	PD12	OCTOSPIM_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_A1
	PG6	OCTOSPIM_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_EXT_MEMORY_CHIP_SELECT
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	_RCC_OSC_IN
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	_RCC_OSC_OUT
SAI1	PE3	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	_AUDIO_CODEC_SAI_SD_OUT
	PF7	SAI1_MCLK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	_AUDIO_CODEC_SAI_MCLK
	PF8	SAI1_SCK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	_AUDIO_CODEC_SAI_SCK
	PF9	SAI1_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	_AUDIO_CODEC_SAI_FS
	PB2	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	_AUDIO_CODEC_SAI_SD_IN
SAI4	PE2	SAI4_CK1	Alternate Function Push Pull	No pull-up and no pull-down	Low	_AUDIO_MIC_CLK
	PE6	SAI4_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	_AUDIO_MIC_DATA
SDMMC2	PD6	SDMMC2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_CARD_SDMMC_CK
	PD7	SDMMC2_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_CARD_SDMMC_CMD
	PG9	SDMMC2_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_CARD_SDMMC_D0
	PG10	SDMMC2_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_CARD_SDMMC_D1
	PG11	SDMMC2_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_CARD_SDMMC_D2
	PG12	SDMMC2_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	_CARD_SDMMC_D3

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IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI2	PC2_C	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI_USR_MISO
	PC3_C	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI_USR_MOSI
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI_USR_SCK
	PB4(NJTRST)	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI_USR_CS
TIM1	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	_ENCODER_00_B
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	_ENCODER_00_A
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	_ENCODER_00_BUTTON
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	_ENCODER_01_A
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	_ENCODER_01_B
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	_ENCODER_01_BUTTON
TIM3	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	_DISPLAY_BACKLIGHT_PWM
TIM4	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	_MECH_BUTTON_01
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	_LED_00
	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	_LED_01
TIM15	PE5	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	GPIO_18_INT
TIM23	PF0	TIM23_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	GPIO_03_PWM
	PF1	TIM23_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	GPIO_02_PWM
	PF2	TIM23_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	GPIO_01_PWM
	PF3	TIM23_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	GPIO_00_PWM
TIM24	PF12	TIM24_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	_BUTTON_PROGRAMMER
UART4	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_MIDI_ANALOG_IN
	PD1	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_MIDI_ANALOG_OUT
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_IDC_SERIAL_00_RX
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_IDC_SERIAL_00_TX
UART9	PG0	UART9_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_IDC_SERIAL_01_RX
	PG1	UART9_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_IDC_SERIAL_01_TX
USART2	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	SERIAL_USR_RX
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	SERIAL_USR_TX
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_SERIAL_DEBUG_TX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	_SERIAL_DEBUG_RX
USB_OTG_HS	PA9	USB_OTG_HS_VBUS	Input mode	No pull-up and no pull-down	n/a	_USB_DEVICE_HOST_VBUS
	PA11	USB_OTG_HS_DM	n/a	n/a	n/a	_USB_DEVICE_HOST_MINUS
	PA12	USB_OTG_HS_DP	n/a	n/a	n/a	_USB_DEVICE_HOST_PLUS
GPIO	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_11
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_10
	PC14-	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_09

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IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC32_IN					
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_08
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_07
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	_DISPLAY_ON_OFF
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_17
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_06
	PD13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	_DISPLAY_TOUCH_INTERRUPT
	PD14	GPIO_EXTI14	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	_MECH_BUTTON_00
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_16
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_15
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_14
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_13
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_12
	PG15	GPIO_Input	Input mode	Pull-up *	n/a	_CARD_SDMMC_CHIP_DETECT

3.2. DMA configuration

DMA request	Stream	Direction	Priority
SAI1_A	DMA1_Stream0	Peripheral To Memory	Low
SAI1_B	DMA1_Stream1	Memory To Peripheral	Low
UART8_RX	DMA1_Stream2	Peripheral To Memory	Low
UART8_TX	DMA1_Stream3	Memory To Peripheral	Low
UART9_RX	DMA1_Stream4	Peripheral To Memory	Low
UART9_TX	DMA1_Stream5	Memory To Peripheral	Low
UART4_RX	DMA1_Stream6	Peripheral To Memory	Low
UART4_TX	DMA1_Stream7	Memory To Peripheral	Low

SAI1_A: DMA1_Stream0 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: **Half Word ***
 Memory Data Width: **Half Word ***

SAI1_B: DMA1_Stream1 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: **Half Word ***
 Memory Data Width: **Half Word ***

UART8_RX: DMA1_Stream2 DMA request Settings:

Mode: Normal
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

UART8_TX: DMA1_Stream3 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

UART9_RX: DMA1_Stream4 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

UART9_TX: DMA1_Stream5 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

UART4_RX: DMA1_Stream6 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

UART4_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	Enable *
Peripheral Data Width:	Byte
Memory Data Width:	Byte

3.3. BDMA configuration

DMA request	Stream	Direction	Priority
SAI4_A	BDMA_Channel0	Peripheral To Memory	Low

SAI4_A: BDMA_Channel0 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Half Word ***
Memory Data Width: **Half Word ***

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
DMA1 stream3 global interrupt	true	0	0
DMA1 stream4 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
TIM1 break interrupt	true	0	0
TIM1 update interrupt	true	0	0
TIM1 trigger and commutation interrupts	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
DMA1 stream7 global interrupt	true	0	0
UART4 global interrupt	true	0	0
USB On The Go HS End Point 1 Out global interrupt	true	0	0
USB On The Go HS End Point 1 In global interrupt	true	0	0
USB On The Go HS global interrupt	true	0	0
UART8 global interrupt	true	0	0
SAI1 global interrupt	true	0	0
LTDC global interrupt	true	0	0
LTDC Error global Interrupt	true	0	0
DMA2D global interrupt	true	0	0
OCTOSPI1 global interrupt	true	0	0
SDMMC2 global interrupt	true	0	0
BDMA channel0 global interrupt	true	0	0

Interrupt Table	Enable	Preenmption Priority	SubPriority
SAI4 global interrupt	true	0	0
UART9 global interrupt	true	0	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI2 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
FPU global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		
TIM15 global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		
TIM23 global interrupt	unused		
TIM24 global interrupt	unused		

3.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream2 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true
DMA1 stream4 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
TIM1 break interrupt	false	true	true
TIM1 update interrupt	false	true	true
TIM1 trigger and commutation interrupts	false	true	true
TIM1 capture compare interrupt	false	true	true
TIM2 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
DMA1 stream7 global interrupt	false	true	true
UART4 global interrupt	false	true	true
USB On The Go HS End Point 1 Out global interrupt	false	true	true
USB On The Go HS End Point 1 In global interrupt	false	true	true
USB On The Go HS global interrupt	false	true	true
UART8 global interrupt	false	true	true
SAI1 global interrupt	false	true	true
LTDC global interrupt	false	true	true
LTDC Error global Interrupt	false	true	true
DMA2D global interrupt	false	true	true
OCTOSPI1 global interrupt	false	true	true
SDMMC2 global interrupt	false	true	true
BDMA channel0 global interrupt	false	true	true
SAI4 global interrupt	false	true	true
UART9 global interrupt	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware

FATFS ✓

PDM2PCM ✓

USB_HOST ✓

System Core

BDMA ✓

CORTEX_M7 ✓

DMA ✓

GPIO ✓

MDMA

NVIC ✓

RCC ✓

SYS ✓

Analog

ADC1 ✓

ADC2 ✓

ADC3 ✓

DAC1 ✓

Timers

TIM1 ✓

TIM2 ✓

TIM3 ✓

TIM4 ✓

TIM12 ✓

TIM15 ✓

TIM23 ✓

TIM24 ✓

Connectivity

I2C1 ✓

I2C4 ✓

OCTOSPI1 ✓

SDMMC2 ✓

SPI2 ✓

UART4 ✓

UART8 ✓

UART9 ✓

USART2 ✓

USART3 ✓

USB_HS ✓

Multimedia

DMA2D ✓

LTDC ✓

SAI1 ✓

SAI4 ✓

Security

Computing

CRC ✓

Trace and Debug Power and Thermal

DEBUG ✓

5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdل.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h72x-3x_line_product-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7vl.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-

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Application Notes https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

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