

Izhodni kondenzator mora po izračunih imeti vsaj 12uF. Uporabljeni so 4.7u 25V X7R kondenzatorji, ker so cenejši od npr. 22u 25V..

Sheet: /5V ----> +15V_+15V/
File: DCDC_3.3_+ -15.kicad_sch

Title:

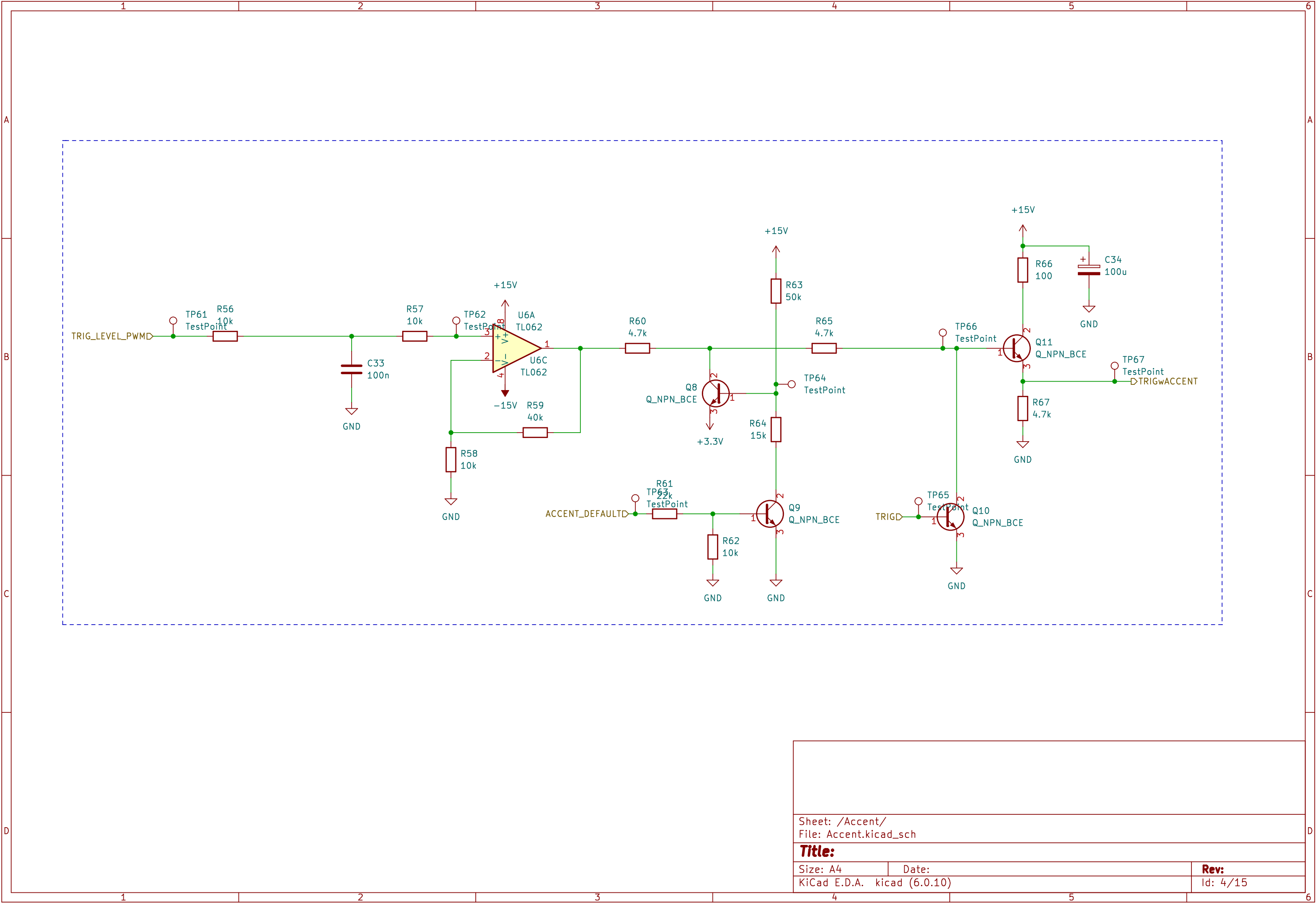
Size: A4

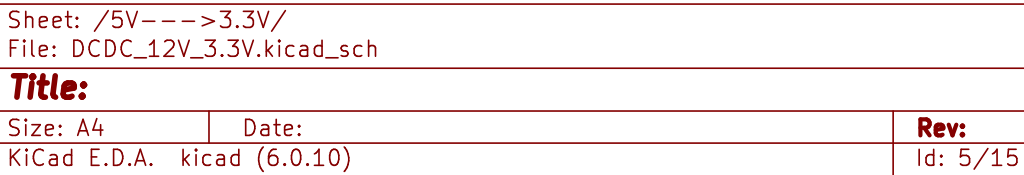
Date:

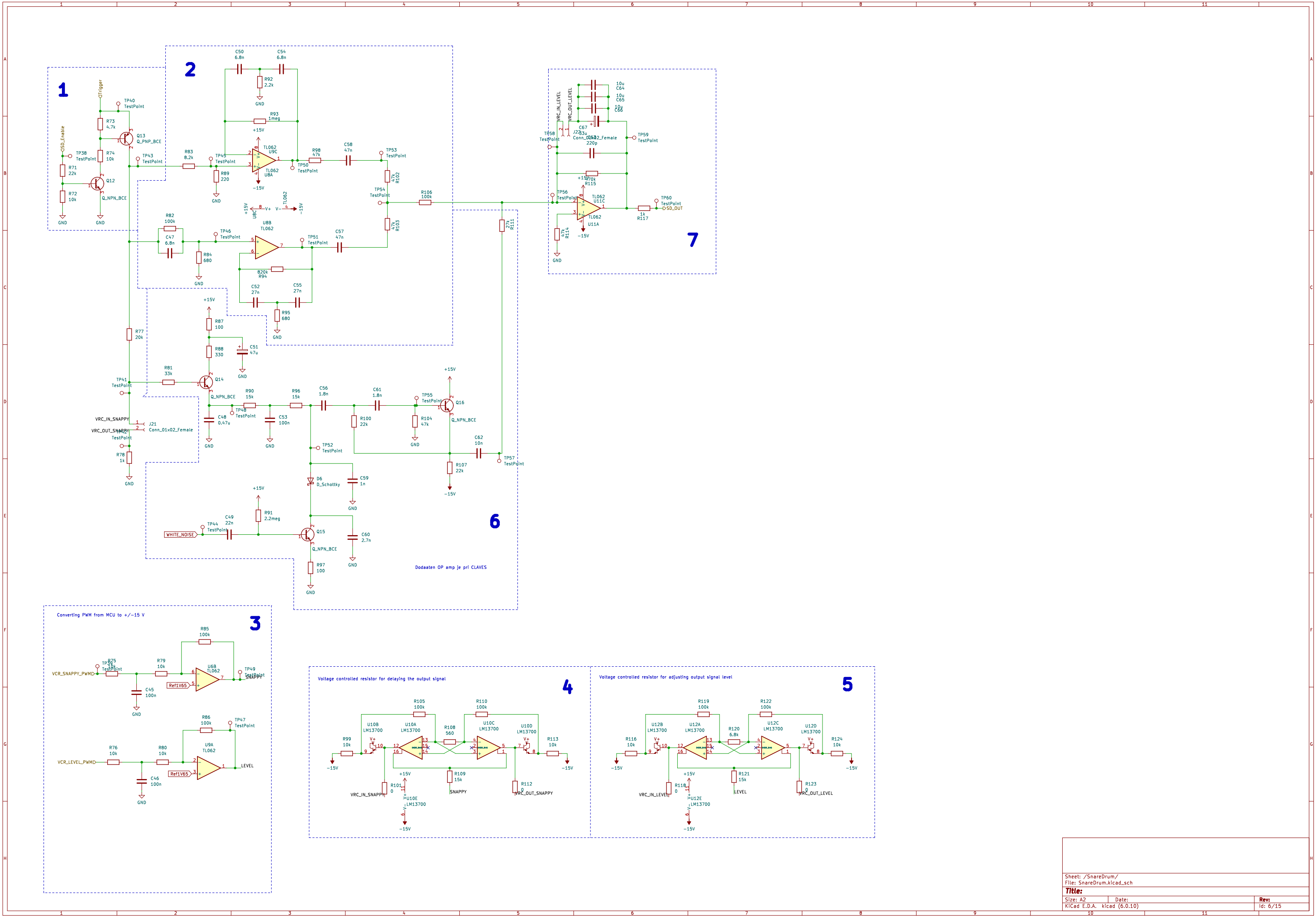
Rev:

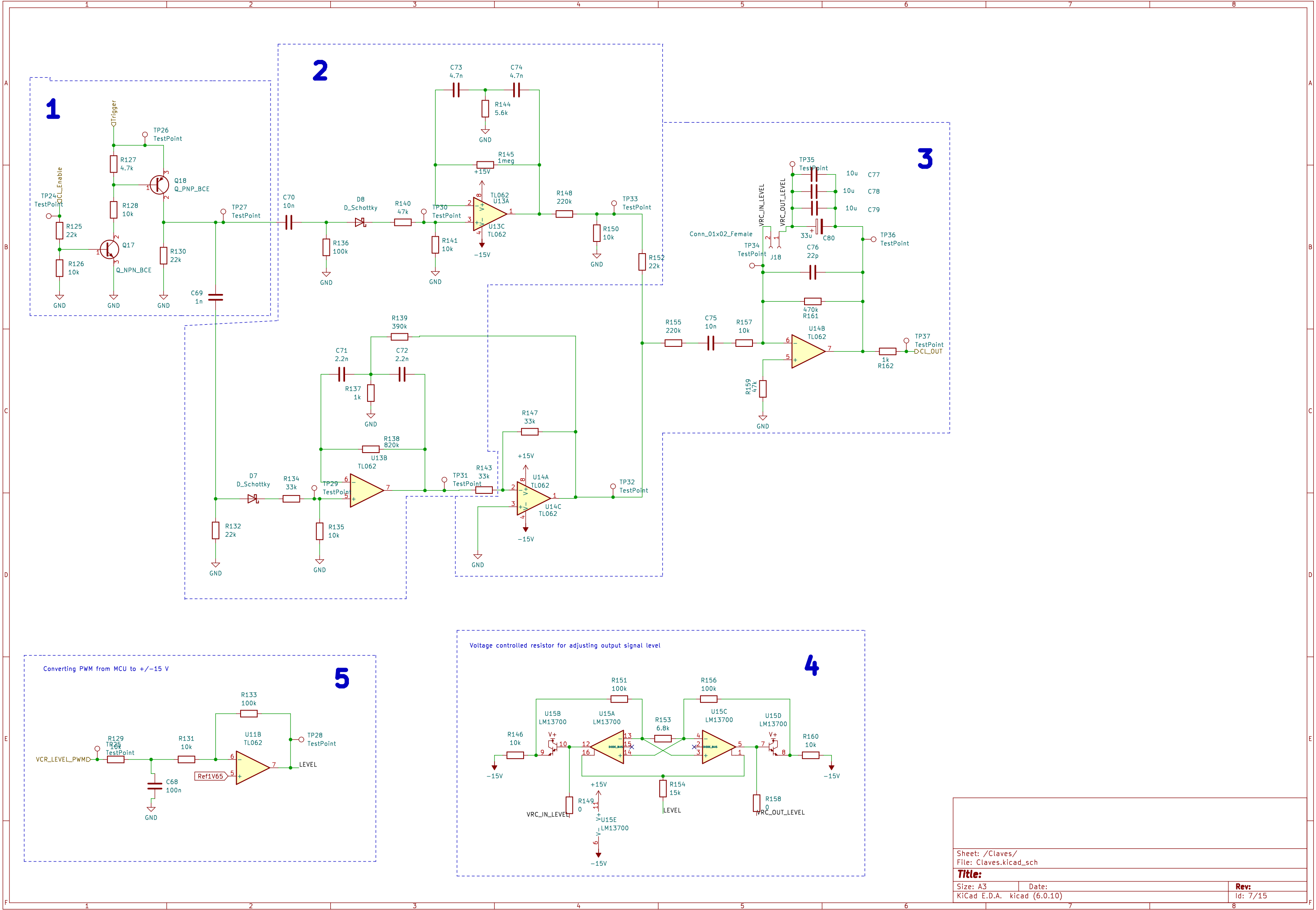
KiCad E.D.A. kicad (6.0.10)

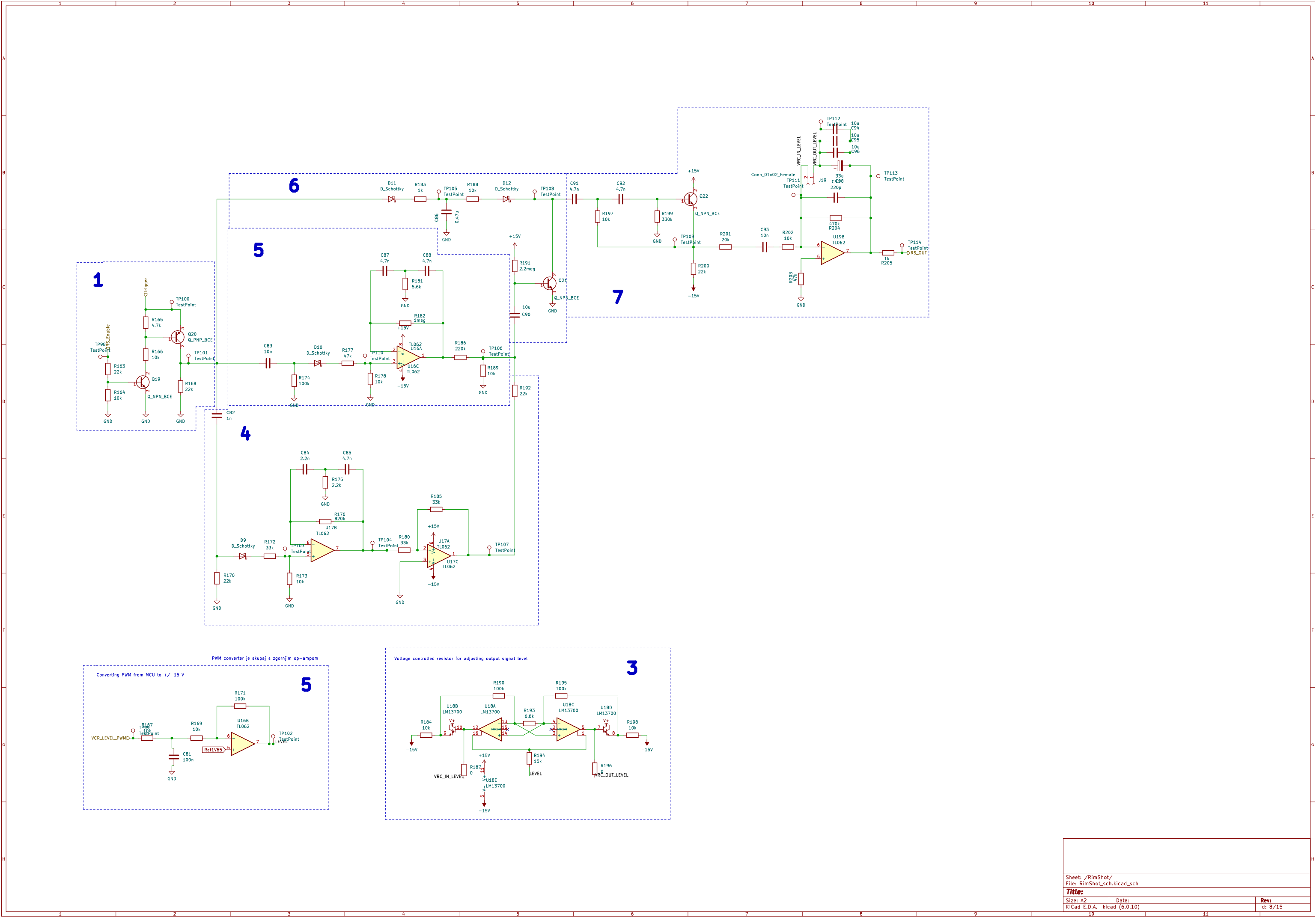
Id: 2/15

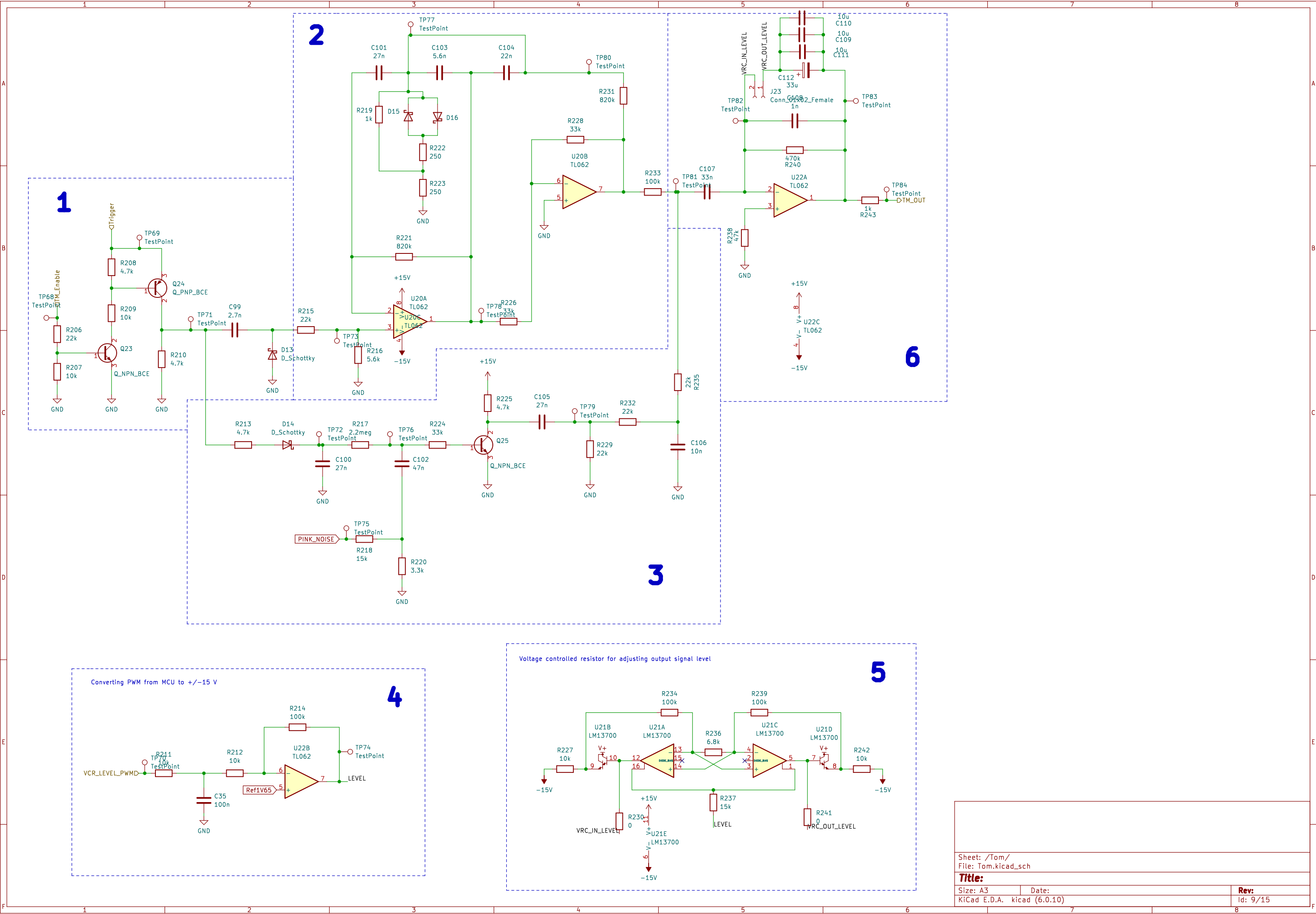


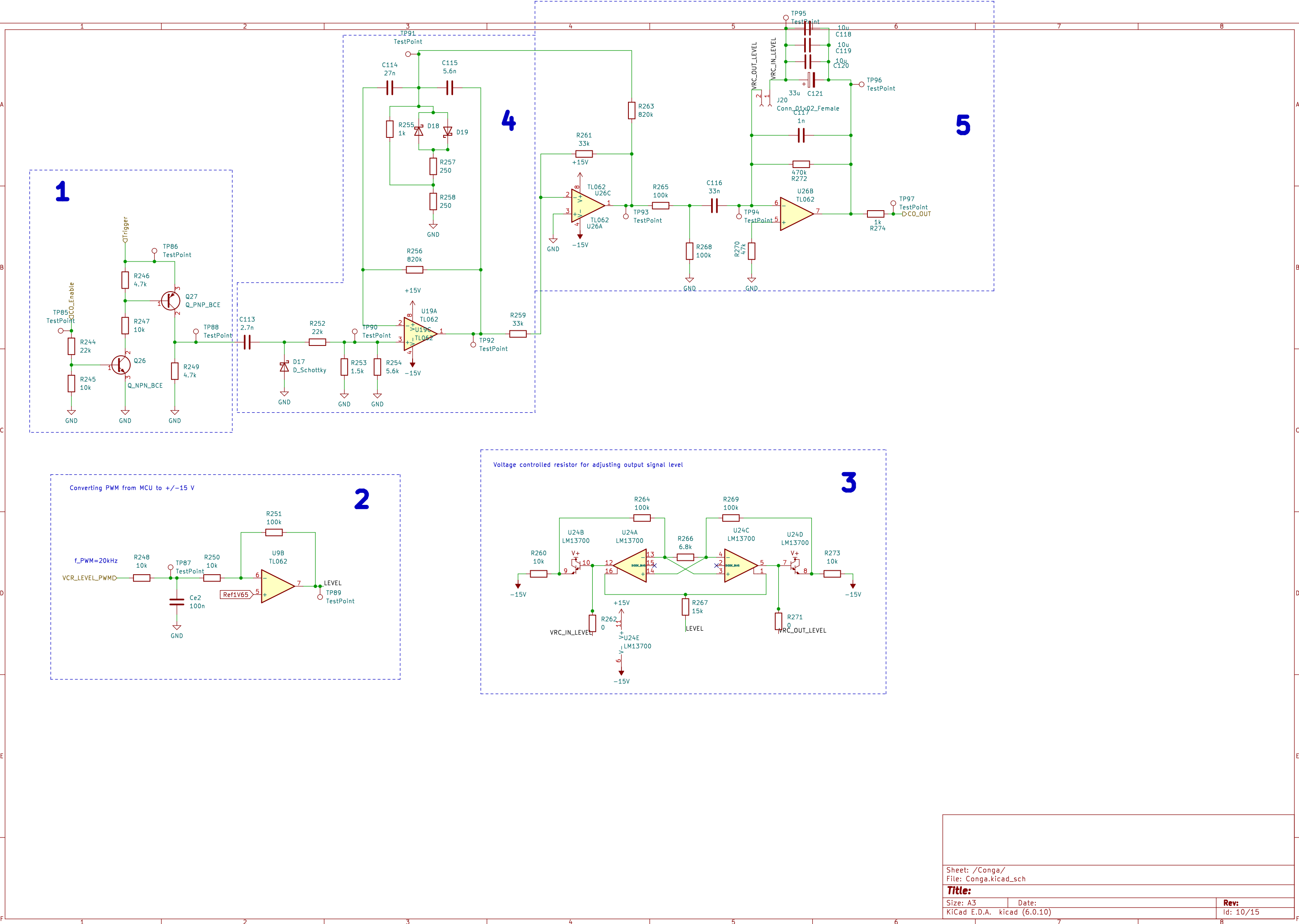


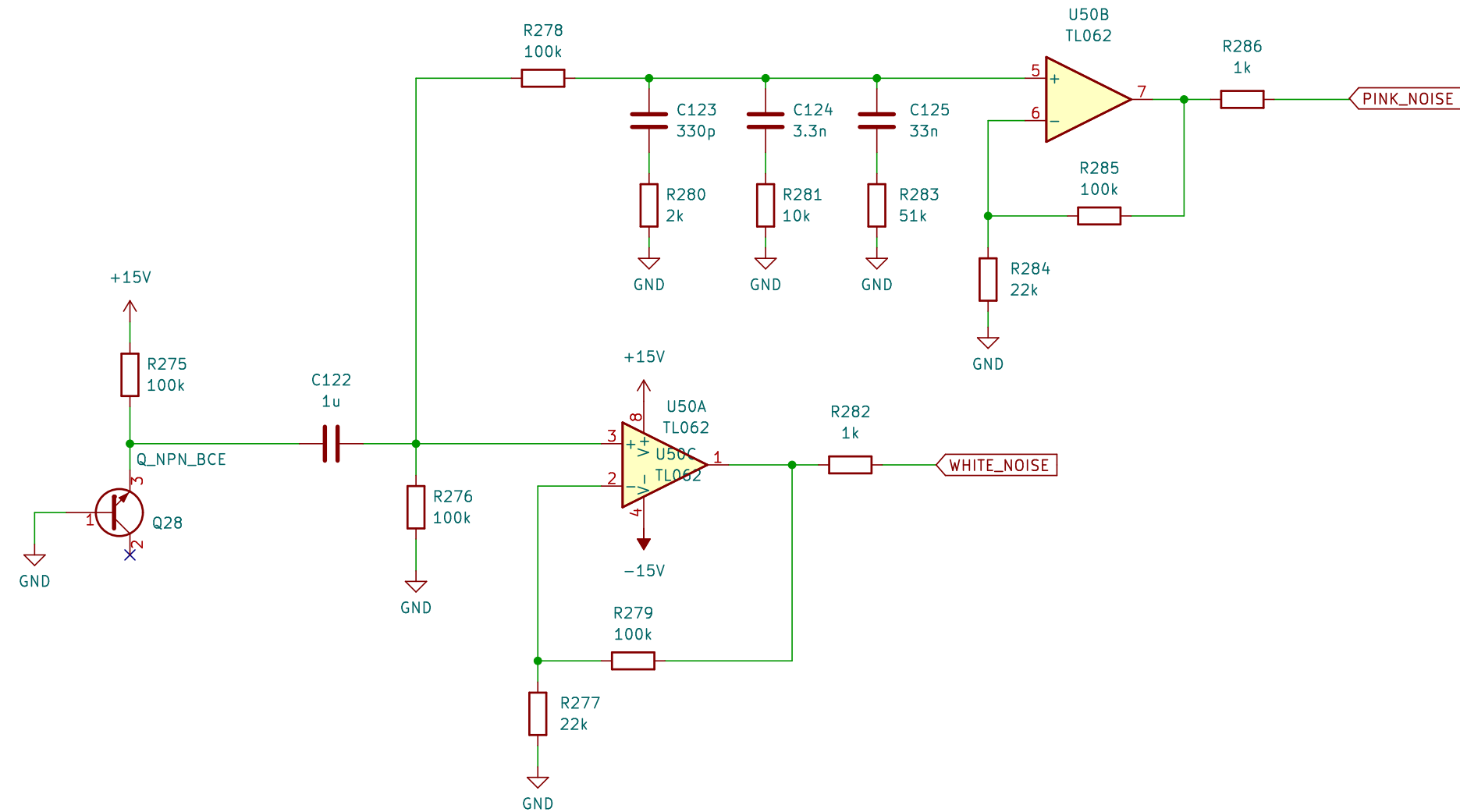












Sheet: /NoiseGenerator/
File: NoiseGenerator.kicad_sch

Title:

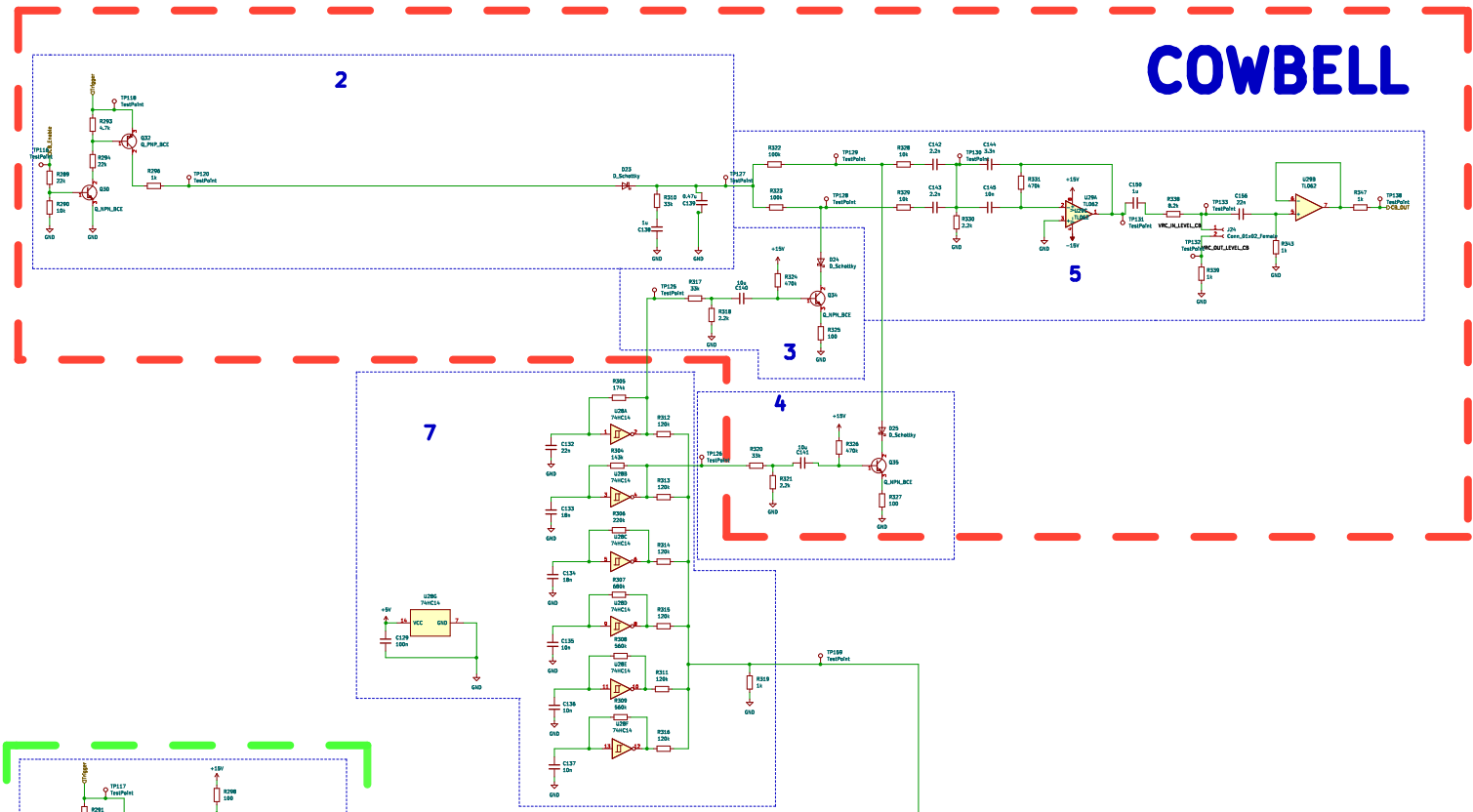
Size: A4
KiCad E.D.A. kicad (6.0.10)

Date:

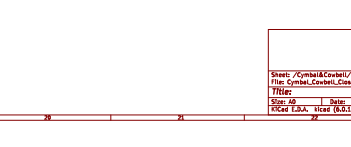
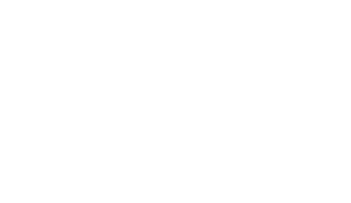
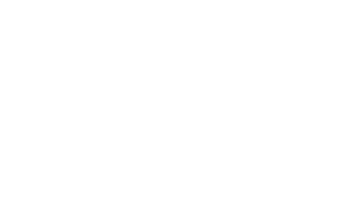
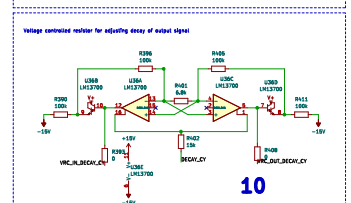
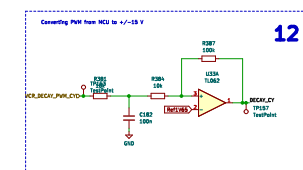
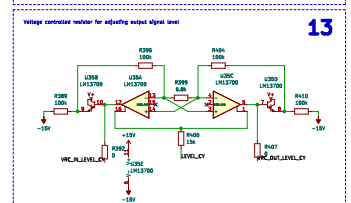
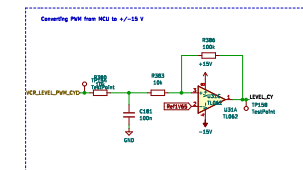
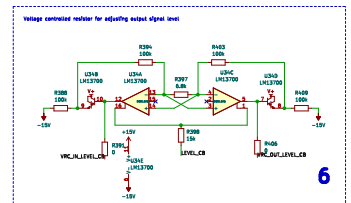
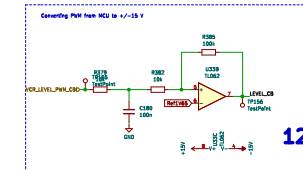
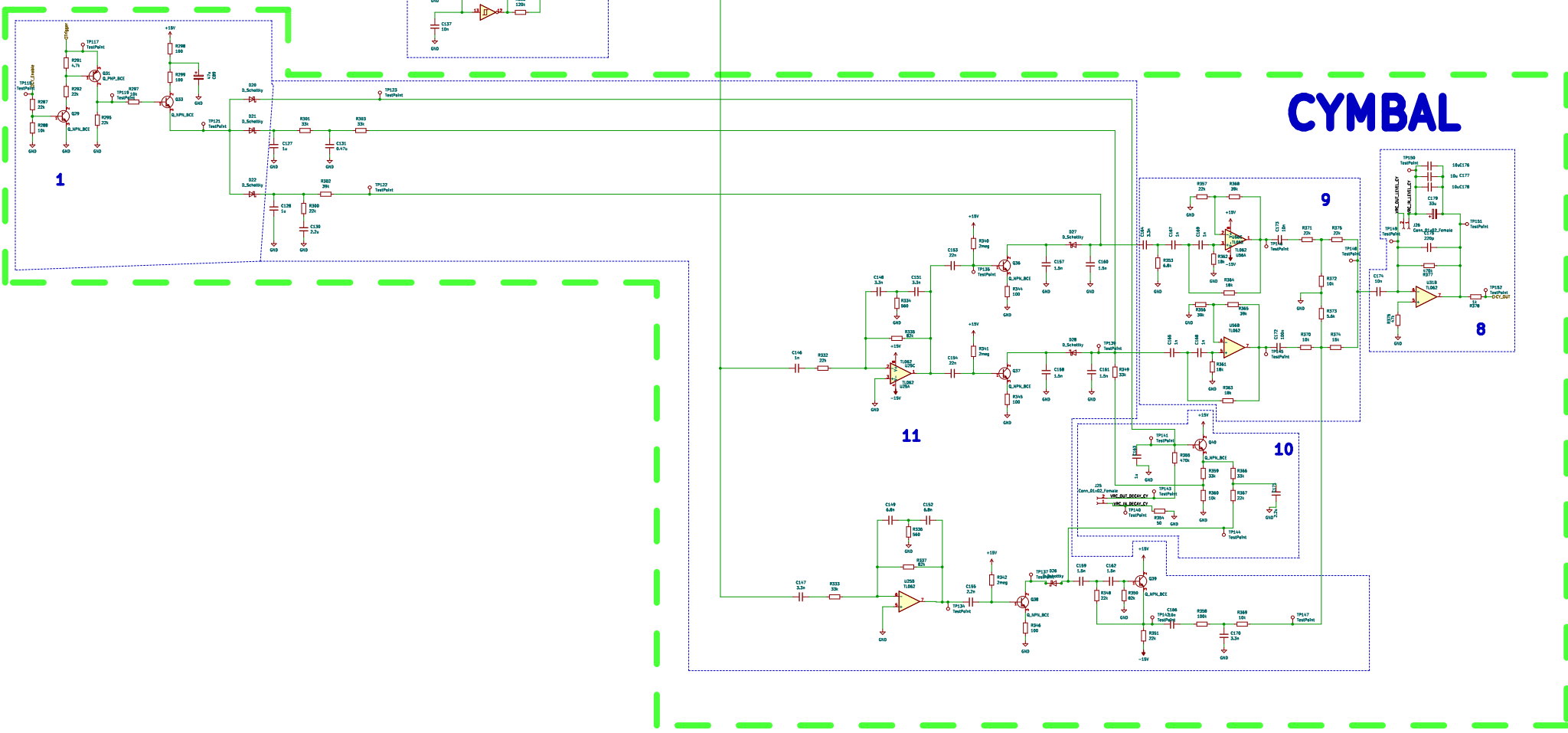
Rev:

Id: 11/15

COWBELL



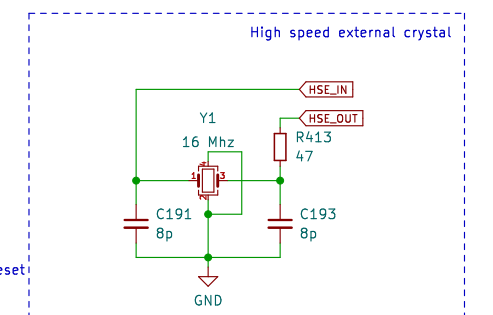
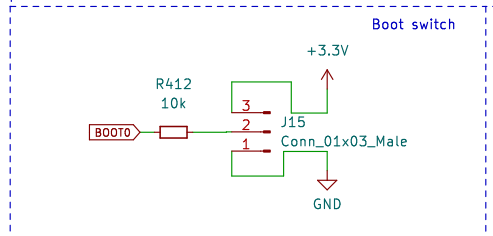
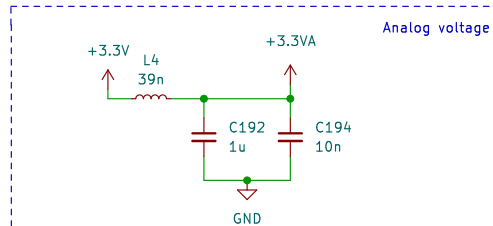
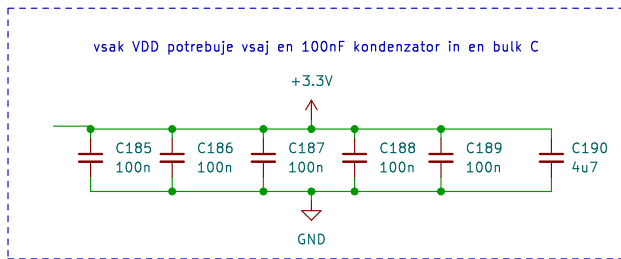
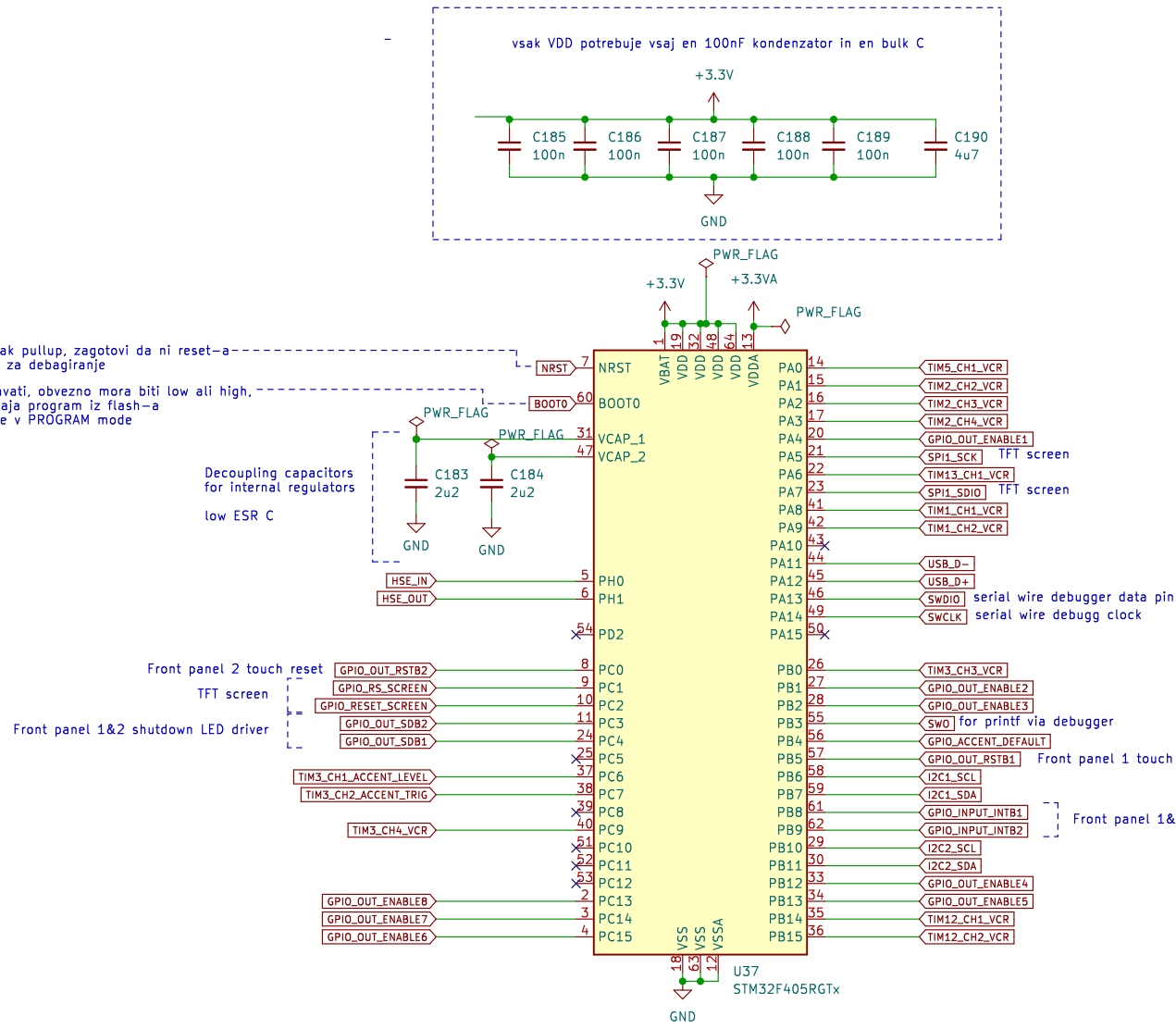
CYMBAL



SYS_JTCK-SWCLK
PA14
VDD
VCA...
PA13 SYS_JTMS-SWDIO
PA12 USB_OTG_FS_DP
PA11 USB_OTG_FS_DM
PA10 GPIO_Output
PA9 TIM1_CH2
PA8 TIM1_CH1
PC9 TIM3_CH4
PC8 TIM8_CH3
PC7 TIM3_CH2
PC6 TIM3_CH1
PB15 TIM12_CH2
PB14 TIM12_CH1
PB13 GPIO_Output
PB12 GPIO_Output
VDD

Hard reset
NRST -> low
interno ima NRST weak pullup, zagotovi da ni reset-a
NRST bomo uporabili za debugiranje

BOOT pin ne sme plavati, obvezno mora biti low ali high,
LOW -> Run state, izvaja program iz flash-a
HIGH 3.3V -> chip je v PROGRAM mode



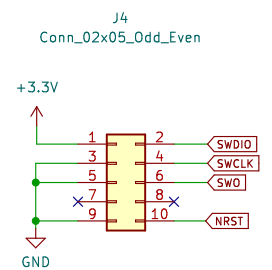
$C_{load} = 2 * (C_L - C_{stray})$
CL...load capacitance of the crystal..12pF
Cstray...cca. 6pF

Feed resistor ni nujno potreben,
omejuje driver znotraj MCUja, ki
driva kristal. Če je drive level
prevelik, se na kristalu pojavijo
višji harmoniki

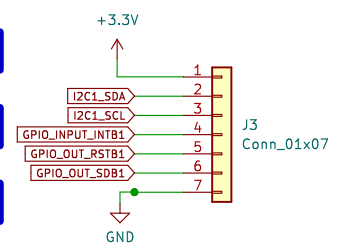
AN2867 application note

Connectors

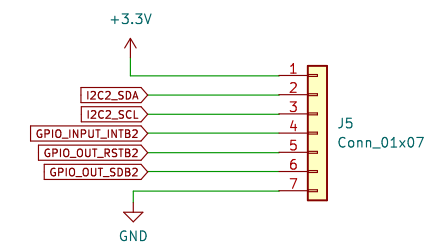
Debug



Front Panel 1

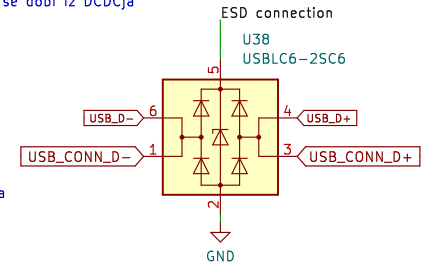
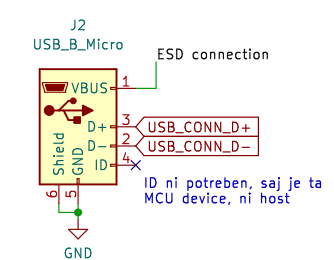


Front Panel 2



USB

+5V je uporabljen samo na tem mestu,
ta globalni simbol je uporabljen samo tu
zakaj je potreben za 5V net?? napajenje se dobi iz DCDCja



MCU ima interno pull-up upore za USB

