Digitalna vezja, 2016-2017

Seminar 2: **Procesor MIPS**

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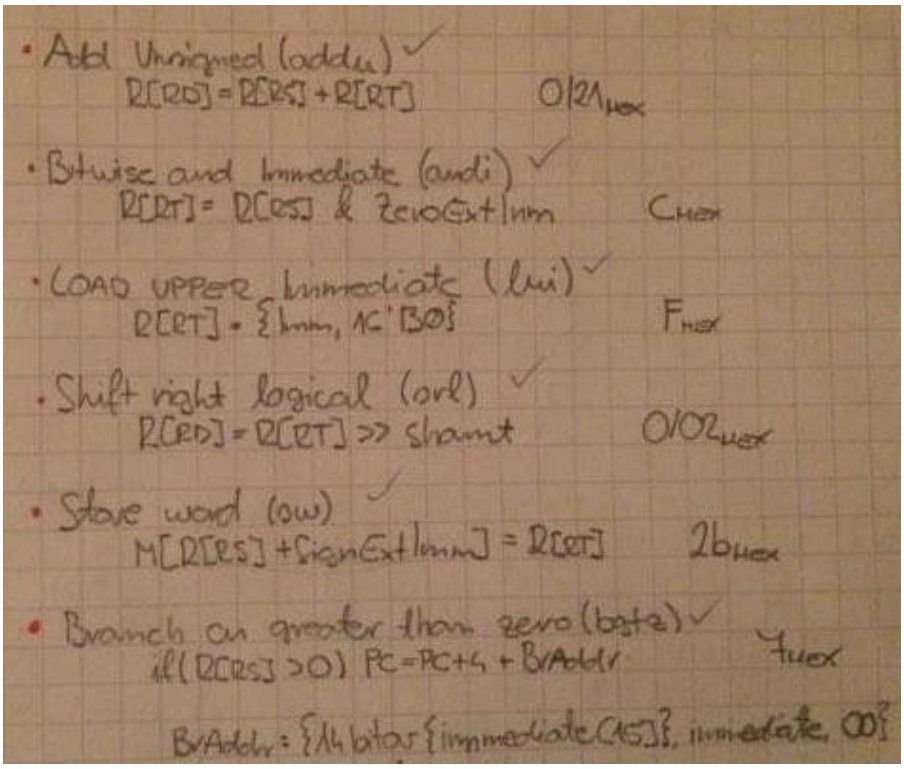
Poročilo

1. Uvod

V sklopu seminarja sva s kolegom implementirala procesor MIPS z šestimi ukazi;

- Add unsigned (addu)
- Bitwise and immediate (andi)
- Load upper immediate (lui)
- Shift Right Logical (srl)
- Store word (sw)
- Branch on greater than zero (bgtz)

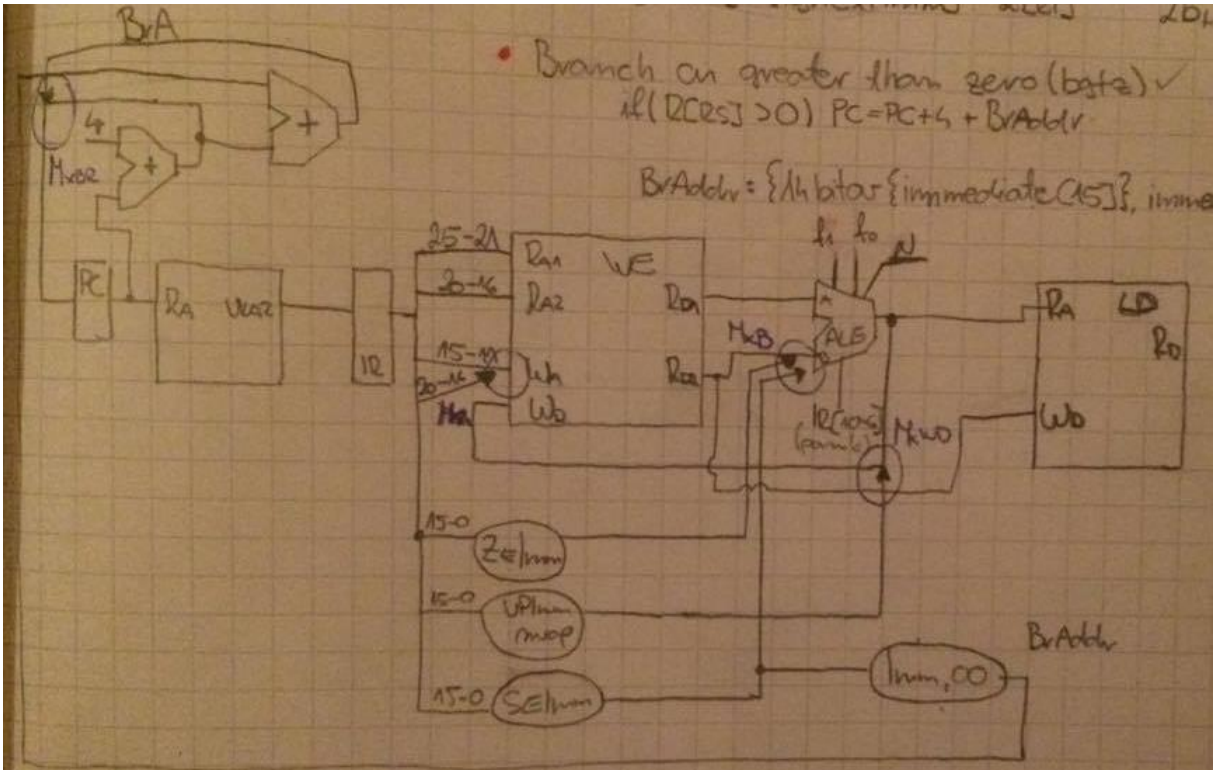


Slika 1 Nabor ukazov

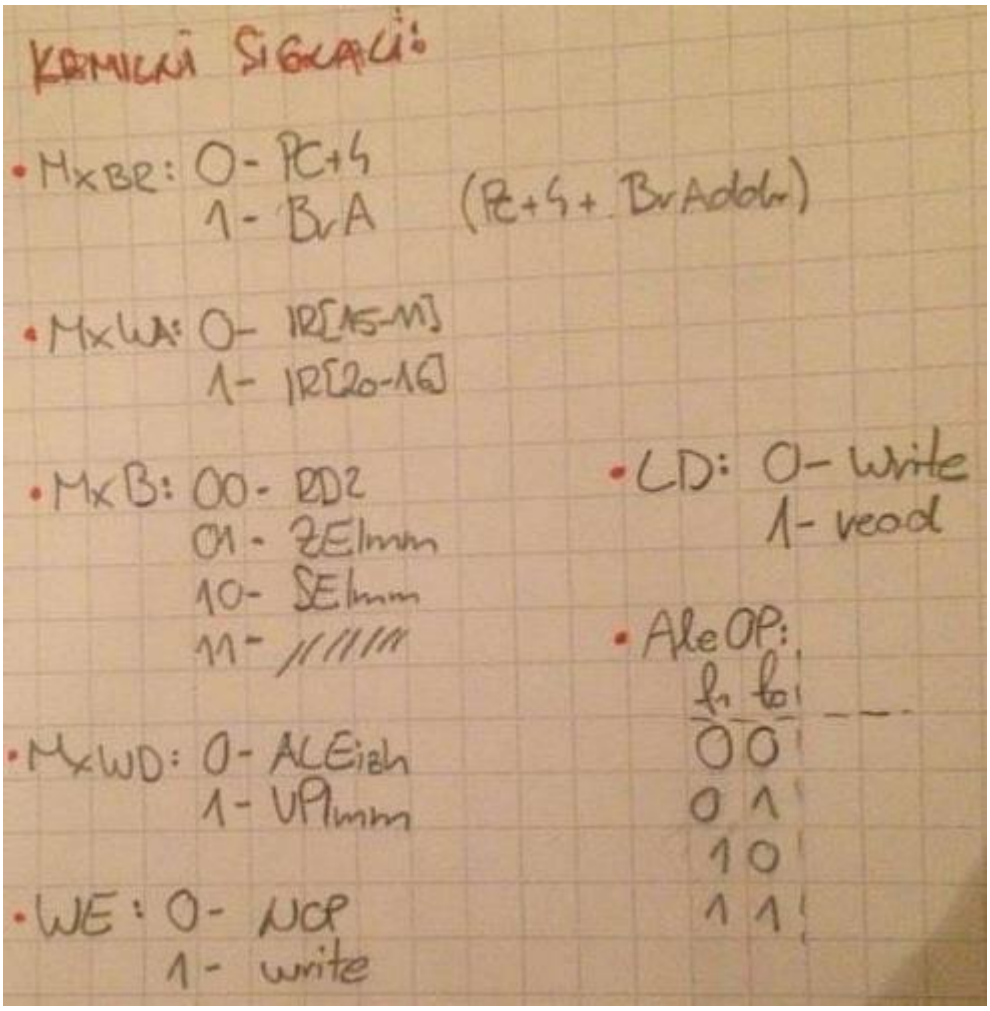
2. Načrtovanje in implementacija

UKAZ	OPERACIJSKA KODA & OPERACIJA UKAZA
ADDU	10|0001
ANDI	00|1100
LUI	00|1111
SRL	00|0010
SW	10|1011
BGTZ	00|0111

Table 1 Operacijska koda & operacija ukaza



Slika 2 Blok shema z gradniki in povezavami



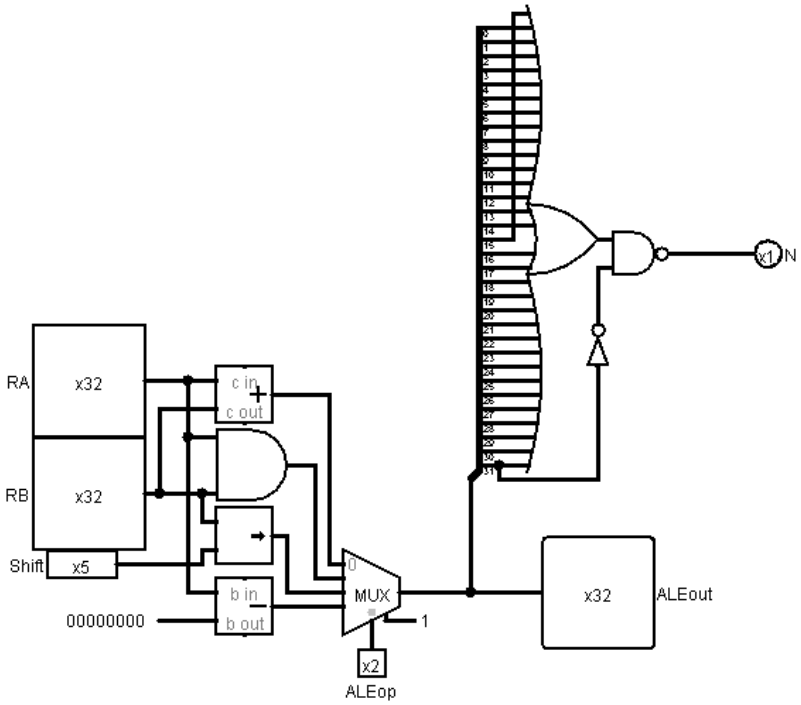
Slika 3 Krmilni signali

UKAZ	MXWA	MXB	MXWD	WE	LD	ALEOP	BR
ADDU	0	00	0	1	1	00	0
ANDI	1	00	0	1	1	00	0
LUI	1	00	1	1	1	00	0
SRL	0	00	0	1	1	10	0
SW	1	10	0	0	1	00	0
BGTZ	0	00	0	0	0	11	1

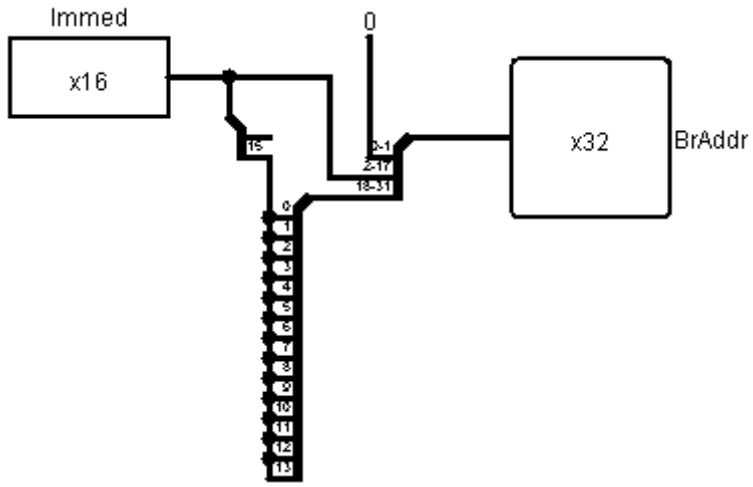
Tabela 2 Tabela krmilnih signalov

UKAZ	HEX
ADDU	18
ANDI	118
LUI	138
SRL	1C
SW	188
BGTZ	7

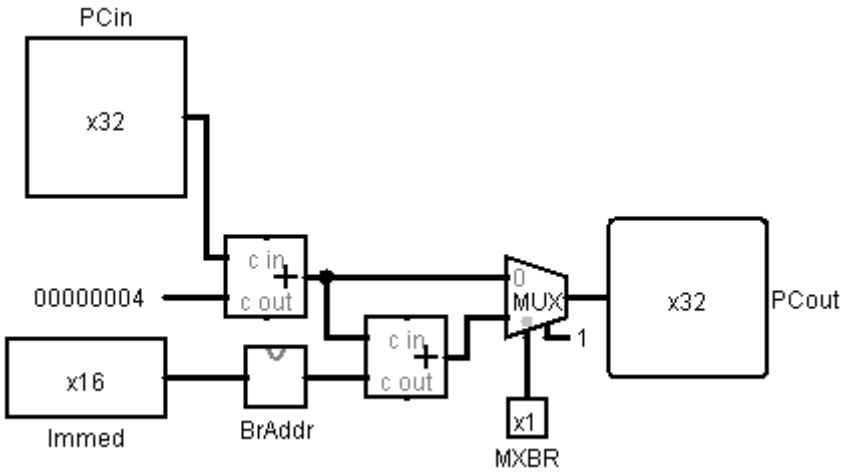
Tabela 3 Tabela krmilnih signalov v HEX



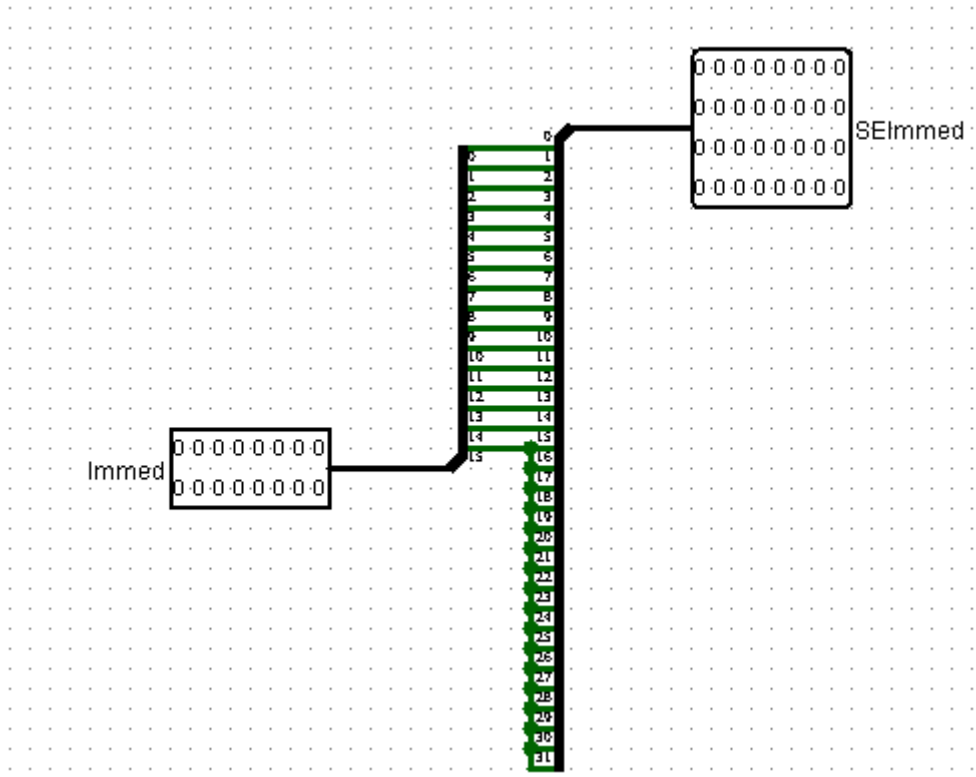
Slika 4 ALE



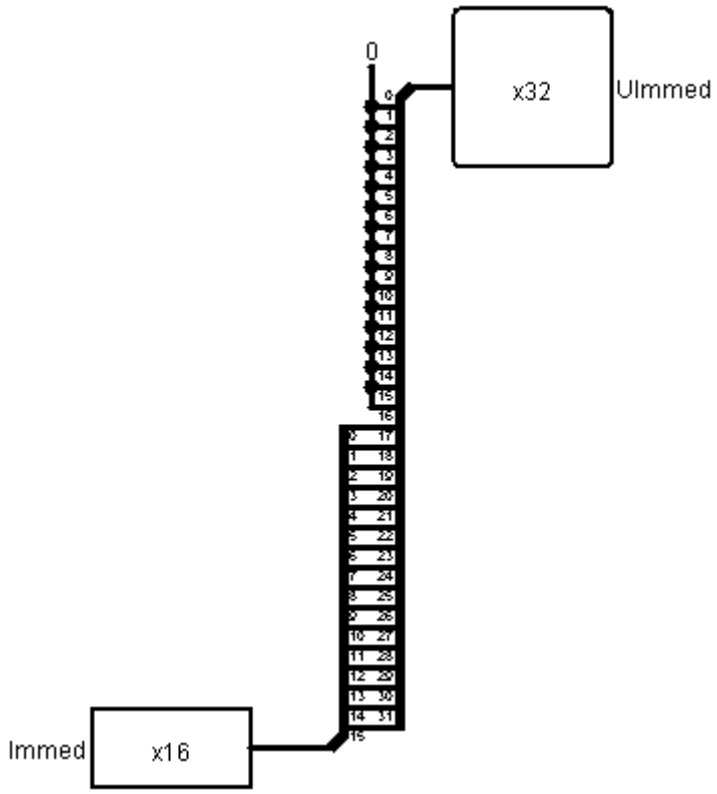
Slika 5 Branch Address



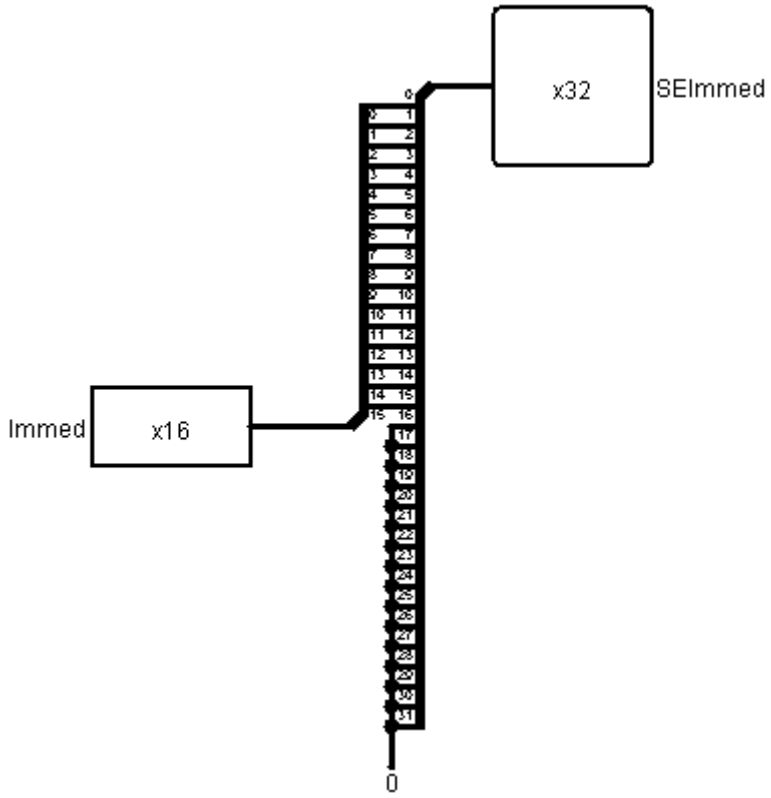
Slika 6 Program counter



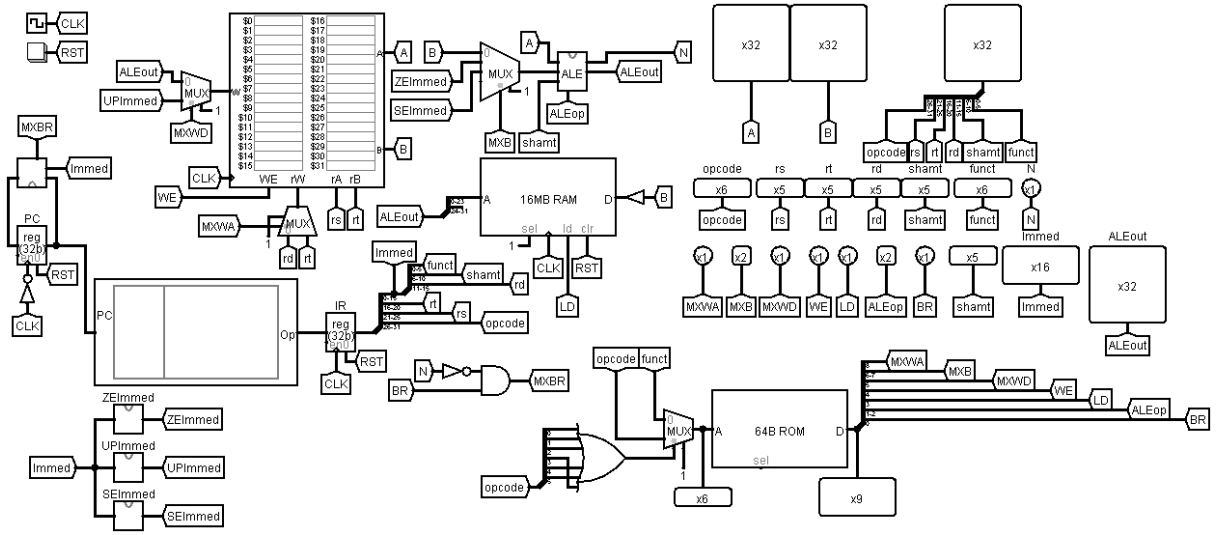
Slika 7 Signed Extended



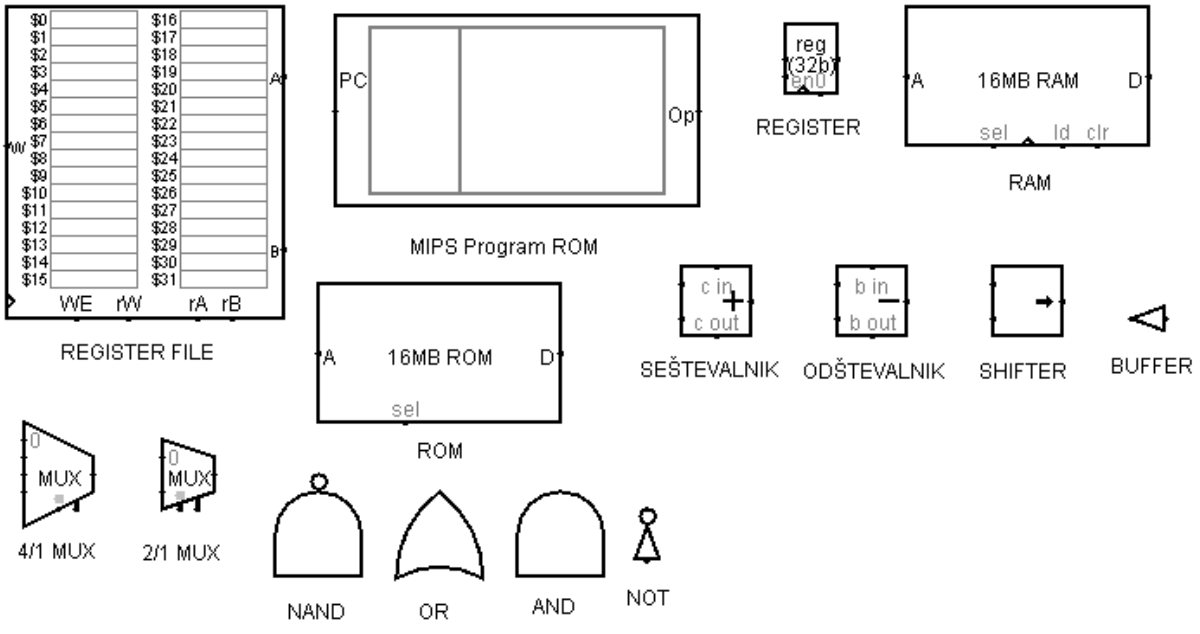
Slika 8 Upper Immediate



Slika 9 Zero Extended



Slika 10 Celotno vezje MIPS



Slika 11 Elementi

3. Testiranje

Rezultati v registrih, pomnilniku

REGISTRI	VREDNOST (HEX)
R1	8
R2	2
R3	3
R4	a
R5	2

Table 4 Rezultati v registrih

Literatura:

Patterson A. D., Hennessy L. J., Computer Organization and Design, Third Edition, Elsevier inc., 2005

Spletna učilnica FRI, DV VSŠ