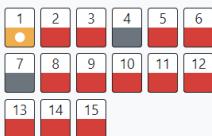
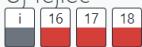


Computer Architectures 2020/21/2

Quiz navigation



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Started on Tuesday, 18 May 2021, 6:38 PM

State Finished

Completed on Tuesday, 18 May 2021, 6:43 PM

Time taken 4 mins 54 secs

Grade Not yet graded

Question 1

Partially correct

Mark 1.25 out of 2.00

[Flag question](#)

Which of the following statements are true for the simple single-level page tables?

- TRUE ✓ The entire page table has to be present in the memory all the time
- TRUE ✓ The address translation is always faster than with a 3-level hierarchical page table
- TRUE ✓ The number of entries is proportional to the size of the virtual memory
- TRUE ✗ Parts of it can be swapped to the hard disk drive

Question 2

Not answered

Marked out of 2.00

[Flag question](#)



Which task is done by the compiler/programmer and which by the hardware in the EPIC architecture?

	Compiler/programmer	Hardware (processor)
Detecting data hazards and inserting pipeline stalls		✗ [X]
Assigning instructions to functional units		✗ [X]
Collecting independent instructions into groups	✗ [X]	

Question 3

Not answered

Marked out of 2.00

[Flag question](#)

How many of the following components does a 3-way in-order superscalar CPU have?

Number of ALUs: ✗ [3]

Number of program counters: ✗ [1]

Number of separate data caches: ✗ [1]

Question 4

Complete

Marked out of 2.00

[Flag question](#)

How did we resolve the structural hazard regarding the memory resource, in the 5-stage pipeline we have studied? (Thus, how did we avoid using the memory in the IF and in the MEM phases at the same time?)

Anything

Question 5

Not answered

Marked out of 2.00

[Flag question](#)

The data and the instructions are stored in separate memory in the...

- ✗ Neumann architecture
- ✗ Harvard architecture
- ✗ In the modified Harvard architecture
- ✗ In all control-flow based computer architectures

Question 6

Not answered

Marked out of 2.00

[Flag question](#)

Why is it beneficial to keep the last row open for the memory controller of a DRAM based memory system?

- ✗ Because it can serve the next request faster, when it refers to an other row
- ✗ Because it can serve the next request faster, when it refers to the same row
- ✗ It increases the data transmission speed between the memory and the controller
- ✗ It increases the lifespan of the memory modules

Question 7

Complete

Marked out of 2.00

[Flag question](#)

List the components of the service times of HDD read requests! Which of them can be overlapped in time?

Anything

Question 8
Not answered
Marked out of 2.00
[Flag question](#)

In our 5-stage pipeline, which of the following phases do useful (effective) work on a *Load*, and on an *Add* (integer summation) instruction?

	Load	Add
IF	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> [X]
ID	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> [X]
EX	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> [X]
WB	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> [X]

Question 9
Not answered
Marked out of 2.00
[Flag question](#)

To which component of a computer can a PCI peripheral initiate data transfer?

- The CPU
- The system memory
- An other PCI peripheral
- A PCI Express peripheral

Question 10
Not answered
Marked out of 2.00
[Flag question](#)

Which statements are true for the PIC (programmable interrupt controller) based interrupt handling?

- Round-robin serving of interrupts is possible
- The priority of the devices can not be changed
- It does not work when more than one devices generate interrupt at the same time
- It can be expanded arbitrarily (in theory)

Question 11
Not answered
Marked out of 2.00
[Flag question](#)

How many transistors are needed to store 18 bits in an SLC, in a MLC, and in a TLC flash based SSD drive?

- In case of SLC: [18]
- In case of MLC: [9]
- In case of TLC: [6]

Your answer is incorrect.

Question 12
Not answered
Marked out of 2.00
[Flag question](#)

Which of the following statements are true for the direct-mapped cache organization?

- The cache always stores the most recently used blocks of the system memory
- By fixed cache size, this organization leads to the widest cache tags
- The cache tags are shorter than in case of the fully associative organization
- It is not possible to store more than 1 block having the same index

Question 13
Not answered
Marked out of 2.00
[Flag question](#)

Which of the following features are characteristic for RISC instruction set architectures?

- (Nearly) non-redundancy
- No support for register - memory arithmetic operations
- A large number of instructions in the instruction set architecture
- Variable length instruction encoding

Question 14
Not answered
Marked out of 2.00
[Flag question](#)

Which speeds are NOT supported by the following versions of the USB standard?

	USB 2.0	USB 1.1	USB 3.0
Super speed	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> [X]	<input checked="" type="checkbox"/> [X]
Full speed	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
High speed	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> [X]

Question 15
Not answered
Marked out of 0

2.00

 Flag question

When can an operation be executed in the three information processing model we have studied?

	Control-driven model	Data-flow model	Demand-driven model
When its result is needed	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/> X [PJ]
When the control token reaches it	<input checked="" type="checkbox"/> X [PJ]	<input type="checkbox"/>	<input type="checkbox"/>
When all of its operands are available	<input type="checkbox"/>	<input checked="" type="checkbox"/> X [PJ]	<input type="checkbox"/>

Your answer is incorrect.

Information

 Flag question

Consider the following sequence of instructions:

```
i1: R2 ← R0 * R1
i2: R3 ← MEM[R2 + 4]
i3: R8 ← MEM[R2 + 8]
i4: R5 ← R3 + R8
i5: R6 ← R0 + 12
i6: R9 ← R3 * R6
i7: R10 ← R6 - R1
```

Assume we need to compile the program above on a VLIW processor where the following type of instructions can be placed in an instruction group:

- 2 memory load/store operations (latency: 3 cycles, iteration interval: 1 cycle)
- 2 integer arithmetic instructions (latency: 1 cycle)

Question 16

Not answered

Marked out of 3.00

 Flag question

(a) Mark the data dependent instruction pairs by putting "X" characters to the table!

RAW dependencies:

	i1	i2	i3	i4	i5	i6
i1						
i2	<input checked="" type="checkbox"/> X					
i3	<input checked="" type="checkbox"/> X	<input type="checkbox"/>				
i4		<input checked="" type="checkbox"/> X	<input checked="" type="checkbox"/> X			
i5				<input type="checkbox"/>		
i6		<input checked="" type="checkbox"/> X	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/> X	
i7					<input checked="" type="checkbox"/> X	

WAR dependencies:

i1	i2	i3	i4	i5	i6
<input type="checkbox"/>					
	<input type="checkbox"/>				
		<input type="checkbox"/>			
			<input type="checkbox"/>		
				<input type="checkbox"/>	
					<input type="checkbox"/>

WAW dependencies:

i1	i2	i3	i4	i5	i6
<input type="checkbox"/>					
	<input type="checkbox"/>				
		<input type="checkbox"/>			
			<input type="checkbox"/>		
				<input type="checkbox"/>	
					<input type="checkbox"/>

Your answer is incorrect.

Question 17

Not answered

Marked out of 3.00

 Flag question

(b) Schedule the instructions for the given VLIW processor. Determine the content of the instruction groups and the time when the instruction groups can be executed. The number of instruction groups needed has to be minimal. When an instruction can be placed into multiple locations, always choose the earlier instruction to the functional unit having a lower id. (3p)

Instruction group:	MEM 1:	MEM 2:	INT 1:	INT 2:
1:	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/> X [i1 or 1]	<input checked="" type="checkbox"/> X [i5 or 5]
2:	<input checked="" type="checkbox"/> X [i2 or 2]	<input checked="" type="checkbox"/> X [i3 or 3]	<input checked="" type="checkbox"/> X [i7 or 7]	<input type="checkbox"/>
3:	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4:	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
5:	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/> X [i4 or 4]	<input checked="" type="checkbox"/> X [i6 or 6]
6:	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

(All the instruction groups might not be needed)

Your answer is incorrect.

Question 18

Not answered

Marked out of 2.00

 Flag question

(c) How many instruction groups will be created by the compiler in case of a "classical" and in case of a "dynamic" VLIW architecture?

Classical VLIW: X [5] instruction groups

Dynamic VLIW: X [3] instruction groups

Your answer is incorrect.

Question 19

Not answered
Marked out of 6.00
Flag question

Assume that a CPU has a fully associative cache memory of size 256 bytes ($=2^8$). The block size is 64 bytes ($=2^6$). The CPU uses 28 bit wide addresses.

- (a) The length of the cache tags is: X [22] bits
- (b) The number of comparisons done simultaneously during a cache lookup: X [4]
- (c) The number of bits to compare by the comparators at each cache lookup: X [22] bits
- (d) The program, while being executed, reads the following blocks of the system memory:
- 42, 315, 9

How does the content of the cache memory change, when the program reads the given blocks in the initial state provided below? Use LRU replacement policy, and record the relative age of the blocks (between 1 and 4) in the gray fields! (The greater the age is, the older the content is.) When there are several possibilities for block placement, choose the left-most place! It is enough to fill in those fields that have changed.



Your answer is incorrect.

Information
Flag question

A computer has a single-channel DDR3-DRAM based system memory with 64 bit data units. The burst size is set to 8 data units. Let us ignore the presence of multiple banks and ranks.

The memory controller receives the following read requests, given by row and column coordinates

- (row 2, column 32), (row 4, column 8), (row 2, column 4)

Question 20
Not answered
Marked out of 3.00
Flag question

[192] 2 16 SAVE OPEN LOAD 128 PRECHARGE 8 READ 64 ACTIVATE 32 4 CLOSE 32

List the commands sent by the memory controller to the memory modules (in the right order) according to FCFS and FR-FCFS command scheduling, assuming that there can be a single row open at a time.

The DRAM bank is in precharged state initially. After the last command the memory controller **has to close** the active row. (3 points)

FCFS scheduling:

Command	Parameter
1: [ACTIVATE]	<input type="text"/> X [2]
2: [READ]	<input type="text"/> X [32]
3: [PRECHARGE]	<input type="text"/>
4: [ACTIVATE]	<input type="text"/> X [4]
5: [READ]	<input type="text"/> X [8]
6: [PRECHARGE]	<input type="text"/>
7: [ACTIVATE]	<input type="text"/> X [2]
8: [READ]	<input type="text"/> X [4]
9: [PRECHARGE]	<input type="text"/>

FR-FCFS scheduling:

Command	Parameter
1: [ACTIVATE]	<input type="text"/> X [2]
2: [READ]	<input type="text"/> X [32]
3: [READ]	<input type="text"/> X [4]
4: [PRECHARGE]	<input type="text"/>
5: [ACTIVATE]	<input type="text"/> X [4]
6: [READ]	<input type="text"/> X [8]
7: [PRECHARGE]	<input type="text"/>
8: [ACTIVATE]	<input type="text"/>
9: [ACTIVATE]	<input type="text"/>

(You might not need all lines.)

Your answer is incorrect.

Question 21
Not answered
Marked out of 3.00

Assuming DDR3-2800 DRAM technology (with 64 bit wide data units and burst size of 8), answer the following questions with a single number for each!

a) The internal clock frequency of the memory is MHz X 12501 MHz

Flag question

a) The internal clock frequency of the memory is (in MHz): [500] MHz

b) The number of internal clock cycles needed to transmit one full burst: [1] cycles

c) The data transfer speed during the transmission of the burst (in MB/s): [22400 or 22 400 or 22.400] MB/s

Your answer is incorrect.

Question 22

Not answered
Marked out of 6.00

Flag question

Let the virtual addresses be 20 bit wide, and the physical addresses 15 bit wide. The page size is $2^{11} = 2\text{kB}$. The CPU uses a 3-level hierarchical page table with 16 bit wide entries.

- The number of pages in the virtual memory: [512]
- The number of frames in the physical memory: [16]
- If there is no page fault, how many times does the CPU need to access the system memory in order to perform address translation? Count only the memory accesses corresponding to the address translation itself, do not include the memory operation that triggered the address translation!
 - in case of TLB hit?: [0]
 - in case of TLB miss?: [3]
- What is the total size of the page table? (in bytes): [1168]
- What is the minimal size of the page table? (in bytes): [48]
- What would be the size of the page table if we used a single level page table instead of the three level one? (in bytes): [1024]
- What is the TLB coverage if the TLB consists of 4 entries (in bytes): [8192] bytes

Your answer is incorrect.

Question 23

Not answered
Marked out of 1.00

Flag question

Reorder the instructions to improve the execution time (while keeping the semantics of the program)! (1 point)

The new (reordered) sequence of instructions: - - - -

Your answer is incorrect.

The correct answer is:

Reorder the instructions to improve the execution time (while keeping the semantics of the program)! (1 point)

The new (reordered) sequence of instructions: - - - -

Question 24

Not answered
Marked out of 3.00

Flag question

Consider the following sequence of instructions:

i1: R1 \leftarrow R1 + R4
i2: R2 \leftarrow MEM[R0+4]
i3: R1 \leftarrow R1 + R2
i4: R3 \leftarrow R1 * R2
i5: MEM[R0+0] \leftarrow R3

These instructions are executed on a CPU which uses a 6-stage pipeline. The execution of the instructions consists of 5 phases: fetch (IF), decode (ID), execute arithmetic-logic operations (EX), perform memory operations (MEM), and writing back the result into the register file (WB). The latency of the ID, EX, MEM, WB phases is 1 clock cycle, while the latency of the IF phase is 2 clock cycles, the iteration interval is still 1. This means that the instruction fetch phase consists of two stages: IF0 and IF1.

Schedule the instructions in the pipeline (determine which instruction is in which stage in every time step). If a pipeline stall needs to be inserted, provide the reason by the following notation:

- D*: the reason of the stall is data hazard
- S*: the reason of the stall is structural hazard
- C*: the reason of the stall is control hazard

Write the solution to the following table! If a forwarding was needed during the execution of the instruction, write the pipeline register, from which the operand is taken, to the last column! In case of multiple forwarding was needed for a single instruction, list the affected pipeline registers separated by comma, without spaces! (3p)

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	Forwarding
i1 <input type="text"/> [IF0]	<input type="text"/> [IF1]	<input type="text"/> [ID]	<input type="text"/> [EX]	<input type="text"/> [MEM]	<input type="text"/> [WB]	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	
i2 <input type="text"/>	<input type="text"/> [IF0]	<input type="text"/> [IF1]	<input type="text"/> [ID]	<input type="text"/> [EX]	<input type="text"/> [MEM]	<input type="text"/> [WB]	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	
i3 <input type="text"/>	<input type="text"/>	<input type="text"/> [IF0]	<input type="text"/> [IF1]	<input type="text"/> [ID]	<input type="text"/> [EX]	<input type="text"/> [MEM]	<input type="text"/> [WB]	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	(MEM/WB)
i4 <input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/> [IF0]	<input type="text"/> [IF1]	<input type="text"/> [S*]	<input type="text"/> [ID]	<input type="text"/> [EX]	<input type="text"/> [MEM]	<input type="text"/> [WB]	<input type="text"/>	<input type="text"/>	(EX/MEM)
i5 <input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/> [IF0]	<input type="text"/> [S*]	<input type="text"/> [IF1]	<input type="text"/> [ID]	<input type="text"/> [EX]	<input type="text"/> [MEM]	<input type="text"/> [WB]	<input type="text"/>	(EX/MEM or MEM/WB)

Your answer is incorrect.

Finish review