

- (row 4, column 24), (row 1, column 0), (row 4, column 8)

**Question 12**

Not answered

Marked out of  
3.00

Flag  
question

64 16 4 8 0 32 24 PRECHARGE SAVE ACTIVATE OPEN 192 LOAD CLOSE 1 READ 128

List the commands sent by the memory controller to the memory modules (in the right order) according to FCFS and FR-FCFS command scheduling, assuming that there can be a single row open at a time.

Row 1 is assumed to be in activated state initially. After the last command the memory controller does not close the active row. (3 points)

FCFS scheduling:

	Command	Parameter
1:	[PRECHARGE]	
2:	[ACTIVATE]	[4]
3:	[READ]	[24]
4:	[PRECHARGE]	
5:	[ACTIVATE]	[1]
6:	[READ]	[0]
7:	[PRECHARGE]	
8:	[ACTIVATE]	[4]
9:	[READ]	[8]

FR-FCFS scheduling:

	Command	Parameter
1:	[READ]	[0]
2:	[PRECHARGE]	
3:	[ACTIVATE]	[4]
4:	[READ]	[24]
5:	[READ]	[8]
6:		
7:		
8:		
9:		

(You might not need all lines.)

**Question 8**

Incorrect

Mark 0.00 out  
of 2.00 Flag  
question

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order: [HS] - [SS+] - [SS] - [FS] - [LS]

The correct answer is:

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order: [LS] - [FS] - [HS] - [SS] - [SS+]

**Question 9**

Incorrect

Mark 0.00 out  
of 2.00 Flag  
question

Compare the following data storage technologies!

	SRAM	SLC NAND flash
Preserves its content without power supply	[blank]	[X]
Its content needs to be refreshed periodically	[blank]	
Supports byte-level addressing	✓	
6 capacitors are needed to store 1 bit	[blank]	

**Question 10**

Not answered

Marked out of  
4.00 Flag  
question

Let us consider a special computer with a heat sensitive peripheral and a temperature sensor. The CPU can read the temperature sensor any time (a readout needs 800 clock cycles from the CPU), and it does not support interrupts. The peripheral overheats twice in a minute in average. In case of overheating the CPU switches off the peripheral and switches it on again a bit later. The switch on and off times are short enough to consider them negligible.

a) How many times does the CPU have to poll the temperature sensor in each second, if the peripheral tolerates overheating only for 0.4 ms time? (1 point)

Answer: [2500 or 2.500] poll/sec

b) With the polling time calculated in part a) what is the average delay to get the CPU informed on the overheating? (expressed in ms) (1 point)

Answer: [0.2 or 0,2] ms

of 4 pages. For each page the state of the page ("U"=used, "I"=invalid, "E"=erased) and the LBA address of the stored data are provided.

In the initial state blocks 1, 2 and 5 are erased, and the write frontier is block 6.

block 0	4	block 1	7	block 2	8
I	6	E		E	
U	10	E		E	
U	8	E		E	
U	7	E		E	
block 3	2	block 4	9	block 5	16
I	7	I	12	E	
U	1	U	9	E	
U	3	U	19	E	
I	8	I	7	E	
block 6	5	block 7	3		
U	6	I	19		
U	14	U	12		
U	17	I	15		
E		U	15		

- a) How does the state of the SSD change when read requests arrive to LBA addresses **4**, **8** and **6**, accordingly. If a new write frontier is needed, select one that ensures the most balanced wearing of the blocks. When the number of erased blocks **after** a write operation decreases below 3, execute the garbage collection algorithm, potentially multiple times, till the number of erased block increases back to 3. The garbage collector always selects the block containing the most invalid pages. If

Which of the following arbitration procedures are centralized?

- Daisy chain-based arbitration
- TRUE  Parallel arbitration
- Distributed arbitration
- FALSE  Collision detection-based arbitration

Please answer all parts of the question.

Given the DRAM technologies provided by the table, in which clock cycle does the first data appear on the data (according to FCFS scheduling), measured in clock cycles (part a), and measured in nanoseconds (part b)? The init above. The timing parameters are given in format  $T_{CAS} - T_{RCD} - T_{RP}$ , where  $T_{RP}$  is the delay of the PRECHARGE command. The time till response is the sum of all three times. The time till response is measured in (external) clock cycles. (Write only a single number into the fields!) (3 points)

Technology	(a) Time till the response, in cycles	(b) Time till response, in ns
DDR2-800, 5-5-5	x [5]	x [12.5 or 12,5]
DDR3-1600, 7-8-8	x [7]	x [8.75 or 8,75]
DDR3-2000, 11-13-13	x [11]	x [11]

Your answer is incorrect.

**Question 5**Not yet  
answeredMarked out of  
2.00

Flag question

Which of the following exceptions can occur in the instruction fetch (IF) phase?

- FALSE ✘ Arithmetic error
- TRUE ✘ Page fault
- FALSE ✘ Invalid instruction
- TRUE ✘ Protection fault

**Question 6**Not yet  
answeredMarked out of  
2.00

Flag question

Which of the following tasks have to be done by the compiler/programmer in the (classical) VLIW architecture?

- TRUE ✘ Collecting and grouping independent instructions
- FALSE ✘ Detecting hazards and insert stalls
- TRUE ✘ Assigning instructions to the functional units
- FALSE ✘ Execution of the instructions

	DRAM	SRAM
This is the faster form the two		X
The storage cell consists of only transistors		X
6 transistors are needed to store 1 bit		X
The cache memory is based on this technology		X

X

Which components of the computer can act as an initiator and as a target in a PCI/PCI Express transaction?

	As initiator	As target
The CPU	X	
An other PCI/PCI Express peripheral	X	X
The memory	I	X



Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
This is the faster form the two		X
The storage cell consists of only transistors		X
6 transistors are needed to store 1 bit	X	
The cache memory is based on this technology		X

A hard disk drive contains 2 double-sided platters, with 50000 tracks on each recording surface and with 500 sectors in each track. The size of the sectors is 500 byte. There is no ZBR, and the speed of the data transmission interface is  $100 \cdot 10^6$  byte/s. The command processing time is neglected, because it is very low. The average seek time is 5 ms, and the revolution speed is 6000 RPM-

a) The storage capacity of the hard disk drive, measured in  $10^9$  bytes, is: 25   $10^9$  byte (1 point)

b) The full revolution time of the disk, given in ms, is: 10  ms (1 point)

c) How long does it take to read one sector from the recording surface, given that the head is at the appropriate position (it points to the beginning of the sector): 0,02  ms (1 point)

d) How long does it take to transmit one sector on the data transmission interface? (in ms) 0,0005  ms (1 point)

e) How much slower is the full service time of a request for 100 consecutive sectors than the full service time of a request for 1 sector? (2 points)

The answer is: 1,98  ms

f) We would like to slow down the rotation time from 6000 RPM to 4000 RPM. What should be the new seek time, which ensures that the average full service time of 1 sector remains the same with the slower rotation speed?

The answer is: 4,9  ms

Which phases of the instruction execution belong to the **backend** of the pipeline?

- ◆ The fetching of the instructions
- ◆ Putting the instructions to the instruction window
- ◆ Scheduling the instructions for execution to the appropriate functional unit
- ◆ The execution of the instructions

64	LOAD	OPEN	SAVE	PRECHARGE	4	16	0	CLOSE	32	128	8	ACTIVATE	1	192
24	READ													

List the commands sent by the memory controller to the memory modules (in the right order) according to FCFS and FR-FCFS command scheduling, assuming that there can be a single row open at a time.

Row 1 is assumed to be in activated state initially. After the last command the memory controller does not close the active row. (3 points)

**FCFS scheduling:**

	Command	Parameter
1:		
2:		
3:		
4:		
5:		
6:		

**FR-FCFS scheduling:**

	Command	Parameter
1:		
2:		
3:		
4:		
5:		
6:		

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order: LS - FS - HS - SS - SS+

HIT

- TRUE ✅ ✓ It does not support real interrupt handling, only polling

Question 3

Correct

Mark 2.00 out of  
2.00

Flag question

Which of the following statements are true for the data-driven information processing model?

- FALSE ✅ ✓ The Harvard architecture follows this principle
- TRUE ✅ ✓ It can exploit the parallelism of the program automatically
- FALSE ✅ ✓ It does not execute an instruction till its result is required by an other instruction
- TRUE ✅ ✓ The program is described by a precedence graph

Question 4

Correct

Mark 2.00 out of  
2.00

Flag question

Which of the following arbitration procedures are centralized?

- TRUE ✅ ✓ Daisy chain-based arbitration
- TRUE ✅ ✓ Parallel arbitration
- FALSE ✅ ✓ Distributed arbitration
- FALSE ✅ ✓ Collision detection-based arbitration

Question 5

Correct



block 0	4	✓	block 1	8	✗ [7 or blank]	block 3	4	✗ [3]	block 4	10	✗ [9 or blank]	block 7	4	✗ [3 or blank]
I	6	✓	U	8	✓	U	12	✗ [7 or blank]	E	✗ [I or blank]		E	✗ [I or blank]	
✓	✓		✓	✓		U	15	✗ [1 or blank]	E	✗ [U or blank]		E	✗ [I or blank]	
U	10	✓	U	6	✗ [1]	U	9	✗ [3 or blank]	E	✗ [U or blank]		E	✗ [U or blank]	
✓	✓		✓	✓		U	19	✗ [8 or blank]	E	✗ [I or blank]		E	✗ [U or blank]	
U	8	✓	U	1	✗ [3]	E	✓		E	✓		U	6	✓
✗ [I]	✓		✓	✓		E	✓		E	✓		E	✗ [I or blank]	
U	7	✓	U	3	✗ [6]	E	✓		E	✓		U	14	✓
✓	✓		✓	✓		E	✓		E	✓		E	✗ [U or blank]	
												U	17	✓
												E	✗ [U or blank]	
												U	4	✓
												E	✗ [U or blank]	

<b>Started on</b>	Wednesday, 7 April 2021, 6:03 PM
<b>State</b>	Finished
<b>Completed on</b>	Wednesday, 7 April 2021, 6:08 PM
<b>Time taken</b>	5 mins 8 secs
<b>Grade</b>	1.25 out of 30.00 (4%)

**Question 1**

Partially correct

Mark -0.25 out of 2.00

Flag question

Which statements are true related to the information processing models?

- TRUE ✅ ✗ The flow-chart is a typical formalism to describe a problem in the demand-driven model
- FALSE ✅ ✗ The only way to express parallelism in the control-flow model is to use the FORK/JOIN primitives
- TRUE ✅ ✅ The spread-sheets update the cells according to the data-flow model
- TRUE ✅ ✗ In the data-flow model, the precedence graph describing a program can contain only one single token

**Question 2**

Incorrect

**Question 5**

Not answered

Marked out of 2.00

Flag question

Compare the following data storage technologies!

	SRAM	SLC NAND flash
Preserves its content without power supply	<input type="checkbox"/>	<input checked="" type="checkbox"/> <b>[X]</b>
Its content needs to be refreshed periodically	<input type="checkbox"/>	<input type="checkbox"/>
Supports byte-level addressing	<input checked="" type="checkbox"/> <b>[X]</b>	<input type="checkbox"/>
6 capacitors are needed to store 1 bit	<input type="checkbox"/>	<input type="checkbox"/>

**Question 6**

Partially correct

Mark 0.50 out of 2.00

Flag question

Which signals of the PCI bus are shared (not dedicated) among the peripherals?

# Architectures 2020/21/2

Question 1

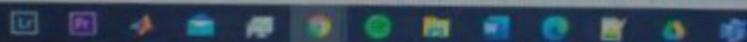
Not yet  
answered

Marked out of  
2.00

Flag question

In our 5-stage pipeline, which of the following phases do useful (effective) work on an arithmetic operation?

- TRUE ✅ EX (Execute)
- TRUE ✅ WB (Write Back)
- TRUE ✅ ID (Instruction Decode)
- FALSE ✅ MEM (Memory)



Escritorio

**Question 7**

Answer saved

Marked out of  
2.00

Flag question

A hard disk drive contains 2 double-sided platters. There are 1000 tracks in each platter. There are 10 sectors in each track. The size of the sectors is 500 byte.

*Please enter only a number, without space, comma or dot.*

Capacity: 360 ·  $10^9$  byte

**Question 8**

Answer saved

Marked out of  
2.00

Flag question

How many transistors are needed to store 18 bits in memory?

- In case of SLC: 18
- In case of MLC: 5
- In case of TLC: 3

**Question 9**

Answer saved

Marked out of  
2.00

Flag question

What does the **TLB coverage** mean in virtual memory systems?

TLB coverage is the amount of memory covered by page tables. The larger the TLB coverage is, the less we need to access the memory.

# lectures 2020/21/2

## Question 1

Not yet  
answered

Marked out of  
2.00

Flag  
question

X

Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
This is the faster form the two	<input type="checkbox"/>	X
The storage cell consists of only transistors	<input type="checkbox"/>	X
6 transistors are needed to store 1 bit	<input type="checkbox"/>	X
The cache memory is based on this technology	<input type="checkbox"/>	X

**Question 13**

Not yet  
answered

Marked out of  
2.00

 Flag question

What is the most important difference between the Neuma

The instructions and the data is stored separately

I

**Question 14**

Not yet

List the benefits of larger and the benefits of smaller page size

**Question 5**

Answer saved

Marked out of  
2.00

Flag question

Which of the following exceptions can occur in the instruction fetch (IF) phase?

- FALSE Arithmetic error
- TRUE Page fault
- FALSE Invalid instruction
- TRUE Protection fault

**Question 6**

Answer saved

Marked out of  
2.00

Flag question

Which of the following tasks have to be done by the compiler/programmer in the (classical) VLIW architecture?

- TRUE Collecting and grouping independent instructions
- FALSE Detecting hazards and insert stalls
- TRUE Assigning instructions to the functional units
- FALSE Execution of the instructions

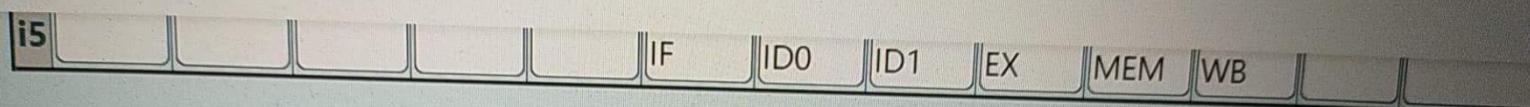
of the time spend in ID1.

Schedule the instructions in the pipeline (determine which instruction is in which stage in every time step). If a pipeline stall needs to be inserted, provide the reason by the following notation:

- **D\***: the reason of the stall is data hazard
- **S\***: the reason of the stall is structural hazard
- **C\***: the reason of the stall is control hazard

Write the solution to the following table! If a forwarding was needed during the execution of the instruction, write the pipeline register, from which the operand is taken, to the last column ! In case of multiple forwarding was needed for a single instruction, list the affected pipeline registers separated by comma, without spaces! (3p)

	1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	Forwarding
i1	IF	ID0	ID1	EX	MEM	WB							
i2		IF	ID0	ID1	D*	EX	MEM	WB					MEM/WB
i3			IF	ID0	S*	ID1	EX	MEM	WB				EX/MEM
i4				IF	S*	ID0	ID1	EX	MEM	WB			
i5					IF	ID0	ID1	EX	MEM	WB			



Reorder the instructions to improve the execution time (while keeping the semantics of the program)! (1 point)

The new (reordered) sequence of instructions: i1 - i4 - i2 - i3 - i5

- FALSE ✅ Collision detection-based arbitration

Which of the following statements are true for the logical/architectural registers?

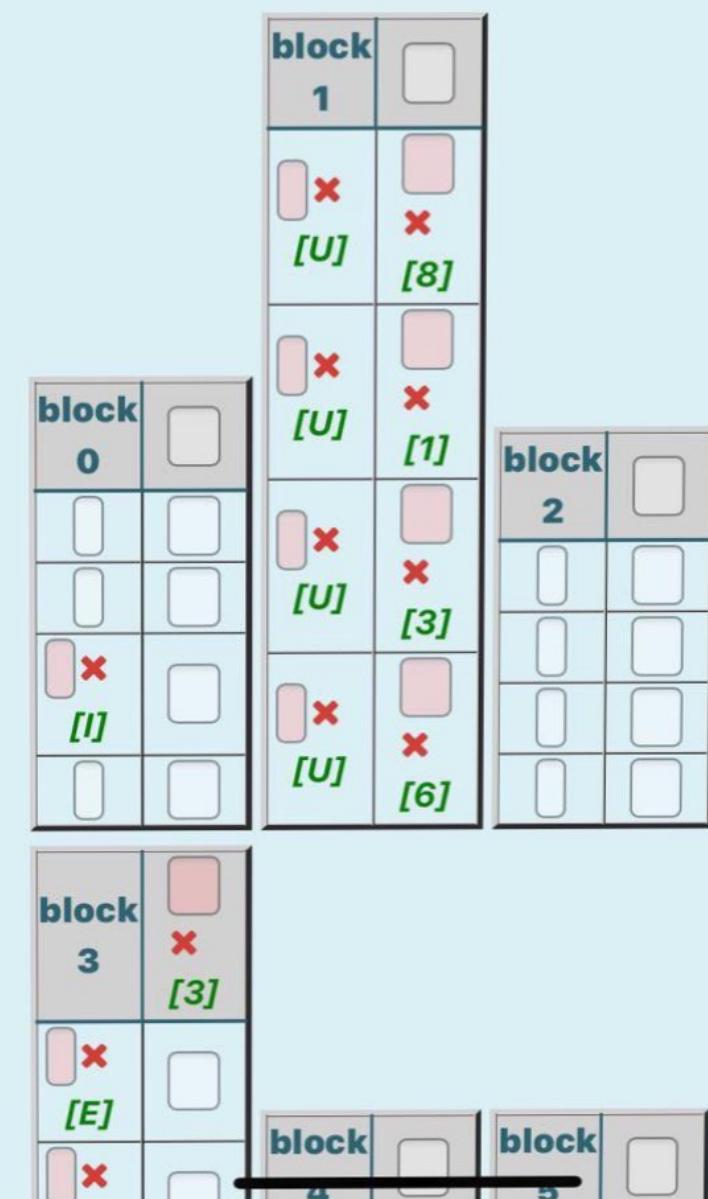
- FALSE ✅ There are more logical/architectural registers in a CPU than physical registers
- TRUE ✅ The programmer can use these, instead of the physical registers
- FALSE ✅ They are hidden from the programmers
- TRUE ✅ The instruction set architecture specifies the number of them, and also their names

In our 5-stage pipeline, which of the following phases do useful (effective) work on an arithmetic instr.

- TRUE ✅ EX (Execute)

E		U	15
---	--	---	----

a) How does the state of the SSD change when read requests arrive to LBA addresses **4**, **8** and **6**, accordingly. If a new write frontier is needed, select one that ensures the most balanced wearing of the blocks. When the number of erased blocks **after** a write operation decreases below 3, execute the garbage collection algorithm, potentially multiple times, till the number of erased block increases back to 3. The garbage collector always selects the block containing the most invalid pages. If there are many of such candidate blocks, it picks the least weared one.



X

Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
<b>Its content is lost when the power supply is switched off</b>	X [X]	X ✓
<b>Its content needs to be refreshed periodically</b>	X ✓	
<b>This has the larger data storage density</b>	X ✓	
<b>To store 1 bit, 6 capacitors are needed</b>		

→

**Question 2**

Not answered

Marked out of  
4.00

Flag question

Let us consider a special computer with a heat sensitive peripheral and a temperature sensor. The CPU can read the temperature sensor any time (a readout needs 800 clock cycles from the CPU), and it does not support interrupts. The peripheral overheats twice in a minute in average. In case of overheating the CPU switches off the peripheral and switches it on again a bit later. The switch on and off times are short enough to consider them negligible.

- a) How many times does the CPU have to poll the temperature sensor in each second, if the peripheral tolerates overheating only for 0.4 ms time? (1 point)

Answer: ✖ **[2500 or 2.500]** poll/sec

- b) With the polling time calculated in part a) what is the average delay to get the CPU informed on the overheating? (expressed in ms) (1 point)

Answer: ✖ **[0.2 or 0,2]** ms

- c) What is the minimal clock frequency for the CPU so that it can fully handle the heat sensitive peripheral? Assume that the CPU has an average load of  $98 \cdot 10^6$  clock cycles for other purposes, too.

Answer: ✖ **[100]  $\cdot 10^6$**  clock cycles/sec

<b>memory operations are also supported</b>	X	
<b>redundancy</b>		X
<b>instruction execution times</b>	X	
<b>instruction encoding</b>		X

statements are true for the SRAM, and which ones for the DRAM memory techn

	DRAM	SRAM
<b>Information is lost when the power supply is switched off</b>		X
<b>Information needs to be refreshed periodically</b>	X	
<b>the larger data storage density</b>	X	
<b>1 bit, 6 capacitors are needed</b>		X

A hard disk drive contains 2 double-sided platters, with 120000 tracks on each recording side. Each track contains 50 sectors. Each sector is 500 byte. What is the storage capacity of the hard disk drive? Answer only a number, without space, comma and dot characters!

360

$\cdot 10^9$  byte

Enumerate the 5 most common DRAM commands!

ACTIVATE

READ

WRITE

PRECHARGE

**Question 1**

Not yet  
answered

Marked out of  
2.00

Flag question

How many transistors are needed to store 18 bits in an SLC, in a MLC, and in a TLC flash based SSD drive?

- In case of SLC:
- In case of MLC:
- In case of TLC:

Next page

(You might not need all lines.)

Given the DRAM technologies provided by the table, in which clock cycle does the first data appear on the data lines of the memory m  
first memory request provided above (according to FCFS scheduling), measured in clock cycles (part a), and measured in nanoseconds  
initial state of the memory controller is the one provided in the description above. The timing parameters are given in format  $T_{CAS} - T_{RAS}$ .  
 $T_{RP}$  is the delay of the PRECHARGE command,  $T_{RCD}$  is the row activation delay, and  $T_{CAS}$  is the column latency, all of them given in (ex)  
cycles. (Write only a single number into the fields!) (3 points)

Technology	(a) Time till the response, in cycles	(b) (b) Time till response, in ns
DDR2-800, 5-5-5		
DDR3-1600, 7-8-8		
DDR3-2000, 11-13-13		

Mark 0.50 out of 2.00

Flag question

Which statements are true for the "bulk" data transmission mode in USB?

- TRUE ✓ The USB system guarantees error-free data transmission
- FALSE ✓ "Bulk" data is guaranteed to be scheduled in every frame up to 90% of the frame capacity
- TRUE ✗ "Bulk" data is guaranteed to be scheduled in every frame up to 10% of the frame capacity
- TRUE ✗ "Bulk" data transfers can have an "output" direction only

Information

Flag question

A computer has a single-channel DRAM based system memory with 64 bit data units. The burst size is set to 8 data units. Let us ignore the presence of multiple banks and ranks.

The memory controller receives the following read requests, given by row and column coordinates

- (row 4, column 24), (row 1, column 0), (row 4, column 8)

Question 1

Incorrect

Mark 0.00 out of  
2.00

 Flag question



Compare the following data storage technologies!

	SRAM	SLC NAND flash
Preserves its content without power supply		X ✓
Its content needs to be refreshed periodically	X ✗ [blank]	
Supports byte-level addressing	X ✓	
6 capacitors are needed to store 1 bit		X ✗ [blank]



...

ENGLISH

العربية



order according to FCFS and FR-FCFS

command scheduling, assuming that there can be a single row open at a time.

Row 1 is assumed to be in activated state initially. After the last command the memory controller does not close the active row. (3 points)

#### FCFS scheduling:

	Command	Parameter
1:		
1:	✗ [PRECHARGE]	
2:		✗
2:	✗ [ACTIVATE] [4]	
3:		✗
3:	✗ [READ] [24]	
4:		
4:	✗ [PRECHARGE]	
5:		
5:	✗ [ACTIVATE] [1]	
6:		✗
6:	✗ [READ] [0]	



Which of the following statements are true for the data-driven informati

- TRUE ✕ The Harvard architecture follows this principle
- TRUE ✅ It can exploit the parallelism of the program automatically
- FALSE ✅ It does not execute an instruction till its result is required
- TRUE ✅ The program is described by a precedence graph

these words that have changed.

After reading block 475:

Initial state:

184
249
123
76
413
334
183



After reading block 26:

Initial state:

184
249
123
76
413
334
183



**Question 12**Not yet  
answeredMarked out of  
3.00

Flag question

Given the DRAM technologies provided by the table, in which clock cycle does the first data appear on the data lines of the memory module for the first memory request provided above (according to FCFS scheduling), measured in clock cycles (part a), and measured in nanoseconds (part b)? The initial state of the memory controller is the one provided in the description above. The timing parameters are given in format  $T_{CAS} - T_{RCD} - T_{RP}$ , where  $T_{RP}$  is the delay of the PRECHARGE command,  $T_{RCD}$  is the row activation delay, and  $T_{CAS}$  is the column latency, all of them given in (external) clock cycles. (Write only a single number into the fields!) (3 points)

Technology	(a) Time till the response, in cycles	(b) Time till response, in ns
DDR2-800, 5-5-5	<input type="text"/>	<input type="text"/>
DDR3-1600, 7-8-8	<input type="text"/>	<input type="text"/>
DDR3-2000, 11-13-13	<input type="text"/>	<input type="text"/>



2		

block 3	

block 4	

block 5	

block 6	

block 7	

Fill in only those fields that changed! (5 points)

Question 8

Not answered

X

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

	CISC	RISC
<b>Register-memory operations are also supported</b>		
<b>Nearly no redundancy</b>		
<b>Variable instruction execution times</b>		
<b>Fixed length instruction encoding</b>		

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

	CISC	RISC
<b>Register-memory operations are also supported</b>		X
<b>Nearly no redundancy</b>		X
<b>Variable instruction execution times</b>	X	
<b>Fixed length instruction encoding</b>		X

Mark 0.00 out of  
2.00

Flag question

drive?

Please enter only a number, without space, or unit.

Capacity: 7360 ✖ [360] · 10<sup>9</sup> byte

### Question 5

Complete

Mark 0.00 out of  
2.00

Flag question

What does the **TLB coverage** mean in virtual memory?

IT IS A MEMORY CACHE USED TO REDUCE THE NUMBER OF ADDRESS TRANSLATIONS.  
TLB IS BELONGS TO CHIP MEMORY MANAGEMENT UNIT.  
TLB IS USED BY MMU WHEN VIRTUAL ADDRESS IS TRANSLATED INTO PHYSICAL ADDRESS.

### Question 6

Correct

Mark 2.00 out of  
2.00

Flag question

Which of the following statements are true for Harvard architecture?

- FALSE ✅ The Harvard architecture features two separate memory spaces for code and data.
- TRUE ✅ It can exploit the parallelism between code and data execution.
- FALSE ✅ It does not execute an instruction at a time.
- TRUE ✅ The program is described by two separate programs.

- In case of TLC: 54 54 X [6]

A hard disk drive contains 2 double-sided platters, with 120000 tracks and 1500 sectors in each track. The size of the sectors is 500 byte. What is the capacity of the drive?

*Please enter only a number, without space, comma and dot character.*

Capacity: 7360 X [360] ·  $10^9$  byte

What does the **TLB coverage** mean in virtual memory systems?

IT IS A MEMORY CACHE USED TO REDUCE THE USAGE OF THE TIME.  
TLB IS BELONGS TO CHIP MEMORY MANAGEMENT UNIT [ MMU ].  
TLB IS USED BY MMU WHEN VIRTUAL ADDRESS NEEDS TO BE TRANSLATED.

Which of the following statements are true for the data-driven information?



70%

TRUE ✅ ✓ The program is described by a precedence graph

X

Which statements are true for the RISC, and which ones for the CISC instruction set architecture?

	CISC	RISC
Register-memory operations are also supported	✗ [X]	✗
Nearly no redundancy	✗ [blank]	✗
Variable instruction execution times	✗ ✓	
Fixed length instruction encoding		✗ ✓

Which statements are true for the USB interface?

TRUE ✅ ✓ It uses serial data transfer

FALSE ✅ ✓ The components communicate with each other through dedicated point-to-point links

FALSE ✅ ✓ A serial (daisy chain-based) arbitration procedure is applied to select devices



**Question 17**Incomplete  
answerMarked out of  
3.00 Flag question

Mark the data dependent instruction pairs by putting "X" characters into the appropriate fields of the table!

**RAW dependencies:**

	i1	i2	i3	i4
i1				
i2	X			
i3				
i4			X	

**WAR dependencies:**

	i1	i2	i3	i4
i1				
i2	X			
i3		X		
i4				

**WAW dependencies:**

	i1	i2	i3	i4
i1				
i2	X			
i3				
i4	X			

HIT

Question 2

Incorrect

Mark 0.00 out  
of 2.00

Flag  
question



Which statements are true for systems based on north and south bridges?

	North bridge	South bridge
Has its own I/O instructions and runs I/O programs	X X [blank]	
Its most important task is to serve memory transactions	X ✓	
It has a direct connection with the CPU	X ✓	
All I/O devices are connected to it, except the graphics card	X X [blank] X X [X]	

Question 3

Partially  
correct

Mark -0.25 out  
of 2.00

Flag  
question

Which statements are true for the "bulk" data transmission mode in USB?

- TRUE ✅ ✓ The USB system guarantees error-free data transmission
- TRUE ✅ ✗ "Bulk" data is guaranteed to be scheduled in every frame up to 90% of the frame capacity
- TRUE ✅ ✗ "Bulk" data is guaranteed to be scheduled in every frame up to 10% of the frame capacity
- TRUE ✅ ✗ "Bulk" data transfers can have an "output" direction only

Question 4

Partially  
correct

Mark -0.25 out  
of 2.00

Flag  
question

What is the purpose of the garbage collection in SSD devices?

- TRUE ✅ ✗ To move the pages belonging to the same file next to each other to make read and write operations faster
- TRUE ✅ ✓ The creation of new erased blocks
- TRUE ✅ ✗ To increase the storage capacity by deleting the unnecessary files
- TRUE ✅ ✗ To remove the unnecessary electrons from the drive

Question 5

Partially  
correct

Which statements are true related to the information processing models?

- TRUE ✅ ✗ The flow-chart is a typical formalism to describe a problem in the demand-driven model

020/21/2

Which of the following statements are true for the data-driven information processing model?

- FALSE  The Harvard architecture follows this principle
- TRUE  It can exploit the parallelism of the program automatically
- FALSE  It does not execute an instruction till its result is required by another instruction
- TRUE  The program is described by a precedence graph

the frame capacity

- TRUE ✅ ❌ "Bulk" data transfers can have an "output" direction only

Information

Flag question

A computer has a single-channel DRAM based system memory with 64 bit data units. The burst size is set to 8 data units. Let us ignore the presence of multiple banks and ranks.

The memory controller receives the following read requests, given by row and column coordinates

- (row 4, column 24), (row 1, column 0), (row 4, column 8)

### Question 12

Not answered

Marked out of 3.00

Flag question



List the commands sent by the memory controller to the memory modules (in the right

**Question 10**

Answer saved

Marked out of  
2.00

Flag question



Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
This is the faster form the two		X
The storage cell consists of only transistors		X
6 transistors are needed to store 1 bit		X
The cache memory is based on this technology	X	X

**Question 11**

Answer saved

Marked out of  
2.00

Flag question



Which components of the computer can act as an initiator and as a target in a PCI/PCI Express transaction?

	As initiator	As target
The CPU	X	
An other PCI/PCI Express peripheral	X	X
The memory		X

Question 6

Not answered

Marked out of  
2.00

 Flag question



Which statements are true for systems based on north and south bridges?

	North bridge	South bridge
<b>Has its own I/O instructions and runs I/O programs</b>	<input type="checkbox"/>	<input type="checkbox"/>
<b>Its most important task is to serve memory transactions</b>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>It has a direct connection with the CPU</b>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
<b>All I/O devices are connected to it, except the graphics card</b>	<input type="checkbox"/>	<input checked="" type="checkbox"/>

## Architectures 2019/20/2

A hard disk drive contains 2 double-sided platters, with 50000 tracks on each recording surface and with 500 sectors per track. The size of the sectors is 500 byte. There is no ZBR, and the speed of the data transmission interface is  $10^6$  byte/s. The command processing time is neglected, because it is very low. The average seek time is 5 ms, and the revolution speed is 6000 RPM.

The storage capacity of the hard disk drive, measured in  $10^9$  bytes, is:   $\cdot 10^9$  byte (1 point)

The full revolution time of the disk, given in ms, is:  ms (1 point)

How long does it take to read one sector from the recording surface, given that the head is at the appropriate position (points to the beginning of the sector):  ms (1 point)

) How long does it take to transmit one sector on the data transmission interface? (in ms)  ms (1 point)

) How much slower is the full service time of a request for 100 consecutive sectors than the full service time of a request for 1 sector? (2 point)

The answer is:  ms

) We would like to slow down the rotation time from 6000 RPM to 4000 RPM. What should be the new seek time, which ensures that the average full service time of 1 sector remains the same with the slower rotation speed?

The answer is:  ms

**Question 8**

Not answered

Marked out of 2.00

Flag question

Enumerate the 5 most common DRAM commands!

**Question 9**

Not answered

Marked out of 4.00

Flag question

Let us consider a special computer with a heat sensitive peripheral and a temperature sensor. The CPU can read the temperature sensor any time (a readout needs 800 clock cycles from the CPU), and it does not support interrupts. The peripheral overheats twice in a minute in average. In case of overheating the CPU switches off the peripheral and switches it on again a bit later. The switch on and off times are short enough to consider them negligible.

a) How many times does the CPU have to poll

- FALSE Collision detection-based arbitration

Question 2

Answer saved

Marked out of  
2.00

Flag question

Which of the following statements are true for the logical/architectural registers?

- FALSE There are more logical/architectural registers in a CPU than physical registers
- TRUE The programmer can use these, instead of the physical registers
- FALSE They are hidden from the programmers
- TRUE The instruction set architecture specifies the number of them, and also their names

Question 3

Answer saved

Marked out of  
2.00

Flag question

In our 5-stage pipeline, which of the following phases do useful (effective) work on an arithmetic instruction?

- TRUE EX (Execute)
- FALSE WB (Write Back)
- FALSE ID (Instruction Decode)

What is the theoretically minimal size of the entire page table (including level 1 and 2)?

8 ✓

b) How many pages does the virtual memory have? 20 ✗ [16]

How many frames does the physical memory have? 4096 ✗ [4]

c) Where is

- page 6 located: disk ✓
- page 9 located: frame3 ✓

(Possible answers: "disk", or "frame0", "frame1", etc. (without space), please enter the answer field)

d) Which page is located:

- on frame 0: 2 ✓
- on frame 1: 8 ✓

(The answer should be only a single integer number, starting from 0)

e) Modify the page table according to the following changes:

- Page 9 has been moved to the disk
- Page 0 has been loaded from the disk and placed to frame 3

Please write the modifications to the page table below. It is enough to fill in only those

Level 1 page table:

V	Address
00:1	
01:1	

(The answer should be only a single integer number, starting from 0)

e) Modify the page table according to the following changes:

- Page 9 has been moved to the disk
- Page 0 has been loaded from the disk and placed to frame 3

Please write the modifications to the page table below. It is enough to fill in only those fields that have changed.

Level 1 page table:

V	Address
00: 1	
01: 1	
10: 1	
11: 1	

Level 2 page tables:

	V	Cím
00:	✗ [1]	✗ [3]
01:		
10:		
11:		

	V	Cím
00:		
01:		
10:		
11:		

	V	Cím
00:		
01:	✗ [0]	
10:		
11:		

	V	Cím
00:		
01:		
10:		
11:		

Your answer is partially correct.

Information

Flag question

A computer has a single-channel DRAM based system memory with 64 bit data units. The burst size is set to 8 data units. Let us ignore the presence of multiple banks and ranks.

The memory controller receives the following read requests, given by row and column coordinates

- (row 4, column 24), (row 1, column 0), (row 4, column 8)

Completed on	Tuesday, 14 April 2020, 7:59 PM
Time taken	50 mins 1 sec
Grade	Not yet graded

Question 1

Partially correct

Mark 0.25 out of

Flag question

Which components can initiate data transfer to a PCI peripheral?

- TRUE ✅ ✓ The CPU
- FALSE ✅ ✓ The system memory
- TRUE ✅ ✓ An other PCI peripheral
- FALSE ✅ ✗ A PCI Express peripheral

Question 2

Partially correct

Mark 2.00 out of

0

Flag question

Which statements are true for the USB interface?

- TRUE ✅ ✓ It uses serial data transfer
- FALSE ✅ ✓ The components communicate with each other through de
- FALSE ✅ ✓ A serial (daisy chain-based) arbitration procedure is applied
- TRUE ✅ ✓ It does not support real interrupt handling, only polling

Question 3

Partially correct

Mark 1.25 out of  
2.00

Flag question

Which of the following statements are true for the data-driven information proce

- TRUE ✅ ✗ The Harvard architecture follows this principle
- TRUE ✅ ✓ It can exploit the parallelism of the program automatically
- FALSE ✅ ✓ It does not execute an instruction till its result is required by an
- TRUE ✅ ✓ The program is described by a precedence graph

Question 4

Partially correct

Mark 1.25 out of  
2.00

Flag question

Which of the following arbitration procedures are centralized?

- TRUE ✅ ✓ Daisy chain-based arbitration
- FALSE ✅ ✗ Parallel arbitration
- FALSE ✅ ✓ Distributed arbitration
- FALSE ✅ ✓ Collision detection-based arbitration

**Question 4**

Incorrect

Mark -1.00 out  
of 2.00

 Flag question

Which statements are true related to the information processing models?

- TRUE ✘ The flow-chart is a typical formalism to describe a problem in the demand-driven model
- FALSE ✘ The only way to express parallelism in the control-flow model is to use the FORK/JOIN primitives
- FALSE ✘ The spread-sheets update the cells according to the data-flow model
- TRUE ✘ In the data-flow model, the precedence graph describing a program can contain only one single token

Which components of the computer can act as an initiator and as a target in a PCI/PCI Express transaction?

	As initiator	As target
The CPU	X	
An other PCI/PCI Express peripheral		X
The memory		X

**addressing****[X]**

6 capacitors are needed to store 1 bit

**Question 6**

Partially correct

Mark 0.50 out of 2.00

Flag question

Which signals of the PCI bus are shared (not dedicated) among the peripherals?

- TRUE The address and the data (A/D) lines
- TRUE The TRDY and IRDY lines used for the flow-control
- FALSE The FRAME line that indicates the end of the current transaction
- TRUE The REQ and the GNT lines used for the arbitration

**Question 7**

Not answered

Marked out of 5.00

Flag question

The current state of an SSD consisting of 8 blocks is depicted in the following figure.

### Question 3

Not answered

Marked out of 2.00

Flag question

X

Which statements are true for systems based on north and south bridges?

	North bridge	South bridge
<b>Has its own I/O instructions and runs I/O programs</b>	<input type="checkbox"/>	<input type="checkbox"/>
<b>Its most important task is to serve memory transactions</b>	<input checked="" type="checkbox"/> [X]	<input type="checkbox"/>
<b>It has a direct connection with the CPU</b>	<input checked="" type="checkbox"/> [X]	<input type="checkbox"/>
<b>All I/O devices are connected to it, except the graphics card</b>	<input type="checkbox"/>	<input checked="" type="checkbox"/> [X]

### Question 4

Partially correct

Mark 0.50 out of 2.00

Flag question

What is the purpose of the garbage collection in SSD devices?

- FALSE  To move the pages

Which phases of the instruction execution belong to the **backend** of the pipeline?

- TRUE  The fetching of the instructions
- FALSE  Putting the instructions to the instruction window
- TRUE  Scheduling the instructions for execution to the appropriate functional unit
- FALSE  The execution of the instructions

**Question 3**Not yet  
answeredMarked out of  
5.00

Flag question

The current state of an SSD consisting of 8 blocks is depicted in the following figure.

One table represents one block. The top left corner of the blocks refer to the number of the block (in bold), and the top right corner of the blocks contain the number of programming/erase cycles. Each block consists of 4 pages. For each page the state of the page ("U"=used, "I"=invalid, "E"=erased) and the LBA address of the stored data are provided.

In the initial state blocks 1, 2 and 5 are erased, and the write frontier is block 6.

block <b>0</b>	4	block <b>1</b>	7	block <b>2</b>	8	block <b>3</b>	2	block <b>4</b>	9	block <b>5</b>	16	block <b>6</b>	5
I	6	E		E		I	7	I	12	E		U	6
U	10	E		E		U	1	U	9	E		U	14
U	8	E		E		U	3	U	19	E		U	17
U	7	E		E		I	8	I	7	E		E	

block <b>7</b>	3
I	19
U	12
I	15
U	15

In our 5-stage pipeline, which of the following phases do useful (effective) work on an arithmetic instruction?

- TRUE ↴ EX (Execute)
- FALSE ↴ WB (Write Back)
- TRUE ↴ ID (Instruction Decode)
- FALSE ↴ MEM (Memory)

# Computer Architectures 2020/21/2

## Question 10

Not yet answered

Marked out of 2.00

Flag question

List the benefits of larger and the benefits of smaller page sizes in virtual memory systems!

Previous page

Next page

Quiz navigation



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
i	19	20	21	22						▲	▲						

Finish attempt ...

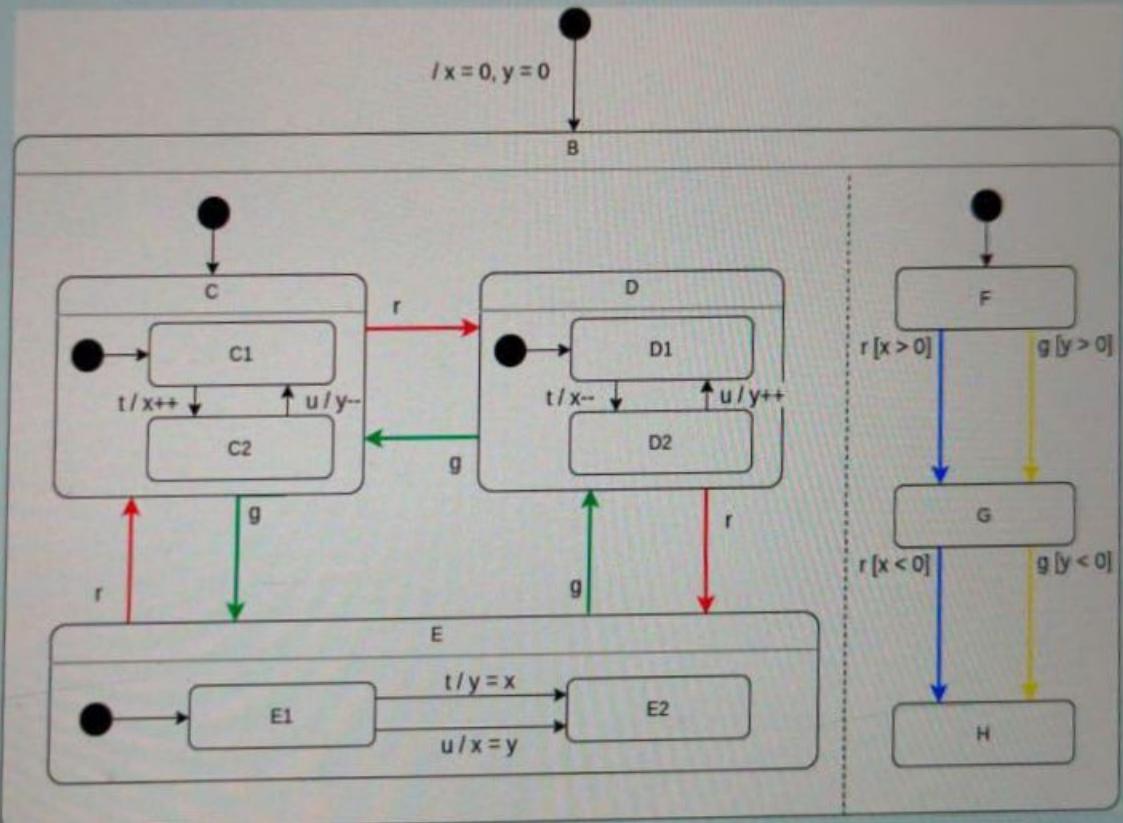
Time left 0:49:40

**Question 3**

Not answered

Mark 0.00 out  
of 6.00 Flag  
question

A composite Harel-statechart is given below. The statechart accepts the following events: {  $g, r, t, u$  }. The variables  $x$  and  $y$  are integers.



Your task is to give an event sequence, which fulfills **all** of the conditions below. The event sequence...

- covers at least 2 red edges,

In our 5-stage pipeline, which of the following phases do useful (effective)

- TRUE ⇔ EX (Execute)
- TRUE ⇔ WB (Write Back)
- FALSE ⇔ ID (Instruction Decode)
- FALSE ⇔ MEM (Memory)

Which phase of the instruction execution belongs to the backend of the pipeline?

Question 5

Correct

Mark 2,00 out of  
2,00

Flag question



Which statements are true for the RISC, and which ones for the CISC instruction set architecture?

	CISC	RISC
Register-memory operations are also supported	X ✓	
Nearly no redundancy		X ✓
Variable instruction execution times	X ✓	
Fixed length instruction encoding		X ✓

Question 6

Partially correct

Mark 1,00 out of  
2,00

Flag question



Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
Its content is lost when the power supply is switched off	✗ [X]	X ✓
Its content needs to be refreshed periodically	X ✓	
This has the larger data storage density	X ✓	
To store 1 bit, 6 connections are needed		



Search the web and Windows



	Command	Parameter
1:	x [PRECHARGE]	
2:	x [ACTIVATE]	x [4]
3:	x [READ]	x [24]
4:	x [PRECHARGE]	
5:	x [ACTIVATE]	x [1]
6:	x [READ]	x [0]
7:	x [PRECHARGE]	
8:	x [ACTIVATE]	x [4]
9:	x [READ]	x [8]

FR-FCFS scheduling:

	Command	Parameter
1:	x [READ]	x [0]
2:	x [PRECHARGE]	
3:	x [ACTIVATE]	x [4]
4:	x [READ]	x [24]
5:	x [READ]	x [8]
6:		
7:		
8:		
9:		

X

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

	CISC	RISC
<b>Register-memory operations are also supported</b>	X	
<b>Nearly no redundancy</b>		X
<b>Variable instruction execution times</b>	X	
<b>Fixed length instruction encoding</b>		X

?	00:0	?	00:1	1	00:0	?
?	01:1	2	01:1	3	01:0	?
0	10:0	?	10:0	?	10:0	?
?	11:0	?	11:0	?	11:0	?

The questions are as follows:

What is the theoretically maximal size of the entire page table (including level 1 and level 2 tables), given in bytes?

What is the theoretically minimal size of the entire page table (including level 1 and level 2 tables), given in bytes?

a) How many pages does the virtual memory have?

b) How many frames does the physical memory have?

c) Where is

- page 6 located:
- page 9 located:

(Possible answers: "disk", or "frame0", "frame1", etc. (without space), please enter the answer in this format to the answer field)

d) Which page is located:

- on frame 0:
- on frame 1:

(The answer should be only a single integer number, starting from 0)

e) Modify the page table according to the following changes:

- Page 9 has been moved to the disk
- Page 0 has been loaded from the disk and placed to frame 3

Please write the modifications to the page table below. It is enough to fill in only those fields that have changed.

Level 1 page table:

V	Address
00:1	
01:1	
10:1	
11:1	

Level 2 page tables:

<input type="text" value="V"/>	<input type="text" value="Cím"/>						
00:		00:		00:		00:	
01:		01:		01:	0	01:	
10:		10:		10:		10:	
11:1	0	11:		11:		11:	

**Question 4**Not yet  
answeredMarked out of  
2.00Flag  
question

Which phases of the instruction execution belong to the **backend** of the pipeline?

- The fetching of the instructions
- Putting the instructions to the instruction window
- Scheduling the instructions for execution to the appropriate functional unit
- The execution of the instructions

**Question 5**Not yet  
answeredMarked out of  
2.00Flag  
question

Which of the following exceptions can occur in the instruction fetch (IF) phase?

- Arithmetic error
- Page fault
- Invalid instruction
- Protection fault

**Question 6**Not yet  
answeredMarked out of  
2.00Flag  
question

Which of the following tasks have to be done by the compiler/programmer in the (classical) VLIW architecture?

- Collecting and grouping independent instructions
- Detecting hazards and insert stalls
- Assigning instructions to the functional units
- Execution of the instructions

**Question 24**

Incorrect

Mark 0.00 out of  
6.00

Flag question

Let the virtual addresses be 20 bit wide, and the physical addresses 15 bit wide. The page size is  $2^{11} = 2\text{kB}$ . The CPU uses a 3-level hierarchical page table with 16 bit wide entries.

- The number of pages in the virtual memory:  ✘ [512]
- The number of frames in the physical memory:  ✘ [16]
- If there is no page fault, how many times does the CPU need to access the system memory in order to perform address translation? Count only the memory accesses corresponding to the address translation itself, do not include the memory operation that triggered the address translation!
  - in case of TLB hit?  ✘ [0]
  - in case of TLB miss?:  ✘ [3]
- What is the total size of the page table? (in bytes):  ✘ [1168]
- What is the minimal size of the page table? (in bytes):  ✘ [48]
- What would be the size of the page table if we used a single level page table instead of the three level one? (in bytes):  ✘ [1024]
- What is the TLB coverage if the TLB consists of 4 entries (in bytes):  bytes

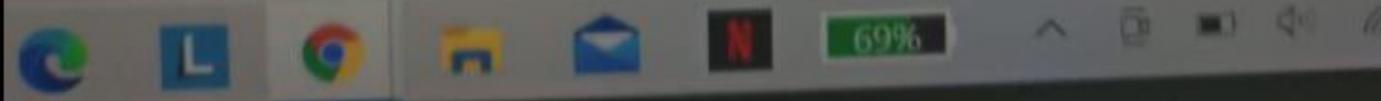
re true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
when the power supply is switched off	X [X]	X ✓
to be refreshed periodically	X ✓	
for data storage density	X ✓	
capacitors are needed		X ✗ [blank]

single-channel, DRAM based system memory with 64 bit data units. The burs ignore the presence of multiple banks and ranks.

oller receives the following read requests, given by row and column coordinates (row, column), (7. row, 24. column), (8. row, 32. column)

LOAD 128 64 CLOSE OPEN READ 192 56 7 PRECHARGE 32



Which are the characteristics of the three cache organisations we have studied?

	Fully associative organization LRU	+	N-way set associative organization + LRU	Direct mapped organization
The cache always contains the most recently used blocks of the memory	<input type="checkbox"/>		<input type="checkbox"/>	<input type="checkbox"/>
The simplest and most power efficient solution out of the three	<input type="checkbox"/>		<input type="checkbox"/>	X
Can be used with transparent cache addressing	<input type="checkbox"/>		<input type="checkbox"/>	<input type="checkbox"/>

Which phases of the instruction execution belong to the **backend** of the pipeline?

- TRUE    The fetching of the instructions
- FALSE    Putting the instructions to the instruction window
- TRUE    Scheduling the instructions for execution to the appropriate functional unit
- FALSE    The execution of the instructions

What control flow anomalies can occur in the instruction fetch (IF) phase?

Eliminate the WAW and WAR data dependencies with register renaming! Apply register renaming on each instruction systematically. The physical registers are denoted by U0, U1, U2, ..., etc. The initial state of the register alias table is provided below. When a new physical register is required, choose the one right after the biggest appearing in the register alias table. Update the register alias table after the renaming of each instruction (it is enough to fill in only those fields that have changed)! (3 points)

**The instruction sequence after register renaming:**

i1': U13	← MEM[U4+0]
i2': MEM[U13+0]	← U12
i3': U14	← U4+4
i4': U15	← MEM[U14+0]

**Register alias table:**

	Initially:	i1	i2	i3	i4
R0:	U4				
R1:	U7	U13			U15
R2:	U3				
R3:	U12			U14	

S command scheduling, assuming that there can be a single row open at a time.

8 is assumed to be in activated state initially. After the last command the memory controller *has to close* the active (3 points)

FCFS scheduling:

	Command	Parameter
1:	PRECHARGE	
2:	READ	16
3:	PRECHARGE	
4:	ACTIVATE	7
5:	READ	24
6:	PRECHARGE	
7:	ACTIVATE	8
8:	READ	32
9:		

FR-FCFS scheduling:

	Command	Parameter
1:	READ	16
2:	READ	32
3:	PRECHARGE	
4:	ACTIVATE	7
5:	READ	24
6:		
7:		
8:		
9:		

might not need all lines.)

HIT

**Question 16**

Answer saved

Marked out of  
6.00 Flag question

Assume that a CPU has a direct mapped cache memory of size 1024 bytes ( $=2^{10}$ ). The block size is 128 bytes ( $=2^7$ ). The CPU uses 24 bit wide addresses.

- (a) The length of the cache tags is:  bit
- (b) The length of the cache indices is:  bit
- (c) The number of comparisons done simultaneously during a cache lookup:  bit
- (d) The number of bits to compare by the comparators at each cache lookup:  bits
- (e) The program, while being executed, reads the following blocks of the system memory:
- 475, 26

How does the content of the cache memory change, when the program reads the given blocks in the initial state provided below? An empty field means invalid (empty) content. When there are several possibilities for block placement, choose the top-most place! It is enough to fill in those fields that have changed.

After reading block 475:

Initial state:

184
249
123
76
413
334
183

184
249
475
123
76
413
334
183

Which of the following statements are true for the logical/architectural registers?

- FALSE    There are more logical/architectural registers in a CPU than physical
- TRUE    The programmer can use these, instead of the physical registers
- FALSE    They are hidden from the programmers
- TRUE    The instruction set architecture specifies the number of them, and all



In our 5-stage pipeline, which of the following phases do useful (effective) work on a

Question 1  
complete  
Answer  
Marked out of  
0.00  
Flag question

Which components can initiate data transfer to a PCI peripheral?

- TRUE ↗ The CPU
- FALSE ↗ The system memory
- TRUE ↗ An other PCI peripheral
- FALSE ↗ A PCI Express peripheral

Please answer all parts of the question.

Question 2

Which stat...

# Architectures 2019/20/2

X

Which are the characteristics of the three cache organisations we have studied?

	Fully associative organization + LRU	N-way set associative organization + LRU	Direct mapped organization
The cache always contains the most recently used blocks of the memory	X	-	
The simplest and most power efficient solution out of the three			X
Can be used with transparent cache addressing	X	X	X

X

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

Which components of the computer can act as an initiator and as a target in a PCI/PCI Express

	As initiator	As target
The CPU	X	
An other PCI/PCI Express peripheral	X	
The memory		X

X

Which are the characteristics of the three cache organisations we have studied?

	Fully associative organization + LRU	N-way set associative organization + LRU	Direct mapped organization
The cache always contains the most recently used blocks of the memory	X		
The simplest and most power efficient solution out of the three		X	X
Can be used with transparent cache addressing	X	X	X



X

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

A hard disk drive contains 2 double-sided platters, with 120000 tracks on each recording surface and with 1500 sectors in each track. The size of the sectors is 500 byte. What is the storage capacity of the hard disk drive?

*Please enter only a number, without space, comma and dot characters!*

Capacity:  ·  $10^9$  byte

**Started on** Tuesday, 14 April 2020, 7:10 PM

**State** Finished

**Completed on** Tuesday, 14 April 2020, 7:57 PM

**Time taken** 46 mins 32 secs

**Grade** Not yet graded

Question 1

Partially correct

Mark 1.25 out of 2.00

Flag question

Which components can initiate data transfer to a PCI peripheral?

- TRUE ✅ ✓ The CPU
- FALSE ✅ ✓ The system memory
- TRUE ✅ ✓ An other PCI peripheral
- FALSE ✅ ✗ A PCI Express peripheral

Question 2

Partially correct

Mark 1.25 out of 2.00

Flag question

Which statements are true for the USB interface?

- FALSE ✅ ✗ It uses serial data transfer
- FALSE ✅ ✓ The components communicate with each other through dedicated point-to-point connections
- FALSE ✅ ✓ A serial (daisy chain-based) arbitration procedure is applied to select devices on the bus
- TRUE ✅ ✓ It does not support real interrupt handling, only polling

Which of the following arbitration procedures are centralized?

- TRUE ✓ Daisy chain-based arbitration
- FALSE ✗ Parallel arbitration
- FALSE ✓ Distributed arbitration
- FALSE ✓ Collision detection-based arbitration

X

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

	CISC	RISC
Register-memory operations are also supported	x ✓	
Nearly no redundancy		x ✗ ✓
Variable instruction execution times	x ✓	
Fixed length instruction encoding		x ✓

X

Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
Its content is lost when the power supply is switched off	x ✗ [X] ✓	x ✓
Its content needs to be refreshed periodically	x ✓	
This has the larger data storage density	x ✓	
To store 1 bit, 6 capacitors are needed		

Your answer is partially correct.

Question 7

Correct

Mark 2.00 out of

A hard disk drive contains 2 double-sided platters, with 120000 tracks on each recording surface and with 1500 capacity of the hard disk drive?



...

ENGLISH

العربية



6:	<b>[READ]</b>	[0]
7:	<b>[PRECHARGE]</b>	
8:	<b>[ACTIVATE]</b> [4]	x
9:	<b>[READ]</b>	x

(You might not need all lines.)

Finish review

## Quiz navigation

1	2	3	4	5	6	7	8	9	10
11	i	12							

Show one page at a time

Finish review



cycles/sec

**Question 10**

Not answered

Marked out of 2.00

Flag question

What is the difference between the DMA controllers and the I/O processors?

**Question 11**

Partially correct

Mark 0.50 out of 2.00

Flag question

Which statements are true for the "bulk" data transmission mode in USB?

- TRUE The USB system guarantees error-free data transmission
- FALSE "Bulk" data is guaranteed to be scheduled in every frame up to 90% of the frame capacity
- TRUE "Bulk" data is guaranteed to

Let us consider a special computer with a heat sensitive peripheral and a temperature sensor. The CPU can read the temperature sensor any time (a readout needs 800 clock cycles from the CPU), and it does not support interrupts. The peripheral overheats twice in a minute in average. In case of overheating the CPU switches off the peripheral and switches it on again a bit later. The switch on and off times are short enough to consider them negligible.

- a) How many times does the CPU have to poll the temperature sensor in each second, if the peripheral tolerates overheating only for 0.4 ms time? (1 point)

Answer: **[2500 or 2.500]**

poll/sec

- b) With the polling time calculated in part a) what is the average delay to get the CPU informed on the overheating? (expressed in ms) (1 point)

Answer: **[0.2 or 0,2]** ms

- c) What is the minimal clock frequency for the CPU so that it can fully handle the heat sensitive peripheral? Assume that the CPU has an average load of  $98 \cdot 10^6$  clock cycles for other purposes, too.

Answer: **[100]  $\cdot 10^6$  clock**  
cycles/sec

Question **10**

Not answered

Marked out of 2.00

precedence graph describing a program can contain only one single token

**Question 2**

Incorrect

Mark 0.00 out of 2.00

Flag question

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order: [LS] -  
[SS] - [SS+] - [FS] - [HS]

The correct answer is:

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order: [LS] - [FS] - [HS] - [SS] - [SS+]

**Question 3**

Not answered

Marked out of 2.00

Flag question



Let us consider a special computer with a heat sensitive peripheral and a temperature sensor. The CPU can read the temperature sensor any time (a readout needs 800 clock cycles from the CPU), and it does not support interrupts. The peripheral overheats twice in a minute in average. In case of overheating the CPU switches off the peripheral and switches it on again a bit later. The switch on and off times are short enough to consider them negligible.

- a) How many times does the CPU have to poll the temperature sensor in each second, if the peripheral tolerates overheating only for 0.4 ms time? (1 point)

Answer:  **[2500 or 2.500]** poll/sec

- b) With the polling time calculated in part a) what is the average delay to get the CPU informed on the overheating? (expressed in ms) (1 point)

Answer:  **[0.2 or 0,2]** ms

- c) What is the minimal clock frequency for the CPU so that it can fully handle the heat sensitive peripheral? Assume that the CPU has an average load of  $98 \cdot 10^6$  clock cycles for other purposes, too.

Answer:  **[100]  $\cdot 10^6$**  clock cycles/sec

lectures 2020/21/2

Question 8

Answer saved

Marked out of  
2.00

Flag question

Which of the following statements are true for the data-driven information processing model?

- FALSE  The Harvard architecture follows this principle
- TRUE  It can exploit the parallelism of the program automatically
- TRUE  It does not execute an instruction till its result is required by an other instruction
- FALSE  The program is described by a precedence graph

Previous page

What is the theoretically minimal size of the entire page table (including level 1 and

8 ✓

b) How many pages does the virtual memory have? 20 ✗ [16]

How many frames does the physical memory have? 4096 ✗ [4]

c) Where is

- page 6 located: disk ✓
- page 9 located: frame3 ✓

(Possible answers: "disk", or "frame0", "frame1", etc. (without space), please enter the answer field)

d) Which page is located:

- on frame 0: 2 ✓
- on frame 1: 8 ✓

(The answer should be only a single integer number, starting from 0)

e) Modify the page table according to the following changes:

- Page 9 has been moved to the disk
- Page 0 has been loaded from the disk and placed to frame 3

Please write the modifications to the page table below. It is enough to fill in only those

Level 1 page table:

V	Address
00:1	
01:1	

Given the DRAM technologies provided by the table, in which clock cycle does the first data appear on the data lines of the memory module for the first memory request provided above (according to FCFS scheduling), measured in clock cycles (part a), and measured in nanoseconds (part b)? The initial state of the memory controller is the one provided in the description above. The timing parameters are given in format  $T_{CAS} - T_{RCD} - T_{RP}$ , where  $T_{RP}$  is the delay of the PRECHARGE command,  $T_{RCD}$  is the row activation delay, and  $T_{CAS}$  is the column latency, all of them given in (external) clock cycles. (Write only a single number into the fields!) (3 points)

Technology	(a) Time till the response, in cycles	(b) Time till response, in ns
DDR2-800, 5-5-5		
DDR3-1600, 7-8-8		
DDR3-2000, 11-13-13		

20/21/2

Which of the following arbitration procedures are centralized?

- TRUE ↴ Daisy chain-based arbitration
- TRUE ↴ Parallel arbitration
- FALSE ↴ Distributed arbitration
- FALSE ↴ Collision detection-based arbitration



### Question 7

Not answered

Marked out of 5.00

Flag question

The current state of an SSD consisting of 8 blocks is depicted in the following figure.

One table represents one block. The top left corner of the blocks refer to the number of the block (in bold), and the top right corner of the blocks contain the number of programming/erase cycles. Each block consists of 4 pages. For each page the state of the page ("U"=used, "I"=invalid, "E"=erased) and the LBA address of the stored data are provided.

In the initial state blocks 1, 2 and 5 are erased, and the write frontier is block 6.

block 0	4	block 1	7	block 2	8
I	6	E		E	
U	10	E		E	
U	8	E		E	
U	7	E		E	

block 3	2	block 4	9	block 5	16
I	7	I	12	E	
U	1	U	9	E	
U	3	U	19	E	
I	8	I	7	E	

- FALSE  A PCI Express peripheral

Which statements are true for the USB interface?

- It uses serial data transfer
- TRUE  The components communicate with each other through dedicated point-to-point channels
- A serial (daisy chain-based) arbitration procedure is applied to select decide which master can talk at a time
- TRUE  It does not support real interrupt handling, only polling

Please answer all parts of the question.

Which of the following statements are true for the data-driven information processing model?

- The data and code share memory space and follow this principle

X

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

	CISC	RISC
Register-memory operations are also supported	X	
Nearly no redundancy		X
Variable instruction execution times	X	
Fixed length instruction encoding		X

X

Which of the following statements are true for the data-driven information processing model?

- FALSE ↴ The Harvard architecture follows this principle
- TRUE ↴ It can exploit the parallelism of the program automatically
- FALSE ↴ It does not execute an instruction till its result is required by another instruction
- TRUE ↴ The program is described by a precedence graph

Next

**Question 11**

Not yet  
answered

Marked out of  
2.00

Flag  
question

X

Which components of the computer can act as an initiator and as a target?

	<b>As initiator</b>	<b>As target</b>
<b>The CPU</b>		
<b>An other PCI/PCI Express peripheral</b>		
<b>The memory</b>		

Previous page

Sample mid-term test: Attempt review — Mozilla Firefox

0 🔒 26 https://moodle.hit.bme.hu/mod/quiz/review.php?attempt=56771&cmid=12019

HIT

Show one page at a time

Finish review

**Time taken** 6 mins 12 secs  
**Grade** 0.00 out of 30.00 (0%)

**Question 1**  
Not answered  
Marked out of 4.00  
Flag question

Let us consider a special computer with a heat sensitive peripheral and a temperature sensor. The CPU can read the temperature sensor any time (a readout needs 800 clock cycles from the CPU), and it does not support interrupts. The peripheral overheats twice in a minute in average. In case of overheating the CPU switches off the peripheral and switches it on again a bit later. The switch on and off times are short enough to consider them negligible.

a) How many times does the CPU have to poll the temperature sensor in each second, if the peripheral tolerates overheating only for 0.4 ms time? (1 point)

Answer:  ✗ [2500 or 2.500] poll/sec

b) With the polling time calculated in part a) what is the average delay to get the CPU informed on the overheating? (expressed in ms) (1 point)

Answer:  ✗ [0.2 or 0.2] ms

c) What is the minimal clock frequency for the CPU so that it can fully handle the heat sensitive peripheral? Assume that the CPU has an average load of  $98 \cdot 10^6$  clock cycles for other purposes, too.

Answer:  ✗ [100] : $10^6$  clock cycles/sec

**Question 2**  
Not answered  
Marked out of 2.00  
Flag question

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order:  -  -  -  -   
 SS+  SS  HS  FS  LS

The correct answer is:  
List the data transmission speeds supported by USB 3.1 in increasing order!  
USB speeds in increasing order: [LS] - [FS] - [HS] - [SS] - [SS+]

**Question 3**  
Not answered  
Marked out of 2.00  
Flag question

Which statements are true related to the information processing models?

- ✗ The flow-chart is a typical formalism to describe a problem in the demand-driven model
- ✗ The only way to express parallelism in the control-flow model is to use the FORK/JOIN primitives
- ✗ The spread-sheets update the cells according to the data-flow model

**Question 2**

Not answered

Marked out of  
4.00

Flag question

Let us consider a special computer with a heat sensitive peripheral and a temperature sensor. The CPU can read the temperature sensor any time (a readout needs 800 clock cycles from the CPU), and it does not support interrupts. The peripheral overheats twice in a minute in average. In case of overheating the CPU switches off the peripheral and switches it on again a bit later. The switch on and off times are short enough to consider them negligible.

- a) How many times does the CPU have to poll the temperature sensor in each second, if the peripheral tolerates overheating only for 0.4 ms time? (1 point)

Answer: ✗ **[2500 or 2.500]** poll/sec

- b) With the polling time calculated in part a) what is the average delay to get the CPU informed on the overheating? (expressed in ms) (1 point)

Answer: ✗ **[0.2 or 0,2]** ms

- c) What is the minimal clock frequency for the CPU so that it can fully handle the heat sensitive peripheral? Assume that the CPU has an average load of  $98 \cdot 10^6$  clock cycles for other purposes, too.

Answer: ✗ **[100]  $\cdot 10^6$**  clock cycles/sec

76
413
334
183

Initial state:
184
249
123
76
413
334
183

After reading block 26:

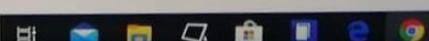
26
249
475
123
76
413
334
183

Previous page

Next page

Quiz navigation

Type here to search



^ D E ENG 6

with the CPU	[X]
All I/O devices are connected to it, except the graphics card	[X]

**Question 4**

Partially correct

Mark 0.50 out of 2.00

Flag question

What is the purpose of the garbage collection in SSD devices?

- FALSE To move the pages belonging to the same file next to each other to make read and write operations faster
- TRUE The creation of new erased blocks
- TRUE To increase the storage capacity by deleting the unnecessary files
- TRUE To remove the unnecessary electrons from the drive

**Question 5**

Not answered

Marked out of 2.00

Flag question

Which of the following arbitration procedures are centralized?

- TRUE Daisy chain-based arbitration
- TRUE Parallel arbitration
- FALSE Distributed arbitration
- FALSE Collision detection-based arbitration

Question 7

Not yet answered

Marked out of 2.00

 Flag question

Which of the following statements are true for the data-driven information processing model?

- FALSE  The Harvard architecture follows this principle
- TRUE  It can exploit the parallelism of the program automatically
- FALSE  It does not execute an instruction till its result is required by an other instruction
- TRUE  The program is described by a precedence graph

Which statements are true for the SRAM, and which ones for the DRAM memory technology?

	DRAM	SRAM
This is the faster form the two	<input type="checkbox"/>	X
The storage cell consists of only transistors	<input type="checkbox"/>	X
6 transistors are needed to store 1 bit	<input type="checkbox"/>	X
The cache memory is based on this technology	X	<input type="checkbox"/>



**Question 5**Not yet  
answeredMarked out of  
2.00

Flag question

Which of the following exceptions can occur in the instruction fetch (IF) phase?

- Arithmetic error
- Page fault
- Invalid instruction
- Protection fault

**Question 6**Not yet  
answeredMarked out of  
2.00

Flag question

Which of the following tasks have to be done by the compiler/programmer in the (classical) VLIW architecture?

- Collecting and grouping independent instructions
- Detecting hazards and insert stalls
- Assigning instructions to the functional units
- Execution of the instructions

**Question 5**

Not answered

Marked out of  
2.00

Flag question

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order:  -  -  -  -

LS    SS    HS    SS+    FS

The correct answer is:

List the data transmission speeds supported by USB 3.1 in increasing order!

USB speeds in increasing order: [LS] - [FS] - [HS] - [SS] - [SS+]

X

Mark the data dependent instruction pairs by putting "X" characters into the appropriate fields of the table!

**RAW dependencies:**

	i1	i2	i3	i4
i1				
i2				
i3				
i4				X

**WAR dependencies:**

	i1	i2	i3	i4
i1				
i2				
i3			X	
i4				

**WAW dependencies:**

	i1	i2	i3	i4
i1				
i2				
i3				
i4	X			

Assume that a processor uses 14 bit wide virtual and 12 bit wide physical memory addresses. The page size is 1024 byte ( $=2^{10}$ ). The address translation is based on a two-level page table with the same number of entries at each level. The page table entries are 8 bit (1 byte) wide.

The initial state of the page table is as follows:

Level 1 page table:

V	Address
00:1	
01:1	
10:1	
11:1	

Level 2 page tables:

V	Address	V	Address	V	Address	V	Address
00:0	?	00:0	?	00:1	1	00:0	?
01:0	?	01:1	2	01:1	3	01:0	?
10:1	0	10:0	?	10:0	?	10:0	?
11:0	7	11:0	?	11:0	?	11:0	?

The questions are as follows:

a) What is the theoretically maximal size of the entire page table (including level 1 and level 2 tables), given in bytes?

b) What is the theoretically minimal size of the entire page table (including level 1 and level 2 tables), given in bytes?

c) How many pages does the virtual memory have?

**Question 10**

Answer saved

Marked out of  
2.00 Flag question

Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
This is the faster form the two	X	X
The storage cell consists of only transistors		X
6 transistors are needed to store 1 bit		X
The cache memory is based on this technology		X

**Question 11**

Answer saved

Marked out of  
2.00 Flag question

Which components of the computer can act as an initiator and as a target in a PCI/PCI Express transaction?

	As initiator	As target
The CPU	X	
An other PCI/PCI Express peripheral	X	X
The memory		X

AA

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BMEVIHIAA02/EA-2019/20/2: Exam 1, June 3



Exam 1, .

X

Which are the characteristics of the three cache organisations we have studied?

	Fully associative organization + LRU	N-way set associative organization + LRU	Direct mapped organization
<b>The cache always contains the most recently used blocks of the memory</b>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<b>The simplest and most power efficient solution out of the three</b>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<b>Can be used with transparent cache addressing</b>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

X

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

**Question 11**Not yet  
answeredMarked out of  
2.00 Flag question

Which components of the computer can act as an initiator and as a target in a PCI/PCI Express transaction?

	As initiator	As target
The CPU	X	
An other PCI/PCI Express peripheral	X	X
The memory		X

[Previous page](#)[Next page](#)

- ✓ serial (daisy chain-based) arbitration procedure is applied to select decide which mas
- TRUE ♦ It does not support real interrupt handling, only polling

Which of the following statements are true for the data-driven information processing model?

- ♦ The Harvard architecture follows this principle
- TRUE ♦ It can exploit the parallelism of the program automatically
- FALSE ♦ It does not execute an instruction till its result is required by an other instruction
- TRUE ♦ The program is described by a precedence graph

Which of the following arbitration procedures are centralized?

X

Which statements are true for the SRAM, and which ones for the DRAM memory technologies?

	DRAM	SRAM
<b>Its content is lost when the power supply is switched off</b>	<input type="checkbox"/>	X
<b>Its content needs to be refreshed periodically</b>	<input type="checkbox"/>	X
<b>This has the larger data storage density</b>	<input type="checkbox"/>	<input type="checkbox"/>
<b>To store 1 bit, 6 capacitors are needed</b>	<input type="checkbox"/>	<input type="checkbox"/>

Your task is to give an event sequence, which fulfills **all** of the conditions below. The event sequence...

- covers at least 2 red edges,
- covers all green edges,
- covers **no** blue edges,
- covers all yellow edges,
- results in a 100% state coverage.

Give your answer in the field below. The events should be divided with a comma and a space.

*Example: If your answer is g, t, t, then provide "g, t, t" in the field (without quotation marks).*

**Attention!** The precheck only performs a syntactic check. It does not state anything about the correctness of your solution!

**Tip!** The precheck outputs the state configuration of the state machine and the values of the variables after executing the given event sequence. It might be useful to check its output.

Answer: (penalty regime: 0 %)

HIT

98·10<sup>9</sup> clock cycles for other purposes, too.

Answer:  X [100] ·10<sup>9</sup> clock cycles/sec

**Question 11**

Partially correct

Mark 1.25 out of 2.00

Flag question

Which signals of the PCI bus are shared (not dedicated) among the peripherals?

- TRUE ✓ The address and the data (A/D) lines
- TRUE ✓ The TRDY and IRDY lines used for the flow-control
- TRUE ✓ The FRAME line that indicates the end of the current transaction
- TRUE ✗ The REQ and the GNT lines used for the arbitration

**Information**

Flag question

A computer has a single-channel DRAM based system memory with 64 bit data units. The burst size is set to 8 data units. Let us ignore the presence of multiple banks and ranks.

The memory controller receives the following read requests, given by row and column coordinates

- (row 4, column 24), (row 1, column 0), (row 4, column 8)

**Question 12**

Not answered

Marked out of 3.00

Flag question

64 16 4 8 0 32 24 PRECHARGE SAVE ACTIVATE OPEN 192 LOAD CLOSE 1 READ 128

List the commands sent by the memory controller to the memory modules (in the right order) according to FCFS and FR-FCFS command scheduling, assuming that there can be a single row open at a time.

Row 1 is assumed to be in activated state initially. After the last command the memory controller does not close the active row. (3 points)

FCFS scheduling:

Command	Parameter
1: <span style="color: red;">✗</span> [PRECHARGE]	
2: <span style="color: red;">✗</span> [ACTIVATE] <span style="color: red;">✗</span> [4]	
3: <span style="color: red;">✗</span> [READ]	<span style="color: red;">✗</span>

FR-FCFS scheduling:

Command	Parameter
1: <span style="color: red;">✗</span> [READ]	<span style="color: red;">✗</span> [0]
2: <span style="color: red;">✗</span>	

20/21/2

Which phases of the instruction execution belong to the **backend** of the pipeline?

- TRUE ↗ The fetching of the instructions
- FALSE ↗ Putting the instructions to the instruction window
- TRUE ↗ Scheduling the instructions for execution to the appropriate functional unit
- FALSE ↗ The execution of the instructions

page

Next page

Which statements are true for the USB interface?

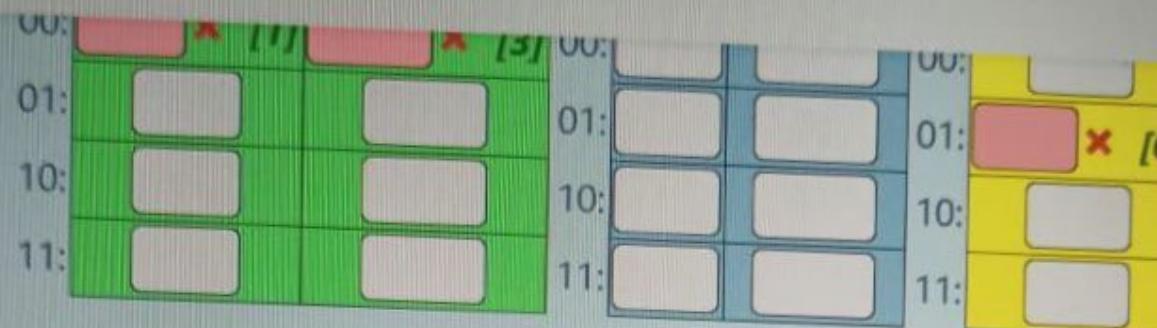
- It uses serial data transfer
- The components communicate with each other through dedicated point-to-point channels
- A serial (daisy chain-based) arbitration procedure is applied to select decide which master can use the bus
- TRUE  It does not support real interrupt handling, only polling

are many of such candidate blocks, it picks the least weared one.



Which of the following arbitration procedures are centralized?

- TRUE  Daisy chain-based arbitration
- TRUE  Parallel arbitration
- FALSE  Distributed arbitration
- FALSE  Collision detection-based arbitration



How many transistors are needed to store 18 bits in an SLC, in a MLC,

- In case of SLC: 18 ✓
- In case of MLC: 36 ✗ [9]
- In case of TLC: 54 ✗ [6]

A hard disk drive contains 2 double-sided platters, with 120000 tracks  
1500 sectors in each track. The size of the sectors is 500 byte. What is  
drive?

*Please enter only a number, without space, comma and dot characters!*

Capacity: 7360 ✗ [360] ·  $10^9$  byte



are many of such candidate blocks, it picks the least weared one.



## Architectures 2019/20/2



Which are the characteristics of the three cache organisations we have studied?

	Fully associative organization + LRU	N-way set associative organization + LRU	Direct mapped organization
The cache always contains the most recently used blocks of the memory	X		
The simplest and most power efficient solution out of the three		X	
Can be used with transparent cache addressing	X	X	X



Level 2 page tables:

V	Address
00:0	?
01:0	?
10:1	0
11:0	?
00:0	?
01:1	2
10:0	?
11:0	?
00:1	1
01:1	3
10:0	?
11:0	?
00:0	?
01:0	?
10:0	?
11:0	?

The questions are as follows:

- a) What is the theoretically maximal size of the entire page table (including level 1 and level 2 tables), given in bytes?
- b) How many pages does the virtual memory have?  16
- c) How many frames does the physical memory have?  4
- d) Where is
- page 6 located:  disk
  - page 9 located:  frame3
- (Possible answers: "disk", or "frame0", "frame1", etc. (without space), please enter the answer in this format to the answer field)
- d) Which page is located:  frame 0:2

**Question 9**

Answer saved

Marked out of  
2.00 Flag question

Which statements are true for the RISC, and which ones for the CISC instruction set architectures?

	CISC	RISC
Register-memory operations are also supported	X	
Nearly no redundancy		X
Variable instruction execution times	X	
Fixed length instruction encoding		X

**Question 1**Not yet  
answeredMarked out of  
2.00Flag  
question

Which of the following arbitration procedures are centralized?

- Daisy chain-based arbitration
- Parallel arbitration
- Distributed arbitration
- Collision detection-based arbitration

**Question 2**Not yet  
answeredMarked out of  
2.00Flag  
question

Which of the following statements are true for the logical/architectural registers?

- There are more logical/architectural registers in a CPU than physical registers
- The programmer can use these, instead of the physical registers
- They are hidden from the programmers
- The instruction set architecture specifies the number of them, and also their names

**Question 3**Not yet  
answeredMarked out of  
2.00Flag  
question

In our 5-stage pipeline, which of the following phases do useful (effective) work on an arithmetic instruction?

- EX (Execute)
- WB (Write Back)
- ID (Instruction Decode)
- MEM (Memory)

**Question 4**Not yet  
answeredMarked out of  
2.00Which phases of the instruction execution belong to the **backend** of the pipeline?

- The fetching of the instructions
- Putting the instructions to the instruction window

HIT

Question 4

Partially correct

Mark -0.25 out of 2.00

Flag question

What is the purpose of the garbage collection in SSD devices?

- TRUE ✘ ✗ To move the pages belonging to the same file next to each other to make read and write operations faster
- TRUE ✘ ✓ The creation of new erased blocks
- TRUE ✘ ✗ To increase the storage capacity by deleting the unnecessary files
- TRUE ✘ ✗ To remove the unnecessary electrons from the drive

Question 5

Partially correct

Mark 0.50 out of 2.00

Flag question

Which statements are true related to the information processing models?

- TRUE ✘ ✗ The flow-chart is a typical formalism to describe a problem in the demand-driven model
- TRUE ✘ ✓ The only way to express parallelism in the control-flow model is to use the FORKJOIN primitives
- TRUE ✘ ✓ The spread-sheets update the cells according to the data-flow model
- TRUE ✘ ✗ In the data-flow model, the precedence graph describing a program can contain only one single token

Question 6

Not answered

Marked out of 2.00

Flag question

What is the difference between the DMA controllers and the I/O processors?

Question 7

Not answered

Marked out of 2.00

Flag question

Enumerate the 5 most common DRAM commands!



a) How does the state of the SSD change when read requests arrive to LBA addresses **4**, **8** and **6**, accordingly. If a new write frontier is needed, select one that ensures the most balanced wearing of the blocks. When the number of erased blocks **after** a write operation decreases below 3, execute the garbage collection algorithm, potentially multiple times, till the number of erased block increases back to 3. The garbage collector always selects the block containing the most invalid pages. If there are many of such candidate blocks, it picks the least weared one.

<b>block 0</b>		<b>block 1</b>		<b>block 2</b>		<b>block 3</b>		<b>block 4</b>		<b>block 5</b>	
<b>block 6</b>		<b>block 7</b>									

Fill in only those fields that changed! (5 points)

→) Schedule the instructions for the given VLIW processor. Determine the content of the instruction groups and the time when the instruction groups can be executed. The number of instruction groups needed has to be minimal. When an instruction can be placed into multiple locations, always choose the earlier instruction to the functional unit having a lower id. (3p)

Instruction group:	MEM 1:	MEM 2:	INT 1:	INT 2:
1:			✗ [i1 or 1]	✗ [i5 or 5]
2:	✗ [i2 or 2]	✗ [i3 or 3]		✗ [i7 or 7]
3:				
4:				
5:			✗ [i4 or 4]	✗ [i6 or 6]
6:				

(All the instruction groups might not be needed)

Your answer is incorrect.