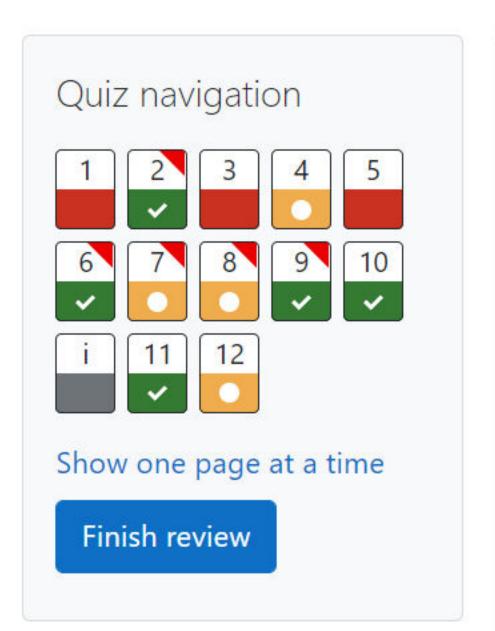
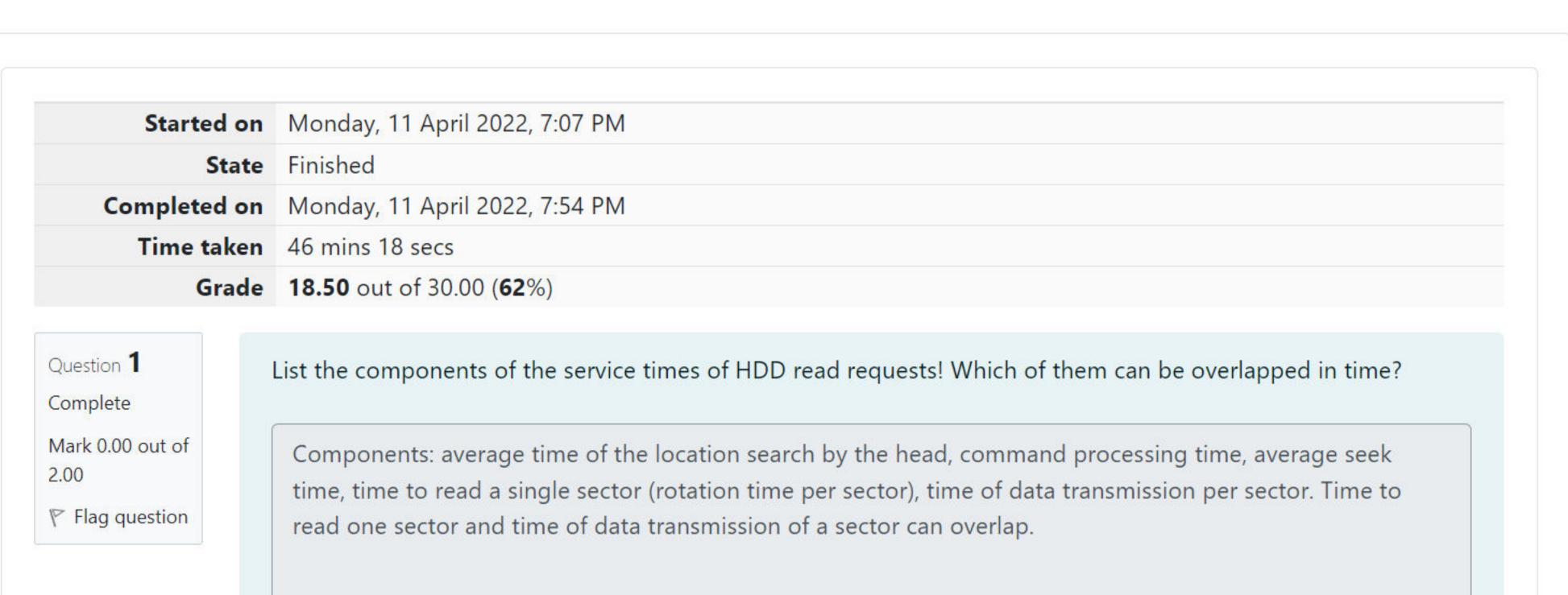
# Computer Architectures 2021/22/2





Comment:

Question 2

Complete

Mark 2.00 out of 2.00

Remove flag

What does the **TLB coverage** mean in virtual memory systems?

The amount of memory taken by pages which translational addresses are stored in the TLB.

Question 2

Complete

Mark 2.00 out of 2.00

Remove flag

What does the **TLB coverage** mean in virtual memory systems?

The amount of memory taken by pages which translational addresses are stored in the TLB.

Comment:

Question **3** 

Complete

Mark 0.00 out of 2.00

▼ Flag question

What are the main advantages of distributed arbitration algorithms over centralized ones?

Centralised ones might cause starvation of the devices that are at the back of the queuque, whereas distributed arbitration is based on priority of each device.

Comment:

Question **4** 

Partially correct

Mark 1.00 out of



Question 4

Partially correct

Mark 1.00 out of 2.00

♥ Flag question



Which USB data transfer mode do the following USB peripherals use (dominantly)?

	Mouse	Web cam	Pendrive
Interrupt transfer mode	X		
Isochronous transfer mode		X	
Bulk transfer mode			<b>X</b> [X]

Question **5** 

Incorrect

Mark 0.00 out of 2.00

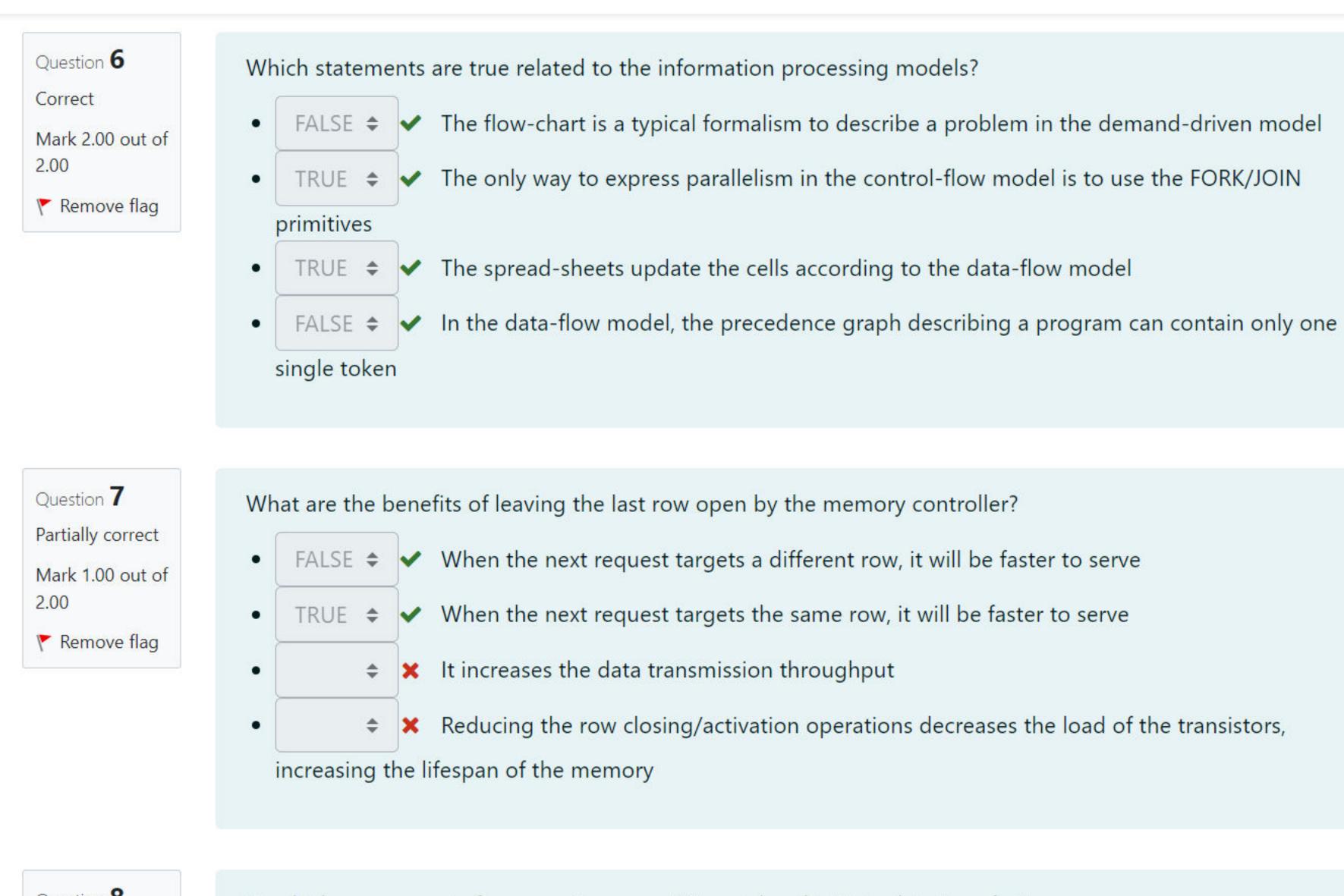
▼ Flag question



Indicate the properties of the write through and the write back cache write policies!

	Write back	Write through
The cache controller updates the main memory each time the cache content is modified	X X [blank]	<b>x</b> [X]
The cache is completely disabled for write operations		
The cache controller updates the main memory only when a cache block is evicted	× [X]	X × [blank]

Your answer is incorrect.



Question 8

Partially correct

Mark 0.50 out of 2.00

To which component of a computer can a PCI peripheral initiate data transfer?

• TRUE **♦** ✓ The system memory

Question 8

Partially correct

Mark 0.50 out of 2.00

Remove flag

Question 9

To which component of a computer can a PCI peripheral initiate data transfer?

- TRUE **♦** ✓ The system memory
- An other PCI peripheral
- A PCI Express peripheral

Correct

Mark 2.00 out of 2.00

▼ Remove flag

What is the purpose of the garbage collection in SSD devices?

- FALSE 
  To move the pages belonging to the same file next to each other to make read and write operations faster
- FALSE 

  ◆ To increase the storage capacity by deleting the unnecessary files
- FALSE 

  ◆ To remove the unnecessary electrons from the drive

Question 10

Correct

Mark 6.00 out of 6.00

▼ Flag question

A hard disk drive contains 4 double-sided platters, with 100000 tracks on each recording surface and with 1000 sectors in each track. The size of the sectors is 500 byte. There is no ZBR, and the speed of the data transmission interface is 200·10<sup>6</sup> byte/s. The command processing time is neglected, because it is very low. The average seek time is 7 ms, and the revolution speed is 4000 RPM.

a) The storage capacity of the hard disk drive, measured in  $10^9$  bytes, is: 400  $\checkmark$  ·10<sup>9</sup> byte (1 point)

Question 10

Correct

Mark 6.00 out of 6.00

▼ Flag question

A hard disk drive contains 4 double-sided platters, with 100000 tracks on each recording surface and with 1000 sectors in each track. The size of the sectors is 500 byte. There is no ZBR, and the speed of the data transmission interface is 200·10<sup>6</sup> byte/s. The command processing time is neglected, because it is very low. The average seek time is 7 ms, and the revolution speed is 4000 RPM.

- a) The storage capacity of the hard disk drive, measured in  $10^9$  bytes, is: 400  $\checkmark$  · $10^9$  byte (1 point)
- b) The full revolution time of the disk, given in ms, is: 15 ms (1 point)
- c) How long does it take to read one sector from the recording surface, given that the head is at the appropriate position (it points to the beginning of the sector): 0.015 

  ms (1 point)
- d) How long does it take to transmit one sector on the data transmission interface? (in ms) 0.0025 w ms (1 point)
- e) How much slower is the full service time of a request for 100 consecutive sectors than the full service time of a request for 1 sector? (2 point)

The answer is: 1.485 ✓ ms

f) We would like to increase the rotation time from 4000 RPM to 6000 RPM. What should be the new seek time, which ensures that the full service time of 1 sector remains the same with the higher rotation speed?

The answer is: 9.505 

ms

Your answer is correct.

Information

A computer has a single-channel DRAM based system memory with 64 bit data units. The burst size is set to 8

Information

♥ Flag question

A computer has a single-channel DRAM based system memory with 64 bit data units. The burst size is set to 8 data units.

The memory controller receives the following read requests, given by row and column coordinates

• (row 8, column 4), (row 2, column 24), (row 2, column 16)

Question 11

Correct

Mark 3.00 out of 3.00

♥ Flag question



List the commands sent by the memory controller to the memory modules (in the right order) according to FCFS and FR-FCFS command scheduling, assuming that there can be a single row open at a time.

Initially, row 2 is open in the DRAM bank. After the last command the memory controller **does not close** the active row. (3 points)

#### FCFS scheduling:

	Command	Parameter
1:	PRECHARGE	
	~	
2:	ACTIVATE	8
	~	~
٠.	READ	4
3.		

#### FR-FCFS scheduling:

	Command	Parameter
1:	READ	24
	>	~
2:	READ	16
	<b>&gt;</b>	~
•	PRECHARGE	

## FCFS scheduling:

	Command	Parameter
1:	PRECHARGE	
	<b>&gt;</b>	
2:	ACTIVATE	8
	~	<b>~</b>
3:	READ	4
	<b>~</b>	<b>~</b>
4:	PRECHARGE	
•	<b>~</b>	
5:	ACTIVATE	2
	<b>✓</b>	<b>~</b>
5:	READ	24
<b>)</b> :	<b>~</b>	<b>~</b>
7:	READ	16
	<b>&gt;</b>	~
3:		
9:		

### FR-FCFS scheduling:

	Command	Parameter
1:	READ	24
	<b>&gt;</b>	~
2:	READ	16
۷.	<b>&gt;</b>	~
2.	PRECHARGE	
3:	<b>&gt;</b>	
4:	ACTIVATE	8
4.	<b>~</b>	~
5:	READ	4
	<b>~</b>	~
6:		
7:		
8:		
9:		

(You might not need all lines.)

(You might not need all lines.)

Your answer is correct.

Question 12

Partially correct

Mark 1.00 out of 3.00

▼ Flag question

Given the DRAM technologies provided by the table, in which clock cycle does the first data appear on the data lines of the memory module for the request (row 4, column 24), measured in clock cycles (part a), and measured in nanoseconds (part b)? The timing parameters are given in format  $T_{CAS} - T_{RCD} - T_{RP}$ , where  $T_{RP}$  is the delay of the PRECHARGE command,  $T_{RCD}$  is the row activation delay, and  $T_{CAS}$  is the column latency, all of them given in (external) clock cycles. (Write only a singe number into the fields!) (3 points)

Technology	(a) Time t	ill the response, in cycles	(b) Time till re	sponse, in ns
DDR2-800, 5-5-5	15	<b>~</b>	×	[37.5 or 37,5]
DDR3-1600, 7-8-8	23	<b>~</b>	×	[28.75 or 28,75]
DDR3-2000, 11-13-13	37	<b>~</b>	×	[37]

Your answer is partially correct.