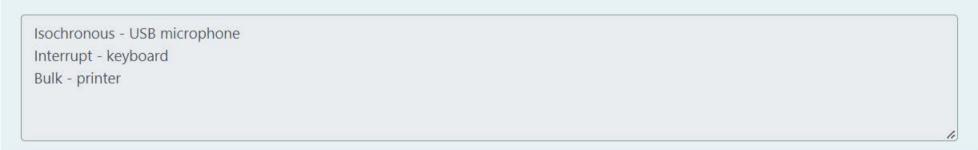
	h
Comment:	
Why is it necessary to refresh the content of the DRAM cells periodically?	
To preserve the stored data	

List a specific USB peripheral that predominantly uses isochronous data transfer mode, an other that uses interrupt data transfer mode, and a third one that uses bulk data transfer mode!

Please write the three answers to different lines. Indicate clearly which peripheral uses which data transfer mode.



## Comment:



When can an operation be executed in the three information processing model we have studied?

	Contr	ol-driven model	Data-flow model	Demand-driven model
When its result is needed				X
When the control token reaches it	X	<b>)~</b>		
When all of its operands are available			X	

Which properties do the MLC NAND, and the SLC NAND flash based SSD drives have?

	MLC		SLC	
The data unit of reading is the page and the data unit of erasing is the block	X	~		<b>X</b> [X]
In its transistors, more than two levels of change is distinguished	X	~		
Stores more data with the same number of transistors		<b>×</b> [X]	X	K [blank
From the two, this one survives more programming/erasing cycles			X	/

Which statements hold true for the fully associative cache organization, managed by LRU cache replacement policy?

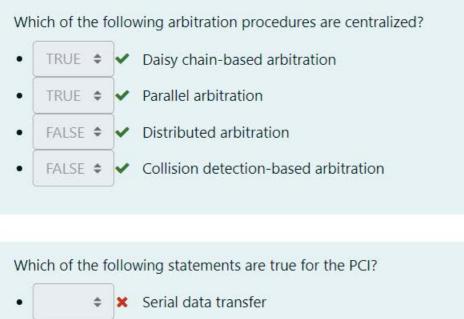
- FALSE 

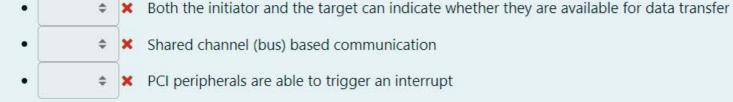
  ◆ Only a single comparator is being used for every cache look-up
- FALSE The cache tags are shorter than in case of the direct mapped organization
- TRUE 

  ◆ Any block can be placed anywhere in the cache memory

Why is it beneficial to enqueue the read/write requests in the buffer of the HDD instead of the buffer of the operating system?

- Because this way the hard disk can process more important requests before the others
- Because this way the hard disk can process the short requests requests before the longer ones
- Because this way the hard disk can process those requests that are fast to serve before the others
- Because this way the hard disk can process those requests that need no row activation before the others





A hard disk drive contains 2 double-sided platters, with 50000 tracks on each recording surface and with 500 sectors in each track. The size of the sectors is 500 byte. There is no ZBR, and the speed of the data transmission interface is 100·10<sup>6</sup> byte/s. The command processing time is neglected, because it is very low. The average seek time is 5 ms, and the revolution speed is 6000 RPM-

- a) The storage capacity of the hard disk drive, measured in 10<sup>9</sup> bytes, is: [50] ·10<sup>9</sup> byte (1 point)
- b) The full revolution time of the disk, given in ms, is:
- c) How long does it take to read one sector from the recording surface, given that the head is at the appropriate position (it points to the beginning of the sector): 

  [0.02 or or 0,02] ms (1 point)
- d) How long does it take to transmit one sector on the data transmission interface? (in ms) (1 point)
- e) How much slower is the full service time of a request for 100 consecutive sectors than the full service time of a request for 1 sector? (2 point)
- The answer is: **x** [1.98 or 1,98] ms
- f) We would like to slow down the rotation time from 6000 RPM to 4000 RPM. What should be the new seek time, which ensures that the average full service time of 1 sector remains the same with the slower rotation speed?

The answer is: **2.49 or 2,49**] ms

A computer has a single-channel DRAM based system memory with 64 bit data units. The burst size is set to 8 data units.

The memory controller receives the following read requests, given by row and column coordinates

• (row 2, column 24), (row 6, column 8), (row 6, column 16)



List the commands sent by the memory controller to the memory modules (in the right order) according to FCFS and FR-FCFS command scheduling, assuming that there can be a single row open at a time.

Initially, row 6 is open in the DRAM bank. After the last command the memory controller has to leave the active row open. (3 points)

## FCFS scheduling:

	Command	Parameter
1:	PRECHARGE	
1.	~	
2:	ACTIVATE	2
۷.	~	2
3:	READ	24
٥.	~	24
4:	PRECHARGE	2 ×
4.	~	[blank]
5:	ACTIVATE	6
Э.	~	0
6:	READ	8
0.	~	0
7:	READ	16
7.	~	16
8:		
9:		

## FR-FCFS scheduling:

	Command		Parameter		
1:	ACTIVATE	×	6	×	
	[READ]		[8]		
2:	READ		8	×	
	READ		[16]		
3:	READ	×	16	×	
	[PRECHARGE]		[blank]		
4:	PRECHARGE	×		×	
	[ACTIVATE]		[2]		
5:	ACTIVATE	×	2	×	
	[READ]		[24]		
6:	READ	×	24	×	
0.	[blank]		[blank]		
7:					
8:		]			
9:		ĺ			

Assuming DDR3-2800 DRAM technology (with 64 bit wide data units and burst size of 8), answer the following questions with a single number for each!

a) The internal clock frequency of the memory is (in MHz): (350) MHz

b) The number of internal clock cycles needed to transmit one full burst: 

[1] cycles

c) The data transfer speed during the transmission of the burst (in MB/s): 

[22400 or 22 400 or 22 400 or 22 400] MB/s