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3.1 What general categories of functions are specified by computer instructions?

Processor-Memory: data may be transferred from Processor to memory or from memory to processor.

Processor I/O: data may be transferred to or from a peripheral device by transferring between the Processor and I/O module.

Data Processing: the Processor may perform some ALU operation on data.

Control: An instruction may specify that the sequence of execution be altered.

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3.2 List and briefly define the possible states that define an instruction execution.

Instruction address Calculation: determine the address of the next instruction to be executed

- **Instruction Fetch:** Read instruction from its memory location into the Processor.
- **Instruction operation decoding:** Analyze instruction to determine the type of operation to be performed and operands to be used.
- **Operand address Calculation:** if the operation involves reference to an operand in memory or available via I/O, then determine the address of the operands.
- **Operand fetch:** Fetch the operand from memory or from I/O
- **Data Operation:** Perform the operation indicated in the instruction
- **Operand Store:** Write the result into memory or out to I/O

3.3 List and briefly define two approaches to dealing with multiple interrupts.

- **disabling interrupts:** the Processor has the ability to enable and disable specific interrupts those remain pending and will be checked after the Processor has enabled interrupts.
- **Interrupt Service Routine (ISR):** Priorities assigned to the different types of interrupt ISRs with higher priorities can interrupt ones with lower priority, in which case the ISR with the lower priority is put on the stack until that ISR is completed.

3.4 What types of transfers must a computer's interconnection structure (e.g., bus) support?

- **Memory to Processor:** the Processor reads an instruction or a unit of data from memory
- **Processor to Memory:** the Processor writes a unit of data to a memory
- **I/O to Processor:** the Processor reads data from an I/O device via an I/O module
- **Processor to I/O:** the Processor sends data to the I/O device
- **I/O to or from Memory:** for these two cases, an I/O module is allowed to exchange data directly with memory, without going through the Processor using direct memory access

3.5 List and briefly define the QPI protocol layers.

- Physical: Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission of the IS and OS
- Link: responsible for reliable transmission and flow control
- Routing: provides the framework for directing packets through fabric.
- Protocol: the high level set of rules for exchanging packets data between devices

3.6 List and briefly define the PCIe protocol layers.

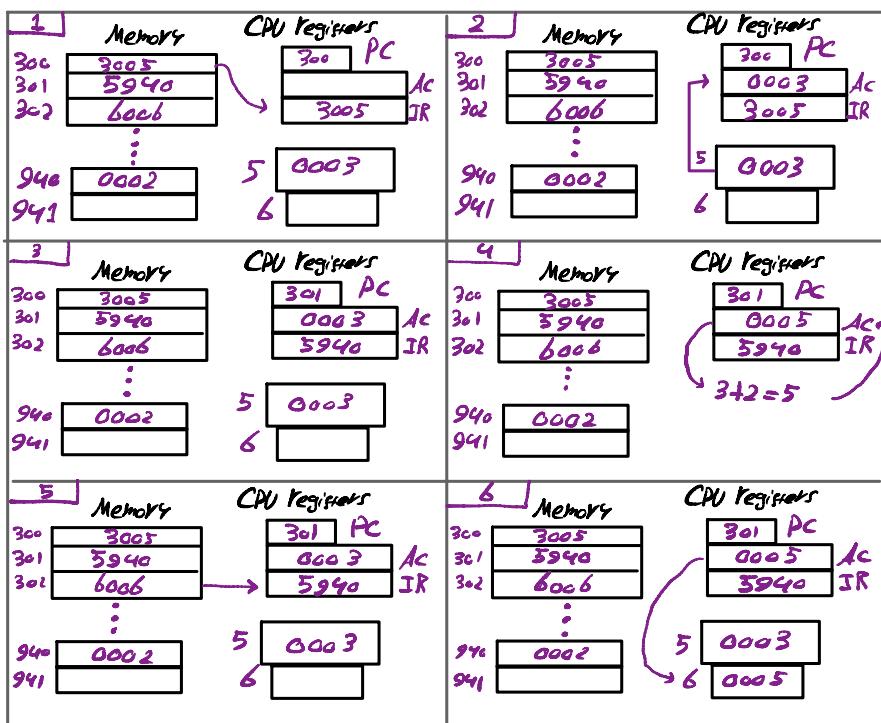
- Physical: consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission of the IS and OS
- Data Link: responsible for reliable transmission and flow control
- Transmission: generates and consumes data packets used to implement load/store data transfer mechanisms and also manages the flow control of those packets between the components on a link.

3.7 The hypothetical machine of Figure 3.4 also has two I/O instructions:

0011 = Load AC from I/O
0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

1. Load AC from device 5.
2. Add contents of memory location 940.
3. Store AC to device 6. Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.



3.8 The program execution of Figure 3.5 is described in the text using six steps.
Expand this description to show the use of the MAR and MBR.

- 1) a. The PC Contains 300, the Address of the First instruction this value is loaded in to the MAR.
 b. the Value in location 300 (which is the instruction with the Value 3940) is loaded into the MBR and the PC is incremented these two Steps can be done in Parallel.
 C. the Value in the MBR is loaded into the IR.
- 2) a. the address Portion of the IR (940) is loaded into the MAR.
 b. the Value in location 940 is loaded into the MBR.
 C. the Value in the MBR is loaded into the AC
- 3) a. the Value in PC (301) is loaded into the MBR.
 b. the Value in location 301 (which is the instruction with the Value 3941) is loaded into the MBR and the PC is incremented
 C. the Value in the MBR is loaded into the IR
- 4) a. the address Portion 940 is loaded into the MBR.
 B. the Value in location 940 is loaded into the MBR.
 C. the Old Value of the AC and the Value of location MBR are added and the result is stored in the AC.
- 5) A. the Value in PC (302) is loaded into the MBR.
 B. the Value in location 302 (which is the instruction with the Value 3941) is loaded into the MBR and the PC is incremented
 C. the Value in the MBR is loaded into the IR
- 6) A. the address Portion of IR (941) is loaded into the MAR.
 b. the Value in the AC is loaded into the MBR.
 C. the Value in the MBR is stored in location 941.

3.9 Consider a nested interrupt processing, with three I/O devices: a printer, a communication line, and a scanner. The interrupt priorities are as 2, 4 and 6. A user program begins at $t = 0$. Printer interrupt occurs at $t = 5$, a communications line interrupt occurs at $t = 10$, and a scanner interrupt occurs at $t = 15$. Having common interrupt time of 10 sec. Calculate the starting and ending time for each interrupt.

