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AN-6093

Design Guideline for Flyback Charger Using FAN104WMX

1.Introduction

More than half of the external power supplies produced are used for portable electronics, such as: smart phones, tablets, and MP3 players that require constant output voltage and current regulation for battery charging. For applications requiring precise Constant-Current (CC) regulation, current sensing in the secondary side is always necessary, which results in sensing loss. For power supply designers faced with stringent energy-efficiency regulations, output current sensing is a design challenge.

The advanced PWM controller FAN104W can alleviate the burden of meeting international energy efficiency regulations in charger designs. The FAN104W uses a proprietary Primary-Side Regulation (PSR) technique where the output current is precisely estimated with only the information in the primary side of the transformer and controlled with an internal compensation circuit. This removes the output current sensing loss and eliminates all external current-control circuitry, facilitating a higher efficiency power supply design without incurring additional costs. A Green-Mode function with an extremely low operating current (600 µA) for lower standby power (<30 mW) and frequency reduction maximizes the light-load efficiency, enabling conformance to worldwide Standby Mode efficiency guidelines. The FAN104W provides self-protection functions, including V_{DD} Over-Voltage-Protection (VDD OVP), Over-Temperature-Protection (OTP), V_S Over-Voltage Protection (V_S OVP), CS pin short-circuit protection, and VS pin single-fault protection. The VDD OVP, brownout protection, VS pin single-fault protection, and CS pin short-circuit protection are implemented as Auto-Restart Mode. The V_S OVP and internal OTP are implemented as Latch Mode.

This application note presents practical design considerations for flyback battery chargers employing the FAN104W. It includes instructions for designing the transformer and output filter, selecting the components, and implementing Constant Current (CC) / Constant Voltage (CV) control. The design procedure is verified through an experimental prototype converter. Figure 1 shows a typical application circuit of a flyback converter using the FAN104W.

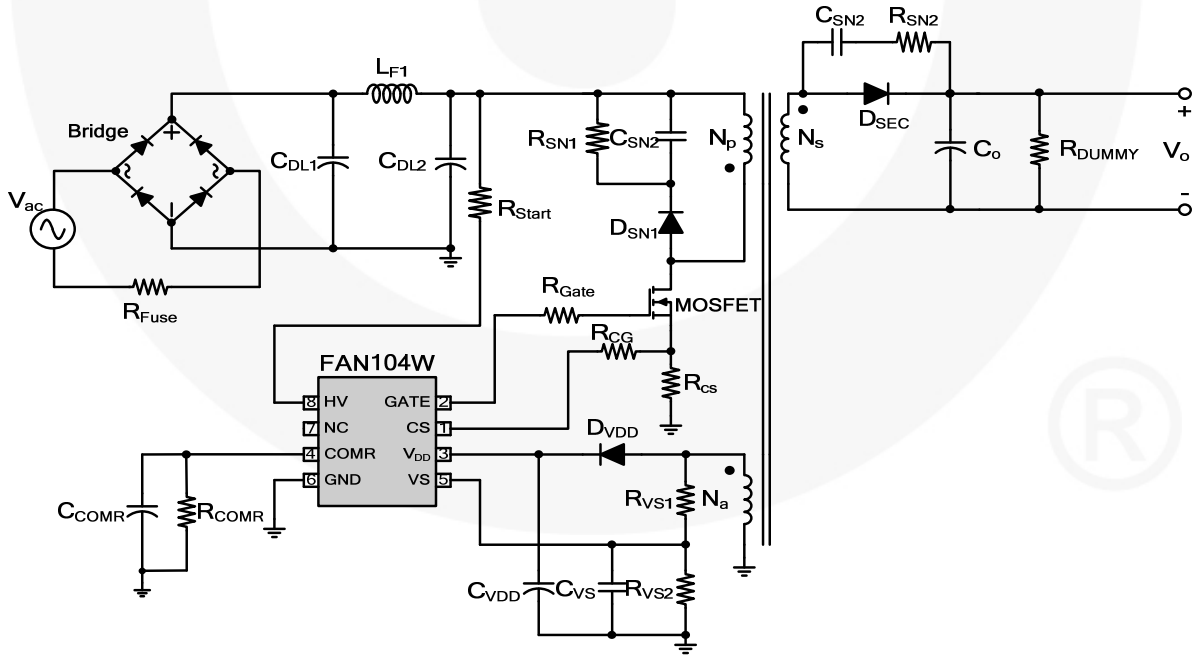

Figure 1. Typical Application Circuit

2.Operation Principles

Basic CV / CC Control Principle

Figure 2 shows the basic circuit diagram of a PSR flyback converter with typical waveforms shown in Figure 4 Generally, Discontinuous Conduction Mode (DCM) or Boundary Conduction Mode (BCM) operation is preferred for primary-side regulation because it allows better output regulation.

Constant Voltage (CV)

When the rectifier diode current reaches zero, the transformer auxiliary winding voltage (V_{Aux}) begins to oscillate by the resonance between the primary-side inductor (L_m) and the effective capacitor loaded across MOSFET. For BCM operation, this period does not exist.

During the rectifier diode conduction time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as $(V_o+V_F) \times N_{Aux} / N_s$. Since the diode forward-voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time, where the diode current diminishes to zero. By sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (V_{sah}) compares the sampled voltage with internal precise reference to generate an error voltage ($V_{EA.V}$), which determines the duty cycle of the MOSFET in CV Mode.

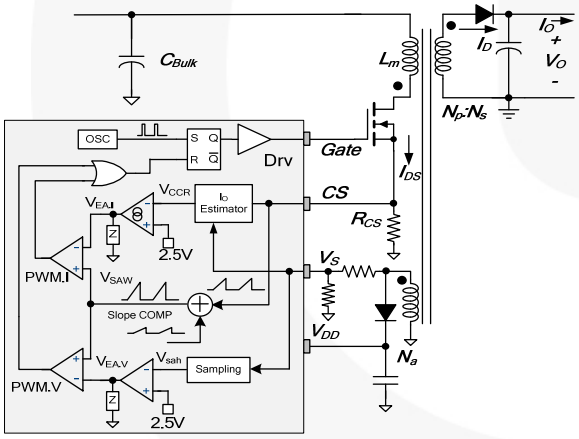

Figure 2. Simplified PSR Flyback Converter Circuit

Constant Current (CC) Regulation

CC regulation is implemented internally without directly sensing the output current. The output current estimator reconstructs output current information (V_{CCR}) using the transformer primary-side current and diode current discharge time. V_{CCR} is then compared with a reference voltage (2.5 V) by an internal error amplifier and generates a $V_{EA.I}$ signal to determine the duty cycle.

$V_{EA.I}$ and $V_{EA.V}$ are compared with an internal sawtooth waveform (V_{SAW}) by PWM comparators PWM.I and PWM.V, respectively, to determine the duty cycle. As seen in Figure 2, the outputs of two comparators (PWM.I and PWM.V) are combined with the OR gate and used as a reset signal of flip-flop to determine the MOSFET turn-off instant. The lower signal, $V_{EA.V}$ or $V_{EA.I}$, determines the duty cycle, as shown in Figure 3.

During CV regulation, $V_{EA.V}$ determines the duty cycle while $V_{EA.I}$ is saturated to HIGH. During CC regulation, $V_{EA.I}$ determines the duty cycle while $V_{EA.V}$ is saturated to HIGH.

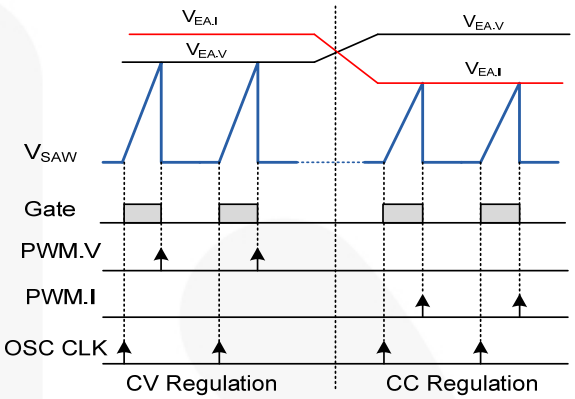

Figure 3. PWM Operation for CV and CC Modes

FAN104W internal circuits identifies the peak value of the drain current with a peak-detection circuit and calculates the output current using the inductor discharge time (t_{DIS}) and switching period (t_S). This output information (V_{CCR}) is compared with an internal precise reference to generate an error voltage ($V_{EA.I}$), which determines the duty cycle of the MOSFET in CC Mode. With Fairchild's innovative TRUECURRENT®, technique (CC) output can be precisely controlled. Meanwhile, the output current is obtained by averaging the triangular output diode current area over a switching cycle, as calculated by:

$$I_O = I_D{}^{AVG} = \frac{1}{2} \cdot I_{PK} \cdot \frac{N_P}{N_S} \cdot \frac{t_{DIS}}{t_S} \quad (1)$$

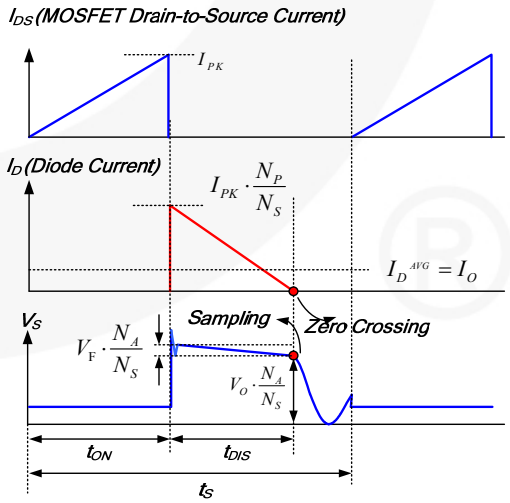

Figure 4. Key Waveforms of DCM Flyback Converter

BCM Operation Function

FAN104W allows BCM operation for better conversion efficiency and low standby power design margin. BCM function the next cycle turn-on of the MOSFET until discharge time (t_{DIS}) on VS pin is obtained, as shown in Figure 5. To utilize BCM operation, FAN104W prohibits the turn-on of the next switching cycle for 10% of its switching period after discharge time (t_{DIS}) is obtained. In Figure 5, the first switching cycle has discharge time (t_{DIS}) before 90% of its original switching period and, therefore, the turn-on instant of the next cycle is determined by its original switching period without being affected by the discharge time (t_{DIS}) point.

The second switching cycle does not have discharge time (t_{DIS}) points by the end of its original switching period. The turn-on of the third switching cycle occurs after the discharge time (t_{DIS}) point is obtained, with a delay of 10% of its original switching period. The minimum switching frequency that BCM allows is 10 kHz ($f_{OSC-BCM}$). If the discharge time point is not given until the end of the maximum switching period of 100 µs (10 kHz), the converter can enter CCM operation, losing output regulation.

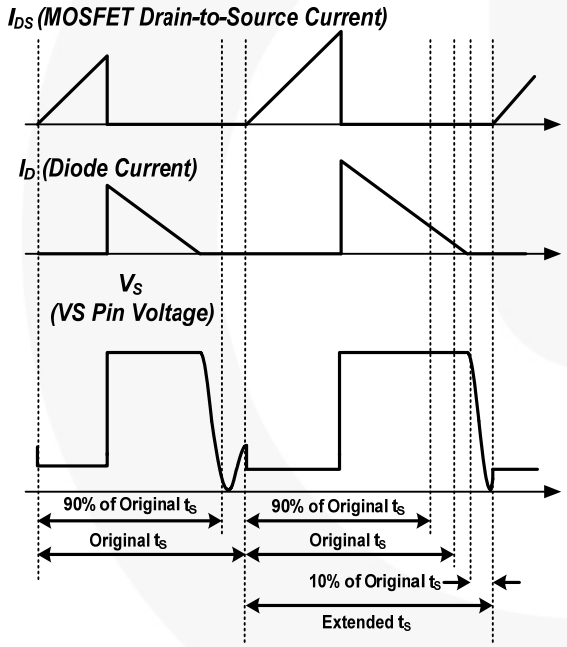

Figure 5. BCM Operation Function Waveform

Green-Mode Operation in CV Mode

The FAN104W uses a voltage regulation error amplifier output (COMV) as an indicator of the output load and modulates the PWM frequency as shown in Figure 6 and Figure 7. The switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is fixed at 85 kHz. Once COMV decreases below ~2.9 V, the PWM frequency linearly decreases from 85 kHz. When FAN104W enters Deep Green Mode, the PWM frequency is reduced to a minimum frequency $f_{OSC-N-MIN}$ of 1.2 kHz, gaining power saving to help meet international power conservation requirements.

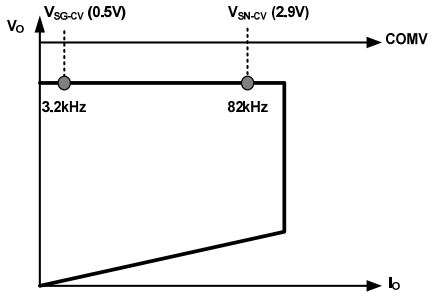

Figure 6. Frequency Reduction with COMV

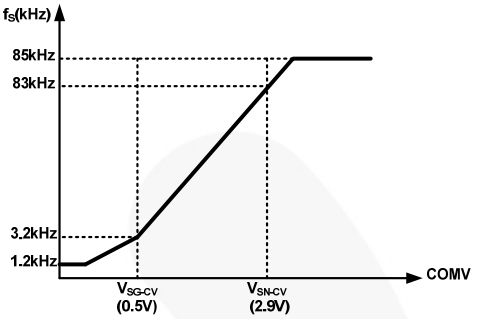

Figure 7. Frequency Reduction Curve in CV Mode

Frequency Reduction in CC Mode

During CC Mode, if frequency is being fixed; MOSFET conduction t_{ON} time reduces slightly as the output voltage drops, making peak current detection difficult. The discharge time (t_{DIS}) of diode current increases as the output voltage decreases, which increases AC ripple in deep BCM operation. To prevent these two conditions as output voltage drops, the FAN104W decreases switching frequency as output voltage drops, as shown in Figure 8. FAN104W indirectly monitors the output voltage by the sample-and-hold voltage (EAV) of VS, which is taken from the diode current discharge time of the previous switching cycle. Figure 9 shows how the frequency reduces as the sample-and-hold voltage (EAV) of V_O decreases.

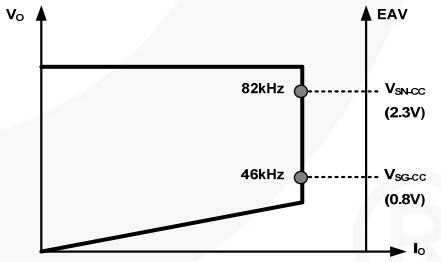

Figure 8. Frequency Reduction with EAV

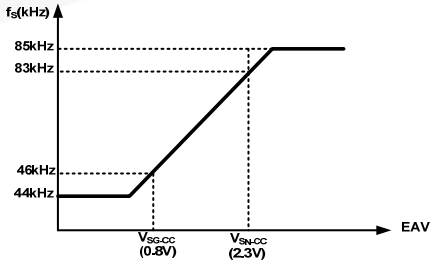

Figure 9. Frequency Reduction in CC Mode

3.Design Consideration

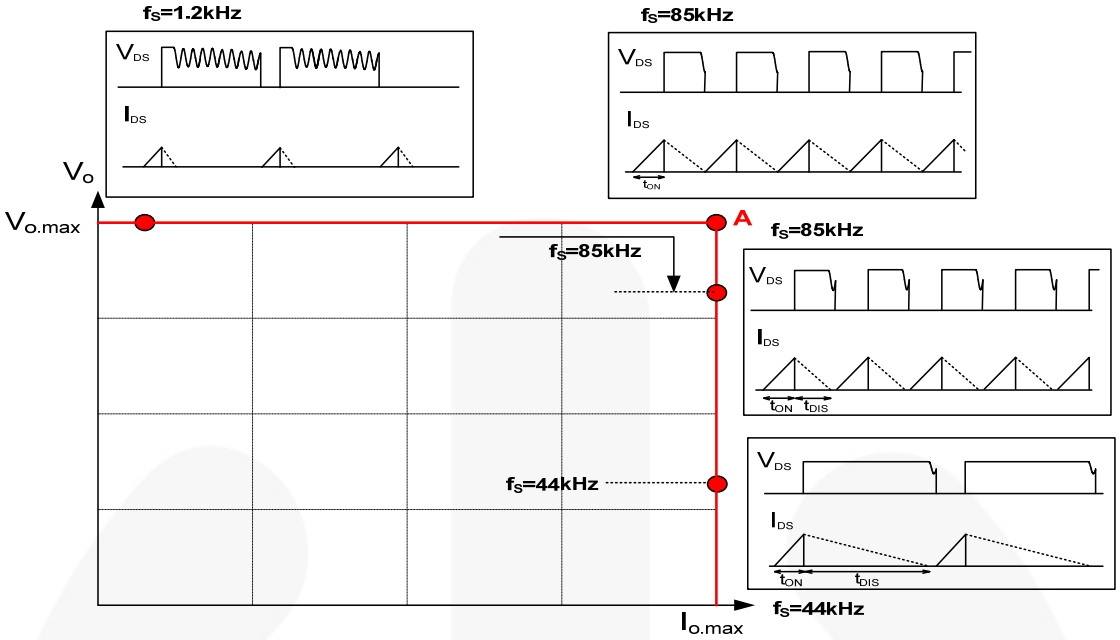

Figure 10. Operation Range of Charger with CC/CV

A battery charger power supply with CC output requires more design consideration than the conventional power supply with a fixed output voltage. In CC operation, the output voltage changes according to the charging condition of battery. The supply voltage for the PWM controller (V_{DD}), which is usually obtained from the auxiliary winding of the transformer, changes with the output voltage. Thus, the allowable V_{DD} operation range determines the output voltage variation range in CC regulation. FAN104W has a wide supply voltage (V_{DD}) operation range from 5 V up to 23 V, which allows stable CC regulation even with output voltage lower than a quarter of its nominal value.

Another important design consideration is primary inductance with BCM operation at maximum power point (point A), as seen in Figure 10. Setting the inductance value to operate in DCM with maximum switching frequency at point A can achieve proper conversion efficiency and lower standby power. For better efficiency and lower standby power, point A can be set to a lower frequency with BCM operation to obtain large inductance.

4.Design Procedure

In this section, a design procedure is presented using the Figure 11 as a reference. An offline charger with 5.0 V / 1.15 A output has been selected as a design example. The design specifications are:

- Line Voltage: 90 V_{AC}~264 V_{AC} , 50 Hz~60 Hz
- Nominal Output Voltage and Current: 5 V / 1.15 A
- Output Voltage Ripple: Less than 150 mV
- Minimum Output Voltage in CC Mode: 25% of Nominal Output (1.25 V)
- Maximum Switching Frequency(f_{OSC}): 85 kHz
- BCM Reduction Frequency ($f_{OSC@BCM}$): 80 KHz

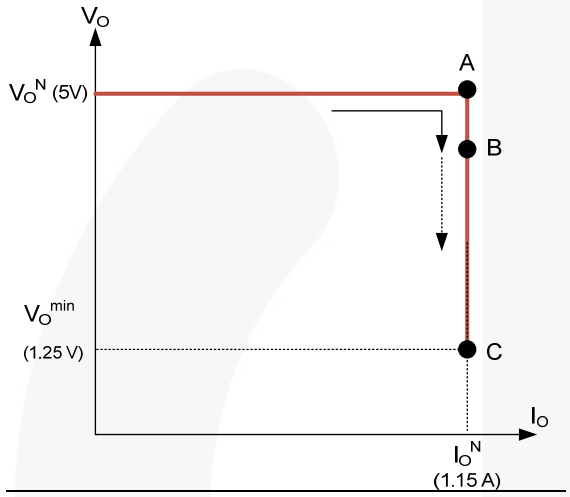

Figure 11. Output Voltage and Current Operating Area

[STEP-1] Estimate the Efficiencies

The charger application has output voltage and current that change over a wide range, as shown in Figure 11, depending on the charging status of the battery. Thus, the efficiencies and input powers of various operating conditions should be specified to optimize the power stage design. The critical operating points for design are:

- **Operating Point A**, where the output voltage and current reach maximum value (nominal output voltage and current) for primary inductance estimation.
- **Operating Point B**, where the frequency reduction starting point is in CC Mode.
- **Operating Point C**, where the output has its minimum voltage in CC Mode for auxiliary winding turns estimation.

Typically, low line at point A is the worst case for the transformer design since the largest duty cycle occurs at the minimum input voltage condition. As a first step, the following parameters should be estimated for low line.

- Estimated efficiency for operating point A ($E_{FF@A}$): The overall power conversion efficiency should be estimated to calculate the input power and maximum DC link voltage ripple. If no reference data is available, use the typical efficiencies in Table 1.
- Estimated primary-side efficiency (EFF.P) and secondary-side efficiency (EFF.S) for operating point A: Figure 12 shows the definition of primary-side and secondary-side efficiencies. The primary-side efficiency is for the power transferred from the AC line to the transformer primary side. The secondary-side efficiency is for the power transferred from the transformer primary side to the power supply output.

Since the rectifier diode forward voltage drop does not change much with its voltage rating, the conduction loss of output rectifier diode tends to be dominant for a low output voltage application. Therefore, the distribution of primary-side and secondary-side efficiencies changes with the output voltage. With a given transformer efficiency, the secondary- and primary-side efficiency, ignoring the diode switching loss, are given as:

$$E_{FF.S} \cong E_{FF.TX} \cdot \frac{V_O^N}{V_O^N + V_F} \quad (2)$$

$$E_{FF.P} = E_{FF} / E_{FF.S} \quad (3)$$

where $E_{FF.TX}$ is transformer efficiency, typically 0.95~0.98; V_O^N is the nominal output voltage; and V_F is the rectifier diode forward-voltage drop.

Table 1. Typical Efficiency of Flyback Converter

Output Voltage	Typical Efficiency at Minimum Line Voltage	
	Universal Input	European Input
3.3 ~ 6 V	65 ~ 70%	67 ~ 72%
6 ~ 12 V	70 ~ 77%	72 ~ 79%
12 ~ 24 V	77 ~ 82%	79 ~ 84%

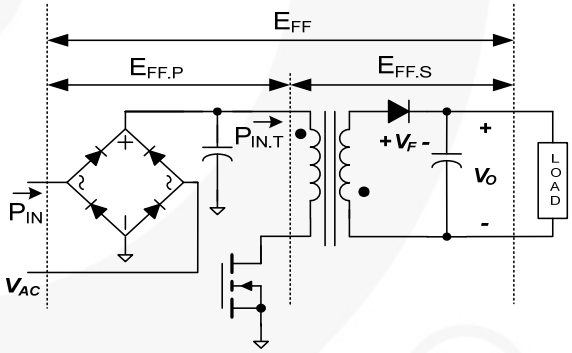

Figure 12. Primary-Side and Secondary-Side Efficiency

With the estimated overall efficiency, the input power at operating point A is given as:

$$P_{IN@A} = \frac{V_O^N I_O^N}{E_{FF@A}} \quad (4)$$

where V_O^N and I_O^N are the nominal output voltage and current, respectively.

The input power of transformer at operating point A is given as:

$$P_{IN.T@A} = \frac{V_O^N I_O^N}{E_{FF.S@A}} \quad (5)$$

(Design Example)

To maximize efficiency, a low-voltage-drop Schottky diode with a forward-voltage drops of 0.3 V is selected. Assuming the overall efficiency is 76% and the transformer efficiency is 95% at operating point A (nominal output voltage and current) for low line, the secondary-side efficiency is obtained as:

$$E_{FF.S@A} \cong E_{FF.TX} \cdot \frac{{V_O}^N}{{V_O}^N + V_F} = 95\% \cdot \frac{5}{5+0.3} = 0.8962$$

The input powers of the power supply and transformer at operating point A are obtained as:

$$P_{IN@A} = \frac{{V_O}^N {I_O}^N}{E_{FF@A}} = \frac{5.75}{0.76} = 7.56W$$

$$P_{IN.T@A} = \frac{{V_O}^N {I_O}^N}{E_{FF.S@A}} = \frac{5.75}{0.8962} = 6.416W$$

[STEP-2] Determine the DC Link Capacitor (C_{DL}) and the DC Link Voltage Range

It is typical to select the DC link capacitor as 2-3 µF per watt of input power for universal input range (90 - 264 V_{AC}) and 1 µF per watt of input power for European input range (195 ~ 265 V_{rms}). With the DC link capacitor chosen, the minimum DC link voltage is obtained as:

$${V_{DL@A}}^{\min} = \sqrt{2 \cdot ({V_{LINE}}^{\min})^2 - \frac{P_{IN@A}(1-D_{ch})}{C_{DL} \cdot f_L}} \quad (6)$$

where ${V_{LINE}}^{\min}$ is the minimum line voltage; C_{DL} is the DC link capacitor; f_L is the line frequency; and D_{ch} is the DC link capacitor charging duty ratio, defined as shown in Figure 13, which is typically about 0.2.

The maximum DC link voltage is given as:

$${V_{DL}}^{\max} = \sqrt{2} \cdot {V_{LINE}}^{\max} \quad (7)$$

where ${V_{LINE}}^{\max}$ is the maximum line voltage.

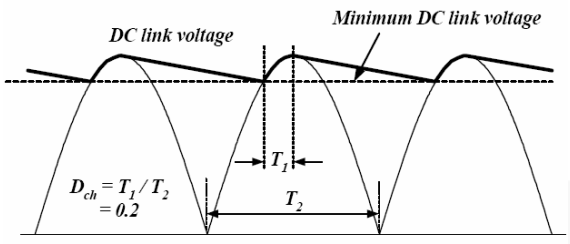

Figure 13. DC Link Voltage Waveforms

(Design Example)

By choosing two 6.8 µF capacitors in parallel for the DC link capacitor, the minimum and maximum DC link voltages for each condition are obtained as:

$${V_{DL@A}}^{\min} = \sqrt{2 \cdot ({V_{LINE}}^{\min})^2 - \frac{P_{IN@A}(1-D_{ch})}{C_{DL} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{7.56 \cdot (1-0.2)}{13.6 \times 10^{-6} \cdot 60}} = 93.7V$$

$${V_{DL}}^{\max} = \sqrt{2} \cdot 264 = 373V$$

[STEP-3] Determine Transformer Turns Ratio

Figure 14 shows the MOSFET drain-to-source voltage waveforms. When the MOSFET is turned off, the sum of the input DC link voltage (V_{DL}) and the output voltage reflected to the primary side is imposed across the MOSFET, calculated as:

$${V_{DS}}^{nom} = {V_{DL}}^{\max} + V_{RO} \quad (8)$$

where V_{RO} is reflected output voltage defined as:

$$V_{RO} = \frac{N_p}{N_s}({V_O}^N + V_F) \quad (9)$$

where N_P and N_S are number of turns for the primary side and secondary side, respectively.

When the MOSFET is turned on; the output voltage, together with input voltage reflected to the secondary, are imposed across the secondary-side rectifier diode calculated as:

$${V_D}^{nom} = \frac{N_S}{N_P}{V_{DL}}^{\max} + {V_O}^N \quad (10)$$

As observed in Equations (8), (9), and (10); increasing the transformer turns ratio (N_P / N_S) increases voltage stress on the MOSFET while reducing voltage stress on the rectifier diode. Therefore, the N_P / N_S should be determined by the trade-off between the MOSFET and diode voltage stresses.

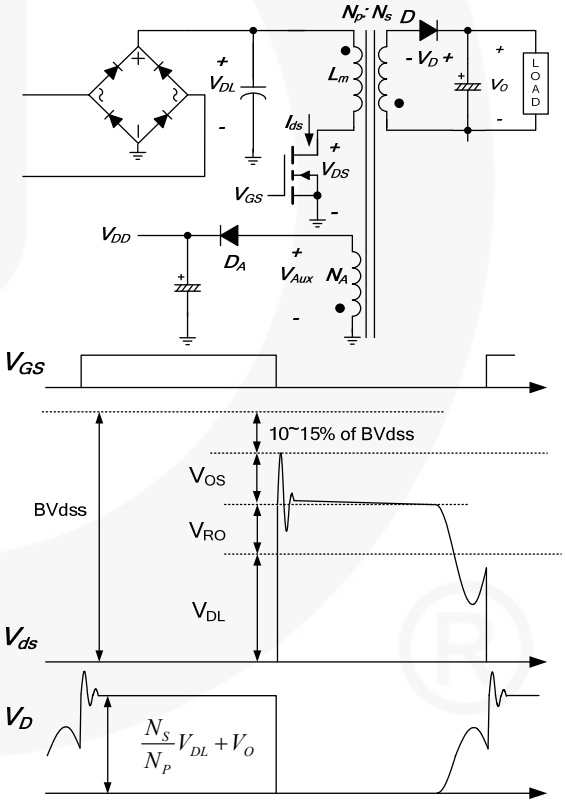

Figure 14. Voltage Stress on MOSFET and Diode

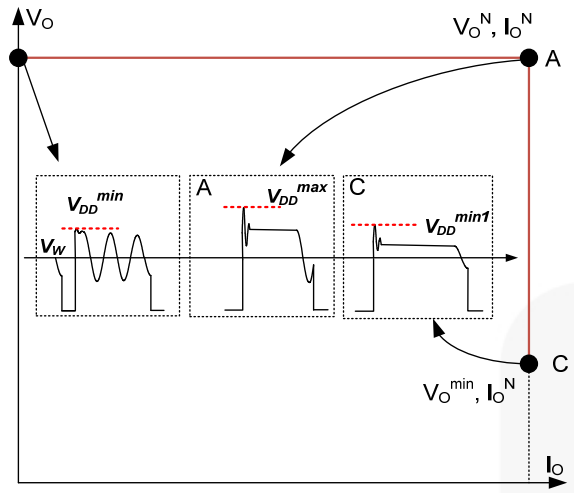

Figure 15. V_{DD} and Winding Voltage

The transformer turns ratio between the auxiliary winding and the secondary winding (N_A / N_S) should be determined by considering the allowable IC supply voltage (V_{DD}) range. The V_{DD} voltage varies with load condition, as shown in Figure 15, where the minimum V_{DD} typically occurs at minimum load condition. Due to the voltage overshoot of the auxiliary winding voltage caused by the transformer leakage inductance; the V_{DD} at operating point C tends to be higher than the V_{DD} at minimum load condition.

The V_{DD} at minimum load condition is obtained as:

$$V_{DD}^{\min} \cong \frac{N_A}{N_S}(V_O + V_F) - V_{FA} \quad (11)$$

where V_{FA} is the diode forward-voltage drop of the auxiliary winding diode. The transformer turns ratio should be determined such that the maximum V_{DD}^{min} is higher than the maximum V_{DD-OFF} UVLO voltage, calculated as:

$$\frac{N_A}{N_S}(V_O + V_F) - V_{FA} > V_{DD-OFF}^{\max} + V_{MRGN} \quad (12)$$

Since the V_{DD}^{min} is related to standby power consumption, smaller N_A / N_S leads to lower standby power consumption. However, 2~3 V margin (V_{MRGN}) is added in to Equation (12), considering the V_{DD} ripple caused by the PFM operation at no-load condition.

(Design Example)

For a 600 V MOSFET to have 10% margin on V_{DS}^{nom}, the reflected output voltage should be:

$$V_{DS}^{nom} = 373 + 2V_{RO} < 0.9 \times 600 = 540V$$
$$\therefore V_{RO} < 83.4V$$

N_P/N_S is obtained as:

$$\frac{N_P}{N_S} = \frac{V_{RO}}{(V_o + V_F)} = \frac{83.4}{5.30} = 15.74$$

N_P/N_S should be under 15.74.

Choose primary-to-secondary turn ratio of 13.2.

Then, the voltage stress of diode is obtained as:

$$V_D^{nom} = \frac{N_S}{N_P}V_{DL}^{\max} + V_O^N = \frac{10}{132} \times 373 + 5 = 33.26V$$

The allowable maximum V_{DD-OFF} is 5.5 V considering the tolerances of V_{DD-OFF}. Considering voltage ripple on V_{DD} caused by PFM operation at no-load condition, a 2 V margin is added for V_{DD} voltage calculation at no-load condition:

$$V_{DD}^{\min} = \frac{N_A}{N_S}(V_O + V_F) - V_{FA} > V_{DD-OFF}^{\max} + V_{MRGN}$$

$$\Rightarrow \frac{N_A}{N_S}(5 + 0.30) - 0.7 > 5.5 + 2$$

$$\therefore \frac{N_A}{N_S} > 1.547$$

where V_{FA}=0.7 V and V_{DD-OFF}^{max}=5.5 V.

To minimize the power consumption of the IC by minimizing V_{DD} at no-load condition, N_A/N_S is determined as 1.6.

[STEP-4] Current-Sensing Resistor Setting

Since the transformer primary-to-secondary turn ratio is determined in STEP-3, output current in CC Mode can be estimated from Equation (2) to obtain the current sensing resistor value as:

$$R_{CS} = \frac{1.25}{K} \cdot \frac{N_P}{N_S} \cdot \frac{1}{I_o} \quad (13)$$

where K is the design parameter of IC, which is 10.5.

(Design Example)

Nominal current is 1.15 A and transformer primary to secondary turn ratio is 13.2 as calculated by:

$$R_{CS} = \frac{1.25}{K} \cdot \frac{N_P}{N_S} \cdot \frac{1}{I_o} = \frac{1.25}{10.5} \cdot (13.2) \cdot \frac{1}{1.15} = 1.37\Omega$$

[STEP-5] Design the Transformer

For the transformer design, choose point A to operate in BCM by setting switching frequency for higher conversion efficiency and standby power design margin. 80 kHz is selected for larger primary inductance in the design example.

Then, the transformer primary-side inductance can be calculated as:

$$L_m = \frac{1}{2}\cdot\frac{1}{P_{IN@A}\cdot f_s}\cdot\left[\frac{V_{DL@A}^{\min}\cdot N_P/N_S\cdot V_O^{N}}{V_{DL@A}^{\min}+N_P/N_S\cdot V_O^{N}}\right]^2 \quad (14)$$

Once the transformer primary-side inductance is obtained, the maximum peak drain current can be calculated at the nominal output condition (operating point A) and current limit level (V_{STH}) can be calculated:

$$I_{DS}^{PK} = \sqrt{\frac{2P_{IN@A}}{L_m\cdot f_S}} \quad (15)$$

$$I_{OCP}^{PK} = \frac{V_{STH}}{R_{CS}} \quad (16)$$

The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P^{\min} = \frac{L_m I_{OCP}^{PK}}{B_{sat} A_e} \quad (17)$$

where Ae is the cross-sectional area of the core in m2 and B_{sat} is the saturation flux density in Tesla.

Figure 16 shows the typical characteristics of a ferrite core from TDK (PC40). Since the saturation flux density (B_{sat}) decreases as the temperature rises, the high-temperature characteristics should be considered, especially for a charger application in an enclosed case. If there is no reference data, use B_{sat}=0.30~0.35T. With the turns ratio obtained in STEP-3, determine the proper integer for N_S, such that the resulting N_P is larger than N_P^{min} obtained from Equation (17).

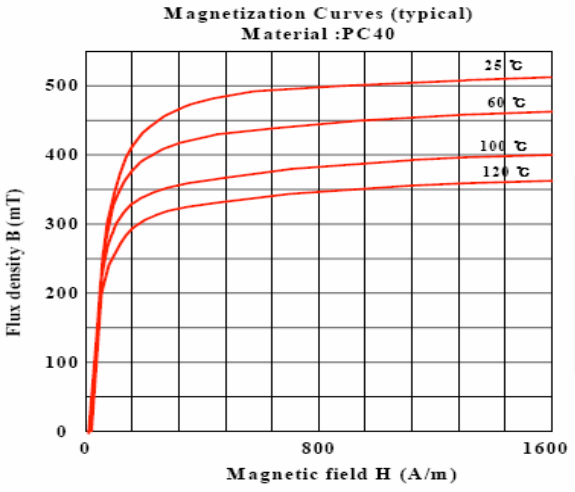

Figure 16. Typical B-H Curves of Ferrite Core (TDK/PC40)

(Design Example)

The transformer primary-side inductance is calculated as:

$$L_m = \frac{1}{2}\cdot\frac{1}{P_{IN@A}\cdot f_s}\cdot\left[\frac{V_{DL@A}^{\min}\cdot N_P/N_S\cdot V_O^{N}}{V_{DL@A}^{\min}+N_P/N_S\cdot V_O^{N}}\right]^2$$

$$= \frac{1}{2}\cdot\frac{1}{7.56\cdot 80\cdot 10^3}\cdot\left[\frac{93.7\times 13.2\times 5}{93.7+13.2\times 5}\right]^2$$

$$= 1.24mH$$

Chosen inductance is 1.2 mH.

The peak drain current at maximum load condition is given as:

$$I_{DS}^{PK} = \sqrt{\frac{2P_{IN@A}}{L_m\cdot f_S}} = \sqrt{\frac{2\cdot 7.57}{1.2m\cdot 80k}} = 391mA$$

The peak drain current in current limit level is given as:

$$I_{OCP}^{PK} = \frac{V_{STH}}{R_{CS}} = 474mA$$

where V_{STH} is the threshold for current limit.

EPC13 core is selected for the transformer (Ae= 12.5 mm^2) and the minimum number of turns for the transformer primary-side, to avoid core saturation is given by:

$$N_P^{\min} = \frac{L_m I_{OCP}^{PK}}{B_{sat} A_e} = \frac{1.2m\cdot 474m}{0.35\cdot 12.5\mu} = 130$$

Then, determine the proper integer for N_S, such that the resulting N_P is larger than N_P^{min}, as:

$$N_P = 13.2\times N_S$$

$$= 13.2\times 10 = 132 > N_P^{\min}$$

The auxiliary winding turns, N_A is obtained as:

$$N_A = \frac{N_A}{N_S}\times N_S = 1.6\times 10 = 16$$

[STEP-6] V_S Sensing Resistor Setting

The system suggests minimum on-time of the MOSFET is 400 ns for better standby power performance (<30 mW) at maximum line voltage. For this on-time, VS pin sources a current (900 µA) from the IC inside to the VS pin resistor. RVS1 and RVS2 are determined by the below equation:

$$R_{VS1} = \frac{1}{900\mu\left(\frac{N_A}{N_S}\left(\frac{V_O^{N}+V_F}{2.5}\right)-1\right)}\left[V_{DL}^{\max}\times\left(\frac{N_A}{N_P}\right)\left(\frac{N_A}{N_S}\left(\frac{V_O^{N}+V_F}{2.5}\right)-1\right)\right]$$

$$R_{VS2} = \frac{R_{VS1}}{\left(\frac{N_A}{N_S}\left(\frac{V_O^{N}+V_F}{2.5}\right)-1\right)} \quad (18)$$

A bypass capacitor of 10~20 pF placed closely between the VS and GND pins is recommended to bypass the switching noise. Too large a capacitor distorts V_S voltage and deteriorates the output current regulation. The RC time constant of the bypass capacitor and voltage divider resistor should be <10% of the switching period, given as:

$$\tau_{RC} = (R_{VS1} // R_{VS2})\cdot C_{VS} < \frac{1}{40f_S} \quad (19)$$

(Design Example)

The R_{VS1} and R_{VS2} is determined by equation:

$$R_{VS1}=\frac{1}{900\mu(\frac{N_A}{N_S}(\frac{V_O^N+V_F}{2.5})-1)}[V_{DL}^{\max}\times(\frac{N_A}{N_P})(\frac{N_A}{N_S}(\frac{V_O^N+V_F}{2.5})-1)]$$

$$R_{VS2}=\frac{R_{VS1}}{(\frac{N_A}{N_S}(\frac{V_O^N+V_F}{2.5})-1)}=23K\Omega$$

The bypass capacitor determined by 40 times the VS pin RC time constant:

$$C_{VS}<\frac{1}{40\cdot f_S\cdot(R_{VS1}//R_{VS2})}=18.5pF$$

Thus, a 18 pF capacitor is selected for C_{VS}.

[STEP-7] Design the RCD Clamping Circuit in the Primary Side

When the MOSFET in the flyback converter is turned off, a high-voltage spike is generated across the MOSFET due to the transformer leakage inductance. This excessive voltage can lead to an avalanche breakdown and, eventually, failure of the MOSFET. Therefore, an RCD clamping circuit must limit the voltage, as shown in Figure 17. The voltage overshoot (V_{OS}) is related to the power dissipation in the clamping circuit. Setting the voltage overshoot too low can lead to severe power dissipation in the clamping circuit. For reasonable clamping circuit design, voltage overshoot (V_{OS}) is typically 1~2 times the reflected output voltage.

It is typical to have a margin of 10~20% of the breakdown voltage for maximum MOSFET voltage stress. The maximum voltage stress of the MOSFET is given as:

$$V_{DS}^{max}=V_{DL}^{max}+V_{RO}+V_{OS} \quad (20)$$

When the drain voltage of the MOSFET reaches the voltage of node **X** (sum of DC link voltage and clamping capacitor voltage), the clamping diode is turned on to limit the drain voltage. It is assumed that the clamping capacitor is large enough that its voltage does not change significantly during one switching cycle.

For medium-power and high-power applications where the leakage inductance energy is much larger than the energy stored in the effective output capacitance of the MOSFET, the output capacitance of the MOSFET is generally ignored when designing the clamping circuit. However, for low-power applications where the leakage inductance energy is almost the same as, or smaller than, the energy stored in the effective output capacitance of the MOSFET, the output capacitance of the MOSFET should be considered for clamping circuit design. Especially for low-power applications of less than 10 W, the transformer typically has a large number of turns, resulting in large inter-winding capacitance. This significantly contributes to the effective output capacitance of the MOSFETs, affecting the operation of the clamping circuit.

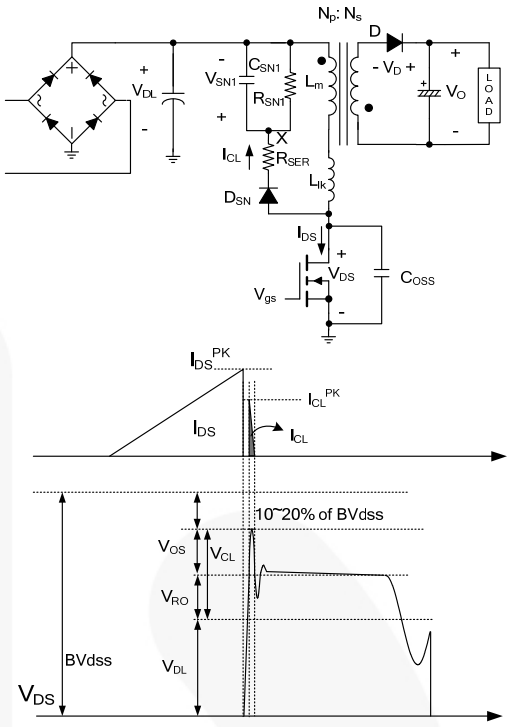

Figure 17. RCD Clamping Circuit and Waveforms

Considering the loading effect of the output capacitance of the MOSFET, the peak current of clamping circuit is given as:

$$I_{SN1}^{PK}=\sqrt{(I_{DS}^{PK})^2-\frac{C_{OSS}}{L_{LK}}V_{OS}^2} \quad (21)$$

where V_{OS} is the voltage overshoot of the drain voltage, as illustrated in Figure 17.

The power dissipated in the RCD network is given as:

$$P_{CLMP}=\frac{1}{2}f_S L_{LK}\cdot(I_{SN1}^{PK})^2\cdot\frac{V_{RO}+V_{OS}}{V_{OS}} \quad (22)$$

where I_{SN1}^{PK} is the peak clamping diode current at full load; L_{LK} is the leakage inductance.

Once the power dissipation in the snubber is obtained, the snubber resistor is calculated as:

$$R_{SN1}=\frac{(V_{RO}+V_{OS})^2}{P_{CLMP}} \quad (23)$$

where R_{SN1} is the clamping resistor.

The maximum ripple of the clamping capacitor voltage is obtained as:

$$\Delta V_{SN1}=\frac{V_{RO}+V_{OS}}{C_{SN1}R_{SN1}f_s} \quad (24)$$

In general, 5~10% ripple of the selected capacitor voltage is reasonable. The clamping capacitor should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable.

The leakage inductance measured with an LCR meter tends to be larger than the actual effective leakage inductance. Moreover, the effective output capacitance of the MOSFET is difficult to measure. The best way to obtain these

parameters correctly is to use the drain voltage waveform as illustrated in Figure 18. Since L_m can be measured with an LCR meter, C_{OSS} and L_{LK} can be calculated from the measured resonant period.

In the clamping design in this section, the lossy discharge of the inductor and stray capacitance is not considered. In the actual converter, the loss in the clamping network is less than the designed value due to this effect.

(Design Example)

Assuming a 600 V MOSFET is used, the voltage overshoot to limit the maximum drain voltage below 540 V is:

$$V_{OS} < 540V - V_{DL}^{\max} - V_{RO} = 90$$

The leakage inductance and the effective output capacitance of MOSFET are calculated from the resonance waveform as 23 μH and 19 pF, respectively.

The peak current of clamping diode is obtained as:

$$I_{SN1}^{PK} = \sqrt{(I_{DS}^{PK})^2 - \frac{C_{OSS}}{L_{LK}} V_{OS}^2} = 388mA$$

The power dissipation in the clamping circuit is obtained as:

$$P_{CLMP} = \frac{1}{2} f_S L_{LK} (I_{SN1}^{PK})^2 \frac{V_{RO} + V_{OS}}{V_{OS}} = 0.285W$$

Then the clamping circuit resistor is calculated as:

$$R_{SN1} = \frac{(V_{RO} + V_{OS})^2}{P_{CLMP}} = 97.8k\Omega$$

R_{SN1} is 100 kΩ.

The actual drain voltage can be lower than the design due to the loss of stray resistance of inductor and capacitor. The resistor value can be adjusted after the power supply is actually built.

To allow less than 40 V ripple on the clamping capacitor voltage, the clamping capacitor should be calculated as:

$$C_{SN1} > \frac{V_{RO} + V_{OS}}{\Delta V_{SN1} R_{SN1} f_s} = 502\,pF$$

A 470 pF capacitor is selected.

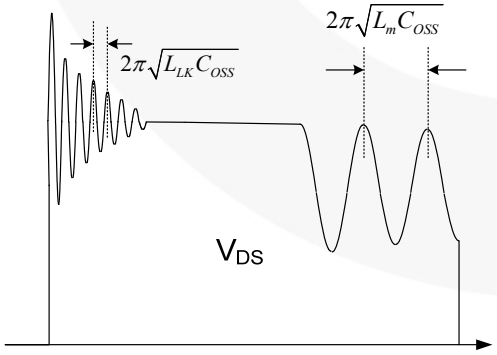

Figure 18. Drain Voltage Waveform

The output information is obtained by auxiliary winding in the PSR system. During the MOSFET off period, leading ringing on the V_S signal affects the determination of discharge time (t_{DIS}). The leading ringing time should be shorter than $t_{VS\text{-}BLANK}$ to prevent t_{DIS} error detection. Figure 19 shows two different ringing times of the V_S waveform. Figure 19(a) shows leading ringing time is shorter than $t_{VS\text{-}BLANK}$ with correct t_{DIS}. Figure 19(b) leading ringing is longer than $t_{VS\text{-}BLANK}$ with correct t_{DIS}. In Figure 19(a), discharge time is determined as t_{DIS2}, but (b) is t_{DIS1}. The leading ringing time of t_{DIS} is adjustable through a R_{SER} and D_{SN}, as shown in Figure 17. Higher R_{SER} lowers ringing time t_{DIS}. A higher recovery-time diode in DSN can lower ringing time.

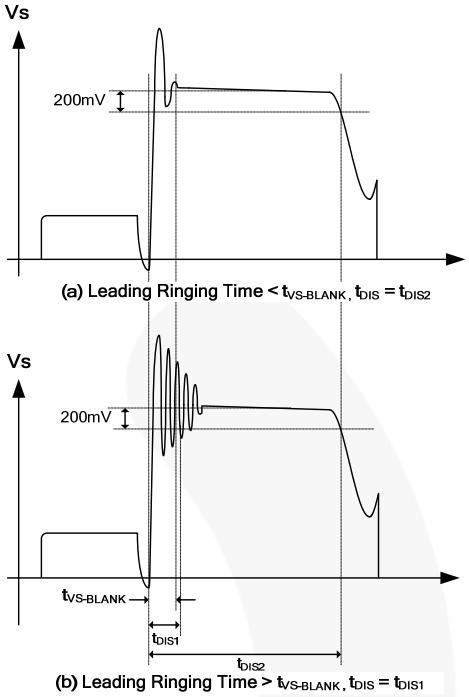

Figure 19. VS Pin Leading Ringing Waveform

[STEP-8] Calculate the Voltage and Current of the Switching Devices

Primary-Side MOSFET: The voltage stress of the MOSFET was discussed when determining the transformer turns ratio in STEP-7. The maximum voltage stress of the MOSFET is given in Equation (20):

The rms current through the MOSFET is given as:

$$I_{DS}^{rms} = I_{DS}^{PK} \sqrt{\frac{t_{ON@A} \cdot f_s}{3}} \quad (25)$$

where t_{ON} is MOSFET conduction time minimum input voltage and maximum load condition, given as:

$$t_{ON} = \frac{1}{V_{DL}^{\min}} \sqrt{\frac{2P_{IN@A} \cdot L_m}{f_S}} \quad (26)$$

Secondary-Side Diode: The nominal reverse voltage of the diode is given in Equation (10).

The rms current of the rectifier diode is obtained as:

$$I_D^{rms} = I_{DS}^{PK} \cdot \frac{N_P}{N_S} \sqrt{\frac{t_{DIS@A} \cdot f_S}{3}}$$

where $t_{DIS@A}$ is given as : (27)

$$t_{DIS@A} = \frac{1}{F_{OSC@BCM}} - (t_{ON} + 1\mu s)$$

(Design Example)

The maximum voltage across the MOSFET is calculated as:

$$V_{DS}^{\max} = V_{DL}^{\max} + V_{RO} + V_{OS} = 373 + 77 + 90 = 540V$$

The rms current through the MOSFET is:

$$I_{DS}^{rms} = I_{DS}^{PK}\sqrt{\frac{t_{ON}\cdot f_s}{3}} = 397m\sqrt{\frac{4.93\mu\cdot 80\cdot 10^3}{3}} = 0.148A$$

The MOSFET conduction time (t_{ON}) at minimum input voltage and maximum load is calculated as:

$$t_{ON,\max} = \frac{1}{V_{DL}^{\min}}\sqrt{\frac{2P_{IN@A}\cdot L_m}{f_S}} = \frac{1}{93.7}\sqrt{\frac{2\cdot 7.56\cdot 1.2mH}{80kHz}} = 5.08\mu s$$

The diode voltage and current are obtained as:

$$V_D = V_O^N + \frac{N_S}{N_P}V_{DL}^{\max} = 5 + \frac{10}{132}\cdot 373 = 33.3V$$

$$I_D^{rms} = I_{DS}^{PK}\cdot\frac{N_P}{N_S}\sqrt{\frac{t_{DIS@A}\cdot f_S}{3}} = 2.13A$$

where the $t_{DIS@A}$ is calculated as:

$$t_{DIS@A} = \frac{1}{F_{OSC@BCM}} - t_{ON} - 1\mu s = \frac{1}{80kHz} - 5.08\mu s - 1\mu s = 6.42\mu s$$

[STEP-9] Determine the Output Filter Stage

The peak-to-peak ripple of the capacitor current is given as:

$$\Delta I_C = \frac{N_P}{N_S}I_{DS}^{PK} \quad (28)$$

The voltage ripple on the output is given by:

$$\Delta V_O = \frac{T_{DIS@A}}{2C_O}\cdot\frac{(\Delta I_C - I_O^N)^2}{\Delta I_C} + \Delta I_C\cdot R_C \quad (29)$$

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of electrolytic or tantalum capacitors. Additional LC filter stages (post filters) can be used. When using post filters, do not to place the corner frequency too low. Too-low corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency.

(Design Example)

Assuming 330 µF solid capacitor with 20 mΩ ESR for the output capacitor, the voltage ripple on the output is:

$$\Delta I_C = \frac{N_P}{N_S}I_{DS}^{PK} = 5.24A$$

$$\Delta V_O = \frac{T_{DIS@A}}{2C_O}\cdot\frac{(\Delta I_C - I_O^N)^2}{\Delta I_C} + \Delta I_C\cdot R_C = 0.133V$$

[STEP-10] Complete the RC Snubber Design for the Diode

When the primary-side MOSFET is turned on, severe voltage oscillation occurs across the secondary-side diode, as shown in Figure 20. This is caused by the oscillation between the diode parasitic capacitance (C_D) and transformer secondary-side leakage inductance (L_{LKS}). To reduce the oscillation, an RC snubber is typically used, as shown in Figure 20. To effectively introduce damping to the resonant circuit, the parameters of the RC snubber should be:

$$R_{SN2} = \sqrt{\frac{L_{LKS}}{C_D}} \quad (30)$$

$$C_{SN2} = 2\sim 3\ times\ of\ C_D \quad (31)$$

The-secondary side leakage inductance and the diode parasitic capacitance are difficult to measure with an LCR meter. The best way is to use a test capacitor across the diode. First, measure the natural resonance period (t_R) without connecting anything to the diode. Then, add a test capacitor across the diode (C_{TST}) such that the test resonance period (t_{RT}) becomes about twice its original value and measure the test resonance period. With the measured t_R, t_{RT}, and C_{TST}; the resonance parameters can be calculated as:

$$C_D = C_{TST}/[(\frac{t_{RT}}{t_R})^2 - 1] \quad (32)$$

$$L_{LKS} = (\frac{t_R}{2\pi})^2\frac{1}{C_D} \quad (33)$$

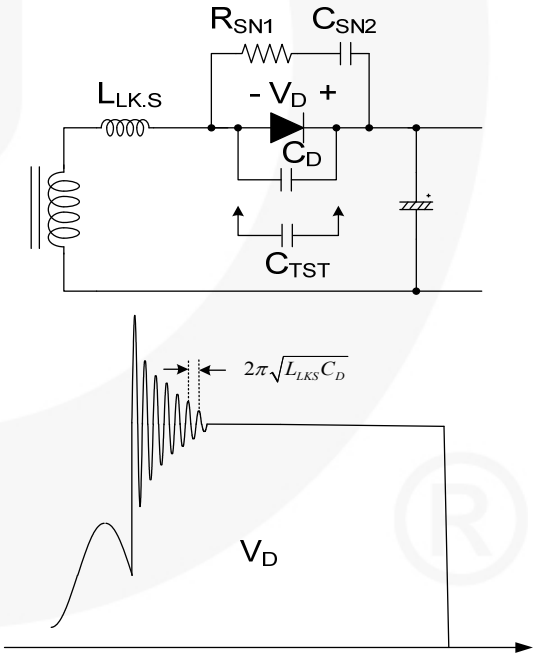

Figure 20. Diode Voltage Waveform

(Design Example)

The original resonance period is measured as t_R=85 ns. Using a 1 nF test capacitor, the resonance period is measure as t_{RT}=158 ns.

Then, the resonant parameters are obtained as:

$$C_D = \frac{C_{TST}}{[(\frac{t_{RT}}{t_R})^2 - 1]} = 260\,pF$$

$$L_{LKS} = (\frac{t_R}{2\pi})^2 \frac{1}{C_D} = 440nH$$

The snubber circuit parameters are calculated as:

$$R_{SNB} = \sqrt{\frac{L_{LKS}}{C_D}} = 13\Omega \quad , \quad C_{SNB} = 2.5, C_D = 1.02nF$$

[STEP-11] Choose Startup Resistor for HV Pin

Figure 21 shows the high-voltage (HV) startup circuit for FAN104W applications. Internally, the JFET is used to implement the high-voltage current source (characteristics shown in Figure 22). Technically, the HV pin can be directly connected to the DC link (V_{DL}). However, to improve reliability and surge immunity, it is typical to use a ~100 kΩ resistor between the HV pin and the DC link. The actual HV current with a given DC link voltage and startup resistor is determined by the intersection of V-I characteristics line and load line, as shown in Figure 22.

During startup, the internal startup circuit is enabled and the DC link supplies the current, I_{HV}, to charge the hold-up capacitor, C_{VDD}, through R_{HV}. When the V_{DD} voltage reaches V_{DD-ON}, the internal HV startup circuit is disabled and the IC starts PWM switching. Once the HV startup circuit is disabled, the energy stored in C_{VDD} should supply the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, C_{DD} should be properly designed to prevent V_{DD} from dropping to V_{DD-OFF} before the auxiliary winding builds up enough voltage to supply V_{DD}. The V_{DD} capacitance tolerance is an important factor to consider for C_{DD} selection. The C_{DD} can be obtained as:

$$C_{DD} \geq (1 + C_{DD}{}^{tol}) \times \frac{I_{DD-OP}{}^{max} \times t_{start}}{V_{DD-ON}{}^{min} - V_{DD-OFF}{}^{max}} \quad (34)$$

To ensure that C_{DD} can be charged from auxiliary winding before V_{DD-OFF} voltage, 1 V margin is needed:

$$t_{start} = \frac{(1+C_{OUT}{}^{tol}) \times C_{OUT} \times \frac{N_S}{N_A} \times (V_{DD-OFF}{}^{max} + V_{FA} + 1V)}{I_O - I_O{}^N} \quad (35)$$

where:
t_{start} is the time from V_{DD-ON} until the transformer auxiliary winding voltage reaches the nominal value;
I_{DD-OP} is operating supply current;
V_{DD-ON} is IC turn-on threshold voltage;
V_{DD-OFF} is FAN104W stop-switching voltage;
I_O is constant-output current;
$I_O{}^N$ is nominal-output current;
$C_{OUT}{}^{tol}$ is the tolerance of process with the system output capacitor;
$C_{DD}{}^{tol}$ is the tolerance of process with the VDD pin capacitor.

Connecting a 22 µF capacitor between the VDD and GND pins is recommended to ensure system stability over a wide operation temperature.

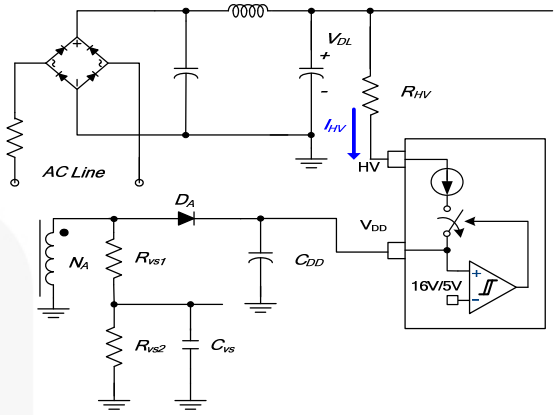

Figure 21. HV Startup Circuit

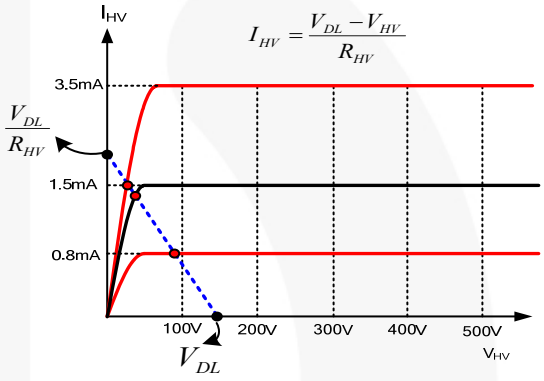

Figure 22. V-I Characteristics of HV Pin

(Design Example)

With 100 kΩ HV resistor and a 22 µF V_{DD} capacitor, the maximum startup time is:

$$t_{start} = \frac{(1+C_{OUT}{}^{tol}) \times C_{OUT} \times \frac{N_S}{N_A}(V_{DD-OFF}{}^{max} + V_{FA} + 1)}{I_O - I_O{}^N}$$

$$= \frac{(1+0.2) \times 330\mu \times 0.625 \times (5.5 + 0.7 + 1)}{1.15 - 1}$$

$$= 11.88ms$$

$$C_{DD} \geq (1 + C_{DD}{}^{tol}) \times \frac{I_{DD-OP}{}^{max} \times t_{start}}{V_{DD-ON}{}^{min} - V_{DD-OFF}{}^{max}}$$

$$C_{DD} \geq (1+0.2) \times \frac{4.5 \times 10^{-3} \times 11.88 \times 10^{-3}}{15 - 5.5}$$

$$C_{DD} \geq 6.75uF$$

For higher system tolerance, the 22 µF was chosen.

[STEP-12] Cable Compensation for Cable Voltage Drop

The FAN104W provides cable voltage-drop compensation through adjusting the resistor on the COMR pin (R_{COMR}). The designer can select a resistor value for different cable voltage drop. The output voltage is regulated by increasing the internal reference voltage of the error amplifier. The compensation voltage is given as:

$$V_{COMR} = \frac{80k \,//\, R_{COMR}}{60k} \cdot \frac{2.5V}{9} \quad (36)$$

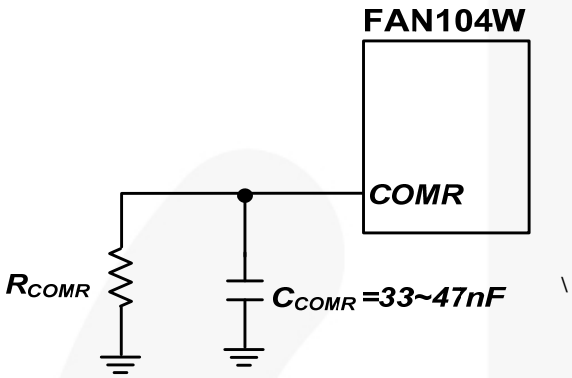

Figure 23. COMR Pin Suggested Circuit

The range of the C_{COMR} capacitor is recommended from 33 nF ~47 nF for better noise immunity.

(Design Example)

With 0.23 V cable drop, to compensate the voltage, place a 39 nF capacitor and R_{COMR} in parallel at the COMR pin; such that:

$$V_{COMR} = \frac{80k \,//\, R_{COMR}}{60k} \cdot \frac{2.5V}{9}$$

$$R_{COMR} = 131k\Omega$$

Choose resistor is 127 kΩ.

[STEP-13] How to Adjust Minimum Output Voltage at CC Mode:

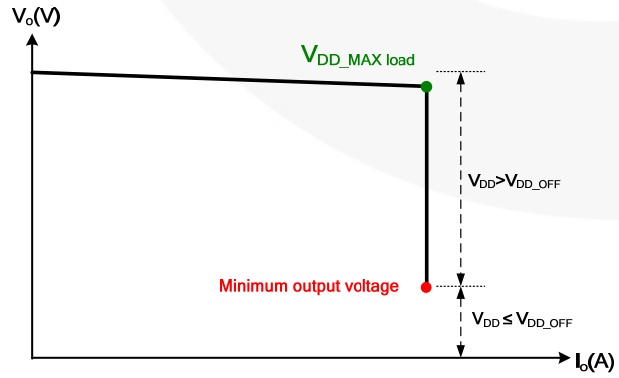

Figure 24. CC Mode Relates with V_{DD}

Minimum output voltage in CC Mode is determined by the below factors that control V_{DD} level because IC turn-off is related to V_{DD-OFF}.

(A) Adjusting series resistor R_{SER} on the auxiliary winding path. Higher value series resistor causes higher voltage drop to reduce energy deliver for the V_{DD} capacitor.

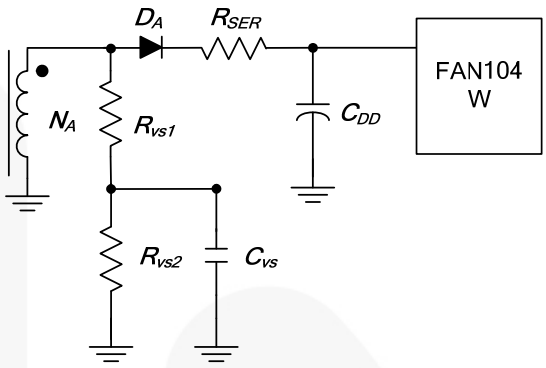

Figure 25. Auxiliary-Side Schematic

(B) Modifying the turns ratio between the auxiliary winding and the secondary winding. This affects the intensity of energy delivered to V_{DD}. When the fold-back point needs to be designed at a lower level, increased turns ratio could be necessary.

(C) Choosing an auxiliary winding rectifier diode (D_A) with a different forward-drop voltage and reverse-recovery time (t_{rr}). Slower t_{rr} causes larger power consumption, which means lower V_{DD}. For example, using FFM107 (t_{rr} =500ns) and FFM103 (t_{rr}=150 ns) deliver different energy to capacitor of V_{DD} (V_{DD}=2 V).

To make sure the MOSFETs turn-on fully, the V_{DD} should be satisfied with below equation (normally 2 V margin is added):

$$V_{DD} - V_{DROP} > V_{TH\_MOSFET} + 2V \quad (37)$$

where V_{DROP} is voltage drop from V_{DD} to the gate voltage in the controller and V_{TH_MOSFET} is the turn-on threshold voltage at the MOSFET gate.

5.PCB Layout Guidelines

Printed Circuit Board (PCB) layout and design are very important for switching power supplies where the voltage and current change with high dv/dt and di/dt. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge / ESD tests. The following guidelines are recommended for layout designs.

- To improve EMI performance and reduce line frequency ripple, the output of the bridge rectifier should be connected to capacitors C_1 and C_2 first, then to the transformer and MOSFET.
- The primary-side high-frequency current loop is **C_2 – Transformer – MOSFET – $R_{11,12}$ – C_2**. The area enclosed by this loop should be as small as possible. The trace for the control signal (VS, CS, and GATE) should not go across this primary high-frequency current loop to avoid interference. The high frequency current loop lay out example show as Figure 27.
- Place R_{HV} for protection from the inrush spike on the HV pin (100 kΩ is recommended).
- **$R_{11,12}$** should be connected to the C_2s ground directly. Keep the trace short and wide (Trace 4→1) and place it close to the CS pin to reduce switching noise. High-voltage traces related to the MOSFET drain and the RCD snubber should be away from control circuits to prevent unnecessary interference. If a heat sink is used for the MOSFET, connect this heat sink to ground.
- As indicated by 2, the area enclosed by the **transformer auxiliary winding, D_2 and C_4**, should be small.
- Place **C_4, R_6, C_5, C_6** and **R_{10}** close to the controller for good decoupling and low switching noise.
- As indicated by 3, the ground of the control circuits should be connected at a single point first, then to other circuitry.
- Connect ground in a 3→2→1, 4→1 sequence. This helps avoid common impedance interference for the sense signal.
- The secondary current flowing loop is: SD1→C_9→ USB Connector. The component placement follows this loop to avoid noise. The secondary current loop layout example is shown in Figure 27.
- Regarding the ESD discharge path; use the shortcut pad between the AC line and the DC output (recommended). Another method is to discharge the ESD energy to the AC line through the primary-side main ground 1. Because ESD energy is delivered from the secondary side to the primary side through the transformer stray capacitor or the Y capacitor, the controller circuit should not be placed on the discharge path. 5 shows where the point-discharge route can be placed to effectively bypass static electricity energy.
- For the surge path, select a fusible resistor of wire-wound type to reduce inrush current and surge energy. Use π input filter (two bulk capacitor and one inductance) to share the surge energy.

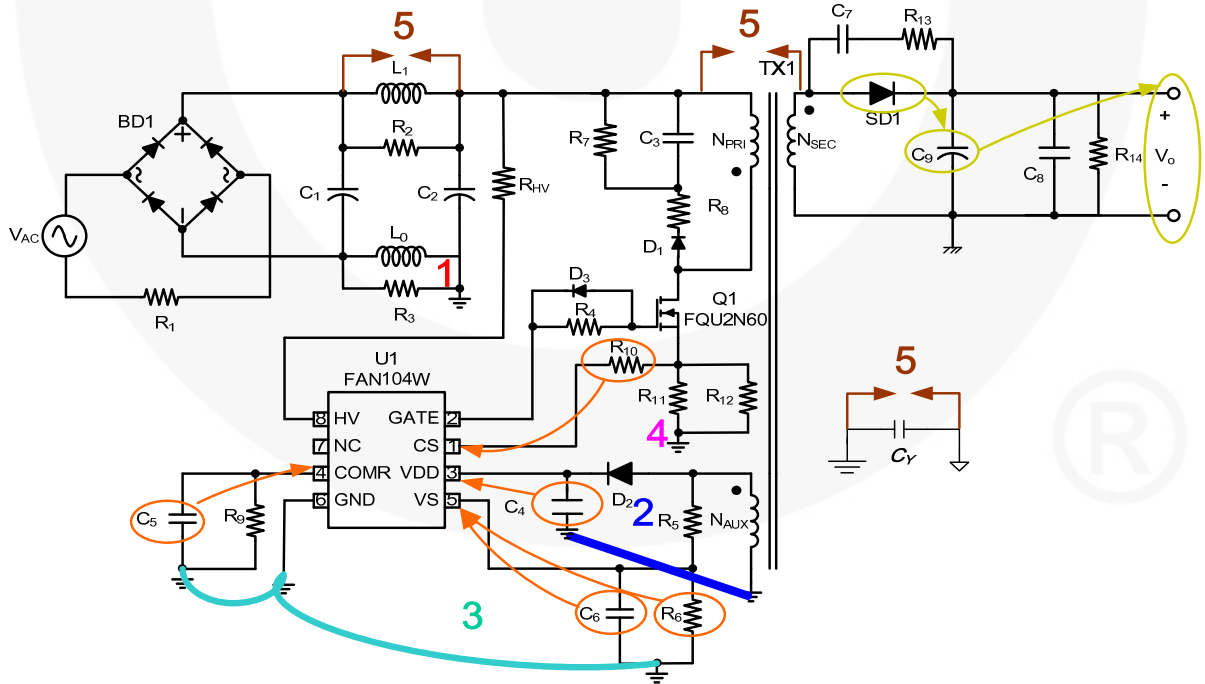

Figure 26. Recommended Layout

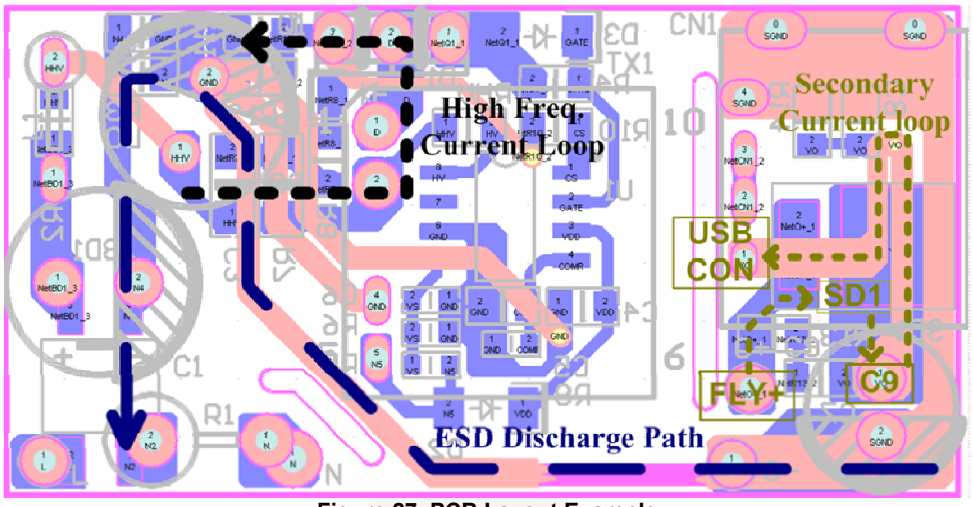

Figure 27. PCB Layout Example

6. Final Schematic and PCB of Design Example

Figure 28 shows the final schematic of the 5 W charger design example. An EPC13 core is used for the transformer. Figure 29 shows the transformer winding structure. Figure 30 and Figure 31 show the PCB pattern.

- Note that the sensing resistor is fine tuned to 1.275Ω based on test result of actual prototype power supply.
- Clamping circuit-resistor R_{SN1} is adjusted to 100 kΩ based on test results from the actual power supply.

Design Notes

- The leakage inductance is measured as 25 µH with an LCR meter. Calculation with the measured resonance period yields 19 µH of effective leakage inductance.

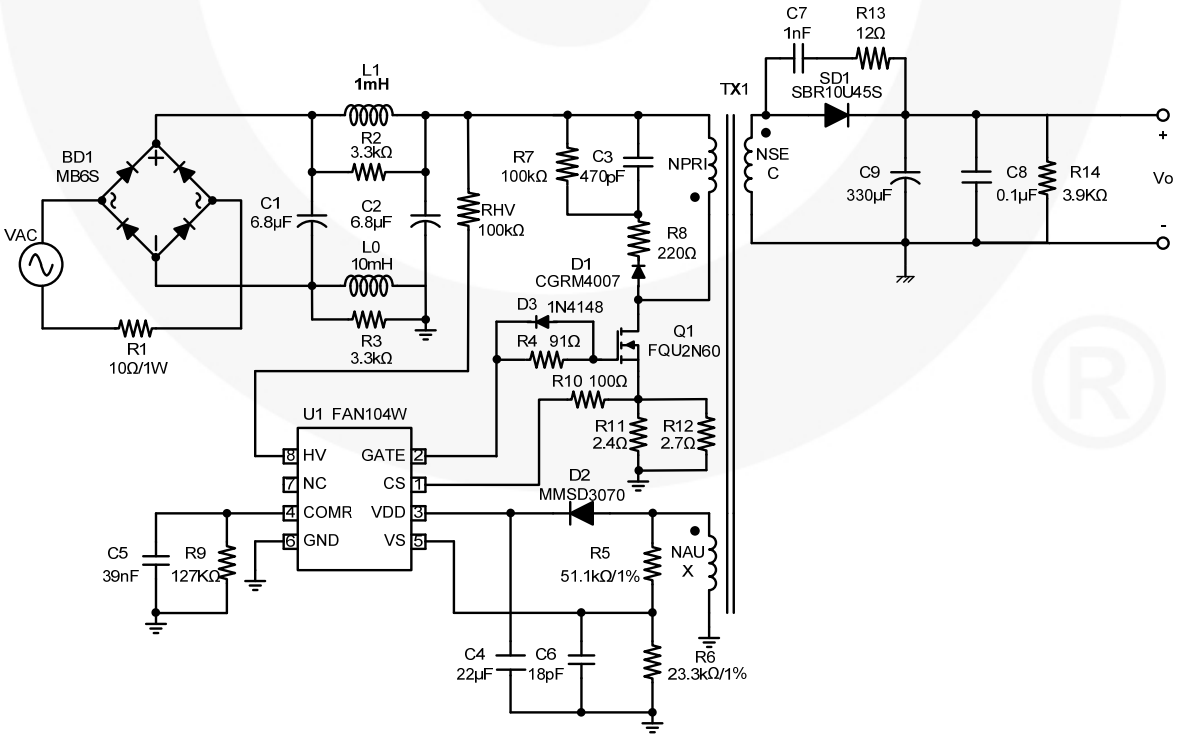

Figure 28. Final Schematic of the FAN104WM 5 W Design Example

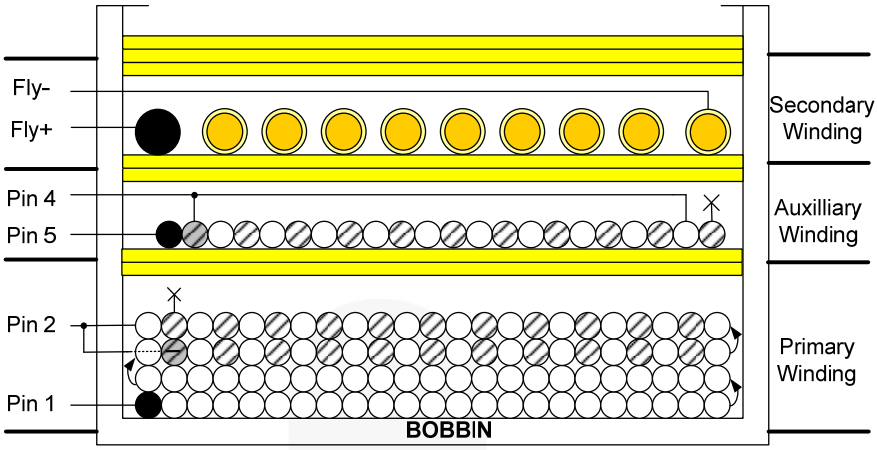

Figure 29. Transformer Winding Structure

Transformer Winding Specification

Winding	Pin (S → F)	Wire	Turns	Isolation Tape (Turns)	Notes
W1	1 → 2	2UEW 0.12φ*1	132	2	Layer 1 : 48 Turns Layer 2 : 47 Turns Layer 3 : 23 + 23 Turns (Parallel) Layer 4 : 14 + 14 Turns (Parallel)
	2 → NC		37		
W2	5 → 4	2UEW 0.18φ*1	16	2	2 Lines in Parallel
	4 → NC	2UEW 0.18φ*1	16		
W4	Fly+ → Fly-	TEX-E 0.45φ*1	10	2	
		Core Rounding Tape		3	

Table 3. Transformer Electronic Characteristic

	Pin	Specification	Remark
Primary-Side Inductance	1 – 2	1.2 mH ±7%	100 kHz, 1 V
Primary-Side Leakage Inductance	1 – 2	23 μH ±5%	Short One of the Secondary Windings

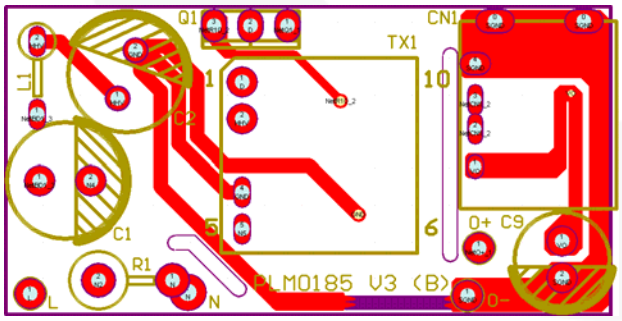

Figure 30. Front Side of PCB

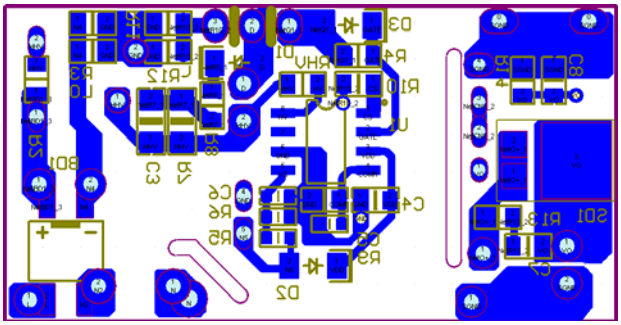

Figure 31. Back Side of PCB

7. Test Results of Design Example

To show the validity of the design procedure presented in this application note, the converter of the design example was built and tested. All the circuit components are used as designed in the design example.

Figure 32 shows the measured efficiency for different load conditions. The average efficiencies at 115 V_{AC} and 230 V_{AC} condition are 78.6% and 75.1%, respectively. Figure 34 shows the measured no-load power consumption at different line voltages. Even in the 264 V_{AC} AC line, the no-load standby power consumption is less than 30 mW, meeting the five-star level of new power consumption regulation for charger.

Figure 33 shows the measured output voltage and output current curve. The output current is regulated between 1.0 A and 1.4 A for output voltage from 5 V down to 1 V.

Figure 34 shows the CV and CC curves. The CV regulation is ±2.6% and CC regulation is ±2.4% at universal line voltage range.

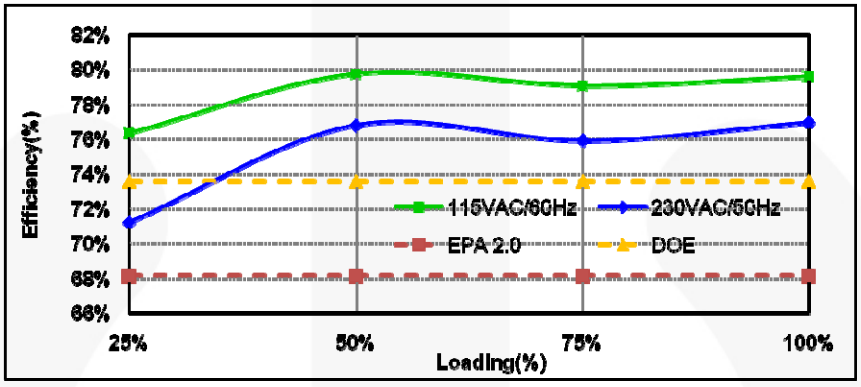

Figure 32. Measured Efficiency at End of Board

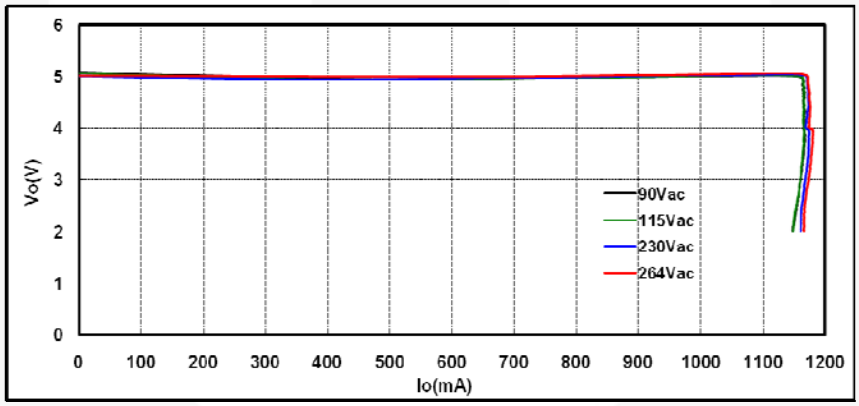

Figure 33. Output Voltage and Current Regulation

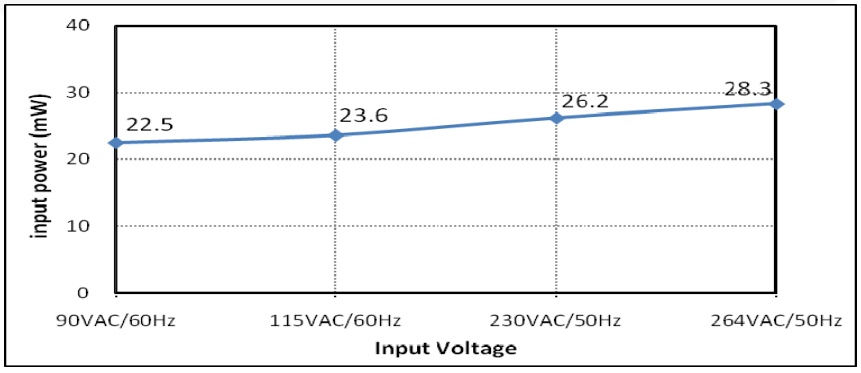

Figure 34. Standby Power Consumption

8. Related Resources

FAN104W — High-Frequency Primary-Side-Regulation PWM Controller

AN-8033 — Design Guideline for Primary-Side Regulated (PSR) Flyback Converter Using FAN103 and FSEZ13X7

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