DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS

Computer Organization and Architecture (CS2600)

Total Time : 50 minutes **Tutorial 3**
Max Marks : 20 **11-03-2024**

A computer has the following page table configuration: **Virtual Address bits: 43**; **Physical DRAM installed: 16GB**; **Page Size: 4KB**; **Page Table Entry Size: 4 bytes**

1. For a single-level page table, how many page-table entries are needed to map the entire the virtual address space of a program? How much physical memory is needed for storing the page table?
   Answer: Worst case is $2^{(43-12)} = 2^{31}$ entries, requiring $2^{(31)} \times 4B = 2^{33} = 8GB$.

2. How many levels of page tables are needed to map the entire virtual address space?
   Answer: Each page table contains 4KB/4=1024 (2^{10}) entries. Each page can hold 4KB, that is 2^{12} bytes. Entire virtual address space is 2^{43} bytes. Therefore, number of levels of page tables are $\lceil (43-12)/10 \rceil = 4$ levels of translation.

3. What is the maximum size of addressable physical memory given a 2-level page translation?
   Answer: First level page table, has 2^{10} PTEs. Each of the second level PTE has 2^{10} PTEs. Thus, there are 2^{20} second level PTEs.

   Each of the second level PTEs points to a 4KB page frame, ie 2^{12} bytes. Thus maximum addressable bytes are $2^{20+12} = 2^{32}$ bytes, or 4GB.

4. Consider a `ld x3, 200(x2)` instruction. Assume that the instruction is already loaded in the CPU. In a 2-level page translation, how many memory accesses are required perform this load operation?
   Answer: Three. One for each level. One for the final load instruction.