BabySoC: Compact RISC-V SoC Project Overview

Project Introduction

- Goal: Create a compact, open-source SoC based on the RVMYTH RISC-V core.
- Key Features:
    - Integrates Phase-Locked Loop (PLL) for accurate clocking.
    - Features a 10-bit Digital-to-Analog Converter (DAC).
    - Enables communication with analog devices (audio/video output).
    - Uses Sky130 technology for fabrication and experimentation.
    - Serves as an educational platform with thorough documentation.

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1. System on a Chip (SoC): The Basics

- Single chip containing all computer components.
- Components:
    - CPU
    - Memory (RAM, ROM, Flash)
    - I/O Ports
    - GPU (optional)
    - Digital Signal Processor (DSP)
    - Power Management
    - Optional features: wireless, security modules
- Advantages:
    - Space-saving: smaller devices.
    - Energy efficiency: less power use.
    - High performance: fast internal communication.
    - Cost-effective: fewer separate parts.
    - Reliability: less prone to hardware failure.
- Applications:
    - Smartphones/tablets
    - Wearables (smartwatches)
    - IoT/sensor devices

- Embedded systems in cars/TVs/appliances

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2. Types of SoCs

- Microcontroller-based:
  - Simple control tasks, low power (IoT, appliances).
- Microprocessor-based:
  - Powerful, runs OS, used in phones/tablets.
- Application-Specific:
  - Tuned for special tasks (graphics, AI, networking).
- SoC Design Flow:
  - Block diagram/specification
  - RTL design/simulation
  - Synthesis/Place & Route
  - Verification/fabrication

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3. VSDBabySoC Architecture

- Core Components:
  - RVMYTH (RISC-V CPU): Open-source, customizable basic processor.
  - PLL: Generates stable/synchronized clock signals.
  - DAC: Converts digital data to analog output.
- Operation Flow:
  - Initialization triggers PLL for clock sync.
  - RVMYTH updates register (r17) for continuous output.
  - DAC converts output to analog signals for device interfacing.
- Applications:
  - Sends audio/video to TVs and phones.

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4. Phase-Locked Loop (PLL)

- Function: Matches output clock frequency/phase to input reference signal.
- Block Diagram Elements:
  - Phase Detector: compares inputs, generates error signal.

    - Loop Filter: smooths error signal.
    - VCO: adjusts output frequency.
- Advantages:
    - Mitigates clock distribution delay/jitter.
    - Adapts to multiple frequency requirements.
    - Corrects errors (ppm) from crystal clocks.
    - Handles frequency drift (temperature/aging).

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5. Digital-to-Analog Converter (DAC)

- Role: Converts digital signals (binary) into analog voltage.
- Types:
    - Weighted Resistor DAC: uses various resistors for conversion.
    - R-2R Ladder DAC: uses repeating resistor networks for scalable design.
- VSDBabySoC Feature: Uses a 10-bit DAC for higher resolution analog signals.

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6. Summary of Project Impact

- Demonstrates integration of open-source RISC-V core with critical analog and digital peripherals.
- Showcases digital-to-analog interfacing for multimedia output.
- Provides a hands-on platform for SoC, analog, and clock design education.
- Illustrates practical design challenges (timing, synchronization, signal conversion) in modern embedded systems.