UE-VLSI2 TP : Cadence RTL Compiler
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1 Set the environment

```
#!/bin/sh
export LM_LICENSE_FILE=30000@licences.cnfm.fr
export PATH=$PATH:/users/soft/opus/Linux/RC-13.12-000/bin
```

2 Load the libraries

n.b: all the libraries are located at `/users/enseig/tuna/ue-vlsi2/techno`.

Two types of cell libraries are available: `_Best.lib` and `_Worst.lib`. The difference between these libraries lies in the timing arcs of their cells : while the Best Library contains Best-Case timings, the Worst Library contains the Worst-Case equivalents. Each timing arcs are estimated via different PVT parameters (**Process - Voltage - Temperature**). These parameters an be found in the headers of each library.

```
/*****************************************************
 Synopsys Technology File

 genstf version 6.4
...
Process values given:
  Library nominal:                1.2
  Tech-file best case:            1.2
  Tech-file centre:               1.2
  Tech-file worst case:           1.2
Voltage values given:
  Library nominal:                1.08
  Tech-file best case:            1.20
  Tech-file centre:               1.08
  Tech-file worst case:           1.0
Temperature values given:
  Library nominal:                85
  Tech-file best case:            25
  Tech-file centre:               125
  Tech-file worst case:           125

  *****************************************************/
```

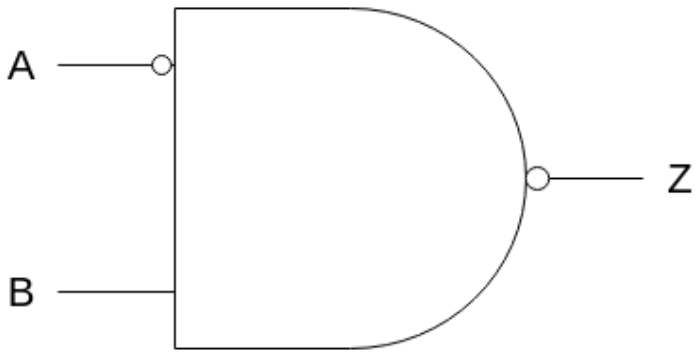
PVT specifications for cmos_120nm_core_Worst

```
/*****************************************************
 Synopsys Technology File

 genstf version 6.4
...
Process values given:
  Library nominal:                0.8
  Tech-file best case:            0.8
  Tech-file centre:               0.8
  Tech-file worst case:           0.8
Voltage values given:
  Library nominal:                1.32
  Tech-file best case:            1.32
  Tech-file centre:               1.32
  Tech-file worst case:           1.20
Temperature values given:
  Library nominal:                0
  Tech-file best case:            -40.0
  Tech-file centre:               0
  Tech-file worst case:           25.0

 *****************************************************/
```

PVT specifications for cmos_120nm_core_Best

In order to synthesize the RTL description, we will use cmos_120nm_core_Worst.lib. This library contains all the generic cells we will need, and with Worst-Case timings in order to thoroughly stress the longest combinational paths.

A practical example of difference in timing arcs between this library and its _Best equivalent can be seen when evaluating the ND2AHS cell, a "2 Input NAND w A Input Inverted and 1x Drive".



Gate-level schematic of the ND2AHS cell

3 Load the design

4 Elaborate

The eaboration process does not differ from the Synthesis per se. The elaboration step is the conversion of the RTL description to a model where every instance object (signal, process, arrays, etc) is converted into a component (adder, multiplexer, register, etc). This step is part of the Synthesis process.