ELECENG 2EI4: Electronic Devices and Circuits I
Project #1

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Kyle Stamp, stampk1, 400291081]**

Summary

The purpose of this report is to design a circuit to convert 120V rms AC input voltage to a 3V +/- 0.1V DC output voltage. The design includes a rectifier to manipulate and obtain the positive voltage from the input, a filter to smooth the obtained voltage and a regulator to stabilize the voltage to 3V.

Design

Transformer

The required input voltage from the transformer is 4V. This can be obtained with a 30:1 turns ratio.

Rectifier

The chosen rectifier for the circuit is a full-wave bridge rectifier. A full-wave rectifier was chosen due to its efficiency over the half-wave rectifier by utilizing both the positive and negative parts of the input wave in a unipolar output, thereby doubling the output frequency. This efficiency means the output voltage will be higher for the full-wave vs. the half-wave rectifier with same input voltage. Thus, a lower input voltage is required for the full-wave, and thereby making the peak inverse voltage lower, making the necessary rating for reverse breakdown voltage of each diode lower. As well, there is less voltage ripple. The full-wave bridge rectifier was chosen because the peak inverse voltage is half that of the alternative center-tapped full-wave rectifier. As well, the bridge rectifier only requires half the turns for the secondary winding of its transformer compared to that of the center-tapped rectifier's transformer [1]. Thus, the bridge rectifier is the best choice. The rectifier contains four 1N4148 diodes, each with a forward voltage rating of 1V, meaning they will have a drop of 1V each when on.

Filter

The chosen filter is an RC circuit with a 100μF capacitor in parallel with the load resistor. This design stabilizes the voltage through the capacitor. When the voltage increases, the capacitor will charge. When the voltage decreases, the capacitor will discharge. Since the capacitor is in parallel with the load resistor, both components have the same voltage and therefore the capacitor will regulate the voltage across the load.

Regulator

The chosen regulator for the circuit is a Zener diode. This Zener diode will enter Zener breakdown once a 3V threshold is surpassed. This will cause some current to pass through the diode in reverse bias, which in turn will prevent any more current passing through the load resistor and effectively capping the voltage across the load at 3V.

Schematic

The circuit schematic can be seen in Appendix A, Figure 1.

Calculations

$$R = \frac{V}{I}$$

$$R = \frac{3V}{10mA}$$

$$R = 300\Omega$$

$$V_{in} - V_D - V_L = 0$$

$$V_{in} = V_D + V_L$$

$$V_{in} = 1V + 3V$$

$$V_{in} = 4V$$

$$V_{rpp} < 0.2V$$

$$C > \frac{I_{out}}{fV_{rpp}}$$

$$C > \frac{10mA}{(1kHz)(0.2V)}$$

$$C > 50\mu F$$

$$\therefore C = 100\mu F$$

$$Turns\ Ratio = \frac{120V}{4V}$$

$$Turns\ Ratio = 30:1$$

Expected Performance

With the above calculations, the output voltage should be 3V with a ripple of 0.1V, and a current of 10mA.

Issues

For the physical circuit testing process, there were no 300Ω resistors available. Thus, two 150Ω resistors were connected in series, which caused a slightly higher tolerance. The only capacitor available that is greater than the required 50µF was a 100µF, which resulted in less voltage ripple than the required threshold. One design margin considered was the diode ratings. These diodes have a forward current of 300mA, meaning if this value were exceeded, the diodes would break. Thus, extra caution was taken to ensure the current never exceeded this value through any of the four diodes. Furthermore, caution was taken to avoid high voltages to ensure the capacitor was not overloaded to avoid risk of damage or injury.

Measurement and Analysis

Circuit

The physical circuit can be seen in Appendix A, Figure 2.

Procedure

To test the physical circuit, a voltage input of 4V was used, which was increased to 4.45V through trial and error to get the desired outputs. The first oscilloscope channel measured the voltage across the load to obtain the output voltage, yielding an average value of about 3V, with a max of 3.08V and a min of 2.94V. The output current was obtained by dividing the voltage from channel 1 by the 300Ω load, yielding an average value of about 10mA. The voltage ripple was obtained by subtracting the lowest point of the output wave form from the highest point, yielding 0.14V.

Table 1: Table of Key Measurements

	Calculated	Simulation	Physical Analysis
Voltage Input	4V	4.65V	4.45V
Max Voltage Output	3.05V	3.027V	3.08V
Min Voltage Output	2.95V	2.990V	2.94V
Average Voltage Output	3V	3.0085V	3.01V
Average Current Output	10mA	10mA	10mA
Voltage Ripple	0.1V	0.05V	0.14V
Load Resistance	300Ω	300Ω	Two 150Ω in series

Oscilloscope

The Waveforms output can be seen in Appendix A, Figures 3 and 4.

Simulation

Schematic

The simulation schematic can be seen in Appendix A, Figure 1.

Netlist

The netlist can be seen in Appendix A, Figure 5.

Simulation Conditions

A transient analysis was performed with a stop time of 1s and a time step of 0.01s, with four 1N4148 diodes and one 1N5225B as seen in Figures 1 and 6. These times were chosen to ensure the proper shape is shown in the output, without oversampling. These diodes were chosen because they were the only diodes available.

Simulation Output

The output waveforms can be seen in Appendix A, Figure 6.

Discussion

Based on the results, the calculated values, simulation, and physical analysis were similar apart from a higher input voltage for the simulation and physical analysis. This discrepancy is due to the use of the actual 1N4148 diode in the simulation and circuit versus the datasheet values used in the calculations. This meant the diodes in the simulation had unrounded, lower forward voltage ratings and unaccounted for resistances that caused the need for a larger voltage input. As well, there were no 300Ω resistors available, so two 150Ω resistors in series were used. Furthermore, LTSpice does not have the exact Zener diode used in the circuit, so one was made with datasheet values, which could differ slightly from the physical diode's behaviour.

To troubleshoot these discrepancies, the circuit was rebuilt section-by-section to ensure each part of the circuit was functioning correctly. As well, the input voltage was adjusted through trial and error to get as close to the expected value as possible. The circuit was rebuilt many times to ensure no connections were missing or assembled improperly. Furthermore, the Zener diode datasheet claimed the breakdown voltage was 3V, however in practice it appears to be around 2.65V. Thus, it limited the voltage to a much lower value, so it was exempt in the physical circuit, but remained in the simulation to show its purpose of maintaining a specific voltage at the output.

This design utilized 4.45V for the input voltage, almost the maximum 5V the AD2 can supply. Thus, a load decently higher in resistance will not be able to reach a 3V output since the input voltage will need to be higher. Without a load, the output would solely rely on the drop across the capacitor, which will be the input less the drop across one diode, which is about the input voltage less 1V.

References

[1] A. Sedra, K. Smith, T. Carusone, V. Gaudet, *Microelectronic Circuits*, 8 ed. New York, NY, United States of America: Oxford University Press, 2020.

Appendix A: Figures

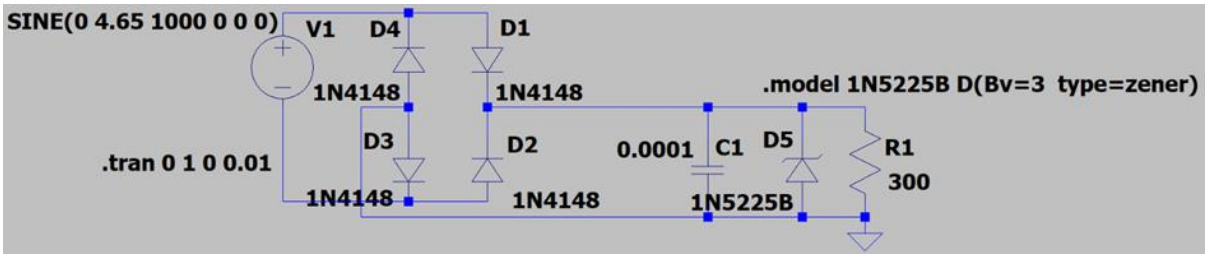

Figure 1: Circuit Schematic

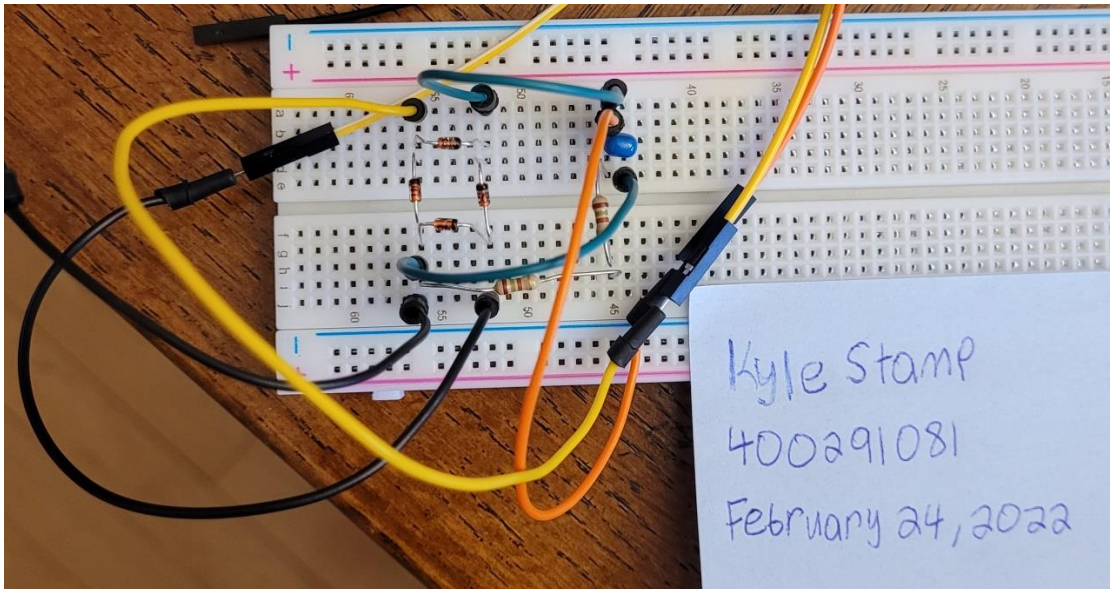

Figure 2: Physical Circuit

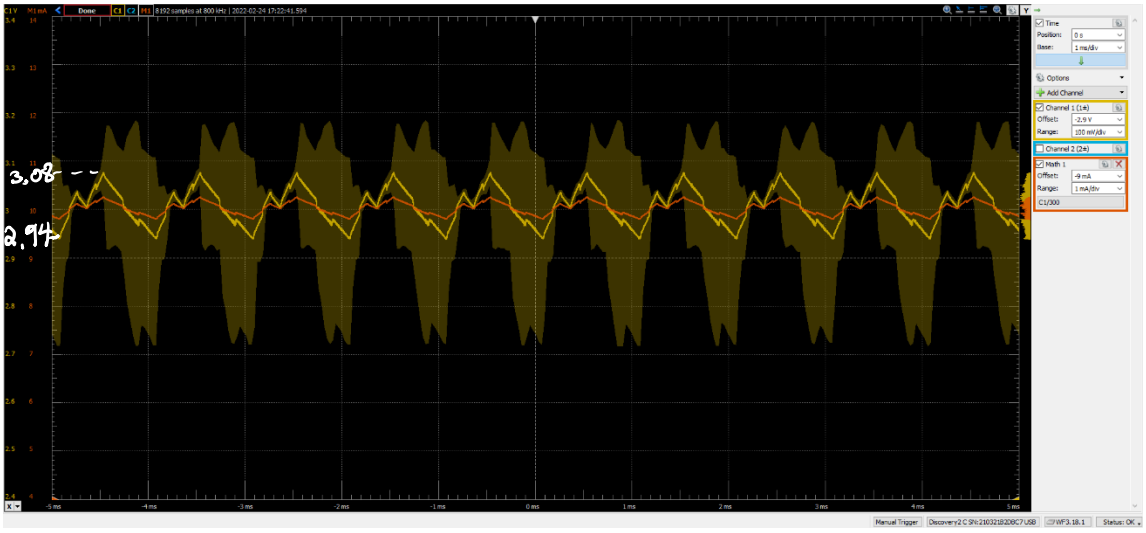

Figure 3: Oscilloscope Output in Waveforms

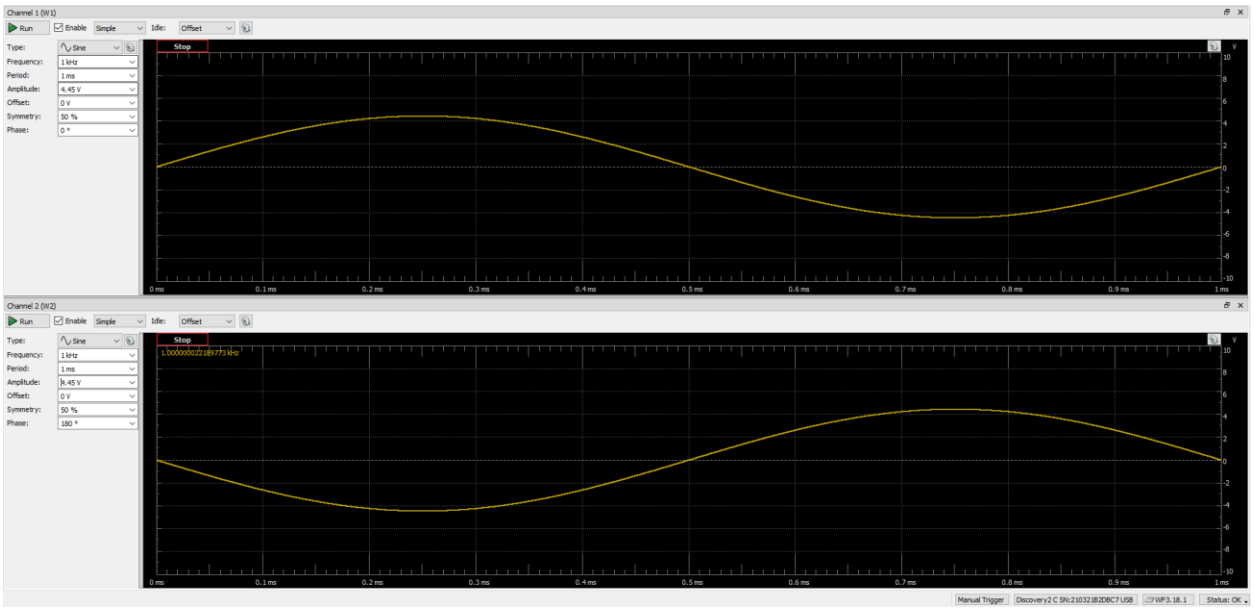

Figure 4: Wavegen in Waveforms

```
* C:\Users\Kyle\Desktop\2EI4_Project1.asc
D1 N001 N002 1N4148
D2 N003 N002 1N4148
D3 0 N003 1N4148
D4 0 N001 1N4148
C1 N002 0 0.0001
D5 0 N002 1N5225B
R1 N002 0 300
V1 N001 N003 SINE(0 4.65 1000 0 0 0)
.model D D
.lib C:\Users\Kyle\Documents\LTspiceXVII\lib\cmp\standard.dio
.model 1N5225B D(Bv=3  type=zener)
.tran 0 1 0 0.1
.backanno
.end
```

Figure 5: LTSpice Simulation Netlist

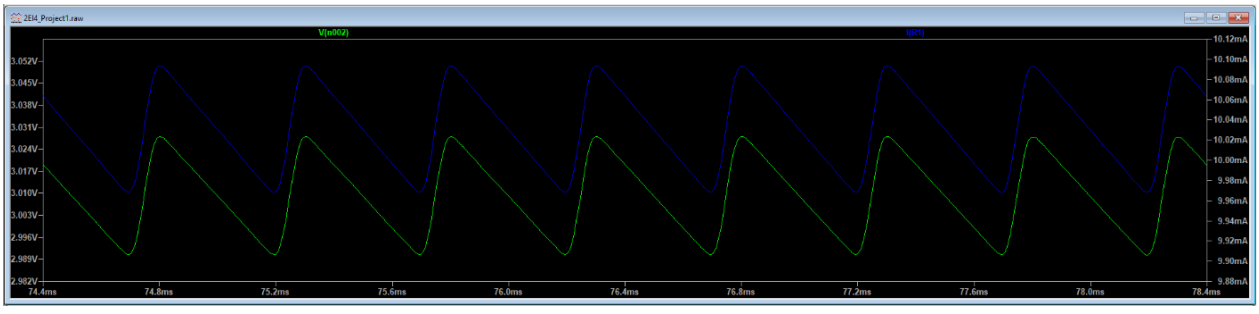

Figure 6: Simulation Transient Analysis