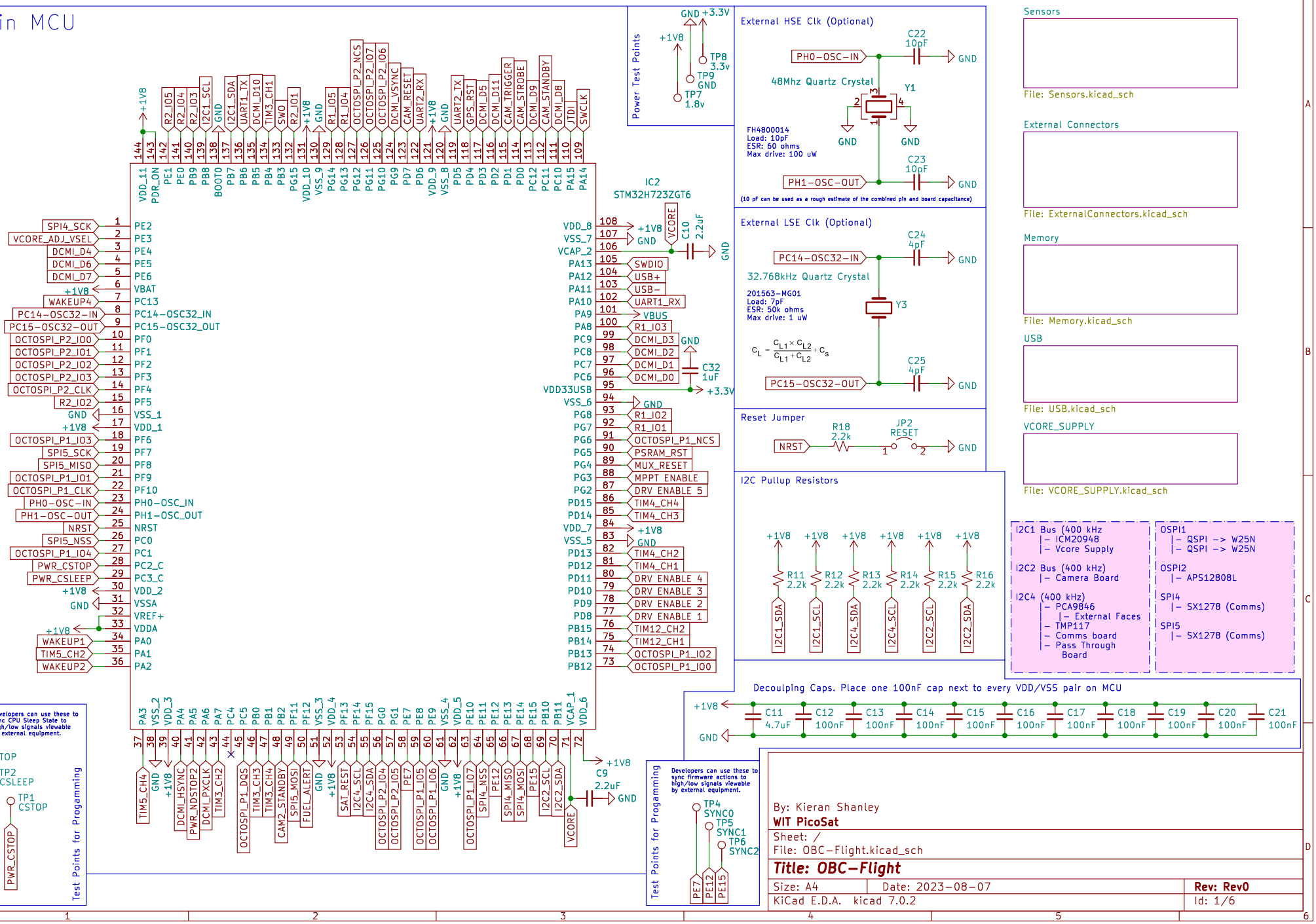
Main MCU



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Sheet: /

File: OBC-Flight.kicad_sch

Title: OBC-Flight

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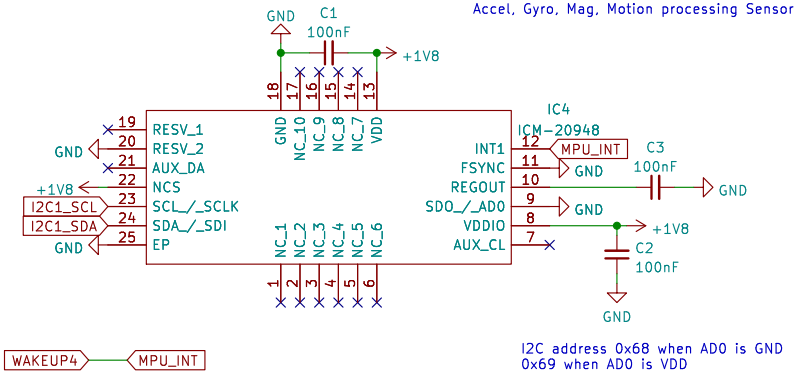
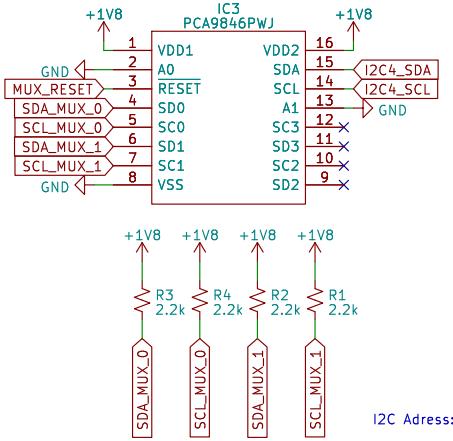
IMU

Accel, Gyro, Mag, Motion processing Sensor



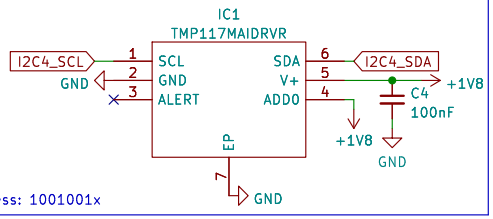
I2C address 0x68 when ADO is GND
0x69 when ADO is VDD

I2C Switch



I2C Adress: 0xE2h

Temperature Sensor



I2C Address: 1001001x

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Sheet: /Sensors/
File: Sensors.kicad_sch

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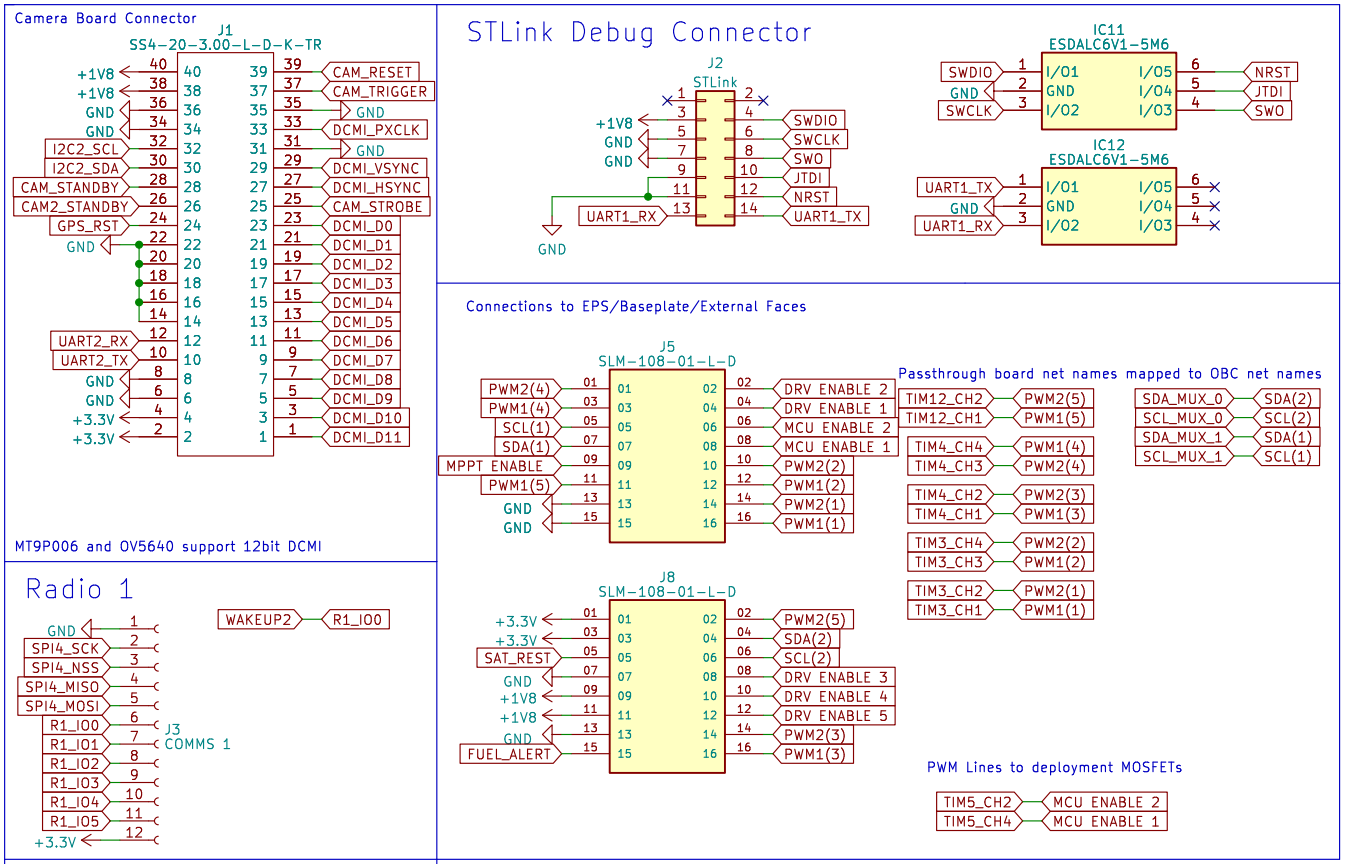

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Sheet: /External Connectors/
File: ExternalConnectors.kicad_sch

Title: OBC-Flight

Size: A4	Date: 2023-08-07	**Rev: Rev0**
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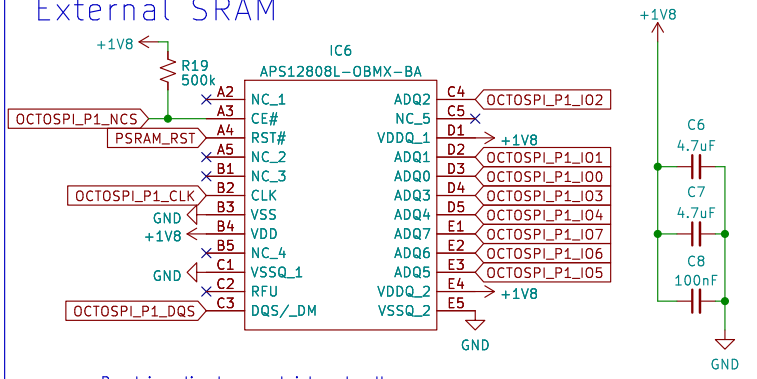
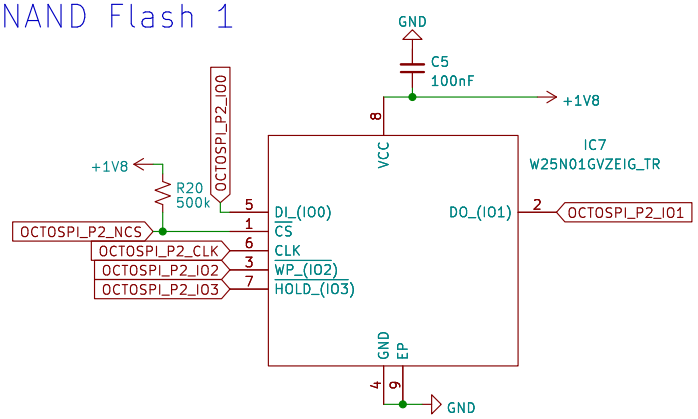
External SRAM



Reset is active low, weak internal pullup

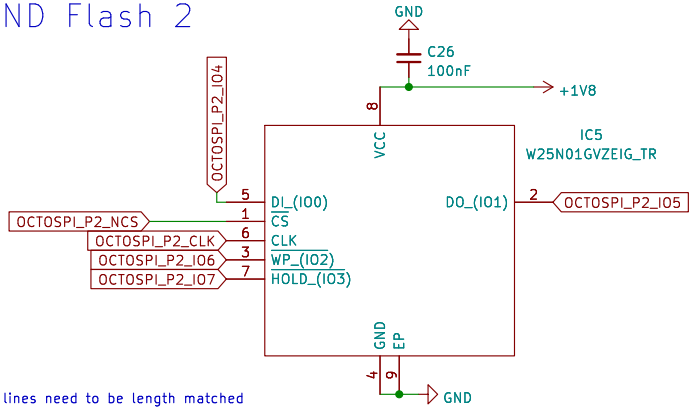
All data lines need to be length matched

NAND Flash 1



All data lines need to be length matched

NAND Flash 2



All data lines need to be length matched

OSPI Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace impedance: 50 Ω for single-ended and 100 Ω for differential pairs (CLK/NCLK)
- The maximum trace length should be less than 120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least three times the width of the trace away from other signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew. Serpentine traces (this is an "S" shape pattern to increase trace length) can be used to match the lengths.
- Avoid using a serpentine routing for the clock signal and use via(s) as little as possible for the whole path. A via alters the impedance and adds a reflection to the signal.
- Avoid discontinuities on high speed traces (vias, SMD components).

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Sheet: /Memory/
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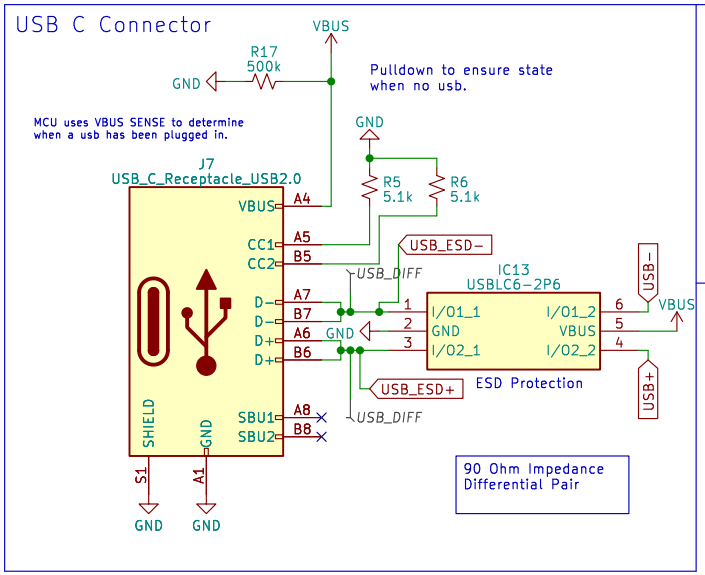

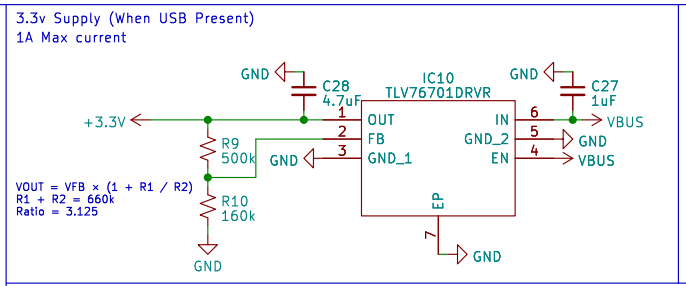

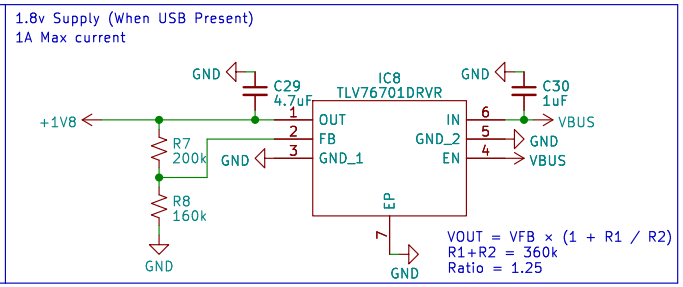

B: USB 2.0 OTG_FS, that is, USB 2.0 FS device/host/OTG controller with on-chip FS PHY

C: USB 2.0 OTG_HS, that is, USB 2.0 FS/HS device/host/OTG controller, integrating the transceivers for full-speed operation, and featuring an ULPI for high-speed operation: an external PHY device connected to the ULPI is required.

Series, lines, or references		Supported USB[1]					Size of dedicated packet buffer SRAM	Dedicated V_{DDUSB}	Embedded pull-up resistor on USB_DP line
		A	B	C	D	E			
STM32H7 series	STM32H743/753 line, STM32H750 value line	-	X[4]	X	-		4 Kbytes	Yes[5]	Yes

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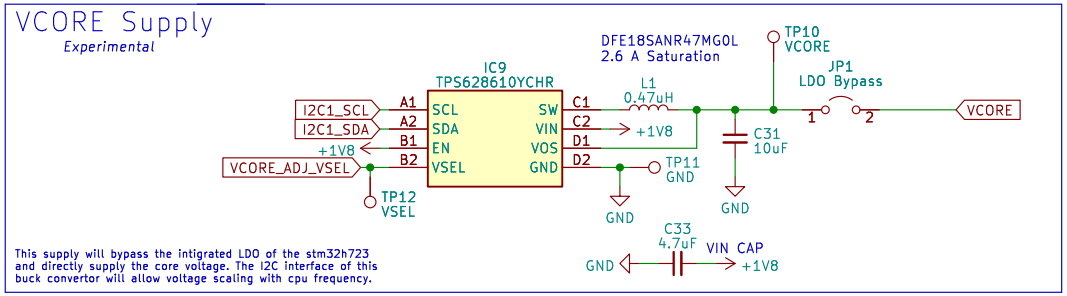

VDD Supply Requirements

Table 13. Supply voltage and maximum temperature configuration

Power scale	V_{CORE} source	Max. T_J (°C)	Min. V_{DD}(V)	Min. V_{DDLDO} (V)
VOS0	LDO	105	1.7	1.7
	External (Bypass)		1.62	-
VOS1	LDO	125	1.62	1.62
	External (Bypass)		-	-
VOS2 or VOS3	LDO	125	1.62	1.62
	External (bypass)		-	-
SVOS4/SVOS5	LDO	125	2	2
		105	1.62	1.62
	External (Bypass)	125	1.62	-

Vcore Supply Operating Conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{CORE}	Internal regulator ON (LDO)(4)	VOS3	0.95	1.0	1.05	V
		VOS2	1.05	1.10	1.15	
		VOS1	1.15	1.21	1.26	
		VOS0	1.30	1.36	1.40	
	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	VOS3	0.98	1.03	1.08	
		VOS2	1.08	1.13	1.18	
		VOS1	1.18	1.23	1.28	
		VOS0	1.33	1.38	1.40	

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File: VCORE_SUPPLY.kicad_sch

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