DATA SHEET

83C453/87C453

80C51 8-bit microcontroller family
8K/256 OTP/ROM, expanded I/O

Preliminary specification
Supersedes data of 1997 Dec 29
IC20 Data Handbook

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Philips
Semiconductors

PHILIPS

80C51 8-bit microcontroller family 8K/256 OTP/ROM, expanded I/O

83C453/87C453

DESCRIPTION

The Philips 8XC453 is an I/O expanded single-chip microcontroller fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC453 is a functional extension of the 87C51 microcontroller with three additional I/O ports and four I/O control lines. The 8XC453 is available in 68-pin LCC packages. Four control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

The 87C453 includes an 8k × 8 EPROM, a 256 × 8 RAM, 56 I/O lines, two 16-bit timer/counters, a seven source, two priority level, nested interrupt structure, a serial I/O port for either a full duplex UART, I/O expansion, or multi-processor communications, and on-chip oscillator and clock circuits.

The 87C453 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

FEATURES

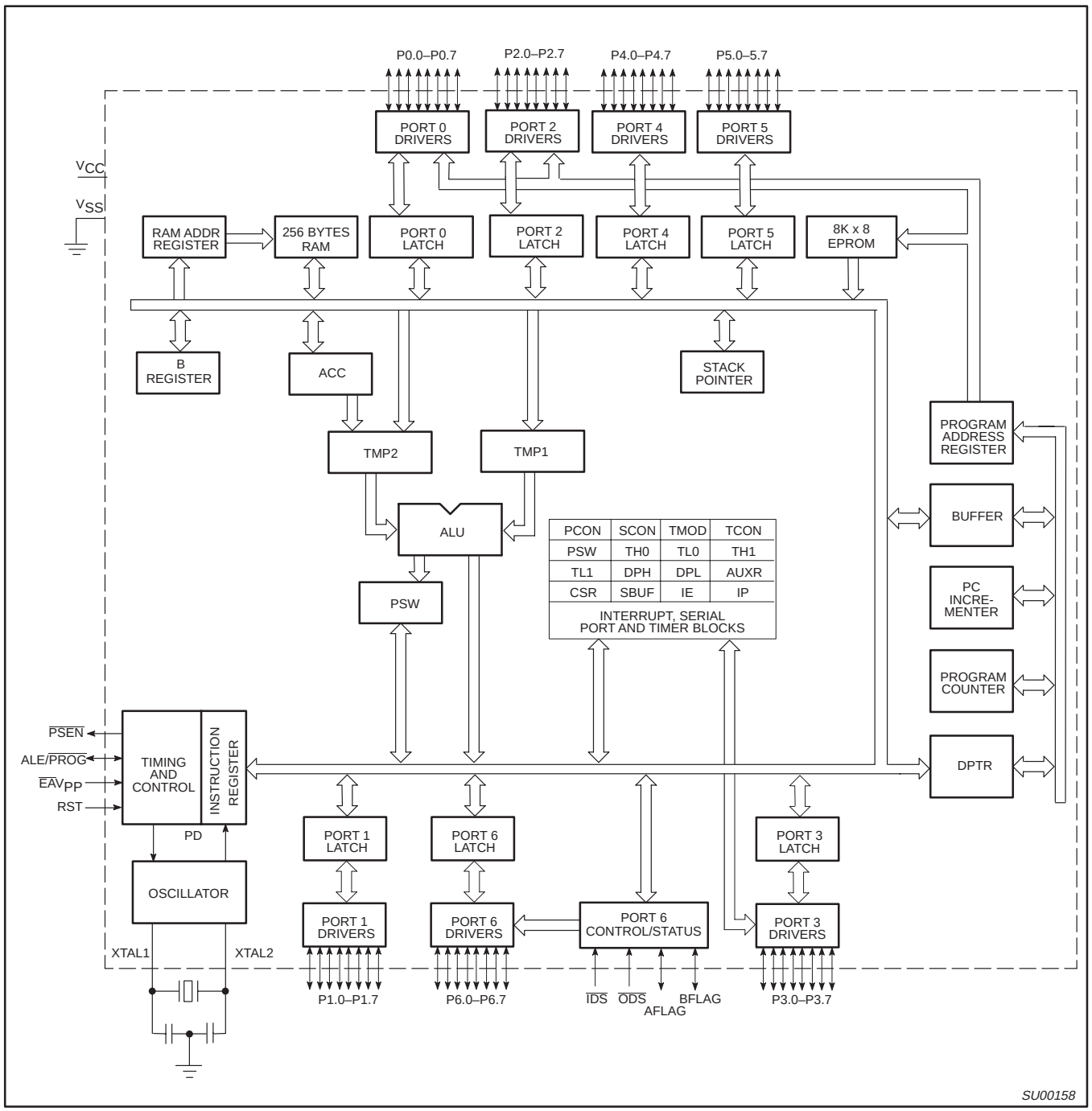
- 80C51 based architecture
- Seven 8-bit I/O ports
- Port 6 features:
  - Eight data pins
  - Four control pins
  - Direct MPU bus interface
  - ISA Bus Interface
  - Parallel printer interface
  - IBF and $\overline{OBF}$ interrupts
  - A flag latch on host write
- On the microcontroller:
  - 8k × 8 EPROM
    Quick pulse programming algorithm
    Two-level program security system
  - 256 × 8 RAM
  - Two 16-bit counter/timers
  - Two external interrupts
- External memory addressing capability
  - 64k ROM and 64k RAM
- Low power consumption:
  - Normal operation: less than 24mA at 5V, 16MHz
  - Idle mode
  - Power-down mode
- Reduced EMI
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition

ORDERING INFORMATION

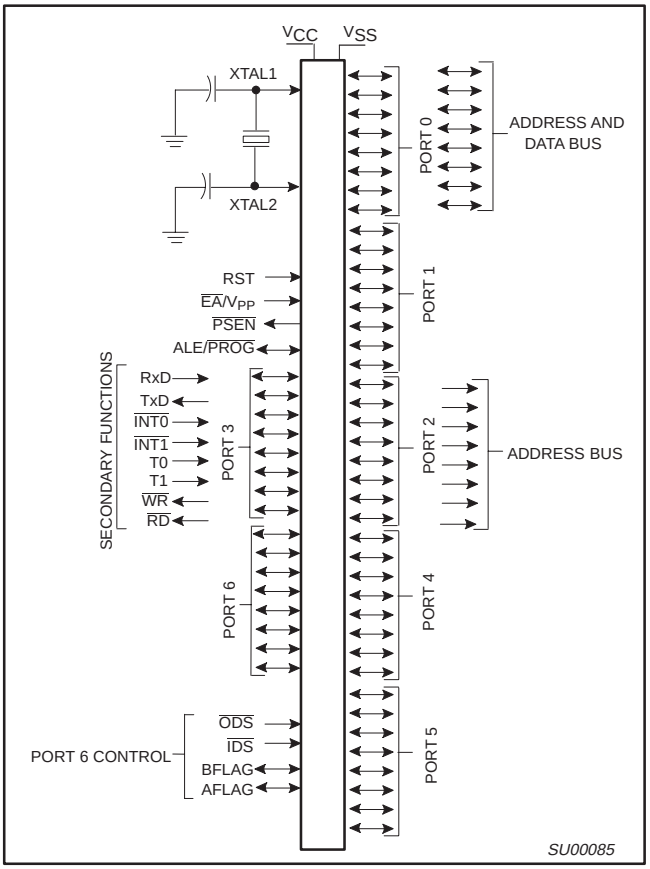
EPROM[1]		ROM	TEMPERATURE °C AND PACKAGE	FREQ. (MHz)	PKG. DWG #
P87C453EBAA	OTP	P83C453EBAA	68–Pin Plastic Leaded Chip Carrier, 0 to +70	3.5 to 16	SOT188-3

NOTE:
1. OTP = One-Time Programmable EPROM.

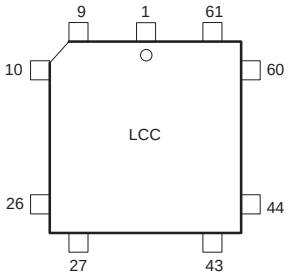
BLOCK DIAGRAM



LOGIC SYMBOL



LCC PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	$\overline{EA}/V_{PP}$	24	P4.2	47	P5.3
2	P2.0/A8	25	P4.1	48	P5.4
3	P2.1/A9	26	P4.0	49	P5.5
4	P2.2/A10	27	P1.0	50	P5.6
5	P2.3/A11	28	P1.1	51	P5.7
6	P2.4/A12	29	P1.2	52	XTAL2
7	P2.5/A13	30	P1.3	53	XTAL1
8	P2.6/A14	31	P1.4	54	V_{SS}
9	P2.7/A15	32	P1.5	55	$\overline{ODS}$
10	P0.7/AD7	33	P1.6	56	$\overline{IDS}$
11	P0.6/AD6	34	P1.7	57	BFLAG
12	P0.5/AD5	35	RST	58	AFLAG
13	P0.4/AD4	36	P3.0/RxD	59	P6.0
14	P0.3/AD3	37	P3.1/TxD	60	P6.1
15	P0.2/AD2	38	P3.2/$\overline{INT0}$	61	P6.2
16	P0.1/AD1	39	P3.3/$\overline{INT1}$	62	P6.3
17	P0.0/AD0	40	P3.4/T0	63	P6.4
18	V_{CC}	41	P3.5/T1	64	P6.5
19	P4.7	42	P3.6/$\overline{WR}$	65	P6.6
20	P4.6	43	P3.7/$\overline{RD}$	66	P6.7
21	P4.5	44	P5.0	67	$\overline{PSEN}$
22	P4.4	45	P5.1	68	ALE/$\overline{PROG}$
23	P4.3	46	P5.2		

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PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{SS}	54	I	**Ground:** 0V reference.
V_{CC}	18	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	17-10	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 is also the multiplexed data and low-order address bus during accesses to external memory. External pull-ups are required during program verification. Port 0 can sink/source eight LS TTL inputs.
P1.0–P1.7	27-34	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 receives the low-order address bytes during program memory verification. Port 1 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.
P2.0–P2.7	2-9	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 emits the high-order address bytes during access to external memory and receives the high-order address bits and control signals during program verification. Port 2 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.
P3.0–P3.7	36-43	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups. Port 3 also serves the special functions listed below:
	36	I	**RxD (P3.0):** Serial input port
	37	O	**TxD (P3.1):** Serial output port
	38	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt
	39	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	40	I	**T0 (P3.4):** Timer 0 external input
	41	I	**T1 (P3.5):** Timer 1 external input
	42	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	43	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
P4.0–P4.3 P4.0–P4.7	26-19	I/O I/O	**Port 4:** Port 4 is an 8-bit bidirectional I/O port with internal pull-ups. Port 4 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P5.0–P5.7	44-51	I/O	**Port 5:** Port 5 is an 8-bit bidirectional I/O port with internal pull-ups. Port 5 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P6.0–P6.7	59-66	I/O	**Port 6:** Port 6 is a specialized 8-bit bidirectional I/O port with internal pull-ups. This special port can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 6 can be used in a strobed or non-strobed mode of operation. Port 6 works in conjunction with four control pins that serve the functions listed below:
$\overline{\text{ODS}}$	55	I	**$\overline{\text{ODS}}$:** Output data strobe
$\overline{\text{IDS}}$	56	I	**$\overline{\text{IDS}}$:** Input data strobe
BFLAG	57	I/O	**BFLAG:** Bidirectional I/O pin with internal pull-ups
AFLAG	58	I/O	**AFLAG:** Bidirectional I/O pin with internal pull-ups
RST	35	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor permits a power-on reset using only an external capacitor connected to V_{CC}.
ALE/$\overline{\text{PROG}}$	68	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE is skipped. ALE can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. This pin is also the program pulse during EPROM programming.
$\overline{\text{PSEN}}$	67	O	**Program Store Enable:** The read strobe to external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external program memory. However, when executing out of external program memory, two activations of $\overline{\text{PSEN}}$ are skipped during each access to external program memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. $\overline{\text{PSEN}}$ can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up. This pin should be tied low during programming.
$\overline{\text{EA}}$/V_{PP}	1	I	**Instruction Execution Control/Programming Supply Voltage:** When $\overline{\text{EA}}$ is held high, the CPU executes out of internal program memory, unless the program counter exceeds 1FFFH. When $\overline{\text{EA}}$ is held low, the CPU executes out of external program memory. $\overline{\text{EA}}$ must never be allowed to float. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	53	I	**Crystal 1:** Input to the inverting oscillator amplifier that forms the oscillator. This input receives the external oscillator when an external oscillator is used.
XTAL2	52	O	**Crystal 2:** An output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

Table 1. 87C453 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT NAMES AND ADDRESSES MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
			EF	EE	ED	EC	EB	EA	E9	E8	
CSR*#	Port 6 command/status	E8H	MB1	MB0	MA1	MA0	OBFC	IDSM	OBF	IBF	FCH
DPTR	Data pointer (2 bytes)										
DPH	Data pointer high	83H									00H
DPL	Data pointer low	82H									00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt priority	B8H	–	POB	PIB	PS	PT1	PX1	PT0	PX0	x0000000B
AUXR#	Auxiliary register	8EH	–	–	–	–	–	–	AF	AO	x0000000B
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt enable	A8H	EA	IOB	IIB	ES	ET1	EX1	ET0	EX0	00000000B
P0*	Port 0	80H	87	B6	85	84	83	82	81	80	FFH
P1*	Port 1	90H	97	96	95	94	93	92	91	90	FFH
P2*	Port 2	A0H	A7	A6	A5	A4	A3	A2	A1	A0	FFH
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
P4*#	Port 4	C0H	C7	C6	C5	C4	C3	C2	C1	C0	FFH
P5*#	Port 5	C8H	CF	CE	CD	CC	CB	CA	C9	C8	FFH
P6*#	Port 6	D8H	DF	DE	DD	DC	DB	DA	D9	D8	FFH
PCON	Power control	87H	SMOD1	SMOD0	–	POF[1]	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial data buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial port control	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer/counter control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TMOD	Timer/counter mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H
TH0	Timer 0 high byte	8CH									00H
TH1	Timer 1 high byte	8DH									00H
TL0	Timer 0 low byte	8AH									00H
TL1	Timer 1 low byte	8BH									00H

NOTES:
* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
1. REset value depends on reset source.

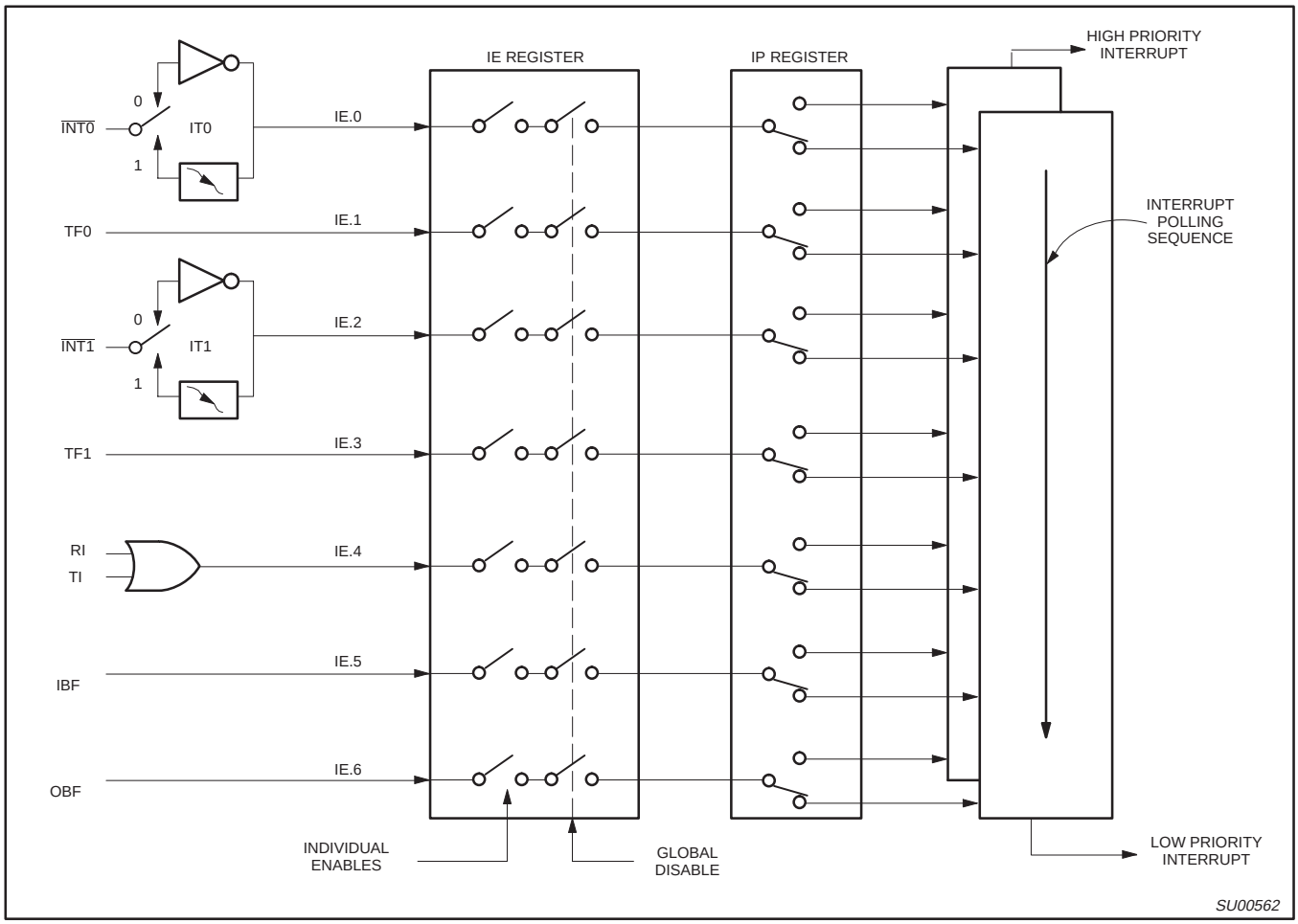

Figure 1. 8XC453 Interrupt Control System

MSB							LSB
EA	IOB	IIB	ES	ET1	EX1	ET0	EX0

BIT	SYMBOL	FUNCTION
IE.7	EA	Disables all interrupts. If EA=0, no interrupt will be acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
IE.6	IOB	Enables or disables the Output Buffer Full (OBF) interrupt. If IOB=0, the interrupt is disabled, If IOB=1, an interrupt will occur if EA is set and data has been read from the output buffer register through Port 6 by the external host pulsing ODS low.
IE.5	IIB	Enables or disables the Input Buffer Full (IBF) interrupt. If IIB=0, the interrupt is disabled. If IIB=1, an interrupt will occur if EA is set and data has been written into the Port 6 Input Data Buffer by the host strobing IDS low.
IE.4	ES	Enables or disables the Serial Port Interrupt. If ES=0, the Serial Port Interrupt. If ES=0, the Serial Port interrupt is disabled.
IE.3	ET1	Enables or disables the Timer 1 Overflow interrupt. If ET1=0, the Timer 1 interrupt is disabled.
IE.2	EX1	Enables or disables External Interrupt 1. If EX1=0, External Interrupt 1 is disabled.
IE.1	ET0	Enables or disables the Timer 0 Overflow interrupt. If ET0=0, the Timer 0 interrupt is disabled.
IE.0	EX0	Enables or disables External Interrupt 0. If EX0=0, external Interrupt 0 is disabled.

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Figure 2. 8XC453 Interrupt Enable (IE) Register

MSB							LSB
—	POB	PIB	PS	PT1	PX1	PT0	PX0

BIT	SYMBOL	FUNCTION
IP.7	—	Reserved.
IP.6	POB	Defines the Output Buffer Full interrupt (IOB) priority level. POB=1 programs it to the higher priority level.
IP.5	PIB	Defines the Input Buffer Full interrupt (IIB) priority level. PIB=1 programs it to the higher priority level.
IP.4	PS	Defines the Serial Port interrupt priority level. PS=1 programs it to the higher priority level.
IP.3	PT1	Defines the Timer 1 interrupt priority level. PT1=1 programs it to the higher priority level.
IP.2	PX1	Defines the External Interrupt 1 priority level. PX1=1 programs it to the higher priority level.
IP.1	PT0	Enables or disables the Timer 0 interrupt priority level. PT0=1 programs it to the higher priority level.
IP.0	PX0	Defines the External Interrupt 0 priority level. PX0=1 programs it to the higher priority level.

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Figure 3. 8XC453 Interrupt Priority (IP) Register

	7	6	5	4	3	2	1	0
PCON (87H)	SMOD1	SMOD2	—	POF	GF1	GF0	PD	IDL

BIT	SYMBOL	FUNCTION
PCON.7	SMOD1	Double Baud rate bit. When set to a 1 and Timer 1 is used to generate baud rate, and the Serial Port is used in modes 1, 2, or 3.
PCON.6	SMOD0	If set to 1, SCON.7 will be the Framing Error bit (FE). If PCON.6 is cleared, SCON.7 will be SM0.
PCON.5	—	Reserved.
PCON.4	POF	Power Off Flag is set during power on of V_{CC}. If then cleared by software, it can be used to determine if a warm start has occurred.
PCON.3	GF1	General-purpose flag bit.
PCON.2	GF0	General-purpose flag bit.
PCON.1	PD	Power-Down bit. Setting this bit activates power-down mode. It can only be set if input $\overline{EW}$ is high.
PCON.0	IDL	Idle mode bit. Setting this bit activates the idle mode.

If logic 1s are written to PD and IDL at the same time, PD takes precedence.

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Figure 4. Power Control Register (PCON)

Table 2. Interrupt Table

POLLING PRIORITY	SOURCE	REQUEST BITS/FLAG	VECTOR ADDRESS
1	INTO	IE0	03H highest priority
2	Timer0	TF0	0BH
3	INT1	IE1	13H
4	Timer1	TF1	1BH
5	Port 6	OBF	33H
6	Serial I/O	RI,TI	23H
7	Port 6	IBF	2BH lowest priority

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7	6	5	4	3	2	1	0

(SMOD0 = 0/1)*

Symbol	Function
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	$f_{OSC}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$
1	1	3	9-bit UART	variable

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
*SMOD0 is located at PCON6.
**f_{OSC} = oscillator frequency

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Figure 5. Serial Port Control Register (SCON)

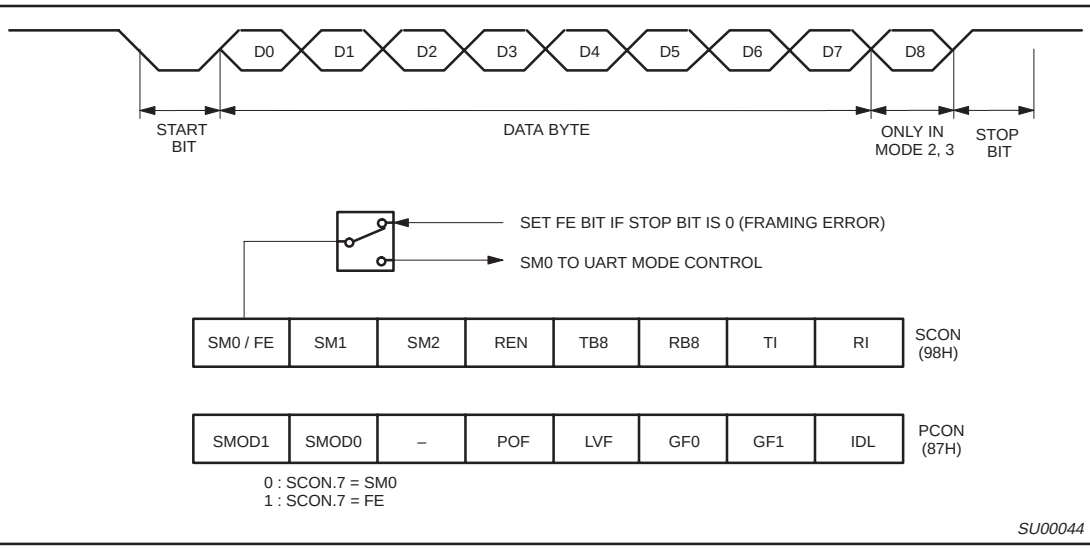

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Figure 6. UART Framing Error Detection

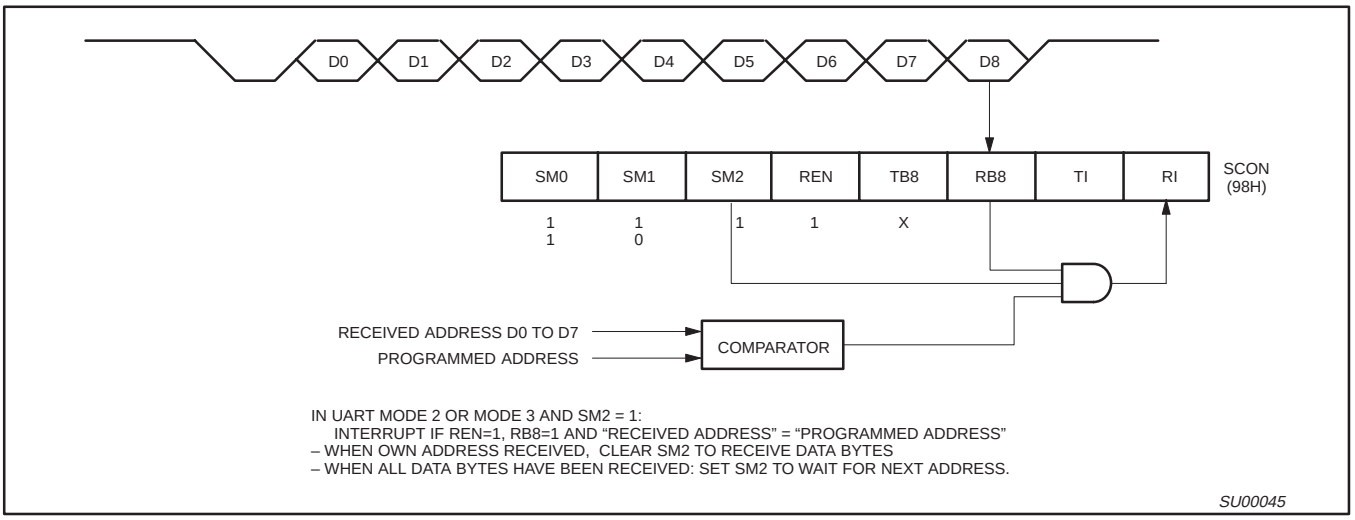


Figure 7. UART Multiprocessor Communication, Automatic Address Recognition

SPECIAL FUNCTION REGISTER ADDRESSES

Special function register addresses for the device are identical to those of the 80C51, except for the additional registers listed in Table 3.

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of this book for the 80C51. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 87C453 UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 5). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 6.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 7.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to b used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1101
	Given	=	1100 00X0
Slave 1	SADDR	=	1100 0000
	SADEN	=	1111 1110
	Given	=	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1001
	Given	=	1100 0XX0
Slave 1	SADDR	=	1110 0000
	SADEN	=	1111 1010
	Given	=	1110 0X0X
Slave 2	SADDR	=	1110 0000
	SADEN	=	1111 1100
	Given	=	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary t make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are teated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are leaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". this effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

The 87C453 UART has all of the capabilities of the standard 80C51 UART plus Framing Error Detection and Automatic Address Recognition. As in the 80C51, all four modes of operation are supported as well as the 9th bit in modes 2 and 3 that can be used to facilitate multiprocessor communication.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

Idle Mode

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 87C453 either a hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Power Off Flag

The Power Off Flag (POF) in PCON is set by on-chip circuitry when the V_{CC} level on the 87C453 rises from 0 to 5V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3V for the POF to remain unaffected by the V_{CC} level.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal rest algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 87C453 without having to remove the IC from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C453 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

PORTS 4 AND 5

Ports 4 and 5 are bidirectional I/O ports with internal pull-ups. Port 4 is an 8-bit port. Port 4 and port 5 pins with ones written to them, are pulled high by the internal pull-ups, and in that state can be used as inputs. Ports 4 and 5 are addressed at the special function register addresses shown in Table 3.

PORT 6

Port 6 is a special 8-bit bidirectional I/O port with internal pull-ups (see Figure 8). This port can be used as a standard I/O port, or in strobed modes of operation in conjunction with four special control lines: $\overline{ODS}$, $\overline{IDS}$, AFLAG, and BFLAG. Port 6 operating modes are controlled by the port 6 control status register (CSR). Port 6 and the CSR are addressed at the special function register addresses shown in Table 3. The following four control pins are used in conjunction with port 6:

$\overline{ODS}$ – Output data strobe for port 6. $\overline{ODS}$ can be programmed to control the port 6 output drivers and the output buffer full flag (OBF), or to clear only the OBF flag bit in the CSR (output-always mode).

$\overline{ODS}$ is active low for output driver control. The OBF flag can be programmed to be cleared on the negative or positive edge of $\overline{ODS}$. Can produce an IOB interrupt (see Figure 2).

$\overline{IDS}$ – Input data strobe for port 6. $\overline{IDS}$ is used to control the port 6 input latch and input buffer full flag (IBF) bit in the CSR. The input data latch can be programmed to be transparent when $\overline{IDS}$ is low and latched on the positive transition of $\overline{IDS}$, or to latch only on the positive transition of $\overline{IDS}$. Correspondingly, the IBF flag is set on the negative or positive transition of $\overline{IDS}$. Can produce an IIB interrupt (see Figure 2).

AFLAG – AFLAG is a bidirectional I/O pin which can be programmed to be an output set high or low under program control, or to output the state of the output buffer full flag. AFLAG can also be programmed to be an input which selects whether the contents of the output buffer, or the contents of the port 6 control status register will output on port 6. This feature grants complete port 6 status to external devices.

BFLAG – BFLAG is a bidirectional I/O pin which can be programmed to be an output, set high or low under program control, or to output the state of the input buffer full flag. BFLAG can also be programmed to input an enable signal for port 6. When BFLAG is used as an enable input, port 6 output drivers are in the high-impedance state, and the input latch does not respond to the $\overline{IDS}$ strobe when BFLAG is high. Both features are enabled when BFLAG is low. This feature facilitates the use of the 87C453 in bused multiprocessor systems.

CONTROL STATUS REGISTER

The control status register (CSR) establishes the mode of operation for port 6 and indicates the current status of port 6 I/O registers. All control status register bits can be read and written by the CPU, except bits 0 and 1, which are read only. Reset writes ones to bits 2 through 7, and writes zeros to bits 0 and 1 (see Table 4).

CSR.0 Input Buffer Full Flag (IBF) (Read Only) – The IBF bit is set to a logic 1 when port 6 data is loaded into the input buffer under control of $\overline{IDS}$. This can occur on the negative or positive edge of $\overline{IDS}$, as determined by CSR.2. When IBF is set, the Interrupt Enable Register bit IIB (IE.5) is set. The Interrupt Service Routine vector address for this interrupt is 002BH. IBF is cleared when the CPU reads the input buffer register.

CSR.1 Output Buffer Full Flag (OBF) (Read Only) – The OBF flag is set to a logic 1 when the CPU writes to the port 6 output data buffer. OBF is cleared by the positive or negative edge of $\overline{ODS}$, as determined by CSR.3. When OBF is cleared, the Interrupt Enable Register bit IOB (IE.6) is set. The Interrupt Service Routine vector address for this interrupt is 0033H.

CSR.2 IDS Mode Select (IDSM) – When CSR.2 = 0, a low-to-high transition on the $\overline{IDS}$ pin sets the IBF flag. The Port 6 input buffer is loaded on the $\overline{IDS}$ positive edge. When CSR.2 = 1, a high-to-low transition on the $\overline{IDS}$ pin sets the IBF flag. Port 6 input buffer is transparent when $\overline{IDS}$ is low, and latched when $\overline{IDS}$ is high.

CSR.3 Output Buffer Full Flag Clear Mode (OBFC) – When CSR.3 = 1, the positive edge of the $\overline{ODS}$ input clears the OBF flag. When CSR.3 = 0, the negative edge of the $\overline{ODS}$ input clears the OBF flag.

CSR.4, CSR.5 AFLAG Mode Select (MA0, MA1) – Bits 4 and 5 select the mode of operation for the AFLAG pin as follows:

MA1	MA0	AFLAG Function
0	0	Logic 0 output
0	1	Logic 1 output
1	0	OBF flag output (CSR.1)
1	1	Select (SEL) input mode

The select (SEL) input mode is used to determine whether the port 6 data register or the control status register is output on port 6. When the select feature is enabled, the AFLAG input controls the source of port 6 output data. A logic 0 on AFLAG input selects the port 6 data register, and a logic 1 on AFLAG input selects the control status register.

The value of the AFLAG input is latched into the Auxiliary Register (AUXR) bit 1 (AUXR.1). Checking this bit (AF) will allow the 87C453's program to determine if Port 6 was loaded with data or a UPI command.

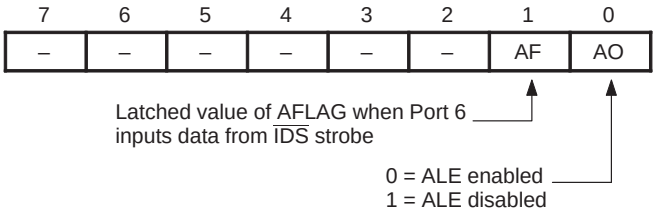
CSR.6, CSR.7 BFLAG Mode Select (MB0, MB1) – Bits 6 and 7 select the mode operation as follows:

MB1	MB0	BFLAG Function
0	0	Logic 0 output
0	1	Logic 1 output
1	0	IBF flag output (CSR.0)
1	1	Port enable ($\overline{PE}$)

In the port enable mode, $\overline{IDS}$ and $\overline{ODS}$ inputs are disabled when BFLAG input is high. When the BFLAG input is low, the port is enabled for I/O.

Reduced EMI Mode – The on–chip clock distribution drivers have been identified as the cause of most of the EMI emissions from the 80C51 family. By tailoring the clock drivers properly, a compromise between maximum operating speed and minimal EMI emissions can be achieved. Typically, an order in magnitude of reduction is possible over previous designs. This feature has been implemented on this chip along with the additional capability of turning off the ALE output. Setting the AO bit (AUXR.0) in the AUXR special function register will disable the ALE output. Reset forces a 0 into AUXR.0 to enable normal 80C51 type operation.

Auxiliary Register (AUXR)



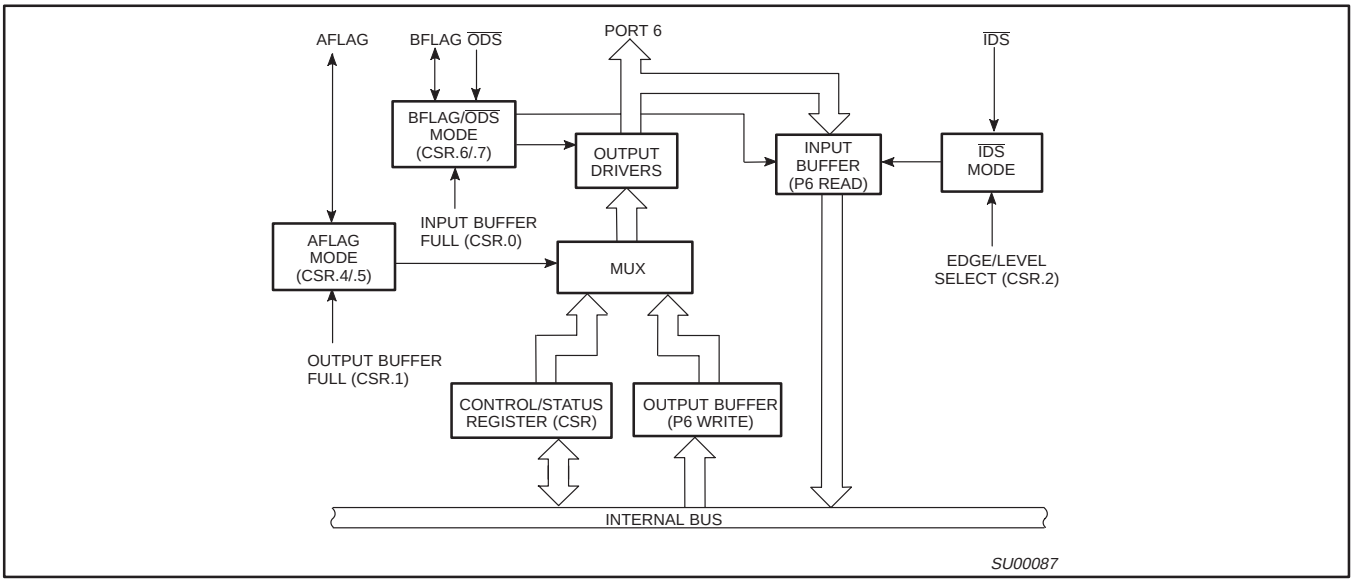


Figure 8. Port 6 Block Diagram

Table 3. Special Function Register Addresses

REGISTER ADDRESS			BIT ADDRESS							
Name	**Symbol**	**Address**	**MSB**							**LSB**
Port 4	P4	C0	C7	C6	C5	C4	C3	C2	C1	C0
Port 5	P5	C8	CF	CE	CD	CC	CB	CA	C9	C8
Port 6 data	P6	D8	DF	DE	DD	DC	DB	DA	D9	D8
Port 6 control status	CSR	E8	EF	EE	ED	EC	EB	EA	E9	E8
Slave address	SADDR	A9								
Slave address mask	SADEN	B9								
Auxiliary Register	AUXR	8E								

Table 4. Control Status Register (CSR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MB1	**MB0**	**MA1**	**MA0**	**OBFC**	**IDSM**	**OBF**	**IBF**
BFLAG Mode Select		AFLAG Mode Select		Output Buffer Flag Clear Mode	Input Data Strobe Mode	Output Buffer Flag Full	Input Buffer Flag Full
0/0 = Logic 0 output* 0/1 = Logic 1 output* 1/0 = IBF output 1/1 = $\overline{PE}$ input (0 = Select) (1 = Disable I/O)		0/0 = Logic 0 output* 0/1 = Logic 1 output* 1/0 = OBF output 1/1 = SEL input (0 = Select) (1 = Control/status)		0 = Negative edge of $\overline{ODS}$ 1 = Positive edge o $\overline{ODS}$	0 = Positive edge of $\overline{IDS}$ 1 = Low level of $\overline{IDS}$	0 = Output data buffer empty 1 = Output data buffer full	0 = Input data buffer empty 1 = Input data buffer full

NOTE:
* Output-always mode: MB1 = 0, MA1 = 1, and MA0 = 0. In this mode, port 6 is always enabled for output. $\overline{ODS}$ only clears the OBF flag.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70	°C
Storage temperature range	–65 to +150	°C
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. Voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage; ports 0, 1, 2, 3, 4, 5, 6, $\overline{IDS}$, $\overline{ODS}$, AFLAG, BFLAG; except $\overline{EA}$		–0.5		$0.2V_{CC}$–0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$		0		$0.2V_{CC}$–0.3	V
V_{IH}	Input high voltage; except XTAL1, RST		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage; XTAL1, RST		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage; ports 1, 2, 3, 4, 5, 6, AFLAG, BFLAG	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage; port 0, ALE, $\overline{PSEN}$	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage; ports 1, 2, 3, 4, 5, 6, AFLAG, BFLAG	I_{OH} = –60µA, I_{OH} = –25µA I_{OH} = –10µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)[3]	I_{OH} = –800µA, I_{OH} = –300µA I_{OH} = –80µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
I_{IL}	Logical 0 input current,; ports 1, 2, 3, 4, 5, 6	V_{IN} = 0.45V			–50	µA
I_{TL}	Logical 1-to-0 transition current; ports 1, 2, 3, 4, 5, 6	See note 4			–650	µA
I_{LI}	Input leakage current; port 0	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{CC}	Power supply current: Active mode @ 16MHz[5] Idle mode @ 16MHz[5] Power down mode	See note 6		 11.5 1.3 3	 25 4 50	 mA mA µA
R_{RST}	Internal reset pull-down resistor		50		300	kΩ
C_{IO}	Pin capacitance[7] – PLCC package				10	pF

NOTES:
1. Typical ratings are based on a limited number of samples from early manufacturing lots, and not guaranteed. Values are room temp., 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and the other ports. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input..
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. Pins of ports 1, 2, 3, 4, 5 and 6 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. I_{CC}MAX at other frequencies is given by:
   Active mode: I_{CC}MAX = 0.94 X FREQ + 13.71
   Idle mode: I_{CC}MAX = 0.14 X FREQ +2.31
   where FREQ is the external oscillator frequency in MHz. I_{CC}MAX is given in mA. See Figure 20.
6. See Figures 21 through 24 for I_{CC} test conditions.
7. C_{IO} applies to ports 1 through 6, $\overline{IDS}$, $\overline{ODS}$, AFLAG, BFLAG, XTAL1, XTAL2.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$		Oscillator frequency			3.5	16	MHz
t_{LHLL}	9	ALE pulse width	85		$2t_{CLCL}$–40		ns
t_{AVLL}	9	Address valid to ALE low	22		t_{CLCL}–40		ns
t_{LLAX}	9	Address hold after ALE low	32		t_{CLCL}–30		ns
t_{LLIV}	9	ALE low to valid instruction in		150		$4t_{CLCL}$–100	ns
t_{LLPL}	9	ALE low to $\overline{PSEN}$ low	32		t_{CLCL}–30		ns
t_{PLPH}	9	$\overline{PSEN}$ pulse width	142		$3t_{CLCL}$–45		ns
t_{PLIV}	9	$\overline{PSEN}$ low to valid instruction in		82		$3t_{CLCL}$–105	ns
t_{PXIX}	9	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	9	Input instruction float after $\overline{PSEN}$		37		t_{CLCL}–25	ns
t_{AVIV}	9	Address to valid instruction in		207		$5t_{CLCL}$–105	ns
t_{PLAZ}	9	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	10, 11	$\overline{RD}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{WLWH}	10, 11	$\overline{WR}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{RLDV}	10, 11	$\overline{RD}$ low to valid data in		147		$5t_{CLCL}$–165	ns
t_{RHDX}	10, 11	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	10, 11	Data float after $\overline{RD}$		65		$2t_{CLCL}$–60	ns
t_{LLDV}	10, 11	ALE low to valid data in		350		$8t_{CLCL}$–150	ns
t_{AVDV}	10, 11	Address to valid data in		397		$9t_{CLCL}$–165	ns
t_{LLWL}	10, 11	ALE low to $\overline{RD}$ or $\overline{WR}$ low	137	239	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	10, 11	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	122		$4t_{CLCL}$–130		ns
t_{QVWX}	10, 11	Data valid to $\overline{WR}$ transition	13		t_{CLCL}–50		ns
t_{WHQX}	10, 11	Data hold after $\overline{WR}$	13		t_{CLCL}–50		ns
t_{RLAZ}	10, 11	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	10, 11	$\overline{RD}$ or $\overline{WR}$ high to ALE high	23	103	t_{CLCL}–40	t_{CLCL}+40	ns
Shift Register							
t_{XLXL}	12	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	12	Output data setup to clock rising edge	492		$10t_{CLCL}$–133		ns
t_{XHQX}	12	Output data hold after clock rising edge	8		$2t_{CLCL}$–117		ns
t_{XHDX}	12	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	12	Clock rising edge to input data valid		492		$10t_{CLCL}$–133	ns
Port 6 input (input rise and fall times = 5ns)							
t_{FLFH}	15	$\overline{PE}$ width	209		$3t_{CLCL}$+20		ns
t_{ILIH}	15	$\overline{IDS}$ width	209		$3t_{CLCL}$+20		ns
t_{DVIH}	15	Data setup to $\overline{IDS}$ high or $\overline{PE}$ high	0		0		ns
t_{IHDZ}	15	Data hold after $\overline{IDS}$ high or $\overline{PE}$ high	30		30		ns
t_{IVFV}	16	$\overline{IDS}$ to BFLAG (IBF) delay		130		130	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
Port 6 output							
t_{OLOH}	13	$\overline{ODS}$ width	209		$3t_{CLCL}+20$		ns
t_{FVDV}	14	SEL to data out delay		85		85	ns
t_{OLDV}	13	$\overline{ODS}$ to data out delay		80		80	ns
t_{OHDZ}	13	$\overline{ODS}$ to data float delay		35		35	ns
t_{OVFV}	13	$\overline{ODS}$ to AFLAG (OBF) delay		100		100	ns
t_{FLDV}	13	$\overline{PE}$ to data out delay		120		120	ns
t_{OHFH}	14	$\overline{ODS}$ to AFLAG (SEL) delay	100		100		ns
External Clock							
t_{CHCX}	17	High time	20		20		ns
t_{CLCX}	17	Low time	20		20		ns
t_{CLCH}	17	Rise time		20		20	ns
t_{CHCL}	17	Fall time		20		20	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

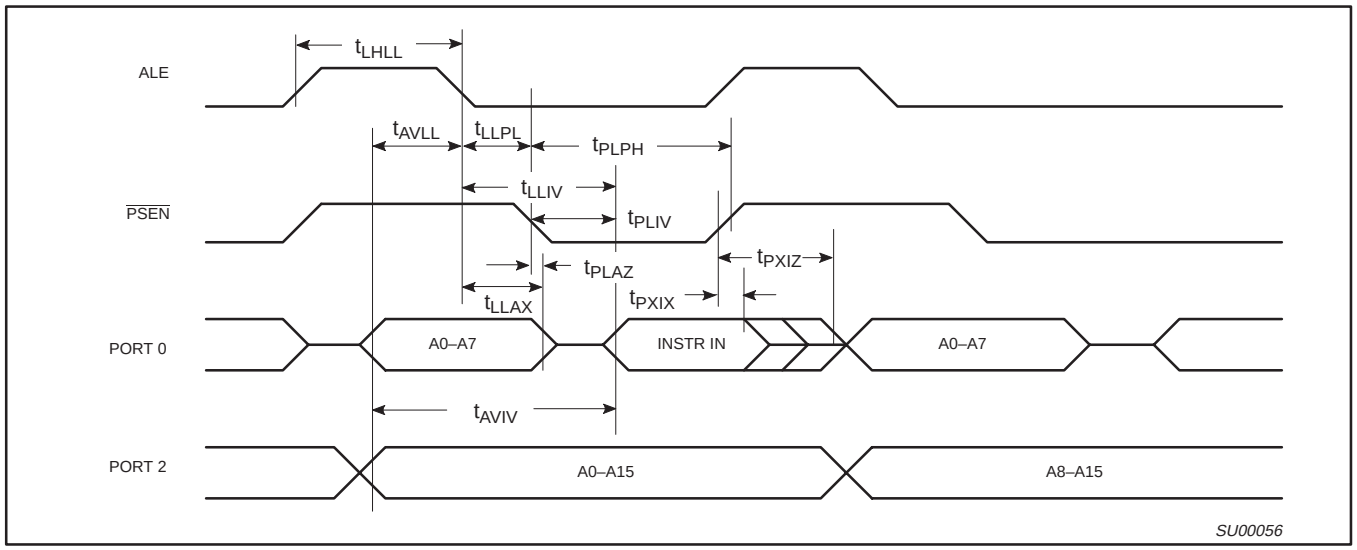


Figure 9. External Program Memory Read Cycle

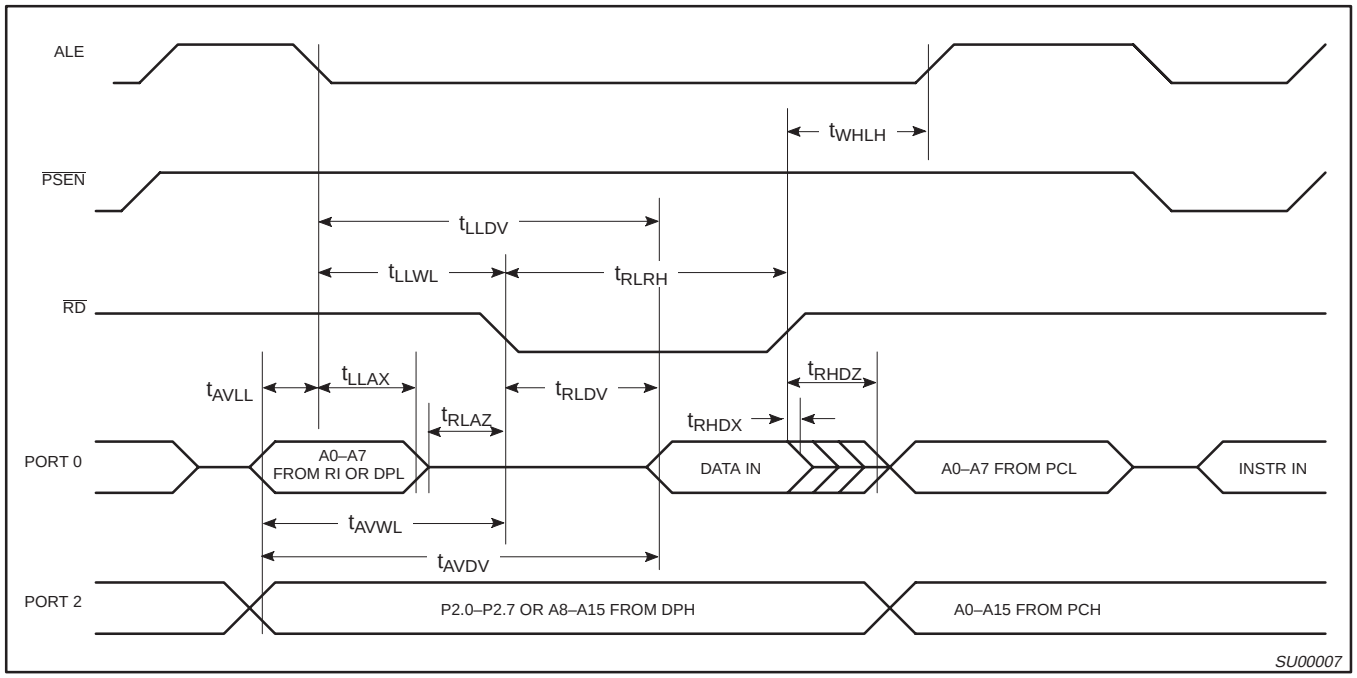


Figure 10. External Data Memory Read Cycle

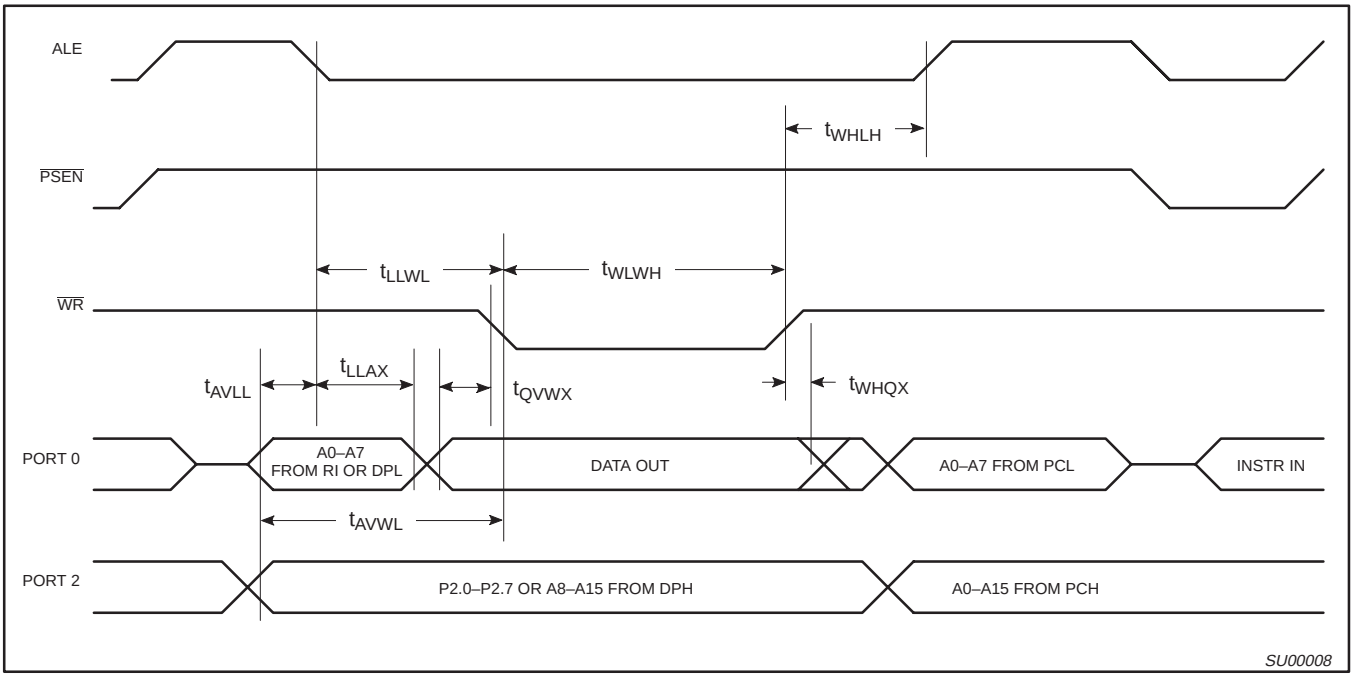


Figure 11. External Data Memory Write Cycle

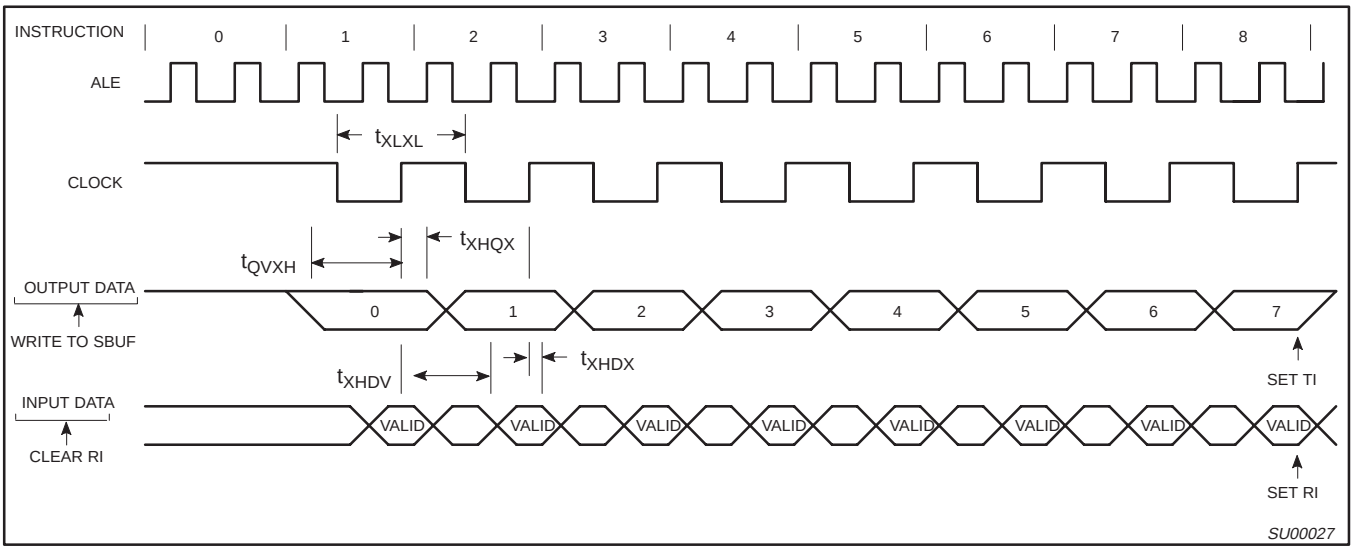


Figure 12. Shift Register Mode Timing

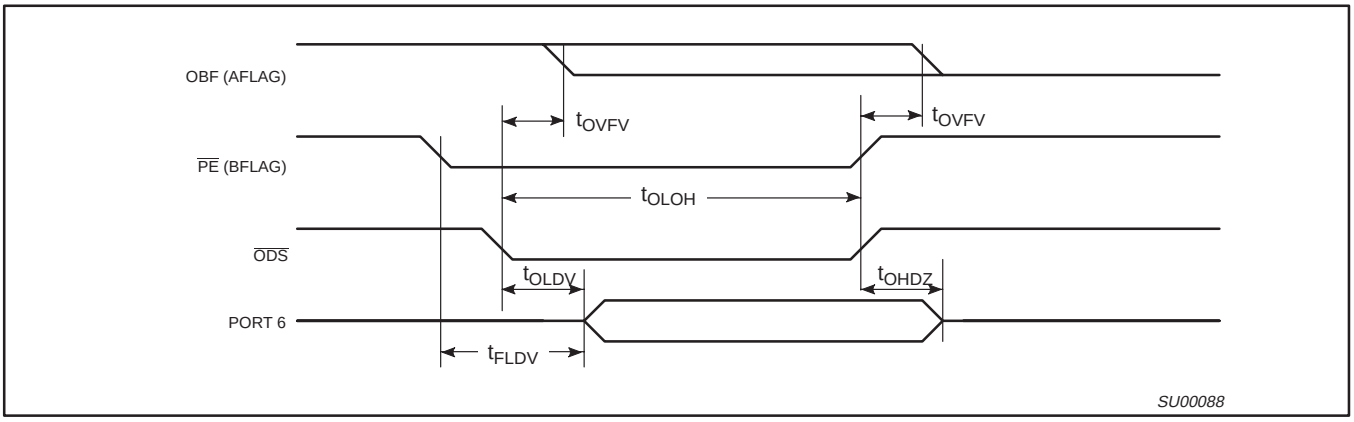


Figure 13. Port 6 Output

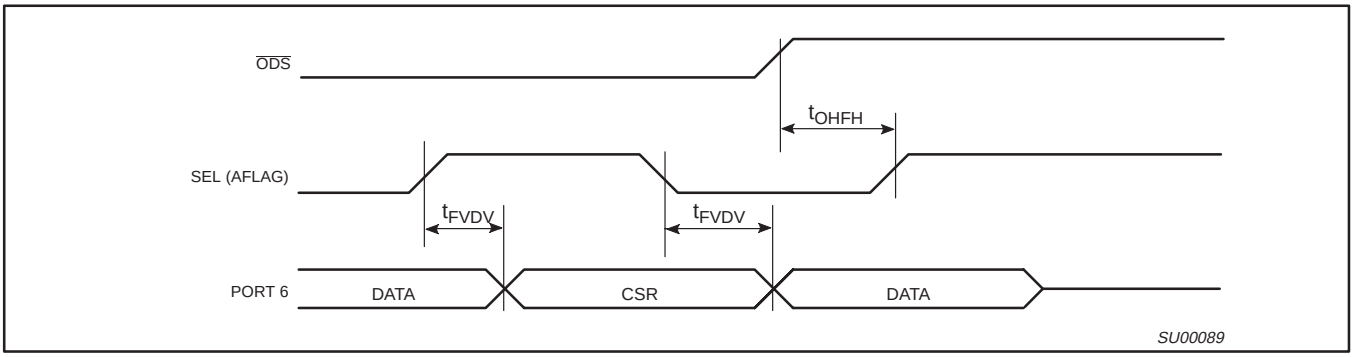


Figure 14. Port 6 Select Mode

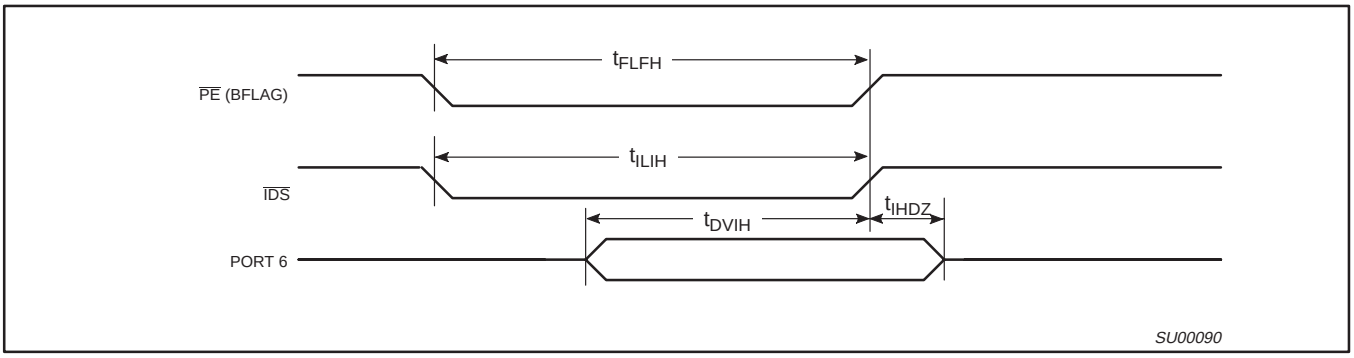


Figure 15. Port 6 Input

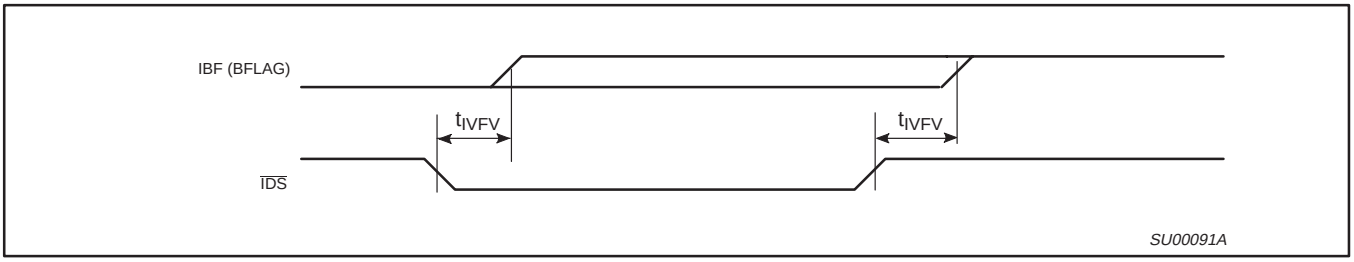


Figure 16. IBF Flag Output

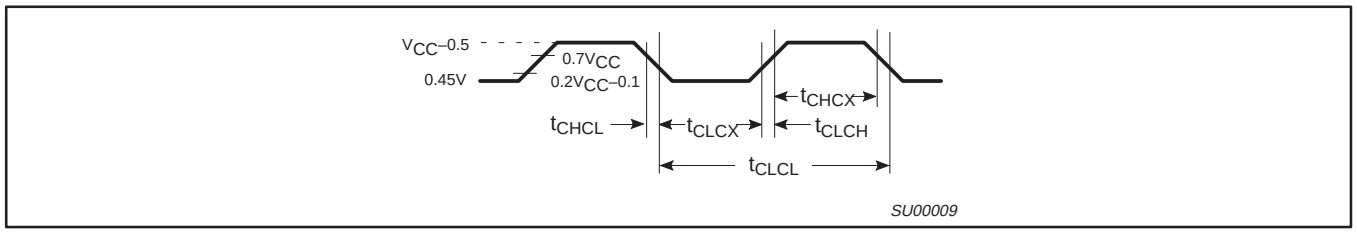


Figure 17. External Clock Drive

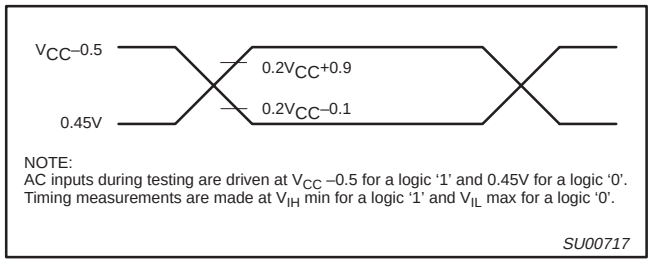


Figure 18. AC Testing Input/Output

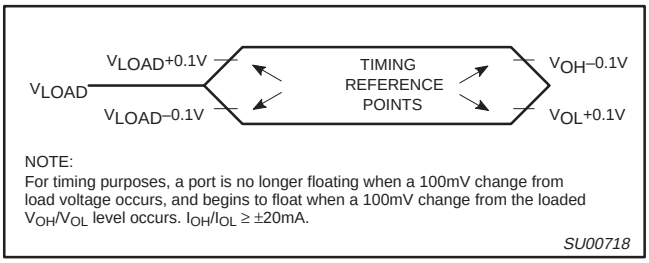


Figure 19. Float Waveform

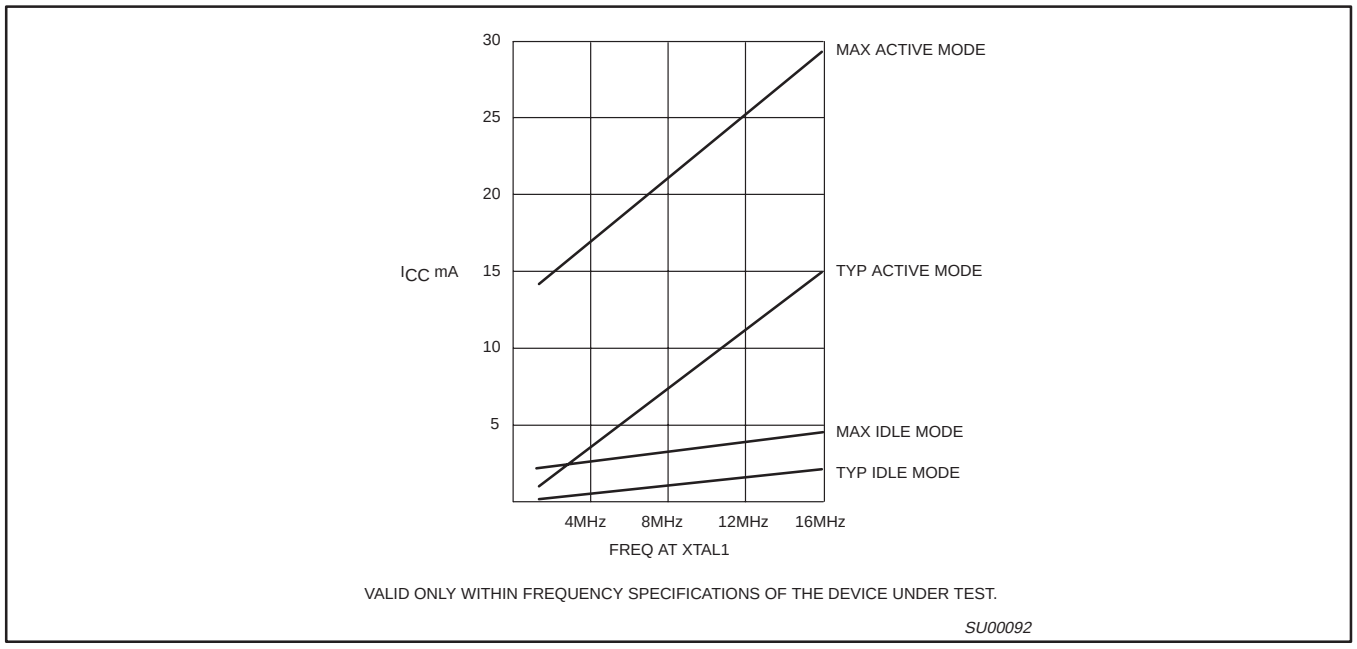


Figure 20. I_{CC} vs. FREQ

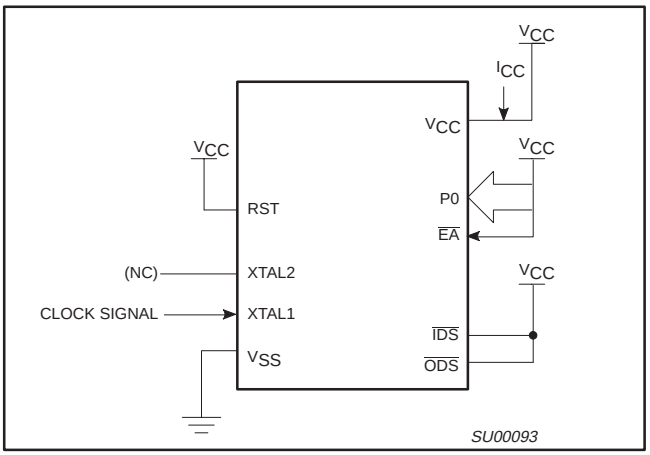


Figure 21. I_{CC} Test Condition, Active Mode
All other pins are disconnected

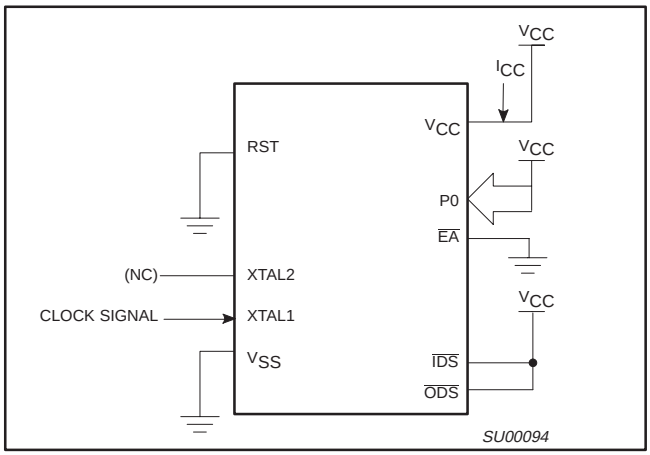


Figure 22. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

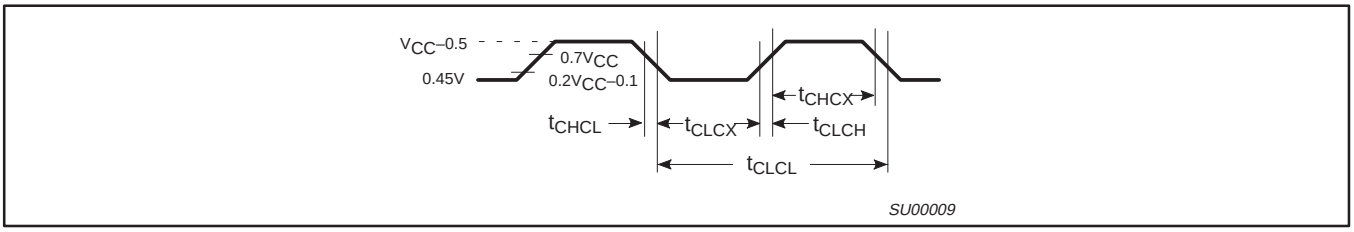


Figure 23. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

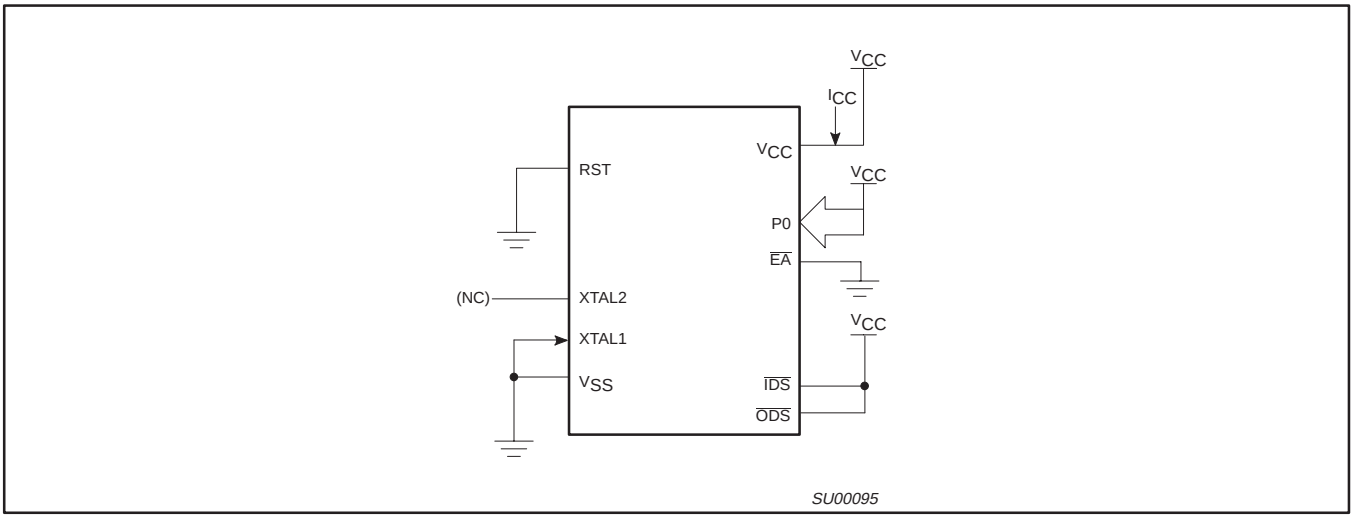


Figure 24. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. V_{CC} = 2V to 5.5V

EPROM CHARACTERISTICS

The 87C453 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C453 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C453 manufactured by Philips Semiconductors.

Table 5 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 25 and 26. Figure 27 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 26. Note that the 87C453 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 25. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 5 are held at the 'Program Code Data' levels indicated in Table 5. The ALE/$\overline{PROG}$ is pulsed low 15 to 25 times, as shown in Figure 26.

To program the encryption table, repeat the 15 to 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 15 to 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 27. The other pins are held at the 'Verify Code Data' levels indicated in Table 5. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:
(030H) = 15H indicates manufactured by Philips
(031H) = B9H indicates 87C453

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 5, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 5. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V ±10% during programming and verification.
* ALE/$\overline{PROG}$ receives 15 to 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

™Trademark phrase of Intel Corporation.

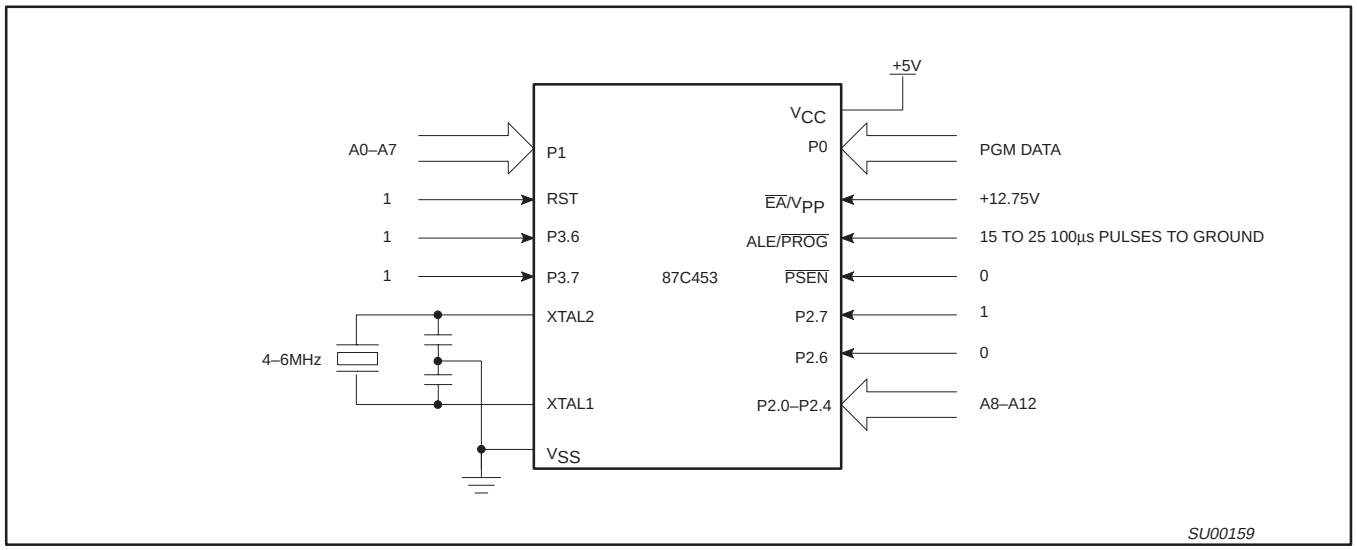


Figure 25. Programming Configuration

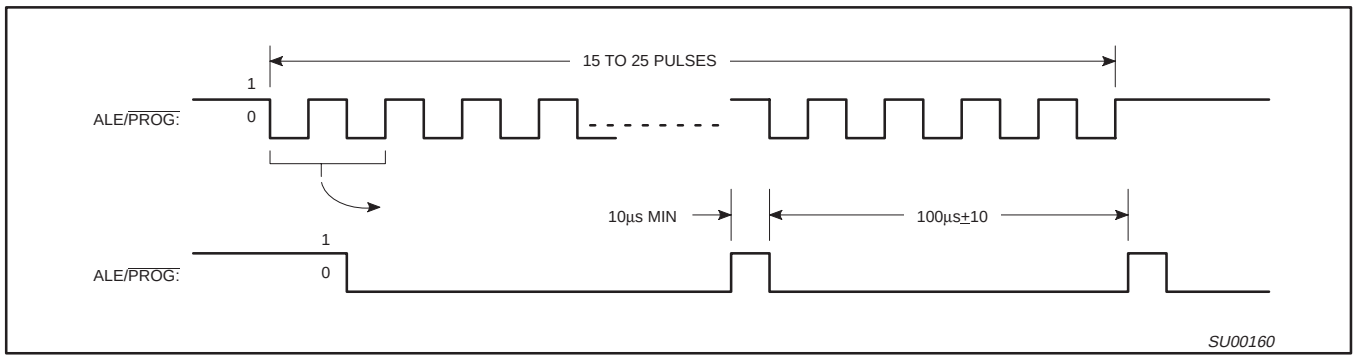


Figure 26. $\overline{\text{PROG}}$ Waveform

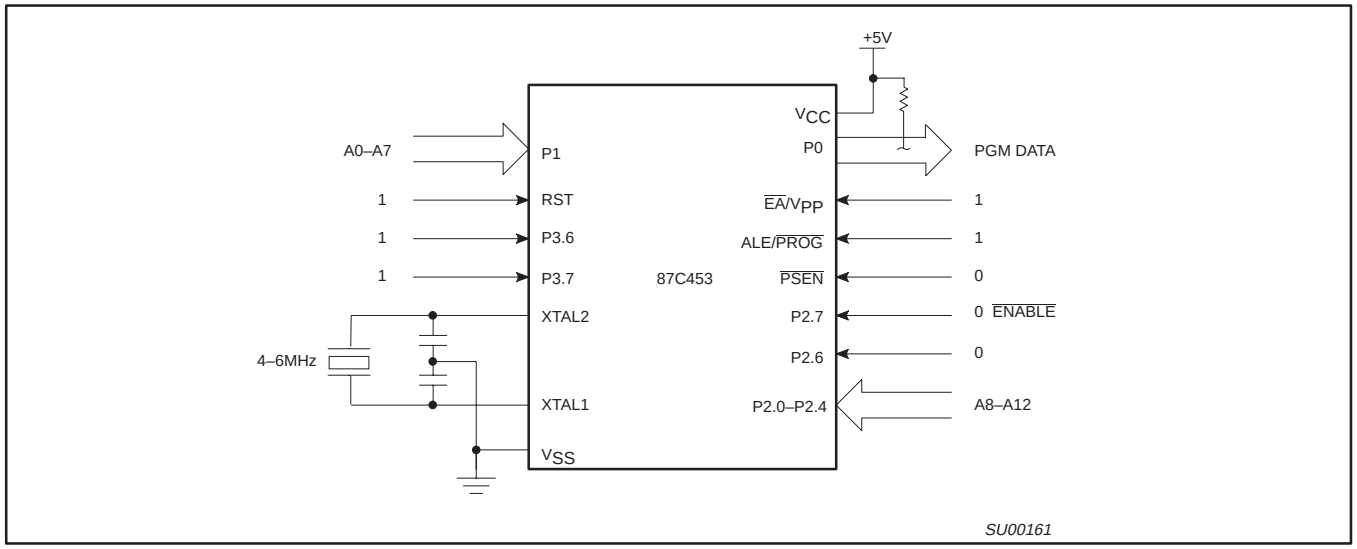
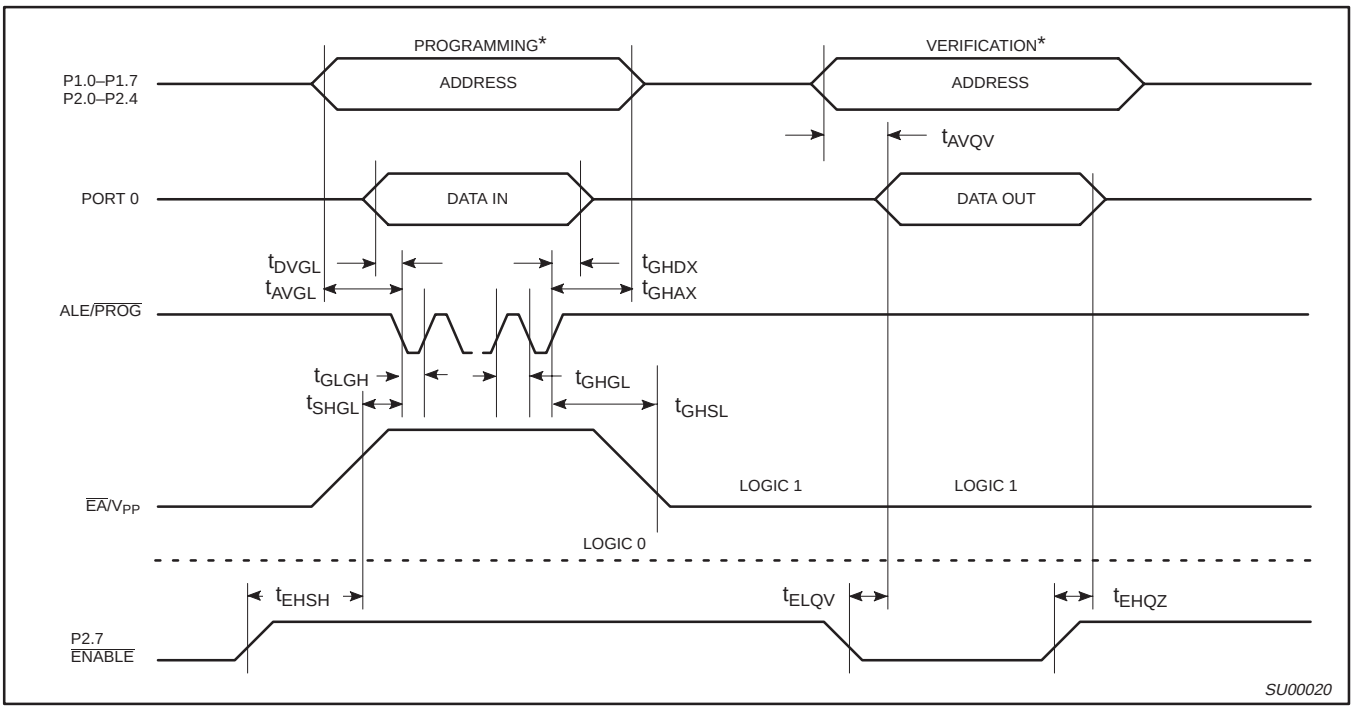


Figure 27. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 28)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

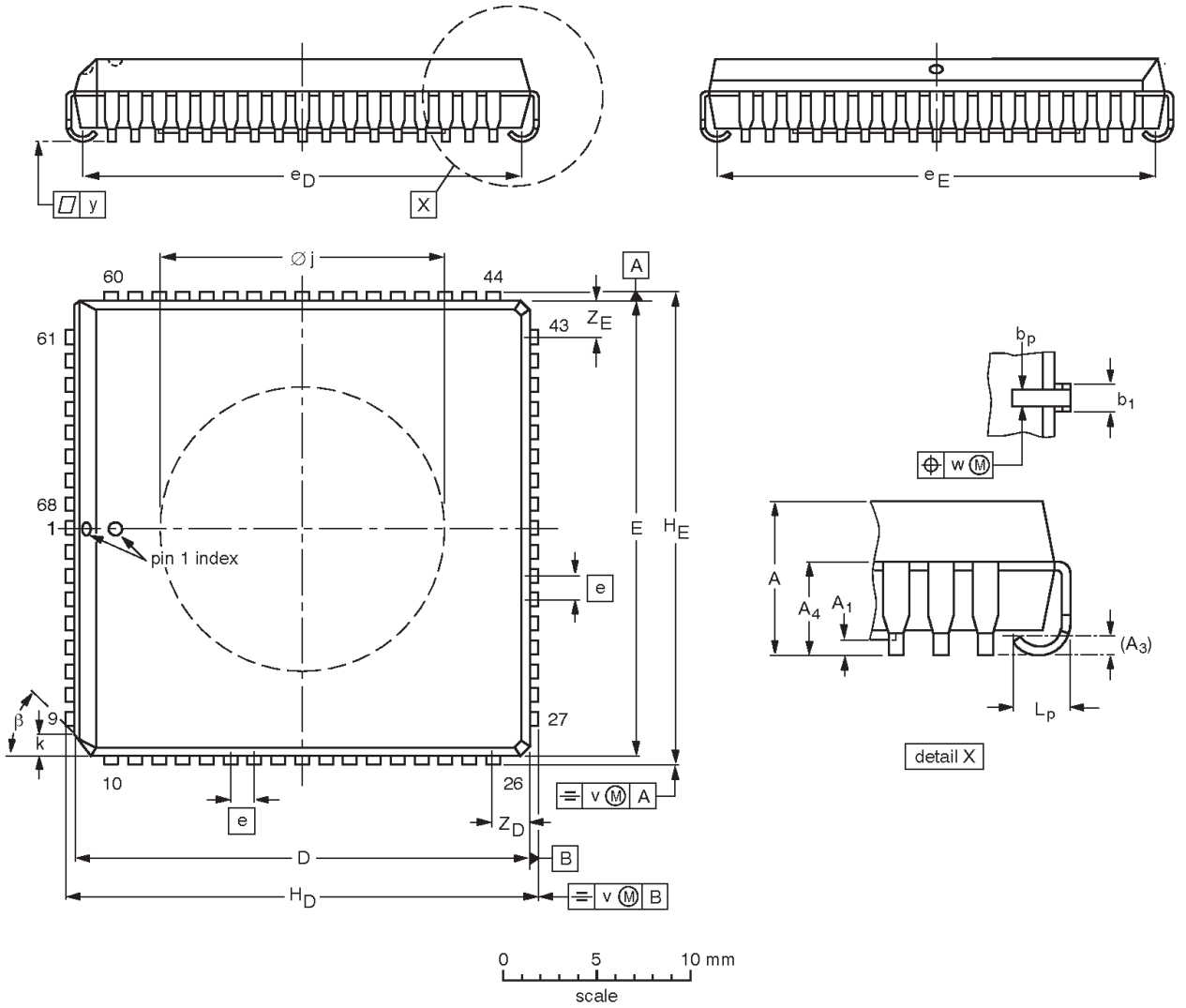


NOTE:

* FOR PROGRAMMING VERIFICATION SEE FIGURE 25.
FOR VERIFICATION CONDITIONS SEE FIGURE 27.

Figure 28. EPROM Programming and Verification

PLCC68: plastic leaded chip carrier; 68 leads; pedestal SOT188-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	15.34 15.19	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.604 0.598	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-3	112E10	MO-047AE				~~95-02-25~~ 97-12-16

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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