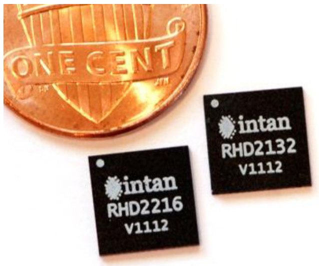
intan TECHNOLOGIES, LLC

RHD2216
RHD2132



Digital Electrophysiology Interface Chips

11 December 2012

Features

- Fully integrated electrophysiology amplifier array with on-chip 16-bit analog-to-digital converter (ADC) and industry-standard serial peripheral interface (SPI)
- ADC operation to 1.05 MSamples per second; supports sampling 32 amplifier channels at 30 kSamples/s each
- Low input-referred noise: 2.4 μV_{rms} typical
- Standard four-wire 16-bit SPI interface with CMOS or low-voltage differential signaling (LVDS) I/O pins
- Upper cutoff frequency of all amplifiers set by on-chip registers; adjustable from 100 Hz to 20 kHz
- Lower cutoff frequency of all amplifiers set by on-chip registers; adjustable from 0.1 Hz to 500 Hz
- Integrated multi-frequency *in situ* electrode impedance measurement capability
- Optional on-chip DSP high-pass filters for amplifier offset removal
- Auxiliary ADC inputs for interfacing additional sensors.
- Individual amplifier power up/down for power minimization

Applications

- Miniaturized multi-channel headstages for neural or ECoG recording
- Low-power wireless headstages or backpacks for electrophysiology experiments
- Recording spikes and/or local field potentials (LFPs) from microelectrodes
- "Smart Petri dish" *in vitro* recording systems
- Portable EKG or EMG monitoring systems
- Advanced prosthetic limb controller front-ends

Description

The Intan Technologies RHD2000-series microchips are complete low-power electrophysiology signal acquisition systems. These patent-pending devices contain arrays of low-noise amplifiers with programmable bandwidths and are suitable for a wide variety of biopotential monitoring applications. Innovative circuit architecture combines amplifiers, analog and digital filters, a multiplexed 16-bit analog-to-digital converter (ADC), and a flexible electrode impedance measurement module onto a single silicon chip. **In practice, many recording electrodes are connected directly to one side of the chip, and serial digital data exits the other side on a standard SPI bus.**

The upper and lower bandwidths of the amplifiers may be dynamically programmed by means of internal registers on each chip. This flexibility allows the chips to be optimized for different types of signals (e.g., 0.1 – 100 Hz for EKG signals, 250 Hz – 7.5 kHz for neural action potentials). Internal capacitors reject DC offset voltages at the input electrodes, eliminating problems with built-in potentials at the electrode-tissue interface.

A low-distortion, high-speed analog multiplexer (MUX) allows many amplifiers to share the on-chip ADC. The ADC can sample each channel up to 30 kSamples/s. Each chip includes three auxiliary input pins for connecting external sensors or other analog voltages which may be sampled using the ADC. Additional on-chip circuitry enables *in situ* electrode impedance measurements at user-programmable frequencies. By transforming weak electrode signals directly into a digital data stream, **the RHD2000 replaces all analog instrumentation circuitry** in electrophysiology monitoring and acquisition systems.

RHD2000-series chips are packaged in standard 8mm × 8mm QFN surface mount packages, or available in bare die form. The small footprint and low power consumption of the multi-channel chips enable the miniaturization of front end electronics for miniature headstages and other wearable or portable biopotential recording systems.

Simplified Chip Diagrams

RHD2000-SERIES FAMILY

There are two devices in the RHD2000-series electrophysiology interface family: the RHD2216 and RHD2132. The following table lists the features of these chips:

DEVICE	AMPLIFIERS PER CHIP	AMPLIFIER INPUT PINS	PACKAGE SIZE	BARE DIE SIZE
RHD2216	16	16 × 2 differential amplifier inputs	8 mm × 8 mm 56-pin QFN	4.8 mm × 4.1 mm
RHD2132	32	32 unipolar amplifier inputs; 1 common reference input	8 mm × 8 mm 56-pin QFN	4.8 mm × 4.1 mm

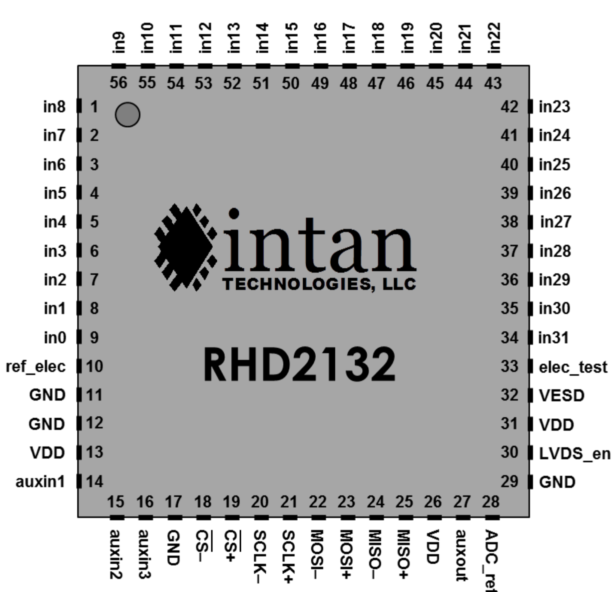
The positive and negative amplifier inputs on the RHD2216 have balanced input impedances; this will provide the best rejection of common-mode noise (most commonly, 50/60 Hz interference) if all electrodes, including reference electrodes, are roughly the same impedance. This is usually the case for surface EMG, EKG, and EEG recording.

The RHD2132 can be used in applications where the reference electrode has a much different impedance than the recording electrodes (e.g., microelectrodes for neural recording with a platinum reference wire) or in cases where common-mode noise will not be severe (e.g., implanted devices). The common reference input on the RHD2132 (**ref_elec**) is connected to the negative input of all 32 amplifiers, and therefore has an input impedance 32 times lower than the individual amplifier inputs. See the "Electrical Characteristics" section for details.

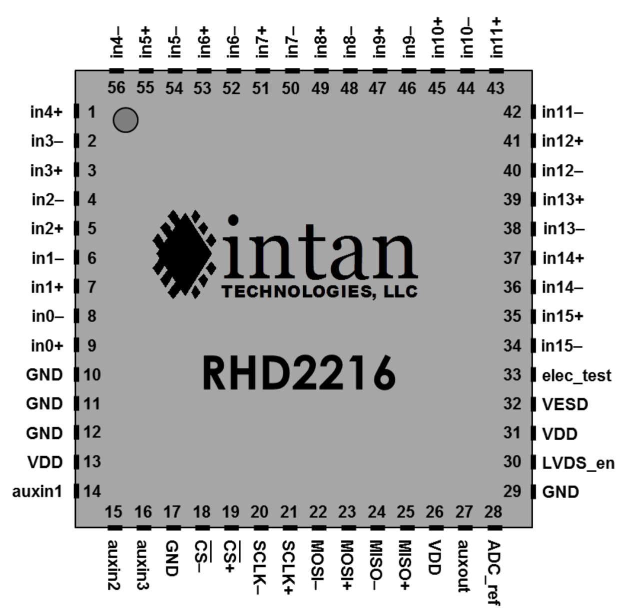
Simplified functional block diagrams of these chips are shown on the following pages.

Package Descriptions

RHD2132: 56-Pin QFN Package

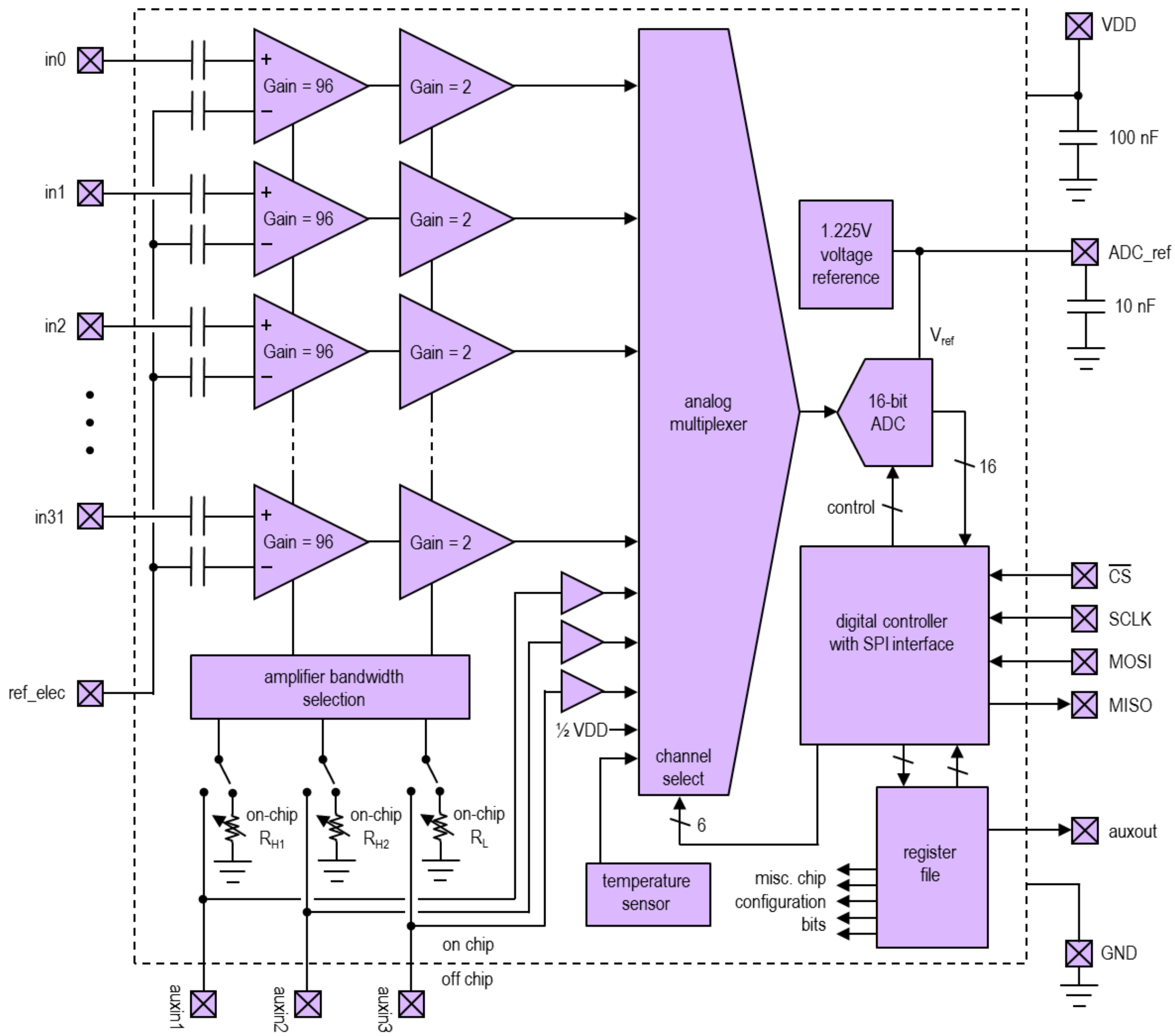


RHD2216: 56-Pin QFN Package



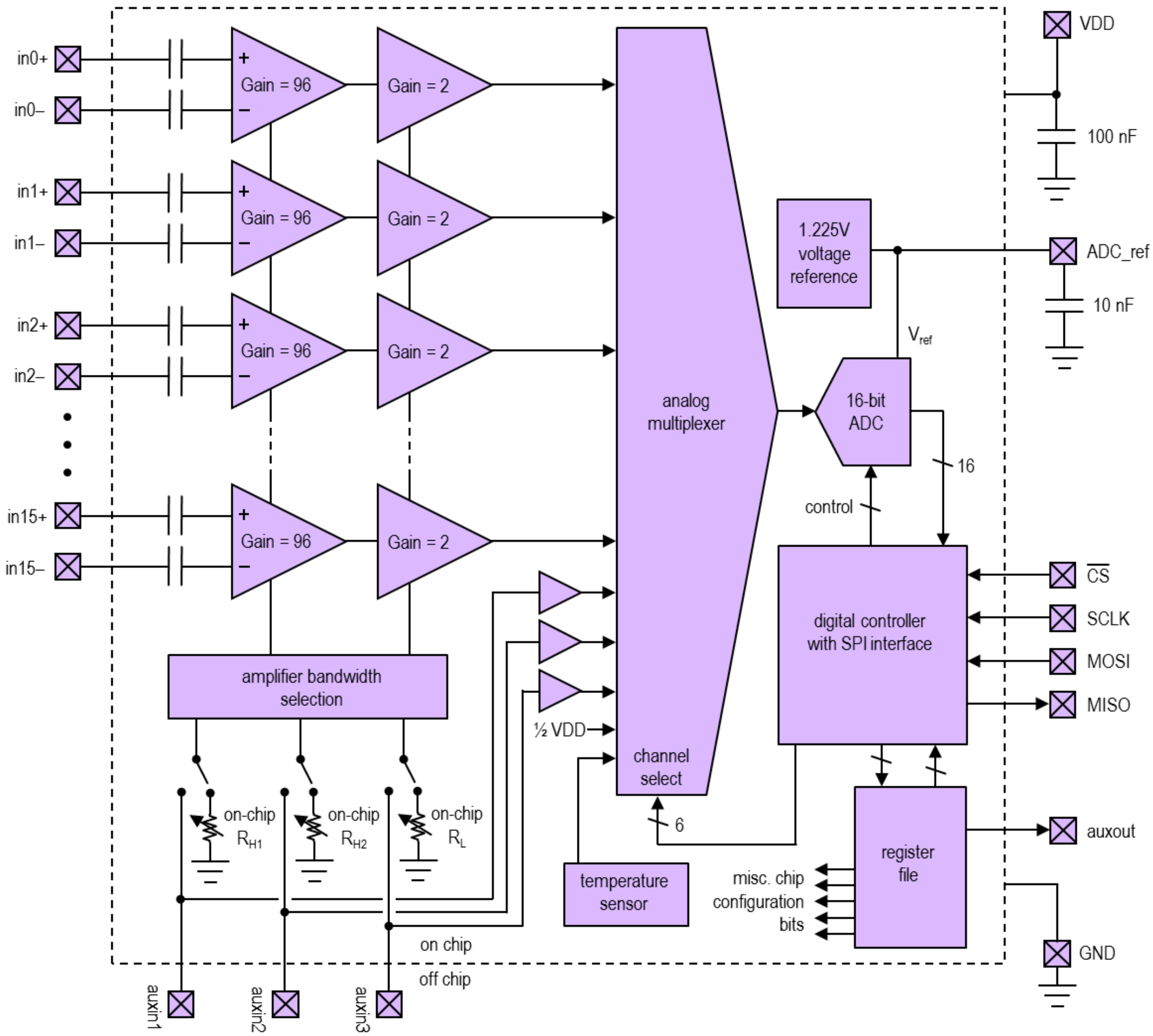
RHD2132 Simplified Diagram

The RHD2132 contains an array of 32 amplifiers having unipolar inputs (**in0**, **in1**,...) and a common, shared reference line (**ref_elec**).



RHD2216 Simplified Diagram

The RHD2216 contains an array of 16 amplifiers having independently accessible differential inputs (**in0+**, **in0–**, **in1+**, **in1–**,…).



Pin Descriptions

PIN	TYPE	FUNCTION
VDD, GND	power	3.3V power supply (3.2V – 3.6V). All **VDD** pins must be connected to the same potential. All **GND** pins must be connected to the same potential. (See the "Supply Voltage Levels" section for derating under 3.0V operation.)
in0, in1, in2,…	analog inputs	Unipolar amplifier inputs (RHD2132 only).
ref_elec	analog input	Amplifier array common reference (negative) input (RHD2132 only).
in0+, in0–,…	analog inputs	Differential (bipolar) amplifier inputs (RHD2216 only).
LVDS_en	digital input	When **LVDS_en** is pulled high, communication with the SPI data bus is conducted using low-voltage differential signaling (LVDS). When **LVDS_en** is pulled low, SPI communication uses traditional CMOS-level signaling.
$\overline{\mathbf{CS}}$**+**, $\overline{\mathbf{CS}}$**–**	digital LVDS input pair	Active-low chip select input for SPI data bus. The falling edge of this signal is also used to trigger an ADC sample. If **LVDS_en** is pulled low, only $\overline{\mathbf{CS}}$**+** is used as a standard CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
SCLK+, SCLK–	digital LVDS input pair	Serial clock input for SPI data bus. The base value of the clock is zero (CPOL = 0). If **LVDS_en** is pulled low, only **SCLK+** is used as a standard CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
MOSI+, MOSI–	digital LVDS input pair	Serial data input ("Master Out, Slave In") for SPI data bus. The RHD2000 chip always acts as slave in an SPI data link. This line is sampled on the rising edge of SCLK. If **LVDS_en** is pulled low, only **MOSI+** is used as a standard CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
MISO+, MISO–	digital LVDS output pair	Serial data output ("Master In, Slave Out") for SPI data bus. The RHD2000 chip always acts as slave in an SPI data link. The value of this line changes in response to a falling edge on SCLK. If **LVDS_en** is pulled low, only **MISO+** is used as a standard CMOS-level output. If **LVDS_en** is pulled high, both pins are used as an LVDS output pair.
auxin1, auxin2, auxin3	analog input	Auxiliary analog inputs to the on-chip ADC (0.10V-2.45V range). Alternatively, off-chip resistors may be connected to these pins to set amplifier bandwidth if the on-chip bandwidth registers are not used. If not used, these pins should be tied to VDD to minimize power dissipation.
auxout	digital output	This pin is an auxiliary CMOS digital output that is controlled or tristated by setting registers on the chip. If not used, this pin should be left unconnected. This pin should never be tied to ground or VDD, as the operation of this pin is undefined at power-up.
elec_test	analog input	Can be used to inject AC current for electrode impedance measurement or DC voltage for electrode activation. If the on-chip electrode impedance test circuits are used, this pin should be left unconnected. Tying this pin to ground will disable all on-chip and off-chip impedance test capabilities.
VESD	power	Electrostatic discharge protection power line for amplifier inputs. This line should be tied to ground whenever the amplifiers are used. It may be tied to a higher voltage *only* during electrode activation. (See the "Amplifier Input Protection" section for more information.)
ADC_ref	analog output	An external 10 nF ceramic capacitor to ground must be connected to this pin, and placed in close proximity to the chip to stabilize the on-chip voltage reference generator used by the ADC. A voltage of approximately 1.225V will appear on this pin during operation. See the "Analog-to-Digital Converter" section for more information.

Electrical Characteristics

T_A = 25ºC, V_{DD} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
V_{DD}	Supply Voltage		3.2 – 3.6	V	Recommended nominal supply voltage is 3.3V. See text for derating under 3.0V operation.
$Z_{diginCMOS}$	CMOS Digital Input Impedance	**LVDS_en** = 0	5	pF	
$Z_{diginLVDS}$	LVDS Digital Input Impedance	**LVDS_en** = 1	150	kΩ	LVDS inputs are weakly pulled to V_{DD} if unconnected. User must add 100 Ω termination.
Z_{auxin}	Auxiliary Analog Input Impedance	On-chip bandwidth selection enabled	4	pF	
V_{inLO}	CMOS Digital "Low" Input Voltage	For all non-LVDS digital inputs to chip	-0.4 – +0.7	V	Nominal "low" input voltage is GND (0 V).
V_{inHI}	CMOS Digital "High" Input Voltage	For all non-LVDS digital inputs to chip	2.4 – 3.6	V	5V signals should never be applied directly to the chips.
$V_{inLVDS\text{-}CM}$	LVDS Input Common-Mode Voltage		1.0 – 1.5	V	Suggested common-mode level is 1.25 V.
$V_{inLVDS\text{-}D}$	LVDS Input Differential Voltage		±250 – ±500	mV	Suggested differential voltage is ±350 mV.
$V_{outLVDS\text{-}CM}$	LVDS Output Common-Mode Voltage		1.25	V	Typical
$V_{outLVDS\text{-}D}$	LVDS Output Differential Voltage	With 100 Ω termination	±350	mV	Typical
A_D	Amplifier Differential Gain	In midband region between f_L and f_H	192 45.7	V/V dB	This gain yields an ADC step size (V_{LSB}) of 0.195 μV, referred to the electrode.
A_0	Amplifier DC Differential Gain		0	V/V	Complete DC rejection, unlike amplifiers that have A_0 = 1 V/V.
V_{LSB}	Voltage Step Size of ADC (Least Significant Bit)	referred to amplifier input referred to auxiliary ADC input referred to supply voltage sensor	0.195 37.4 74.8	μV μV μV	
f_L	Amplifier Low-Frequency 3-dB Cutoff Frequency (High-Pass Filter)	Set by off-chip resistor or on-chip registers; tunable from 0.02 Hz to 1.0 kHz	0.02 – 1000	Hz	1-pole roll-off below f_L. On-chip bandwidth selection registers have range of 0.1 Hz-500 Hz.
f_H	Amplifier High-Frequency 3-dB Cutoff Frequency (Low-Pass Filter)	Set by two off-chip resistors or on-chip registers; tunable from 10 Hz to 20 kHz	10 – 20000	Hz	3-pole 3rd-order Butterworth filter roll-off above f_H. On-chip bandwidth selection registers have range of 100 Hz-20 kHz.

Electrical Characteristics

T_A = 25ºC, V_{DD} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
$V_{amp\text{-}AC}$	Amplifier AC Input Voltage Range		±5.0	mV	
$V_{amp\text{-}DC}$	Amplifier Input Voltage Allowable DC Offset		±0.4	V	ESD diodes conduct to ground as DC offset increases.
V_{OS}	Amplifier Input-Referred Offset Voltage	DSP offset removal filter disabled	< ±100	μV	Output offset varies by 192x this value (i.e., ±19.2 mV).
CMRR	Amplifier Common Mode Rejection Ratio	f = 50 or 60 Hz f = 1 kHz	82 82	dB dB	Typical
PSRR	Amplifier Power Supply Rejection Ratio	f = 50 or 60 Hz f = 1 kHz	75 75	dB dB	Typical
	Amplifier Crosstalk	f = 0.1 Hz to 10 kHz	–68	dB	Typical; measured between adjacent amplifiers on chip.
I_b	Amplifier Input Bias Current	–0.2 V < V_{IN} < +0.2 V –0.3 V < V_{IN} < +0.3 V –0.4 V < V_{IN} < +0.4 V	< 20 < 500 < 20	pA pA nA	Individual amplifier input (**inX**, **inX+**, or **inX–** pin) Voltage referenced to GND.
I_{bREF}	Amplifier Reference Input Bias Current	–0.2 V < V_{REF} < +0.2 V –0.3 V < V_{REF} < +0.3 V –0.4 V < V_{REF} < +0.4 V	< 120 < 3 < 120	pA nA nA	Common amplifier reference (**ref_elec** pin) Voltage referenced to GND.
C_{in}	Amplifier Input Capacitance		12	pF	Individual amplifier input (**inX**, **inX+**, or **inX–** pin)
C_{inREF}	Amplifier Reference Input Capacitance	RHD2132	325	pF	Common amplifier reference (**ref_elec** pin)
$\|Z_{in}\|$	Amplifier Input Impedance	f = 10 Hz f = 1 kHz	1300 13	MΩ MΩ	Individual amplifier input (**inX**, **inX+**, or **inX–** pin)
$\|Z_{inREF}\|$	Amplifier Reference Input Impedance	f = 10 Hz, RHD2132 f = 1 kHz, RHD2132	50 0.5	MΩ MΩ	Common amplifier reference (**ref_elec** pin)
v_{ni}	Amplifier Input-Referred Noise		2.4	μV_{rms}	Typical. Varies slightly (< 15%) with amplifier bandwidth.
THD	Amplifier Total Harmonic Distortion (with f_L = 0.1 Hz, f_H = 10 kHz)	f = 1 kHz V_{IN} = 4 $mV_{P\text{-}P}$ V_{IN} = 10 $mV_{P\text{-}P}$	 0.1 < 0.8	 % %	Includes any nonlinearity in MUX. Distortion may increase near f_L and f_H.
f_{MUX}	Maximum ADC MUX Switching Frequency		1.05	MHz	32 amplifiers can be sampled up to 30 kSamples/s each.
	Size of Packaged RHD2216 or RHD2132		8.0 × 8.0	mm^2	56-pin plastic QFN package (0.85 mm thick)
	Mass of Packaged RHD2216 or RHD2132		168	mg	
	Size of RHD2216 or RHD2132 Bare Die		4.8 × 4.1	mm^2	Bare silicon die (0.20 mm thick)
	Mass of RHD2216 or RHD2132 Bare Die		11	mg	

Measured Performance Characteristics

SAMPLING AMPLIFIERS WITH ON-CHIP ADC

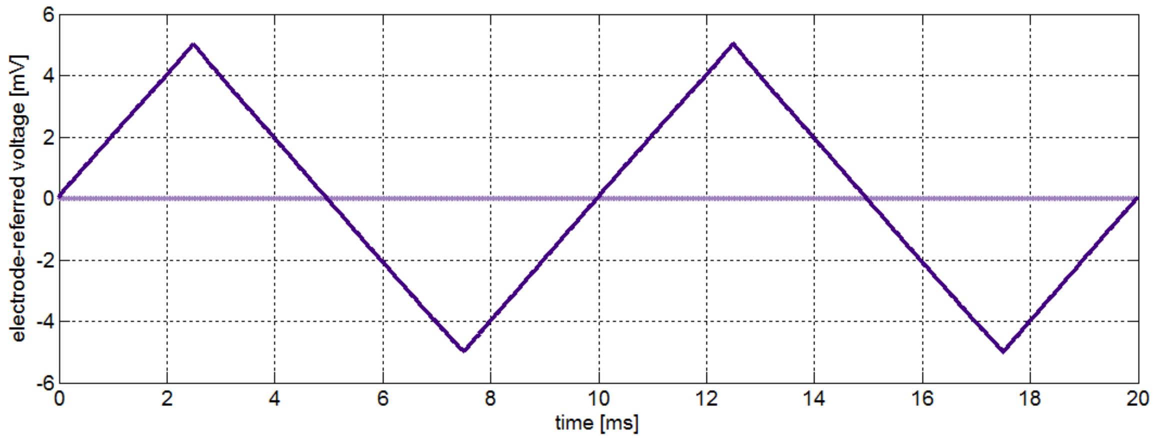


Figure 1. Measurement of **±5.0 mV**, 100 Hz triangle wave on amplifier channel 1 with ADC running at **30 kS/s per channel**, showing large-signal linearity. Amplifier channel 2, also shown, is grounded, showing low noise and lack of crosstalk.

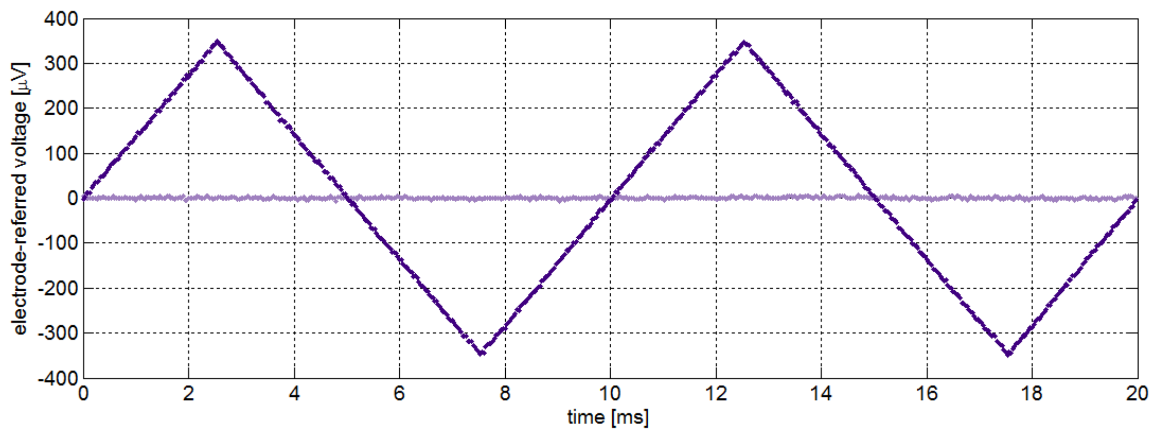


Figure 2. Measurement of **±350 μV**, 100 Hz triangle wave on amplifier channel 1 with ADC running at **30 kS/s per channel**, showing large-signal linearity. Amplifier channel 2, also shown, is grounded, showing low noise and lack of crosstalk.

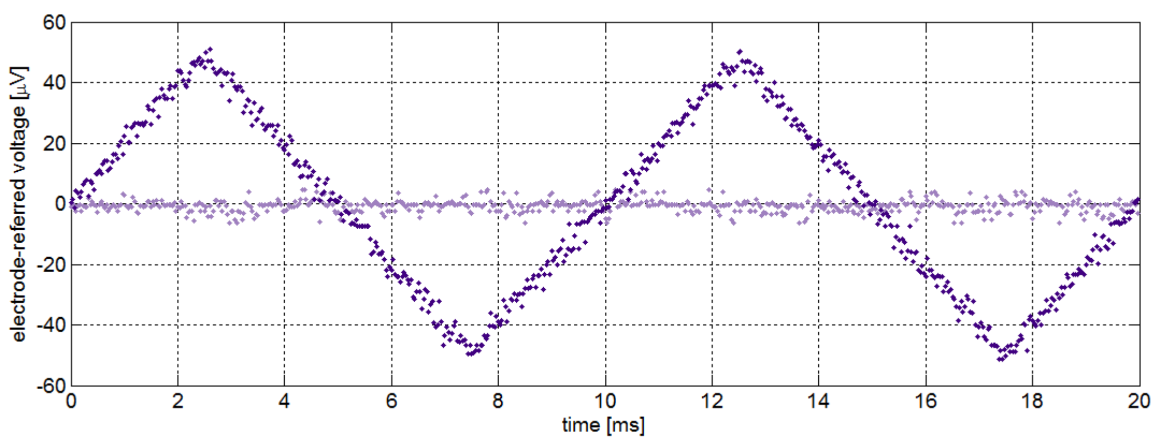


Figure 3. Measurement of **±50 μV**, 100 Hz triangle wave on amplifier channel 1 with ADC running at **30 kS/s per channel**, showing low noise levels. Amplifier channel 2, also shown, is grounded, showing low noise and lack of crosstalk.

Measured Performance Characteristics

BIOPOTENTIALS MEASURED WITH RHD2000-SERIES AMPLIFIERS

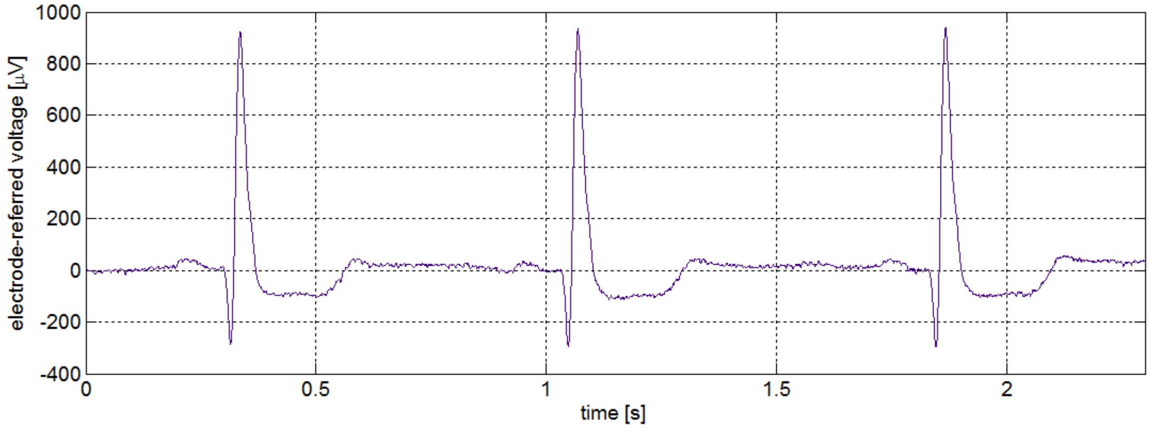


Figure 4. EKG signal recorded with RHD2216 using three Ag/AgCl electrodes (**in0+** and **in0–** on chest, 5 cm apart; ground on elbow). Amplifier was configured with f_L = 0.1 Hz, f_H = 100 Hz, and DSP high-pass filter set to 0.6 Hz. ADC sampling rate was 2 kS/s per channel.

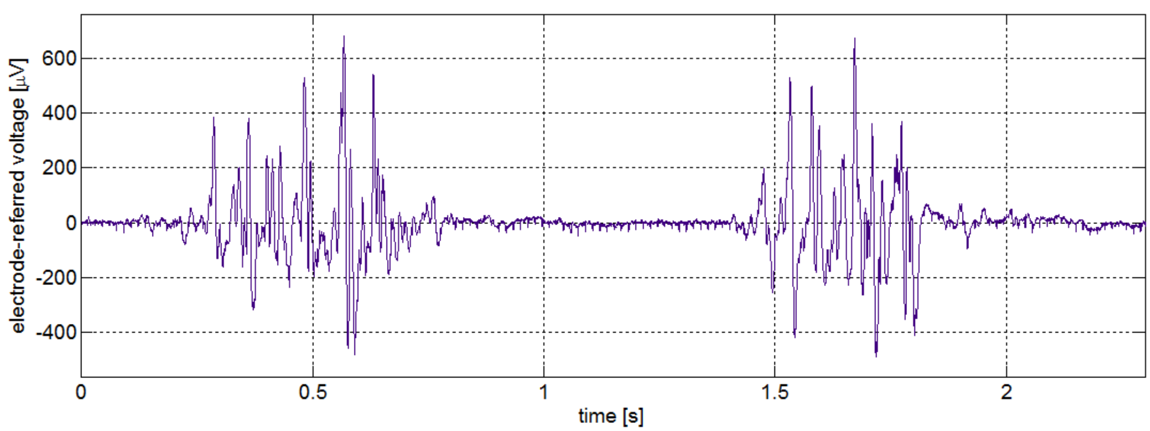


Figure 5. EMG signal recorded with RHD2216 using three Ag/AgCl electrodes during bicep contractions (**in0+** and **in0–** on bicep, 5 cm apart; ground on elbow). Amplifier was configured with f_L = 2.0 Hz, f_H = 1.0 kHz, and DSP high-pass filter set to 10 Hz. ADC sampling rate was 4 kS/s per channel.

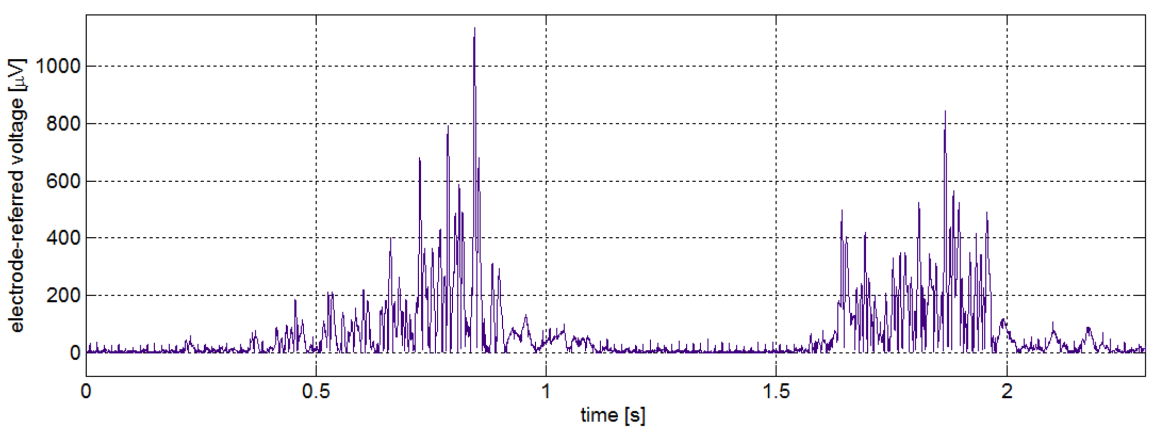
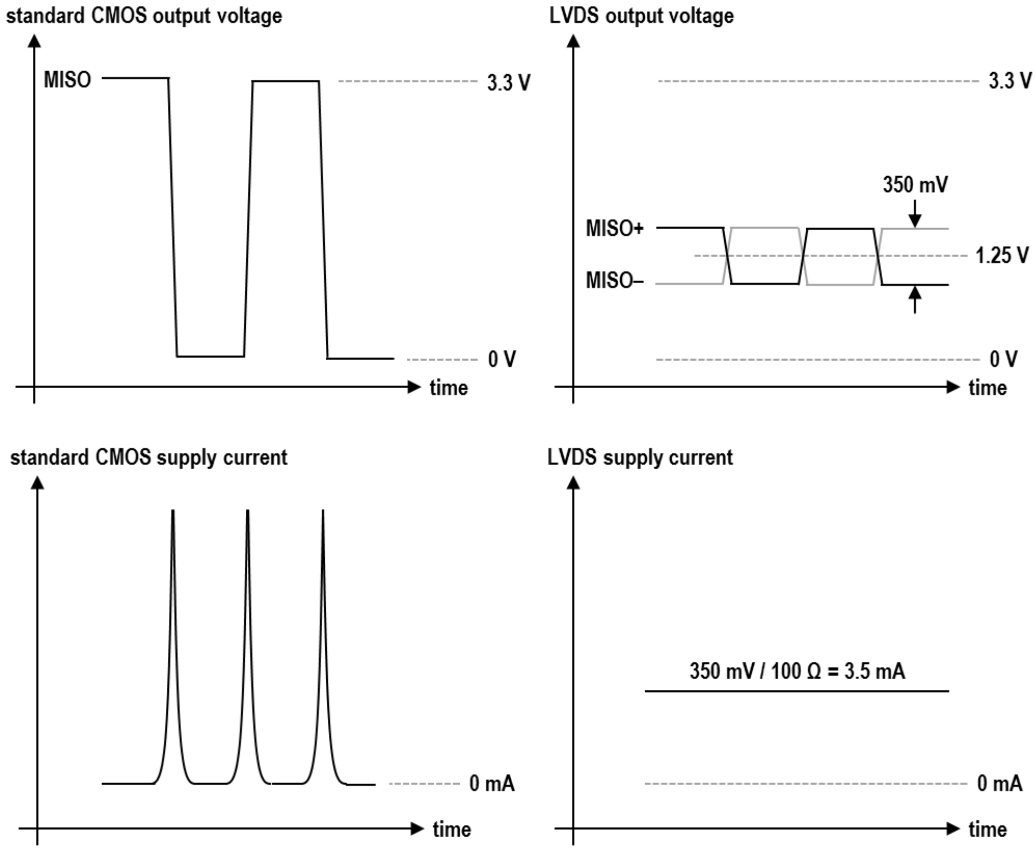


Figure 6. EMG signal recorded with RHD2216 with **absmode = 1** using three Ag/AgCl electrodes during bicep contractions (**in0+** and **in0–** on bicep, 5 cm apart; ground on elbow). Amplifier was configured with f_L = 2.0 Hz, f_H = 1.0 kHz, and DSP high-pass filter set to 10 Hz. ADC sampling rate was 4 kS/s per channel. Absolute value calculation is performed on the chip.

Digital Signaling Modes



The RHD2000 chips communicate over a standard digital Serial Peripheral Interface (SPI) bus. The bus protocol and data structures used are described in later sections. The voltage levels used to send digital signals over this bus can assume one of two forms: standard CMOS signaling or low-voltage differential signaling (LVDS). The above figure illustrates the differences between a digital value (e.g., MISO) transmitted using these two signaling methods.

Standard CMOS Signaling

Standard CMOS signaling (upper left) transmits a digital one or zero by switching the voltage on a single output wire between ground and V_{DD}. The current drawn from the power supply (lower left) is nearly zero until the output switches state; at this point, a burst of current is pulled from the power supply to charge or discharge the capacitance of the output wire. These bursts of supply current introduce high frequency noise to the on-chip power supply; this noise can adversely affect noise levels. For typical data streams containing similar numbers of ones and zeros, the dynamic power dissipation of a standard CMOS output driving a wire with capacitance C_{wire} at R bits/s is

$$P = \frac{1}{2} C_{\text{wire}} V_{\text{DD}}{}^2 R.$$

(The actual power dissipation will be slightly higher than this due to secondary effects like the momentary short-circuit current that leaks through CMOS circuits every time they switch state.)

If we operate an RHD2000 at the maximum sampling rate of 1.05 MS/s, the data rate R is 1.05 MHz × 16 bits = 16.8 Mbit/s. Typical coaxial cables have a capacitance of 100 pF/m. The power required to transmit 16.8 Mbit/s over a 2.0 m cable is approximately 18 mW.

Transmitting high-frequency data reliably over long wires is challenging due to the presence of reflections that occur when a propagating signal reaches the high-impedance input of a digital receiver. These reflections interfere with the transmitted signal and corrupt the data stream. The characteristic impedance Z_0 of a cable is given by

$$Z_0 = \sqrt{L/C}$$

where L is the cable inductance per unit length and C is the cable capacitance per unit length. For most common cable geometries (e.g., coaxial, twisted pair, ribbon), Z_0 falls in the range of 50 – 200 Ω. To eliminate reflections, the cable must be terminated with a parallel resistance equal to Z_0.

Standard CMOS digital outputs lack the current sourcing capability to drive the high DC currents necessary to support V_{DD}-level signals (i.e., 3.3V) across such small resistances, so proper cable termination cannot be used in these cases. A series resistor with a value of Z_0 placed near a CMOS digital output can prevent multiple reflections from the high-impedance input at the far end of a cable by absorbing the first reflection, but this is an imperfect solution that fails with high data rates or long cables.

LVDS Signaling

LVDS signaling (upper right, previous page) uses a pair of wires (e.g., **MISO+** and **MISO–**) to transmit each digital signal; the wires are terminated with a 100 Ω resistor tied between them near the LVDS receiver. The average voltage on the wire pair is held roughly at 1.25V, and a 3.5 mA current is forced through the wires in one direction or the other, creating a ±350 mV differential voltage across the terminating resistor to signal a digital one or zero.

LVDS signaling offers several advantages over standard CMOS signaling. First, the use of terminated wires drastically reduces reflections, maintaining high signal integrity on long wires and at high data rates. Second, the use of small differential voltages greatly reduces crosstalk to other nearby wires in a cable bundle, especially if twisted pairs are used. Electromagnetic interference and emissions are also minimized using LVDS signaling. Finally, the current drawn from the power supply of the LVDS transmitter is nearly constant (lower right, previous page). This constant current draw does not introduce noise to the on-chip power supply. Thus, LVDS signaling is far better suited for low-noise operation on a chip containing both analog and digital components.

The minimum power dissipation of an LVDS transmitter is given by $V_{DD}\cdot(3.5\ \text{mA}) = 11.6\ \text{mW}$ using a 3.3V power supply. At low frequencies and short wire lengths, standard CMOS signaling can operate at far lower power levels. However, as the calculations in the previous section demonstrate, LVDS can operate at lower power levels when data rates are high and wires are long.

Cables several meters in length can be used with LVDS signaling as long as the geometry of the cable is fairly consistent along its length. Twisted pairs are particularly good structures for LVDS signaling, and many standard cables contain multiple twisted pairs (e.g., USB, HDMI). The DC series resistance of the cable typically has no effect on the performance of the system as long as it is much less than the terminating resistance of 100 Ω. Signals propagate along standard cables at approximately two-thirds the speed of light, or 20 cm/ns, so a five-meter cable will introduce a round-trip delay of around 50 ns. As long as the SPI controller accounts for these delays, long cables may be used to communicate with the RHD2000 chips reliably.

The LVDS inputs and outputs on the RHD2000 use industry-standard LVDS signal levels. Many commercially available FPGAs and microcontrollers have built-in LVDS I/O pins, and can be interfaced directly with the RHD2000. If a controller lacks LVDS I/O, a wide variety of commercially available LVDS-to-standard-CMOS driver and receiver interface chips may be used to translate signal levels (e.g., TI SN65LVDS, SN65LVDT, DS90LV, and DS90C lines; Fairchild FIN10xx line).

Selecting Signaling Modes on the RHD2000

If the **LVDS_en** pin on an RHD2000 is tied to GND, the SPI bus operates with standard CMOS signals, using a single wire for each digital signal. The digital input pins on the RHD2000 interpret any voltage below 0.7V as logic "low" and any voltage above 2.4V as logic "high", so the chip can be interfaced with standard 2.5V, 3.0V, or 3.3V signals. Digital inputs to the RHD2000 should not go below –0.4V, and should never exceed 3.6V. Digital outputs from the RHD2000 chip are driven to ground for logic "low" and to V_{DD} for logic "high".

If the **LVDS_en** pin is tied to V_{DD}, the SPI bus operates in LVDS mode, where every signal in the SPI bus is represented by a differential voltage across a pair of wires (e.g., **SCLK+** and **SCLK–**). The LVDS inputs on the RHD2000 expect a common-mode voltage near 1.25 V and differential signals near ±350 mV, but are fairly tolerant of moderate variations in these values. The LVDS inputs do not include on-chip termination, so a 100 Ω resistor should be placed between each LVDS input signal pair near the chip. Connection diagrams on the following pages provide examples of termination schemes.

Enabling LVDS mode on the RHD2000 increases current consumption by approximately 5.7 mA. This includes the 3.5 mA of current driven through the MISO output as well as current to power the three on-chip LVDS receivers for $\overline{\text{CS}}$, SCLK, and MOSI. (Commercial LVDS interface chips typically consume over 17 mA to perform the same functions as the RHD2000 LVDS I/O system.)

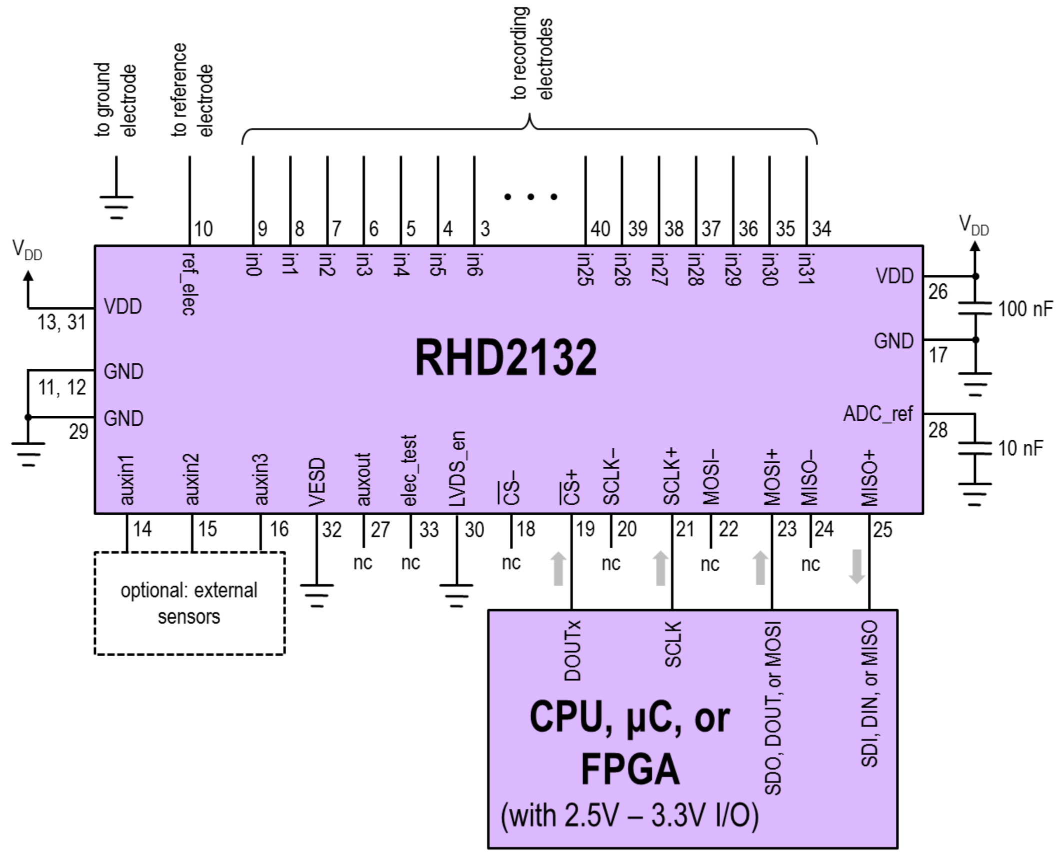
Increased Noise Levels with Standard CMOS Signaling

If standard CMOS signaling is used in combination with high ADC sampling rates, the amplifier noise levels on the RHD2000 will rise above its nominal value of 2.4 μV_{rms}. Even if short wires are used, operating the ADC at 350 kS/s with standard CMOS signaling will increase amplifier noise by at least 10%. Operating the ADC at 1.05 MS/s with standard CMOS signaling will increase amplifier noise by at least 30%. Using long, high-capacitance wires will likely increase the amplifier noise level further. If low noise operation is essential, standard CMOS signaling is recommended only for ADC sampling rates of 175 kS/s or less (i.e., 10 kS/s/channel or less with 16 amplifiers; 5 kS/s/channel or less with 32 amplifiers).

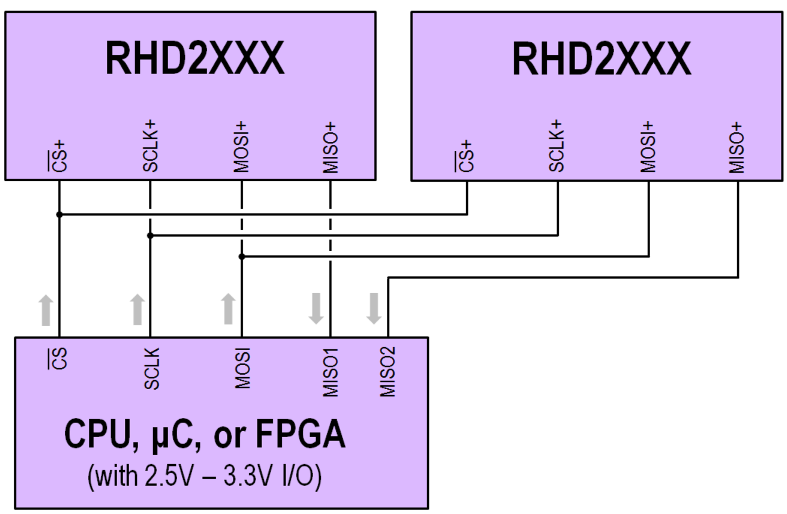
Typical Connection Diagram

STANDARD CMOS SPI INTERFACE (LVDS_en = 0)

The diagram below shows a typical circuit schematic for a single RHD2132 chip interfaced to a controller that is located in close proximity and uses a standard CMOS four-wire SPI interface. In addition to the chip, only two SMD (surface mount device) capacitors are required for a complete biopotential recording front end.

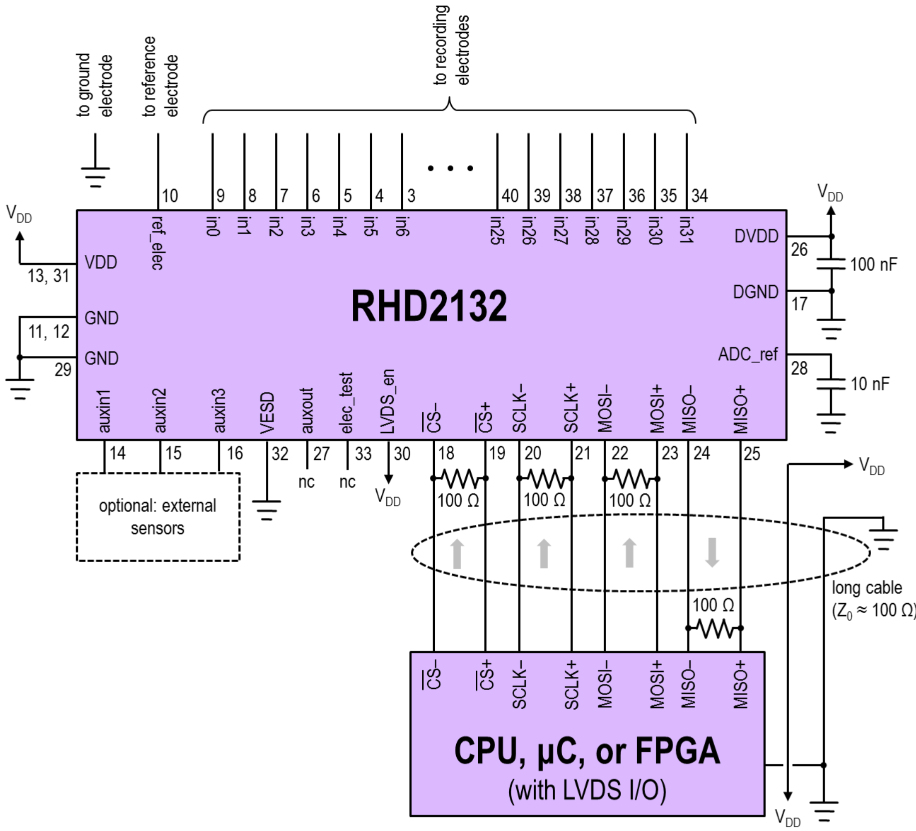


Additional RHD2000 chips can be added using only one additional MISO wire per chip, provided that all chips receive the same commands in parallel, as shown below.

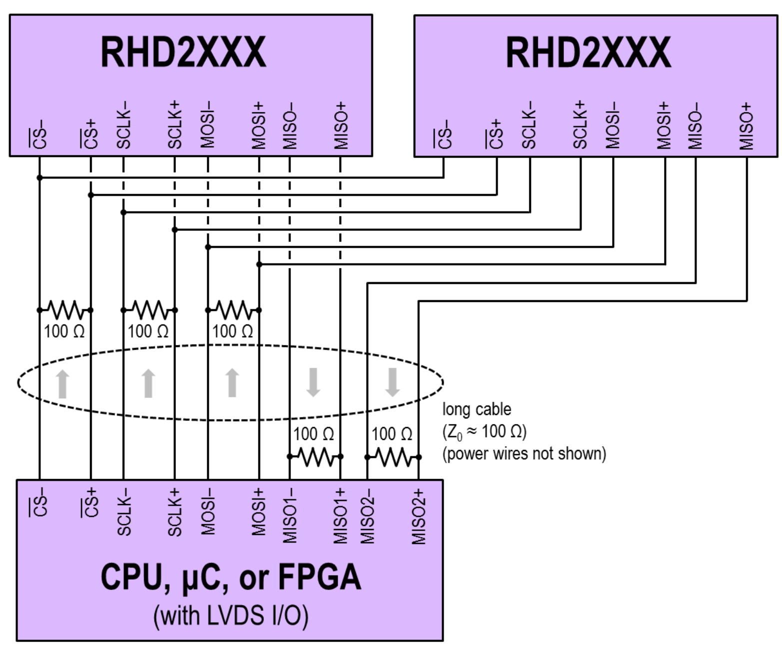


LVDS SPI INTERFACE (LVDS_en = 1)

The diagram below shows a typical circuit schematic for a single RHD2132 chip interfaced to a controller over a long cable, using an SPI interface with low-voltage differential signaling and 100 Ω termination resistors.



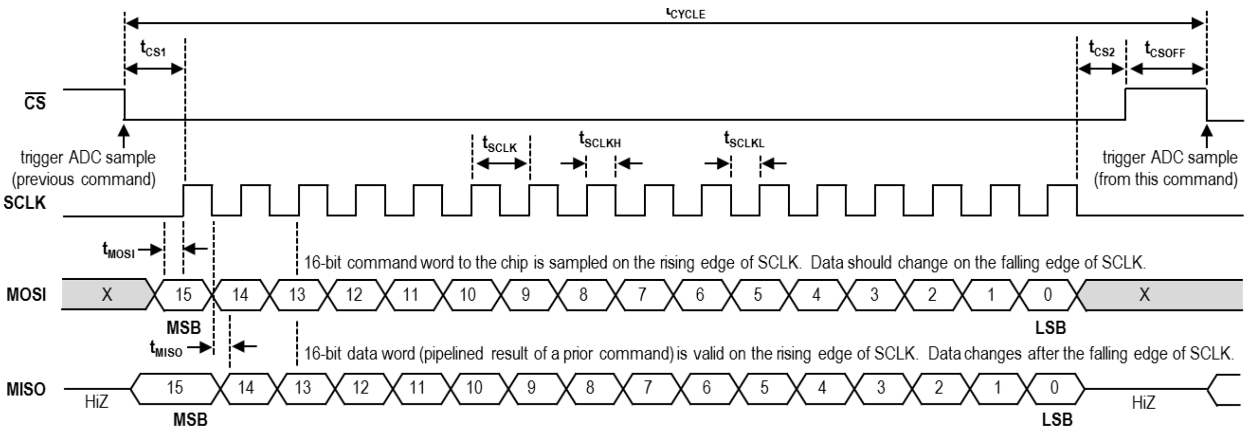
Additional RHD2000 chips can be added as shown below. Only one termination resistor should be used for each LVDS pair (assuming all RHD2000 chip will receive the same commands); this resistor should be located within 20 cm of the RHD2000 chips.



SPI Bus Signals

RHD2000 chips communicate using a standard SPI interface consisting of four signals: an active-low chip select ($\overline{CS}$); a serial data clock (SCLK) with a base value of zero; a "Master Out, Slave In" data line (MOSI) to receive commands from the master device; and a "Master In, Slave Out" data line (MISO) to send pipelined results from prior commands to the master device. The RHD2000 chip always functions as the SPI slave device. During each chip select cycle, 16-bit data words are transferred in each direction, MSB first. As shown below, the RHD2000 samples MOSI on the rising edge of SCLK. The master should sample MISO on the rising edge of SCLK. (The master device SPI interface should be configured with SPI options CPOL=0 and CPHA=0.) The RHD2000 ADC samples the selected analog signal on the falling edge of $\overline{CS}$. The $\overline{CS}$ line must be pulsed high between every 16-bit data transfer, even when the command word does not request an analog-to-digital conversion.

Timing Diagram



SPI BUS TIMING SPECIFICATIONS

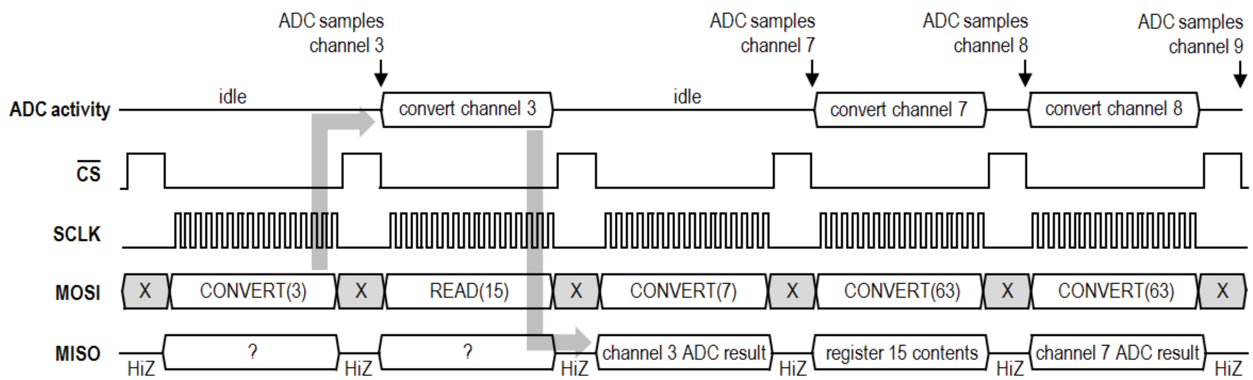
T_A = 25ºC, V_{DD} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
t_{SCLK}	SCLK Period	41.6		ns	Maximum SCLK frequency is 24 MHz
t_{SCLKH}	SCLK Pulse Width High	20.8		ns	
t_{SCLKL}	SCLK Pulse Width Low	20.8		ns	
t_{CS1}	$\overline{CS}$ Low to SCLK High Setup	20.8		ns	
t_{CS2}	SCLK Low to $\overline{CS}$ High Setup	20.8		ns	
t_{CSOFF}	$\overline{CS}$ High Duration	154		ns	
t_{MOSI}	MOSI Data Valid to SCLK High Setup	10.4		ns	
t_{MISO}	SCLK or $\overline{CS}$ Falling Edge to MISO Data Valid		12	ns	
t_{CYCLE}	Total Cycle Time Between ADC Samples	950		ns	Maximum sample rate is 1.05 MS/s, or 30 kS/s per channel for 35 multiplexed channels.

SPI Command Words

Each RHD2000 chip responds to five basic commands: perform an analog-to-digital conversion on a particular signal; run an ADC self-calibration routine; clear ADC calibration; write to a RAM register; or read from a RAM or ROM register. Each chip contains 18 eight-bit RAM registers that configure various aspects of chip behavior and several eight-bit ROM registers that store basic properties of the chip.

The RHD2000 uses a pipelined communication protocol; each command sent over the MOSI line generates a 16-bit result that is transmitted over the MISO line two commands later. Communication with the chip is illustrated in the following example diagram:



After receiving a CONVERT(C) command, the on-chip ADC samples channel C on the falling edge of the next $\overline{\text{CS}}$ pulse. The analog-to-digital conversion is performed during the next 16 SCLK cycles, and the result is relayed to the master over the MISO line during the following 16 SCLK cycles.

The RHD2000 commands are described by the following bit patterns:

Command: CONVERT(C) – Run analog-to-digital conversion on channel C

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	**LSB** 0
0	**0**	**C[5]**	**C[4]**	**C[3]**	**C[2]**	**C[1]**	**C[0]**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**H**

Result:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	**LSB** 0
A[15]	**A[14]**	**A[13]**	**A[12]**	**A[11]**	**A[10]**	**A[9]**	**A[8]**	**A[7]**	**A[6]**	**A[5]**	**A[4]**	**A[3]**	**A[2]**	**A[1]**	**A[0]**

Comments:

The CONVERT(C) command executes an analog-to-digital conversion of analog channel C. Channels 0-31 correspond to the 32 biopotential amplifiers sharing the chip with the ADC. (Only channels 0-15 are active in the RHD2216.) A subset of channels 32-62 are used for auxiliary sensors on and off the chip (see later sections). The conversion result A is sent back to the master (MSB first) two commands later, as shown in the figure above.

A special case of the CONVERT command with C = 63 can be used to cycle through successive amplifier channels. The CONVERT(63) command automatically increments the multiplexer to the next amplifier channel. After reaching the end of the amplifier array, the multiplexer rolls back to channel 0. (Note: The state of the chip is undefined at power-up, so at least one CONVERT(0) command should be sent before executing this variant of the command.)

If the LSB (bit H) of a CONVERT(C) command is set to 1 when DSP offset removal is enabled (see "DSP High-Pass Filter for Offset Removal" section), then the output of the digital high-pass filter associated with amplifier channel C is reset to zero. This can be used to rapidly recover from a large transient and settle to baseline.

Command: CALIBRATE – Initiate ADC self-calibration routine

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Result:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
*****	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Comments:

The CALIBRATE command initiates an ADC self-calibration routine that should be performed after chip power-up and register configuration. Self-calibration takes many clock cycles to execute; since the ADC clock is derived solely from SCLK, nine "dummy" commands must be sent after a CALIBRATE command (along with the usual SCLK and $\overline{\text{CS}}$ pulses) to generate the necessary clock cycles. The nine commands following a CALIBRATE command are not executed by the RHD2000; the chip ignores other operations until calibration is complete. The CALIBRATE should only be sent **once** to initiate a calibration sequence; resending this command before calibration is complete will restart calibration from the beginning.

During the entire calibration cycle, the results returned by the RHD2000 consist of all zeros except for the MSB. The MSB will be zero if two's complement mode is enabled (see Register 4 description below); otherwise it will be one.

Command: CLEAR – Clear ADC calibration

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Result:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
*****	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Comments:

The CLEAR command clears the on-chip calibration parameters acquired by running the CALIBRATE command described above. In the normal operation of the RHD2000, it is not necessary to execute this command.

The result returned by the RHD2000 consists of all zeros except for the MSB. The MSB will be zero if two's complement mode is enabled (see Register 4 description below); otherwise it will be one.

Command: WRITE(R,D) – Write data D to register R

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
1	**0**	**R[5]**	**R[4]**	**R[3]**	**R[2]**	**R[1]**	**R[0]**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**

Result:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**

Comments:

The WRITE(R,D) command writes an eight-bit data byte D to chip register R. The data byte D is echoed back to the master in the lower byte of the result so that correct reception of the data byte can be confirmed. The upper byte consists of all ones.

Any attempt to write to a read-only register (or non-existent register) will produce the same result, but in this case D will not be written to the register.

Command: READ(R) – Read contents of register R

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
1	**1**	**R[5]**	**R[4]**	**R[3]**	**R[2]**	**R[1]**	**R[0]**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Result:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**

Comments:

The READ(R) command reads the contents of chip register R. The data byte D is sent to the master in the lower byte of the result. The upper byte consists of all zeros.

Unknown Commands:

If an invalid command is sent (i.e., any command beginning with '01' that does not correspond to ADC calibration commands), the results returned by the chip will consist of all zeros except for the MSB. The MSB will be zero if two's complement mode is enabled (see Register 4 description below); otherwise it will be one.

On-Chip Registers

Each RHD2000 chip is capable of addressing up to 64 eight-bit registers, in any combination of writable (RAM) registers and read-only (ROM) registers. **Upon power-up, all RAM registers contain indeterminate data and should be promptly configured by the SPI master device.** Initialization of registers should be completed at least 100 μs **before** ADC calibration as some registers set parameters that optimize ADC operation.

Individual bits in a register can be changed only by rewriting the entire eight-bit contents. Therefore, it is recommended that the SPI master device maintain a copy of RHD2000 register contents in its memory so bitwise operations can be performed there before writing the updated byte to the chip using a WRITE command on the SPI bus.

The RAM registers present in each RHD2132 and RHD2216 are described below. The detailed functions of some programmable variables are described later in the datasheet. Note: All multi-bit variables have their most significant bits (MSBs) on the left in the diagrams below, towards the direction of the register MSB D[7]. Bits marked X have no function but should be set to zero for compatibility with any future chip versions.

Register 0: ADC Configuration and Amplifier Fast Settle

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 0	ADC reference BW [1:0]		amp fast settle	amp Vref enable	ADC comparator bias [1:0]		ADC comparator select [1:0]	

ADC reference BW [1:0]: This variable configures the bandwidth of an internal ADC reference generator feedback circuit. This variable should always be set to 3.

amp fast settle: Setting this bit to one closes a switch in each amplifier that drives its analog output to the baseline "zero" level. This can be used to quickly recover from large transient events that may drive the amplifiers to their rails. The switch should be closed for a certain amount of time to settle the amplifiers (see "Fast Settle Function" section for details) and then this register should be reset to zero to resume normal amplifier operation.

amp Vref enable: In normal operation, this bit should be set to one to power up voltage references used by the biopotential amplifiers. This bit can be set to zero to reduce power supply current consumption by 180 μA when the amplifiers will not be used for an extended period of time. After setting this bit to one, at least 100 μs must elapse before ADC samples are valid, or before ADC calibration is executed.

ADC comparator bias [1:0]: This variable configures the bias current of the ADC comparator. This variable should always be set to 3 for normal operation and ADC calibration. This variable can be set to zero to reduce power supply current consumption by 80 μA when the ADC will not be used for an extended period of time.

ADC comparator select [1:0]: This variable selects between four different comparators that can be used by the ADC. This variable should always be set to 2.

Register 1: Supply Sensor and ADC Buffer Bias Current

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 1	X	VDD sense enable	ADC buffer bias [5:0]					

VDD sense enable: Setting this bit to one enables the on-chip supply voltage sensor, whose output may be sampled by the ADC on channel 48 (see "Supply Voltage Sensor" section for details). If the supply voltage is not sampled, this bit can be set to zero to reduce current consumption by 10 μA.

ADC buffer bias [5:0]: This variable configures the bias current of an internal reference buffer in the ADC. The optimum value for this variable is a function of ADC sampling rate and is listed in a table in the "Analog-to-Digital Converter" section later in the datasheet.

Register 2: MUX Bias Current

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 2	X	X	MUX bias [5:0]					

MUX bias [5:0]: This variable configures the bias current of the MUX that routes the selected analog signal to the ADC input. The optimum value for this variable is a function of ADC sampling rate and is listed in a table in the "Analog-to-Digital Converter" section later in the datasheet.

Register 3: MUX Load, Temperature Sensor, and Auxiliary Digital Output

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 3	MUX load [2:0]			tempS2	tempS1	tempen	digout HiZ	digout

MUX load [2:0]: This variable configures the total capacitance at the input of the ADC. This variable should always be set to 0.

tempS1 and **tempS2:** These bits control switches in the on-chip temperature sensor, whose output may be sampled by the ADC on channel 49. The detailed operation of the temperature sensor is described in the "Temperature Sensor" section later in the datasheet. When the temperature sensor is not in use, these bits should each be set to zero to save power.

tempen: Setting this bit to one enables the on-chip temperature sensor. Current consumption may be reduced by approximately 70 μA by setting this bit to zero to disable the sensor.

digout HiZ: The RHD2000 chips have an auxiliary digital output pin **auxout** that may be used to activate off-chip circuitry (e.g., MOSFET switches, LEDs, stimulation circuits). Setting this bit to one puts the digital output into high impedance (HiZ) mode.

digout: This bit is driven out of the auxiliary CMOS digital output pin **auxout**, provided that the **digout HiZ** bit is set to zero. See the "Auxiliary Digital Output" section for details.

Register 4: ADC Output Format and DSP Offset Removal

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 4	weak MISO	twoscomp	absmode	DSPen	DSP cutoff freq [3:0]			

weak MISO: If this bit is set to zero, the MISO line goes to high impedance mode (HiZ) when $\overline{\text{CS}}$ is pulled high, allowing multiple chips to share the same MISO line so long as only one of their chip select lines is activated at any time. If only one RHD2000 chip will be using a MISO line, this bit may be set to one, and when $\overline{\text{CS}}$ is pulled high the MISO line will be driven weakly by the chip. This can prevent the line from drifting to indeterminate values between logic high and logic low.

twoscomp: If this bit is set to one, amplifier conversions from the ADC are reported using a "signed" two's complement representation where the amplifier baseline is reported as zero and values below baseline are reported as negative numbers. If this bit is set to zero, amplifier conversions from the ADC are reported using "unsigned" offset binary notation where the baseline level is represented as 1000000000000000. ADC conversions from non-amplifier channels (i.e., C > 31) are always reported as unsigned binary numbers.

absmode: Setting this bit to one passes all amplifier ADC conversions through an absolute value function. This is equivalent to performing full-wave rectification on the signals, and may be useful for implementing symmetric positive/negative thresholds or envelope estimation algorithms. This bit has no effect on ADC conversions from non-amplifier channels (i.e., C > 31). See the "Absolute Value Mode" section for more information.

DSPen: When this bit is set to one, the RHD2000 performs digital signal processing (DSP) offset removal from all 32 amplifier channels using a first-order high-pass IIR filter. See the "DSP High-Pass Filter for Offset Removal" section for details.

DSP cutoff freq [3:0]: This variable sets the cutoff frequency of the DSP filter used to for offset removal. See the "DSP High-Pass Filter for Offset Removal" section for details.

Register 5: Impedance Check Control

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 5	X	Zcheck DAC power	Zcheck load	Zcheck scale [1:0]		Zcheck conn all	Zcheck sel pol	Zcheck en

Zcheck DAC power: Setting this bit to one activates the on-chip digital-to-analog converter (DAC) used to generate waveforms for electrode impedance measurement. If impedance testing is not being performed, this bit can be set to zero to reduce current consumption by 120 μA. See the "On-Chip AC Current Waveform Generator" section for more information.

Zcheck load: Setting this bit to one adds a capacitor load to the impedance checking network. This mode is only used for chip testing at Intan Technologies. This bit should always be set to zero for normal operation.

Zcheck scale [1:0]: This variable selects the series capacitor used to convert the voltage waveform generated by the on-chip DAC into an AC current waveform that stimulates a selected electrode for impedance testing: 00 = 0.1 pF; 01 = 1.0 pF; 11 = 10 pF. See the "On-Chip AC Current Waveform Generator" section for more information.

Zcheck conn all: Setting this bit to one connects all electrodes together to the **elec_test** input pin. This is only used for applying DC voltages to electroplate electrodes. In normal operation this bit should be set to zero. See the "Electrode Activation" section for details.

Zcheck sel pol: This bit is only used on the RHD2216 where the biopotential amplifiers have separate positive and negative inputs (instead of a reference input common to all amplifiers). Setting this bit to zero selects impedance testing of the positive input of the selected amplifier. Setting the bit to one tests the negative input. See the "Electrode Impedance Test" section for details.

Zcheck en: Setting this bit to one activates impedance testing mode, and connects the on-chip waveform generator (and pin **elec_test**) to the amplifier selected by the **Zcheck select** variable in Register 7. See the "Electrode Impedance Test" section for details.

Register 6: Impedance Check DAC

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 6	Zcheck DAC [7:0]							

Zcheck DAC [7:0]: This variable sets the output voltage of an 8-bit DAC used to generate waveforms for impedance checking. This variable must be updated at regular intervals to create the desired waveform. Note that this DAC must be enabled by setting **Zcheck DAC power** in Register 5. If impedance testing is not in progress, the value of this register should remain unchanged to minimize noise (although writing the same value to the register is acceptable). See the "On-Chip AC Current Waveform Generator" section for more information.

Register 7: Impedance Check Amplifier Select

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 7	X	X	Zcheck select [5:0]					

Zcheck select [5:0]: This variable selects the amplifier whose electrode will be connected to the on-chip impedance testing circuitry if **Zcheck en** is set to one. In 16- and 32-amplifier chips, the MSB of this six-bit register is ignored. See the "Electrode Impedance Test" section for details.

Registers 8-13: On-Chip Amplifier Bandwidth Select

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 8	offchip RH1	X	RH1 DAC1 [5:0]					
Register 9	ADC aux1 en	X	X	RH1 DAC2 [4:0]				
Register 10	offchip RH2	X	RH2 DAC1 [5:0]					
Register 11	ADC aux2 en	X	X	RH2 DAC2 [4:0]				
Register 12	offchip RL	RL DAC1 [6:0]						
Register 13	ADC aux3 en	RL DAC3	RL DAC2 [5:0]					

offchip RH1, offchipRH2, and **offchip RL:** Setting these bits to one switches from using on-chip programmable resistors for setting amplifier upper and lower bandwidths to using external resistors R_{H1}, R_{H2}, and R_L (connected to pins auxin1, auxin2, and/or auxin3) to set amplifier bandwidth. Tables later in the datasheet provide appropriate values for bandwidth-setting resistors.

RH1 DAC1 [5:0], RH1 DAC2 [4:0], RH2 DAC1 [5:0], and **RH2 DAC2 [4:0]:** These variables set the upper cutoff frequency of the biopotential amplifiers. A table later in the datasheet provides appropriate register values for setting the upper cutoff frequency in the range of 100 Hz to 20 kHz.

RL DAC1 [6:0], RL DAC2 [5:0], and **RL DAC3:** These variables set the lower cutoff frequency of the biopotential amplifiers. A table later in the datasheet provides appropriate register values for setting the lower cutoff frequency in the range of 0.1 Hz to 500 Hz.

ADC aux1 en, ADC aux2 en, and **ADC aux3 en:** Setting these bits to one when on-chip bandwidth resistors are selected activates buffers that allow the pins **auxin1**, **auxin2**, and **auxin3** to be used as auxiliary ADC inputs. These auxiliary ADC inputs have a range of 0.10V to 2.45V, and correspond to channels 32, 33, and 34. See the “Auxiliary ADC Inputs” section for more information.

Registers 14-17: Individual Amplifier Power

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 14	apwr[7]	apwr[6]	apwr[5]	apwr[4]	apwr[3]	apwr[2]	apwr[1]	apwr[0]
Register 15	apwr[15]	apwr[14]	apwr[13]	apwr[12]	apwr[11]	apwr[10]	apwr[9]	apwr[8]
Register 16	apwr[23]	apwr[22]	apwr[21]	apwr[20]	apwr[19]	apwr[18]	apwr[17]	apwr[16]
Register 17	apwr[31]	apwr[30]	apwr[29]	apwr[28]	apwr[27]	apwr[26]	apwr[25]	apwr[24]

apwr [31:0]: Setting these bits to zero powers down individual biopotential amplifiers, saving power if there are channels that don’t need to be observed. Each amplifier consumes power in proportion to its upper cutoff frequency. Current consumption is approximately 7.6 μA/kHz per amplifier. Under normal operation, these bits should be set to one.

On-Chip Read-Only Registers

Each RHD2000 chip contains the following ROM registers that provide information on the identity and capabilities of the particular chip.

Registers 40-44: Company Designation

The read-only registers 40-44 contain the characters INTAN in ASCII. The contents of these registers can be read to verify the fidelity of the SPI interface.

Register 60: Die Revision

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 60	die revision [7:0]							

die revision [7:0]: This read-only variable encodes a die revision number which is set by Intan Technologies to encode various versions of a chip.

Register 61: Unipolar/Bipolar Amplifiers

Type: ROM

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 61	unipolar [7:0]							

unipolar [7:0]: This read-only variable is set to zero if the on-chip biopotential amplifiers have independent differential (bipolar) inputs like the RHD2216 chip. It is set to one if the amplifiers have unipolar inputs and a common reference, like the RHD2132 chip.

Register 62: Number of Amplifiers

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 62	number of amps [7:0]							

number of amps [7:0]: This read-only variable encodes the total number of biopotential amplifiers on the chip (e.g., 16, 32).

Register 63: Intan Technologies Chip ID

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 63	chip ID [7:0]							

chip ID [7:0]: This read-only variable encodes a unique Intan Technologies ID number indicating the type of chip. The chip ID for the RHD2132 is 1. The chip ID for the RHD2216 is 2.

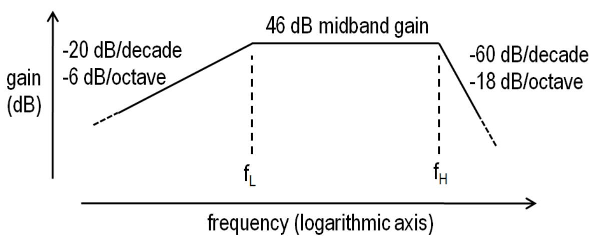
Amplifier Bandwidth

At the core of each RHD2000 chip is an array of low-noise amplifiers with integrated analog filters that can be configured to isolate frequencies of interest and minimize aliasing by attenuating signals above the Nyquist rate (i.e., half the ADC per-channel sampling rate). Each amplifier has a pass band extending from a low-frequency cutoff f_L to a high-frequency cutoff f_H. The upper end of the pass band has a 3rd-order Butterworth low-pass filter at the 3-dB frequency f_H. The lower end of the pass band has a 1st-order high-pass filter characteristic at the 3-dB frequency f_L.

The 3rd-order Butterworth low-pass filter characteristic at f_H has a maximally flat pass band region with -60 dB/decade (-18 dB/octave) of attenuation beyond f_H. The table below lists filter gains for several frequencies above and below f_H.

SIGNAL FREQUENCY	NORMALIZED GAIN V/V	NORMALIZED GAIN dB
$0.5 \cdot f_H$	0.99	-0.07 dB
$0.8 \cdot f_H$	0.89	-1.0 dB
f_H	0.707	-3.0 dB
$1.2 \cdot f_H$	0.50	-6.0 dB
$2 \cdot f_H$	0.12	-18 dB
$10 \cdot f_H$	0.001	-60 dB

The diagram below illustrates the analog frequency response of the RHD2000 amplifiers:



An additional pole of high-pass filtering can be applied using the optional DSP filter module (see below).

Setting Upper Bandwidth

Registers 8-11 are used to configure on-chip resistors that set the upper bandwidth of the amplifiers (f_H) in the range of 100 Hz to 20 kHz. Register values for common bandwidths are listed in a table on the following pages. For bandwidths not listed on this table, contact Intan Technologies for recommended values.

Alternatively, two off-chip resistors, R_{H1} and R_{H2}, may be tied to the pins **auxin1** and **auxin2**, respectively, to set the upper bandwidth of the amplifiers. Using off-chip resistors permits a wider range of f_H to be achieved: 10 Hz to 20 kHz. Standard 1% resistor values are given in the table on the following pages. Any resistor with a power rating of 0.01 W or greater may be used. For bandwidths not listed on this table, interpolate or contact Intan Technologies for recommended resistor values.

If off-chip resistors are used, R_{H1} and R_{H2} should be tied from the **auxin1** and **auxin2** pins to chip ground. Care should be taken to minimize parasitic capacitance (such as stray capacitance resulting from long circuit board traces) at the **auxin1** and **auxin2** pins. Resistors should be kept close to the RHD2000 chip on the printed circuit board, particularly when resistor values exceed 1 MΩ.

Setting Lower Bandwidth

Registers 12-13 are used to configure an on-chip resistor that sets the lower bandwidth of the amplifiers (f_L) in the range of 0.1 Hz to 500 Hz. Register values for common bandwidths are listed in a table on the following pages. For bandwidths not listed on this table, contact Intan Technologies for recommended values.

Alternatively, an off-chip resistor R_L may be tied to the pin **auxin3** to set the lower bandwidth of the amplifiers. Using an off-chip resistor permits a wider range of f_L to be achieved: 0.02 Hz to 1.0 kHz. Standard 1% resistor values are given in the table on the following pages. For bandwidths not listed on this table, interpolate or contact Intan Technologies for recommended resistor values.

If an off-chip resistor is used, R_L should be tied between **auxin3** and chip ground. As with R_{H1} and R_{H2}, care should be taken in minimize parasitic capacitance on the **auxin3** pin. This resistor should be kept close to the RHD2000 chip on the printed circuit board, particularly when the resistor value exceeds 1 MΩ.

Fast Settle Function

Due to the potentially long time constant associated with the low cutoff frequency f_L, it may be useful to reset the amplifiers if a large input signal causes the output signals to saturate. To settle the amplifiers, the **amp fast settle** bit in Register 0 should be set high momentarily and then returned to zero. It is recommended (though not required) to hold **amp fast settle** high momentarily after powering up the chip if low values of f_L (< 1 Hz) are used. The recommended duration of a fast settle pulse is $2.5/f_H$; as the upper bandwidth of the amplifiers is lowered, settling takes more time. Using this guideline, if f_H is set to 10 kHz then setting **amp fast settle** high for 250 μs, and then low, sufficient to settle the amplifiers to baseline.

Setting Upper Bandwidth: On-Chip Register Values

The following settings for variables in Registers 8-11 are used to configure the upper bandwidth (f_H) of the amplifiers.

UPPER BANDWIDTH f_H	RH1 DAC1	RH1 DAC2	RH2 DAC1	RH2 DAC2
20 kHz	8	0	4	0
15 kHz	11	0	8	0
10 kHz	17	0	16	0
7.5 kHz	22	0	23	0
5.0 kHz	33	0	37	0
3.0 kHz	3	1	13	1
2.5 kHz	13	1	25	1
2.0 kHz	27	1	44	1
1.5 kHz	1	2	23	2
1.0 kHz	46	2	30	3
750 Hz	41	3	36	4
500 Hz	30	5	43	6
300 Hz	6	9	2	11
250 Hz	42	10	5	13
200 Hz	24	13	7	16
150 Hz	44	17	8	21
100 Hz	38	26	5	31

Setting Upper Bandwidth: Off-Chip Resistor Values

The following resistor values can be used to set amplifier upper bandwidth (f_H) if off-chip resistors are used.

UPPER BANDWIDTH f_H	R_{H1}	R_{H2}
20 kHz	6.80 kΩ	11.5 kΩ
15 kHz	9.10 kΩ	15.0 kΩ
10 kHz	12.4 kΩ	21.0 kΩ
7.5 kHz	15.8 kΩ	26.7 kΩ
5.0 kHz	22.0 kΩ	37.4 kΩ
3.0 kHz	34.0 kΩ	57.6 kΩ
2.5 kHz	39.2 kΩ	66.5 kΩ
2.0 kHz	47.5 kΩ	80.6 kΩ
1.5 kHz	61.9 kΩ	102 kΩ
1.0 kHz	88.7 kΩ	147 kΩ
750 Hz	115 kΩ	191 kΩ
500 Hz	169 kΩ	274 kΩ
300 Hz	270 kΩ	432 kΩ
250 Hz	324 kΩ	511 kΩ
200 Hz	402 kΩ	634 kΩ
150 Hz	523 kΩ	820 kΩ
100 Hz	787 kΩ	1.20 MΩ
75 Hz	1.05 MΩ	1.58 MΩ
50 Hz	1.60 MΩ	2.32 MΩ
30 Hz	2.70 MΩ	3.83 MΩ
25 Hz	3.30 MΩ	4.64 MΩ
20 Hz	4.12 MΩ	5.76 MΩ
15 Hz	5.62 MΩ	7.68 MΩ
10 Hz	8.87 MΩ	12 MΩ

Setting Lower Bandwidth: On-Chip Register Values

The following settings for variables in Registers 12-13 are used to configure the lower bandwidth (f_L) of the amplifiers.

LOWER BANDWIDTH f_L	RL DAC1	RL DAC2	RL DAC3
500 Hz	13	0	0
300 Hz	15	0	0
250 Hz	17	0	0
200 Hz	18	0	0
150 Hz	21	0	0
100 Hz	25	0	0
75 Hz	28	0	0
50 Hz	34	0	0
30 Hz	44	0	0
25 Hz	48	0	0
20 Hz	54	0	0
15 Hz	62	0	0
10 Hz	5	1	0
7.5 Hz	18	1	0
5.0 Hz	40	1	0
3.0 Hz	20	2	0
2.5 Hz	42	2	0
2.0 Hz	8	3	0
1.5 Hz	9	4	0
1.0 Hz	44	6	0
0.75 Hz	49	9	0
0.50 Hz	35	17	0
0.30 Hz	1	40	0
0.25 Hz	56	54	0
0.10 Hz	16	60	1

Setting Lower Bandwidth: Off-Chip Resistor Values

The following resistor values can be used to set amplifier lower bandwidth (f_L) if an off-chip resistor is used.

LOWER BANDWIDTH f_L	R_L
1.0 kHz	5.36 kΩ
750 Hz	5.49 kΩ
500 Hz	5.76 kΩ
300 Hz	6.20 kΩ
250 Hz	6.34 kΩ
200 Hz	6.65 kΩ
150 Hz	7.15 kΩ
100 Hz	7.87 kΩ
75 Hz	8.45 kΩ
50 Hz	9.53 kΩ
30 Hz	11.3 kΩ
25 Hz	12.0 kΩ
20 Hz	13.0 kΩ
15 Hz	14.3 kΩ
10 Hz	16.9 kΩ
7.5 Hz	19.1 kΩ
5.0 Hz	23.2 kΩ
3.0 Hz	32.4 kΩ
2.5 Hz	36.5 kΩ
2.0 Hz	43.0 kΩ
1.5 Hz	56.0 kΩ
1.0 Hz	86.6 kΩ
0.75 Hz	127 kΩ
0.50 Hz	226 kΩ
0.30 Hz	511 kΩ
0.25 Hz	698 kΩ
0.20 Hz	1.05 MΩ
0.15 Hz	1.74 MΩ
0.10 Hz	3.74 MΩ
0.075 Hz	6.65 MΩ
0.050 Hz	15 MΩ
0.030 Hz	33 MΩ
0.025 Hz	50 MΩ
0.020 Hz	100 MΩ

Supply Voltage Levels

RHD2000 chips require a regulated voltage supply (V_{DD}) between 3.2V and 3.6V for operation meeting all performance specifications. A nominal supply voltage of 3.3V is recommended for most applications. All **VDD** pins should be kept at identical potentials.

The following pins should be connected to ground: all **GND** pins and **VESD**. All of these pins must be kept at the same potential, and the DC level of electrophysiological signals connected to the amplifier inputs and reference should be kept at this same ground potential.

In all applications using these chips, it is necessary to tie the biological tissue under observation to chip ground. The DC electrode potentials always should be near chip ground, although small positive or negative electrode-tissue potentials can be present. Electrode potentials should be held within ±400 mV of chip ground. In this input voltage range, DC currents into the input pins are less than ±20 nA.

Power Supply Decoupling Capacitors

A ceramic 100 nF (0.1 µF) power supply bypass capacitor should be connected between **VDD** and **GND** pins, and should be located less than 1 cm from the bottom side of the chip (i.e. pins 15-28) on the printed circuit board. This capacitor should have an X5R or X7R dielectric, should be no smaller than a 0402 SMD device, and should be rated for at least 16V. (While the capacitor will only be exposed to 3.3V, small SMD capacitors are known to dramatically decrease in capacitance as the voltage across the device approaches the maximum rated voltage. It is best to use a capacitor with a voltage rating several times higher than the expected voltage.)

If LVDS signaling is used, a single 100 nF capacitor near the bottom edge of the chip is sufficient to smooth the power supply for the RHD2000. If standard CMOS signaling is used, an **additional** 100 nF capacitor should be placed within 1 cm of the right side of the chip (i.e., pins 29-42).

3.0V Operation

RHD2000 chips can be operated at a lower supply voltage of 3.0V with derated performance in certain areas. Specifically, the lower supply voltage limits the speed of the MUX to switch voltages near the high end of the ADC range. Under 3.3V operation, the amplifiers have a linear input range of ±5.0 mV and the auxiliary inputs have a linear input range of 2.45 V (see the "Auxiliary ADC Inputs" section for details). The following table lists derated input ranges under 2.9V – 3.1 V operation at a variety of ADC sampling rates.

INPUT DERATING WITH 3.0 V SUPPLY VOLTAGE

ADC sampling rate	amplifier linear input range	maximum auxiliary input level	temp sensor accurate?
35 kS/s	±4.5 mV	2.10 V	Yes
70 kS/s	±4.0 mV	2.00 V	Yes
175 kS/s	±4.0 mV	2.00 V	Yes
350 kS/s	±3.5 mV	1.90 V	Yes
700 kS/s	±2.5 mV	1.70 V	No
875 kS/s	±2.2 mV	1.65 V	No
1.05 MS/s	±2.0 mV	1.60 V	No

At sampling rates above 350 kS/s, the on-chip temperature sensor is no longer accurate under 3.0V power supply operation.

Analog-to-Digital Converter

The RHD2000 contains a 16-bit successive-approximation ADC with an integrated analog MUX, allowing it to sample voltage signals from the amplifier array as well as various sensors and auxiliary inputs across the chip. In most applications, the SPI master device will sample all 32 amplifiers (in the case of the RHA2132) in round-robin fashion and then include perhaps three additional commands for sampling auxiliary sensors or sending commands related to impedance measurement. In this case, the per-channel sampling rate will be 35 times lower than the total ADC sampling rate. (See the "SPI Command Sequences" section for details.)

The ADC may be operated at speeds up to 1.05 MS/s, which permits 35 channels to be sampled at 30 kS/s each. The variables **ADC buffer bias** and **MUX bias** in Registers 1 and 2 should be set to the following values based on the total ADC sampling rate:

ADC sampling rate	ADC buffer bias	MUX bias
≤ 120 kS/s	32	40
140 kS/s	16	40
175 kS/s	8	40
220 kS/s	8	32
280 kS/s	8	26
350 kS/s	4	18
440 kS/s	3	16
525 kS/s	3	7
≥ 700 kS/s	2	4

The ADC contains a temperature- and supply-independent voltage reference that requires an off-chip 10 nF ceramic capacitor to be placed near the chip (within 1 cm) and tied from **ADC_ref** to ground. This capacitor should have an X5R, X7R, C0G, or NP0 dielectric and should be rated for at least 16V. (See the "Supply Voltage Levels" section for an explanation of this requirement.) When the chip is active and **amp Vref enable** in Register 0 is set to one, a DC voltage of approximately 1.225 V should appear on this capacitor.

If multiple RHD2000 chips are used, each chip must have its own 10 nF capacitor. The **ADC_ref** pins of different chips should not be connected.

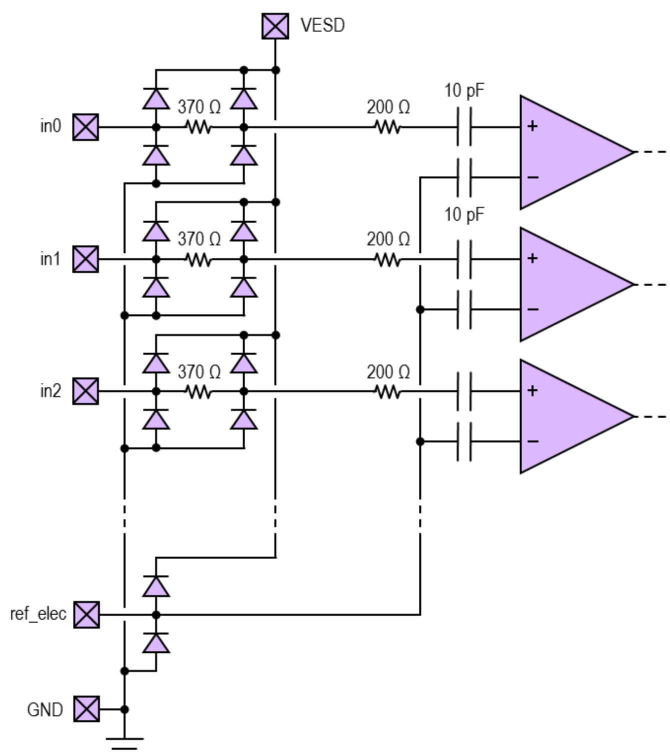
Amplifier Input Protection

All CMOS integrated circuits are susceptible to damage by exposure to electrostatic discharge (ESD) from charged bodies. Electrostatic charges of greater than 1000 V can accumulate on the human body or test equipment and can discharge without detection. All RHD2000 chips incorporate protection circuitry to guard against mild ESD events. However, permanent damage may occur on devices subjected to high energy electrostatic discharges. It is important for users to understand the nature of the ESD protection circuitry used on the chip.

The figure below illustrates the on-chip passive elements (diodes and resistors) used for ESD protection at the input to each amplifier. Diodes are connected to **GND** and **VESD**, and are used to bleed off charge quickly to prevent the voltage on the series capacitors from exceeding damaging levels. Small series resistors (370 Ω and 200 Ω) create voltage drops in response to large ESD currents, further protecting the amplifiers.

The DC level of all amplifier input pins should be within ±400 mV of ground. This prevents the ESD diodes from becoming significantly forward biased and passing current. As long as the voltage across the diodes does not exceed 400 mV, the resulting current will be less than 20 nA. The reference electrode on the RHD2132 has six times more ESD diodes than the amplifier input pins, so input bias current due to excursions away from ground will be six times larger on this pin.

The **VESD** pin should normally be tied to ground for safety and noise reasons. A high-energy ESD event could potentially short out any ESD diode. If **VESD** is tied to ground, then severe damage to any diode will only short the associated electrode to ground. Since any tissue contacted by electrodes should be grounded, no DC current will flow into the tissue. If, instead, **VESD** is tied to a voltage above ground, no significant current will flow under normal conditions since the corresponding diode will be reverse biased. However, if that diode is damaged in an ESD event, the voltage at **VESD** will be tied directly to the electrode, possibly resulting in high DC currents and tissue damage.



The voltage on **VESD** is capacitively coupled to the amplifier input through the capacitance of the reverse-biased ESD diode, so any voltage on this pin should be kept free of AC noise. Otherwise, noise will be injected directly into the amplifier input (and the electrode). For these reasons, it is strongly recommended to tie the **VESD** pin to ground.

The only time it may be useful to tie **VESD** to a higher potential is during electrode activation (see the "Electrode Activation" section for more information). **VESD** should never be tied to voltages higher than V_{DD}.

Additional Off-Chip Components for ESD Protection

Series resistors may be added between electrodes and the input of each amplifier to improve ESD robustness. However, series resistors also add thermal noise that increases the total electrode-referred noise on each channel. The rms noise added by a series resistor R is given by

$$v_{n,\mathrm{rms}} = \sqrt{4kTR \cdot \mathrm{BW}}$$

where BW is the amplifier bandwidth and kT = 4.12×10^{-21} J at 25ºC.

This noise adds to the inherent amplifier noise in a sum-of-squares manner. The following table lists series resistor values that may be used with various amplifier bandwidth settings if a 10% increase in amplifier noise (above the baseline of 2.4 μV_{rms}) can be tolerated.

amplifier bandwidth ($f_H - f_L$)	maximum R for 10% increase in noise
200 Hz	180 kΩ
500 Hz	68 kΩ
1.0 kHz	33 kΩ
2.0 kHz	18 kΩ
5.0 kHz	6.8 kΩ
10 kHz	3.3 kΩ

The resistor values listed in this table assume that series resistors are added to both the positive and negative inputs (or reference input) of each amplifier.

ESD protection may be further strengthened through the use of external transient voltage suppressors manufactured by a variety of semiconductor companies (e.g., Vishay, Littelfuse, STMicroelectronics).

Electrode Impedance Test

All RHD2000 chips have built-in circuitry that provides selectable, direct access to any of the amplifier input pins for the purpose of measuring the impedance of electrodes connected to the chip. Additional on-chip circuitry is provided to generate an AC current waveform needed to measure electrode impedance. Also, an input pin (**elec_test**) is provided for connecting external current or voltage generators to any selected amplifier input pin.

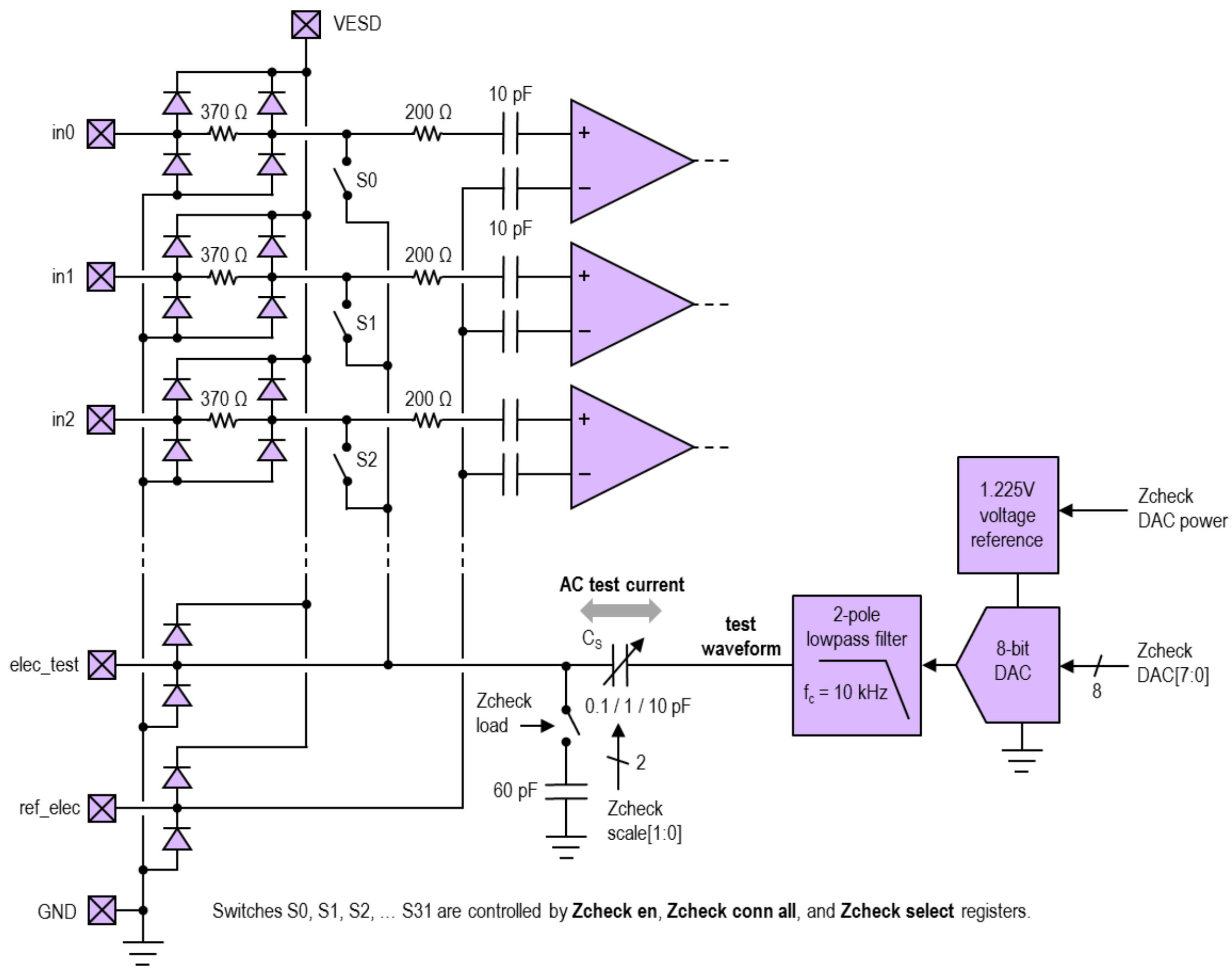
The figure on the next page shows a detailed schematic of the amplifier array input circuitry on the RHD2132; input circuitry for the RHD2216 is similar. Transistor switches S0 through S31 can be closed to connect one selected amplifier to the on-chip current generator as well as the auxiliary input pin **elec_test**. If the register **Zcheck en** is set to zero, all switches remain open. This is the normal mode of operation for the chip.

If **Zcheck en** is set to one, then the switch corresponding to the amplifier that is selected by the **Zcheck select** register is closed, and that amplifier's input is connected to the on-chip current generator and the **elec_test** pin. This mode of operation should be used for measuring the impedance of individual electrodes. If an AC current waveform (with no DC current component) is generated on chip or applied to the **elec_test** pin from an external source, then the resulting voltage waveform will pass through an amplifier and may be observed by the ADC. The impedance of the electrode may then be calculated as the ratio of peak voltage to peak current.

Note that this technique requires small currents, as the RHD2000 amplifiers saturate for input voltages larger than ±5.0 mV. For example, a 5 nA peak current will elicit a 5 mV peak voltage with an electrode impedance of 1 MΩ.

Note that any impedance measurement will include the capacitance of the on-chip amplifiers (10 pF), the ESD protection diodes (0.4 pF), and approximately 1.6 pF of parasitic capacitance associated with the bond pad and QFN package. This 12 pF of capacitance has an impedance magnitude of 13 MΩ at 1 kHz, and should only affect impedance measurements for relatively high-impedance electrodes. The ESD protection resistors have very small values, and are unlikely to significantly affect impedance measurements of typical electrodes.

The RHD2216 has two independent input pins for each amplifier, so an extra register called **Zcheck pol sel** is provided to select between the positive and negative amplifier input pins during electrode impedance testing. When **Zcheck pol sel** is set to zero, **Zcheck en** connects the on-chip current generator and **elec_test** to the positive input terminal (**inX+**) of the selected amplifier. When **Zcheck pol sel** is set to one, the impedance testing circuitry is connected to the negative input terminal (**inX–**).



On-Chip AC Current Waveform Generator

RHD2000 chips include circuitry for generating user-specified AC current waveforms that may be directed to any selected electrode for the purposes of impedance testing. The waveform generator consists of an 8-bit digital-to-analog converter (DAC) followed by a two-pole 10 kHz low-pass filter to smooth the "stairstep" edges of the DAC waveform. The DAC is enabled by setting the **Zcheck DAC power** bit to one. The voltage produced by the DAC varies from a minimum of 0 V to a maximum of (255/256) × 1.225 V = 1.220 V, and is set by the register **Zcheck DAC**. Incrementing this register by one increases the DAC output voltage by (1/256) × 1.225 V = 4.785 mV.

The resulting "test waveform" is connected to the selected electrode via a series capacitor C_S that transforms the AC voltage into an AC current. The value of this capacitor is selectable by means of the **Zcheck scale** register and can have a value of 0.1 pF, 1.0 pF, or 10 pF.

If the DAC/filter produces a voltage waveform $v_{DAC}(t)$, the resulting current $i_{DAC}(t)$ injected to the electrode under test is given by

$$i_{\mathrm{DAC}}(t) = C_{\mathrm{S}} \frac{dv_{\mathrm{DAC}}(t)}{dt}.$$

If the DAC output is unchanging then $i_{DAC} = 0$, so the SPI master must regularly update the output DAC to create an AC voltage waveform in order to produce an AC current waveform through the series capacitor. For example, the DAC could be used to approximate a sine wave with an amplitude V_A and a DC offset of V_{off} (which is needed since the DAC output cannot go below zero), described as

$$v_{\mathrm{DAC}}(t) = V_{\mathrm{A}} \sin(2\pi f t) + V_{\mathrm{off}}.$$

The resulting current injected into the electrode under test will be a cosine wave with zero offset and amplitude given by:

$$i_{\mathrm{DAC}}(t) = 2\pi f C_{\mathrm{S}} V_{\mathrm{A}} \cos(2\pi f t).$$

For example, if we regularly update the DAC to approximate a 1 kHz sine wave with the maximum possible amplitude of 1.225V / 2 = 0.6125V (and an offset of 0.6125V), then the following table shows the current amplitude produced by all possible series capacitor settings:

C_S	CURRENT AMPLITUDE WITH 1 kHz SINE WAVE (MAX. AMPLITUDE)
0.1 pF	0.38 nA
1 pF	3.8 nA
10 pF	38 nA

If we chose a series capacitor value of 1 pF and connected the 3.8 nA amplitude AC current waveform to a 1 MΩ electrode, the resulting electrode voltage would have an amplitude of 3.8 nA × 1 MΩ = 3.8 mV, which is within the ±5.0 mV range of the amplifiers.

If the frequency of the test waveform were reduced to 100 Hz then the test current would also drop by a factor of ten. However, switching C_S from 1 pF to 10 pF would boost the current back to its original value.

By adjusting the series capacitor value and the amplitude of the waveform produced by the DAC, the AC test current amplitude can be adjusted to measure a wide range of electrode impedances at a number of different frequencies.

Electrode Activation

The on-chip switches S0 through S31 may also be used to apply DC voltages to selected amplifier input pins in order to activate or electroplate various types of electrodes after they have been connected to the chip. DC voltages must be applied through the **elec_test** pin. During this process, **VESD** will need to be connected *temporarily* to a higher voltage (such as V_{DD}) to prevent forward biasing of the ESD protection diodes. Note that the "on" resistance of each on-chip transistor switch (nominally around 400 Ω) increases significantly as the applied DC voltage rises above ground.

If negative voltages need to be applied to the electrodes (relative to some electrolyte) then the electrolyte must temporarily be held at a potential above chip ground. The DC voltage applied to **elec_test** must remain between chip ground and **VESD** at all times. See the Intan Technologies RHA2000 Series datasheet for more information on electrode activation and electroplating. The concepts described there can be applied to the RHD2000 chips.

If both the **Zcheck en** and **Zcheck conn all** bits of Register 5 are set to one, all switches are closed simultaneously. This connects all amplifier inputs to the **elec_test** pin in parallel. This mode of connectivity may be used to activate or electroplate all electrodes in an array concurrently. This mode *cannot* be used to test the impedance of all electrodes simultaneously; rather, it shorts all electrodes together, so any impedance measurements would return the impedance of all electrodes in parallel.

Temperature Sensor

The RHD2000 chip includes an on-chip temperature sensor that can be read using the ADC. Making temperature measurements is a multi-step process that requires making several analog-to-digital conversions and performing some simple arithmetic to process the results.

The temperature sensor is controlled by several bits in Register 3: **tempen**, **tempS1**, and **tempS2**. If the temperature sensor is not used, **tempen**, **tempS1**, and **tempS2** can each be set to zero to reduce power consumption by 70 µA. Before performing a temperature measurement the bit **tempen** should be set to one to enable the temperature sensor module. After setting this bit, at least 200 µs should elapse before a temperature reading is made to allow time for the sensor circuitry to reach equilibrium. (All other operations may be performed on the chip during this time.)

The procedure for taking a temperature measurement involves several steps:

1. Set **tempS1** = 1 and **tempS2** = 0, and wait at least 100 µs.
2. Set **tempS1** = 1 and **tempS2** = 1, and wait at least 100 µs.
3. Sample the output of the temperature sensor (channel 49) with the ADC. We will call this number "resultA".
4. Set **tempS1** = 0 and **tempS2** = 1, and wait at least 100 us.
5. Sample the output of the temperature sensor (channel 49) with the ADC. We will call this number "resultB".
6. Calculate "resultB – resultA". We will call this number "result". This will always be a positive number.

Steps 1-6 should be repeated four times, and the four results should be averaged. (The temperature sensor automatically cycles through four distinct configurations as the **tempS1** and **tempS2** bits are toggled.) From the final averaged value of "result", the temperature is calculated as follows:

$$T(^\circ C) = (result / 98.9) - 273.15$$

Note all that other chip operations may be performed during the waiting periods specified in steps 1, 2, and 4 above, so temperature sensor operations may be interleaved between normal amplifier sampling (see the "SPI Command Sequences" section for examples). It is recommended that no "power up/down" operations be performed while a temperature reading is in progress, as any change in overall power consumption may cause the chip temperature to change.

After a temperature reading is complete, set **tempS1** = 0 and **tempS2** = 0 to minimize power consumption. If another temperature reading will not be needed for some time, set **tempen** = 0.

Temperature readings may vary up to ±2ºC from chip to chip. If precise temperature measurements are required, each chip should be calibrated at a known temperature.

Supply Voltage Sensor

The supply voltage of the chip (V_{DD}) may be measured by sampling channel 48 of the ADC. (The **VDD sense enable** bit in Register 1 must be set to one before sampling.) An on-chip voltage divider scales the supply voltage down by a factor of two to accommodate the ADC range of 2.45 V. The supply voltage may be calculated from the ADC result as:

$$V_{DD}(V) = 0.0000748 \times \text{result}$$

This feature is useful when a chip is operated over a long cable, to make sure that the resistance of the power and ground wires do not cause the local power supply voltage to drop below acceptable levels. (See the "Supply Voltage Levels" section for more information on low supply voltage operation.)

Auxiliary ADC Inputs

If on-chip registers are used to set the amplifier bandwidth then the **auxin1**, **auxin2**, and **auxin3** pins may be used as auxiliary inputs to the ADC. This allows external analog sensors (e.g., an ADXL335 3-axis accelerometer) to be easily interfaced to a RHD2000-based system. The MSBs of Registers 8, 10, and 12 must be set to one to select on-chip bandwidth setting resistors, and the MSBs of Registers 9, 11, and 13 must be set to one to enable buffers that drive the auxiliary signals to the ADC.

The **auxin1**, **auxin2**, and **auxin3** pins may be sampled on ADC channels 32, 33, and 34, respectively. The voltage range of these input pins is 0.10 V to 2.45 V, so any voltage that would exceed this level should be scaled down using off-chip voltage dividers or other circuitry. (The chip will not be damaged as long as the voltage on these pins stays between -0.4V and +3.6V, but the ADC value will saturate.) The voltage on an auxiliary input pin may be calculated from the ADC result as:

$$\text{auxin}(V) = 0.0000374 \times \text{result}$$

Each auxiliary input has a buffer with a high-impedance CMOS input that draws nearly zero current. These buffers will introduce a small random offset voltage, typically in the range of ±5 mV.

Auxiliary Digital Output

All RHD2000 chips have a single user-programmable digital output pin **auxout** which may be used to control an external device via SPI commands. Register 3 contains two control registers that configure the state of this signal: setting **digout HiZ** to zero enables the **auxout** pin; if **digout HiZ** is set to one then the **auxout** pin assumes a high-impedance state. The **digout** register controls the value of the **auxout** pin. If **digout** is set to zero then **auxout** is driven to ground; if **digout** is set to one then **auxout** is driven to V_{DD}. The **auxout** pin can supply a maximum of ±2 mA while maintaining proper logic levels. If additional drive current is needed, the user must add external circuitry.

For example, the auxiliary digital output could be used to control the gate of an external MOSFET that optionally shorts **ref_elec** to ground, or enables an LED or laser diode for optogenetic stimulation. It is important to remember that the values of the **digout HiZ** and **digout** registers are indeterminate when the chip is first turned on, so care should be taken to ensure that any device connected to this pin does not cause trouble if the **auxout** pin assumes an unexpected value when the chip is initially powered up.

DSP High-Pass Filter for Offset Removal

RHD2000 chips include a custom digital module that performs digital signal processing (DSP) to implement single-pole high-pass filters on each sampled amplifier channel. This feature can be used to remove the residual DC offset voltages associated with the analog amplifiers, which can range from ±100 μV (referred to the electrode). The DSP module can also be used to add an additional pole of high-pass filtering to the single pole inherent in the amplifier circuits. The chip uses an IIR filter architecture; the magnitude and phase characteristics of this filter are similar to those of an analog high-pass filter implemented with a capacitor and resistor.

The DSP high-pass filter module is enabled by setting the **DSPen** bit in Register 4 to one. The DSP module only affects amplifier channels (ADC channels 0-31); auxiliary ADC inputs, temperature sensor readings, and supply voltage readings are not filtered.

The cutoff frequency of the DSP high-pass filter is determined by two factors: the rate at which each amplifier channel is sampled (f_{sample}), and the four-bit **DSP cutoff freq** variable in Register 4. The cutoff frequency f_c is calculated using the following equation:

$$f_c = k_{freq} \cdot f_{sample} = \frac{\ln\left(\frac{2^N}{2^N - 1}\right)}{2\pi} \cdot f_{sample}$$

where N is the value of the **DSP cutoff freq** variable, ranging from 1 to 15. Calculated values of k_{freq} are presented in the table below for convenience:

DSP cutoff freq [3:0]	k_{freq} ($f_c = k_{freq} \cdot f_{sample}$)
0	differentiator; see below
1	0.1103
2	0.04579
3	0.02125
4	0.01027
5	0.005053
6	0.002506
7	0.001248
8	0.0006229
9	0.0003112
10	0.0001555
11	0.00007773
12	0.00003886
13	0.00001943
14	0.000009714
15	0.000004857

Note that f_{sample} is the sampling frequency of each channel; not the overall ADC sampling frequency.

For example, if we sample each amplifier channel at 30 kSamples/s and set the **DSP cutoff freq** variable to 12, the resulting DSP high-pass cutoff frequency will be 0.00003886 × 30 kHz = 1.2 Hz, which is a good value for removing offsets while preserving low frequency biological signals such as cortical local field potentials (LFPs). Alternatively, if we sample at 30 kSamples/s/channel and set the **DSP cutoff freq** variable to 4, the resulting DSP high-pass cutoff frequency will be 308 Hz, which is a good value for removing LFP fluctuations so that neural action potentials can be subjected to amplitude thresholds.

If the **DSP cutoff freq** variable is set to zero, the DSP filter acts like a perfect differentiator; the output of the filter is the current ADC result minus the previous ADC result for a particular channel.

Since the DSP filter has perfect linearity while the analog amplifier circuits have imperfect linearity, it is good practice to set the DSP cutoff frequency f_c higher than the analog amplifier lower cutoff frequency f_L to minimize the distortion of large signals.

If a large signal is applied to an amplifier channel with the DSP filter enabled, the sampled output will "hard limit" at the numerical minimum or maximum permitted by the 16 bit representation; it will not "roll over" due to numerical overflow or underflow.

When using the DSP filter module, it is important to sample amplifiers at a steady and consistent rate. The filter state variables for each channel are updated only when that particular channel is sampled. If each channel is not sampled at exactly the same rate during the time the DSP filter is enabled, the filter output will not be accurate.

The time constant associated with the DSP high-pass filter is given by $1/(2\pi f_c)$. If a step input is applied to the filter, the output will exponentially decay back to zero with this time constant. If a relatively low value of f_c is used (e.g., less than 1 Hz), the time constant can become quite long and result in long recovery times from large transient signals. Each channel's DSP high-pass filter can be instantly reset to zero by setting the LSB of the ADC convert command to one. This operation clears the digital state variable associated with the selected amplifier channel.

Absolute Value Mode

If the **absmode** bit in Register 4 is set to one, the output result from all amplifier channels (channels 0-31) is passed through an absolute value function: all negative results are sign inverted so that the output of each channel is a strictly positive "full wave rectified" waveform. This destroys some information in the waveform (e.g., both –100 and +100 are reported as +100), but this function may be useful if only the amplitude or "energy" of a signal is required for a particular application. (See Fig. 6 in the "Measured Performance Characteristics" section for an example.)

For example, in a system that detects and counts neural spikes using a simple threshold algorithm, enabling absolute value mode allows the controller to check only one threshold instead of checking both a positive and negative threshold. Also, many EMG-based prosthetic limb controllers estimate the energy or envelope of the EMG signal, and computing the absolute value of the raw EMG waveform is often the first step in this estimation. The ability of the RHD2000 to perform this operation automatically can relieve some of the computational burden on the controller in an electrophysiology acquisition system.

It is recommended that absolute value mode be used with the DSP high-pass filter enabled so that the amplifier offsets are removed and the baseline level of each channel will be precisely zero.

Power Dissipation

Total power dissipation of a RHD2000 chip depends on how it is configured and operated. Following is a list of guidelines for estimating total supply current under various operating conditions.

Baseline amplifier array current: The amplifier array on each RHD2000 pulls 200 μA of quiescent current to power various voltage references and bias current generators.

Amplifiers: Each amplifier consumes current in proportion to its upper cutoff frequency, approximately 7.6 μA/kHz per amplifier.

Baseline ADC currrent: Each ADC pulls 510 μA of quiescent current to power various voltage references and bias current generators. (This baseline level may be reduced by 180 μA by setting **amp Vref enable** to zero, and by another 80 μA by setting **ADC comparator bias** to zero, but the ADC will be unusable with these settings.)

ADC and MUX dynamic current: The ADC/MUX assembly consumes additional current in proportion to the total sampling rate, approximately 2.14 μA/(kS/s).

DSP high-pass filter: The DSP offset removal filter does not consume significant power.

LVDS I/O: If **LVDS_en** is pulled high to enable on-chip LVDS driver and receivers, the chip pulls an additional 5700 μA with 3.3V VDD (4740 μA with 3.0V VDD). Current draw with standard CMOS signaling is proportional to SPI data rate and MISO wire capacitance; for low data rates and short wires, it is very small.

Impedance measurement module: With **Zcheck DAC power** set to one, the DAC used for impedance testing consumes 120 μA.

Temperature sensor: Under normal operation, the temperature sensor consumes roughly 70 μA.

Supply voltage sensor and auxiliary ADC inputs: When enabled, each of these extra inputs to the ADC consumes roughly 10 μA, though this number is somewhat proportional to ADC sampling rate.

Using these guidelines, we can now estimate whole-chip power dissipation for various electrophysiology recording applications. In the examples listed here, we assume that in addition to the 16 or 32 amplifiers, an additional 3 auxiliary sensors are sampled every sampling period.

Example: Wideband neural recording headstage

RHD2132
f_H = 10 kHz
sample rate = 35 × 30 kS/s/channel = 1.05 MS/s

Baseline amplifier array current: 200 μA
Amplifiers: 32 × 7.6 μA/kHz × 10 kHz = 2432 μA
Baseline ADC current: 510 μA
ADC/MUX: 2.14 μA/(kS/s) × 1.05 MS/s = 2247 μA
LVDS I/O: 5700 μA
Impedance measurement: 120 μA
Temperature sensor: 70 μA
Supply voltage, auxiliary inputs: 4 × 10 μA = 40 μA

Total supply current: 11.3 mA
Total power dissipation: 11.3 mA × 3.3 V = 37.3 mW

Note: This example represents the maximum possible power dissipation of the RHD2132 chip.

Example: ECoG recording front-end

RHD2132
f_H = 1 kHz
sample rate = 35 x 2 kS/s/channel = 70 kS/s

Baseline amplifier array current: 200 μA
Amplifiers: 32 × 7.6 μA/kHz × 1 kHz = 243 μA
Baseline ADC current: 510 μA
ADC/MUX: 2.14 μA/(kS/s) × 70 kS/s = 150 μA
LVDS I/O: off (assume nearby microcontroller)
Impedance measurement: 120 μA
Temperature sensor: 70 μA
Supply voltage, auxiliary inputs: 4 × 10 μA = 40 μA

Total supply current: 1.33 mA
Total power dissipation: 1.33 mA × 3.3 V = 4.4 mW

Example: EMG-based prosthetic limb controller

RHD2216
f_H = 1 kHz
sample rate = 19 x 2 kS/s/channel = 38 kS/s

Baseline amplifier array current: 200 μA
Amplifiers: 16 × 7.6 μA/kHz × 1 kHz = 122 μA
Baseline ADC current: 510 μA
ADC/MUX: 2.14 μA/(kS/s) × 38 kS/s = 81 μA
LVDS I/O: off (assume nearby microcontroller)
Impedance measurement: 120 μA
Temperature sensor: off
Supply voltage, auxiliary inputs: 4 × 10 μA = 40 μA

Total supply current: 1.07 mA
Total power dissipation: 1.07 mA × 3.3 V = 3.5 mW

SPI Command Sequences

The rate and timing of SPI commands sent to the chip determines the ADC sampling rate; sample times are set by the falling edge of $\overline{CS}$. In most applications, all 16 or 32 amplifiers on the chips will be sampled in round-robin fashion. This can be accomplished by repeating the following command sequence:

CONVERT(0)
CONVERT(1)
CONVERT(2)
…
CONVERT(30)
CONVERT(31)

If a per-channel sampling rate of R is desired, then SPI commands are sent at a rate of 32R.

The problem with simply repeating 16 or 32 CONVERT commands is that additional commands (e.g., to change a register value or sample an auxiliary sensor) must be substituted for regular CONVERT commands (which results in a missing sample on one channel) or else the sequence must be interrupted by an inserted command, which makes the per-channel sampling rate irregular.

The simplest solution to this problem is to always insert a fixed number (typically 1-3) of extra "auxiliary" commands into the round-robin command sequence:

CONVERT(0)
CONVERT(1)
CONVERT(2)
…
CONVERT(30)
CONVERT(31)
auxiliary command 1
auxiliary command 2
auxiliary command 3

Now having a list of 35 commands, the SPI commands are sent at a rate of 35R to achieve a per-channel sampling rate of R. Extra commands (e.g., to update the impedance check DAC, to control the temperature sensor, or to sample an auxiliary sensor) may be inserted into one of the auxiliary command "slots", and these extra commands will not interrupt the steady, constant-rate sampling of the amplifiers on the chip. Dummy commands (e.g., reading a ROM register) can be inserted into these slots as place holders when no auxiliary actions are required.

Circuit Board Design

Careful printed circuit board (PCB) design is critical for achieving the specified performance of the RHD2000. The chip is designed to work with a single ground and a single V_{DD}; it is not necessary (or recommended) to use separate "analog" and "digital" power lines. Rather, it is important to use a good ground plane and power plane underneath the chip. This requires the use of a four-layer PCB, at minimum. If a four-layer board is used, the top (first) and bottom (fourth) layers should be used for signal routing. The second layer should be a ground plane and the third layer should be a V_{DD} plane.

A 100 nF (0.1 μF) ceramic capacitor between V_{DD} and ground should be placed as close as possible to the bottom of the chip (i.e., pins 15-28). See the "Supply Voltage Levels" section for guidance selecting the proper type of capacitor. If standard CMOS signaling will be used, place an **additional** 100 nF decoupling capacitor near the right side of the chip.

A 10 nF ceramic capacitor should be tied from **ADC_ref** to ground and placed close to the bottom or right side of the chip, near the **ADC_ref** pin. See the "Analog-to-Digital Converter" section above for guidance selecting the proper type of capacitor.

If LVDS signaling is used, 100 Ω termination resistors for $\overline{CS}$, SCLK, and MOSI should be placed within 20 cm of the chip. The 100 Ω termination resistor for MISO should be placed near the controller and will likely not reside on the same board as the RHD2000. (Many LVDS receivers and FPGAs have built-in termination resistors, so this device may not be necessary.)

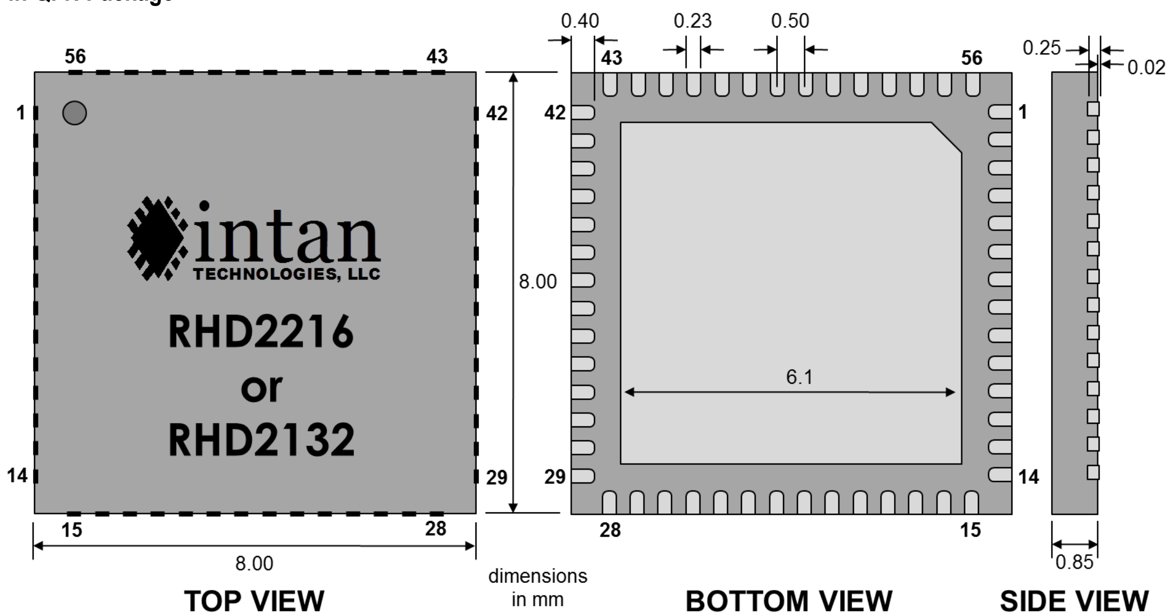
A recommended PCB footprint for QFN-packaged RHD2000 chips is shown on the following page. The center pad of the QFN package is not connected internally, but should be tied to ground for electrical shielding. If a solder paste mask is used for reflow assembly, the paste mask for the center pad should be made smaller than the pad so excess solder is not deposited. When the QFN component is placed on the PCB, excess solder paste from the center pad can short to peripheral pins.

In some size-critical applications, users may wish to use bare die for chip-on-board (COB) assembly. Intan Technologies can supply bond pad diagrams for RHD2000 chips to aid in the development of COB PCBs.

Package Dimensions

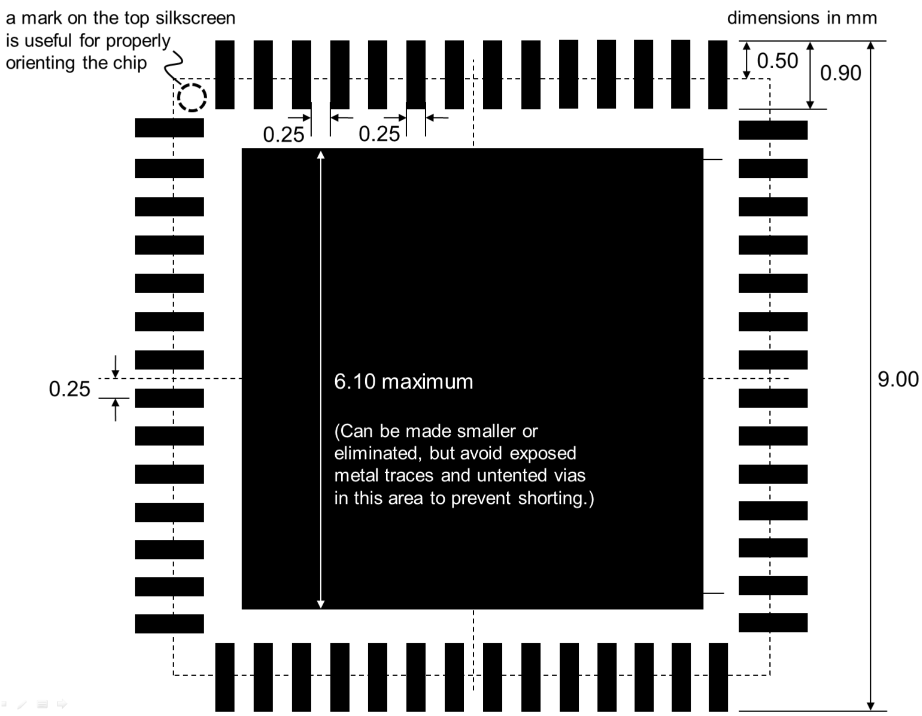
All dimensions are in millimeters.

56-Pin QFN Package



Printed Circuit Board Layout

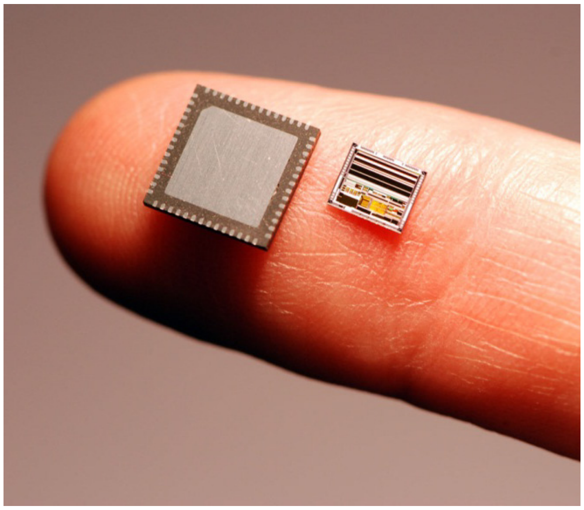
56-Pin QFN Package



Note: The center pad is not internally connected but should be soldered for mechanical integrity and tied to ground (GND) for electrical shielding.

Pricing Information

See **www.intantech.com** for current pricing. All price information is subject to change without notice. Quantities may be limited. All orders are subject to current pricing at time of acceptance by Intan Technologies. Additional charges may apply for international purchases and shipping.



Contact Information

This datasheet is meant to acquaint engineers and scientists with the general characteristics of the RHD2000 series of digital electrophysiology interface chips developed at Intan Technologies. We value feedback from potential end users. We can discuss your specific needs and suggest a custom integrated solution tailored to your applications.

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