

ABSTRACT

YIN, MING. A Multi-Channel Wireless Implantable Neural Recording System. (Under the direction of Dr. Maysam Ghovanloo).

This dissertation presents a multi-channel implantable wireless neural recording (WINeR) system for electrophysiology and behavioral neuroscience research applications. This system consists of two units: a system-on-a-chip (SoC) transmitter unit and a receiver unit built with off-the-shelf components. A novelty of the WINeR system is in its utilization of a wireless single-slope ADC technique by inserting a wireless link in between a pulse width modulator and a time-to-digital converter (TDC). This technique not only offers the WINeR system the benefit of a single-slope ADC, but also makes the WINeR transmitter unit very simple, low power, and small in regards to chip area. In addition, by directly transmitting pulse width modulation (PWM) signal, the pulse rate over the wireless link is reduced to the sampling rate, while a moderate system resolution can still be achieved. Another novelty of this system is that its transmitter uses an asynchronous (clockless) topology and achieves very low noise levels by eliminating the on-chip clock. Some of the other features of this system are the wideband FSK demodulator and FPGA-based TDC in the receiver unit capable of achieving high resolution, low noise, low power, low cost, and ease of implementation.

A 32-channel WINeR transmitter prototype is implemented in a standard CMOS

technology, and operates in the 900MHz ISM band. A prototype WINeR receiver is also built using off-the-shelf components with up to 75MHz bandwidth. A custom developed VC++ GUI running on a PC interface with the receiver unit through a USB port and facilitates data storage and visualization. In addition, detailed noise analysis is conducted both theoretically and experimentally to further characterize the performance of the system. Finally, the full functionality of the entire WINeR system has been validated from bench-top, and through *in vivo* experiments on rats.

A Multi-Channel Wireless Implantable Neural Recording System

by
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DEDICATION

To

My Parents, My Wife, and My Son

BIOGRAPHY

Ming Yin was born in 1978, in Hunan Province, China. He received his Bachelor of Science (B.S.) and Master of Science (M.S.) Degrees in Electronics Engineering from Tsinghua University, Beijing, China, in 2001 and 2004, respectively. In Fall 2004, he started his Ph.D. program in the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh, NC, USA. His Ph.D. research is on developing a wireless microsystem for multi-channel neural recording applications. His research interests include low-noise, low-power analog/RF, and mixed-mode circuit design for wireless and biomedical applications, system integration, and interface design for operating micro, nano, and bio systems.

Ming Yin is a student member of the Institute of Electrical and Electronics Engineers (IEEE) and a member of Phi Kappa Phi. He has received Analog Device Outstanding Student Designer Award in 2006.

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CHAPTER 1 Introduction

1.1 Motivation

Witnessing the rapid growth of the theories and disciplines in modern neuroscience, one can expect a revolution in our understanding of the secrets of the human brain hidden within those intricate rules. Discovering the real principles that govern the operations of the brain will not only provide enormous benefits to the medical fields but will also lead to explaining what makes us human.

Understanding how the brain works requires “understanding the neural code”. “To crack the neural code” is the cutting-edge of modern neuroscience, involving a combination of many other areas of research such as biology, genetics, biomedical engineering, electrical engineering, robotics, and computer sciences. These days, researchers work on building systems called hybrid brain-machine interfaces (HBMI) to record, decode and restore the activities of the brain [1.1]. Aimed to be a bidirectional system, HBMI contain both stimulation and recording subsystems. The stimulation subsystem uses artificial electrical signals to stimulate the neurons in order to deliver some particular type of sensory information to the brain or to mimic a particular neurological function. The recording subsystem uses real-time sampling and processing of large-scale brain activities to detect the intentions of the user and control devices in the user’s environment or his/her artificial limbs.

In both subsystems, the effective outcomes require gathering enough neural information that would lead us to the right direction towards interpreting the myriad activities in the human brain. That is exactly the functional description of the neural recording system, which we aimed to develop.

For decades, many scientists were dedicated to collecting signals from the neurons in different ways. E. D. (Lord) Adrian (1891-1977) was the first to employ instruments sensitive enough to record from single axons of sensory receptor neurons. Adrian's work done in 1920's won him the Nobel Prize in 1932. His work also leaded us to the area of neural recording for the first time. For most of the 20th century, neuroscientists were able to observe the electrical activity of only a single neuron at a time. However, the brain is a very complicated system. It has about 100 billion (10^{11}) neurons and 100 trillion (10^{14}) connections (synapses) between them [1.2]. Modern neuroscientists have found out that neural activities involve the cooperative interaction of large populations of single neurons [1.3]-[1.5]. They are also revealing an ever growing line of new applications for multi-channel neural recording systems.

Defined as a “multi-channel Wireless Implantable Neural Recording (WINeR) system”, we developed a multi-channel neural recording system with wireless capability and implantable characterstics. The advantage of wireless implantable devices over the wired

non-implantable ones is that they can avoid having a large number of wires connected to the patients or test subjects. As such, it offers them great comfort and extended freedom of movement. It is also safer in reducing the risk of infection significantly. Thanks to micromachining technology (MEMS), researchers have already built high density multi-channel microelectrode arrays and interconnects smaller than the size of a button [1.6]-[1.9]. MEMS technology combined with rapid advancements in VLSI, radio frequency (RF) integrated circuits, and communication techniques combined with neuroscience research, set the stage for development of the WINeR system.

1.2 Background

For the past few decades, the field of neural recording systems has been generating great attention and interest. From single channel neural recording using large amplifiers, to multi-channel recording using racks of instrumentation, to wireless neural recording with a small backpack, to wireless implantable neural recording, and finally to the multi-channel WINeR system, neural recording technology has evolved in many different ways. All of these improvements are indispensable parts in the history of the neural recording technology, which will be briefly reviewed in the rest of this section.

After the unprecedented work of E. D. Adrian, one of the earliest works in wireless neural recording was carried out by T. B. Fryer et al. in 1960's and 1970's. Their work

covers both single-channel and multi-channel telemetry systems, and some of them are used for implantable applications [1.10]-[1.17]. There are also other interesting works done at that time, such as J. B. Meindl's work on implantable ultrasonic blood flowmeters [1.18], R. D. Rader's work in cardiovascular telemetry implants [1.19], C. M. Steven's work in blood pressure measurements [1.20], H. Eichenbaum's work in building pioneering telemetry systems for single-neuron recording and wireless brain stimulation [1.21], R. Wertz's work in designing micro-powered multi-channel PAM/FM biotelemetry system for brain research signal [1.22], J. Kruger's work in simultaneous recording from many cerebral neurons [1.23], Y. Yonezawa's work in multi-channel telemetry system for recording cardiovascular neural signals [1.24], and several others. All these works have used telemetry for data transmission. However, because of the technological limitations in IC design and fabrication, all the above systems were built by using discrete components. Therefore, they either suffered from large dimensions and heavy weight or high power consumption, which made them impractical for implanting.

Prior to the 1980s, there were few experiments conducted with meaningful wireless extracellular neural recordings. It was a major challenge to develop robust telemetry systems to record neural signals at that time, because an extracellular single-unit neural action potential is a spike of only 50 μ V to 500 μ V in amplitude and 0.1 Hz to 10 kHz in bandwidth. In 1980s, continuous improvements in manufacturing miniaturized electronic

components (e.g. surface-mount devices) and novel design methodologies in ASIC design resulted in robust multi-channel telemetry microsystems suitable for neuroscience research.

In 1986, K. Najafi and K. D. Wise developed in a pioneering work for the first time, a ten-electrode implantable extracellular recording array with on-chip signal processing circuitry. The circuit operated from a single 5 V supply, consuming an area of 1.3 mm^2 , and dissipating 5 mW of power, but it was not a wireless system [1.25]. In 1994, T. Akin and K. Najafi developed an inductively powered and controlled implantable neural recording system with CMOS interface circuitry and telemetry. The system could handle neural recordings of $\pm 500 \mu\text{V}$ signals from regenerated peripheral nerve axons. The ASIC was dissipating 15 mW of power from a 5V supply, and sized $4 \times 4 \text{ mm}^2$ on chip [1.26]-[1.27]. Later in 1998, they upgraded the system and developed an implantable, fully integrated, multi-channel extracellular neural recording system [1.28]. Their new system including the RF interface circuitry contained over 5000 transistors, had two front-end neural amplifiers, and sized $4 \times 6 \text{ mm}^2$ on chip. However, a big problem of this system is the 90 mW power dissipation and the limited recording sites from two simultaneous channels. In 1997, C. Enokawa et al. built a passive implantable telemetry system for a two-channel EMG measurement system [1.29]. However, this system also had only two channels and suffered with limited data rate of 144 bps. In 1998, H. Maki et al. designed a high capacitance (2.5F) capacitively powered implantable telemetry system [1.30], which was able simultaneously

record the cardiac sympathetic nerve activity and ECG signal. After 5 minutes capacitive charging, this system could operate for 120 minutes. But the big capacitor and limited recording channels made it impractical for implantable applications. In 1997, J. Parramon et al. presented an implantable batteryless telemetric microsystem for EMG recording [1.31]. The system was based on a single 30 mm^2 high-voltage $2.5 \mu\text{m}$ BiCMOS ASIC, including telemetric two-channels recording circuitry. Except the limited number of recording channels, this system suffered from short receiving distance (15mm) and low data rate (112kbps). In 1997, H. J. Song et al. also reported a single-chip system for the acquisition, digitization, and wireless telemetry of biological signals [1.32]. The problem with this single-channel system was that it consumed 10 mW of power, which was not quite efficient. Also in 1997, M. Modareszadeh and R. N. Schmidt developed and clinically tested a mobile, low power, 32-channel, miniature, ISM-band RF telemetry system (902-928 MHz) for real-time electroencephalography (EEG) for epilepsy monitoring and evaluations [1.33]. However, it was very large ($6.4 \times 5.1 \times 1 \text{ cm}^3$) and weighted 68g. From the research done in 70's, 80's and 90's, summarized above, the trends of evolution in neural recording systems can be observed: there is a transition from discrete board-level designs with commercially available electronic components to single-chip, fully integrated, implantable multifunctional ICs; from single neuron recording to multi-channel recording; and from wired communications to wireless systems.

Today, we see even more research on neural recording systems focusing on multi-channel wireless single-chip, fully integrated, implantable, multifunctional designs. One of the major groups active in this field is the Wireless Integrated MicroSystems (WIMS) center at the University of Michigan. In 2001, H. Yu and K. Najafi designed a wireless microsystem for neural recording that contained front-end circuitry, delta-sigma modulator, control logic, and on-chip data transmitter [1.34], but it was a single channel system. In 2003, P. Mohseni and K. Najafi presented a four-channel wireless microsystem suitable for a variety of biomedical neural recording applications [1.35]. This system consisted of a 2.2×2.2 mm² chip and only 4 off-chip components (1 inductor and 3 capacitors) that were wire bonded to the chip. The entire system including two 1.5 V batteries measured $1.8 \times 1.3 \times 0.16$ cm³, weighed 1.1 g, and dissipated less than 2.5 mW. In 2005, P. Mohseni et al. improved their previous work and developed a system with smaller size ($1.7 \times 1.2 \times 0.16$ cm³) and better performance in biological setups (operating distance of 0.5 m with SNR > 8.4 dB, I/O correlation coefficient > 80%) [1.36]. Their final 8-ch system was also developed in 2005 by P. Mohseni and K. Najafi [1.37]. That system had a total size of $2.1 \times 2.1 \times 0.16$ cm³, and was operated at 94~98 MHz carrier frequency, powered with two 1.5 V batteries, and consumed a 2.05 mW power. For those systems developed by P. Mohseni and K. Najafi, they were fully analog systems and suffered huge channel crosstalk. For example, their final 8-channel system had more than 37.1% crosstalk. In addition, the use of commercial FM

receiver limited the bandwidth to be only 150 kHz. Finally, their front-end amplifier had large input referred noise ($\sim 10\mu\text{V}_{\text{rms}}$), which degraded the SNR. Other than the wireless systems, the WIMS group at Michigan has also put a lot of effort in the realization of MEMS-based multi-channel active neural recording (not wireless). So far, they reported systems which can record from up to 256-sites with 32 of them being simultaneous [1.6], [1.7], [1.38], [1.39]. The Michigan group has also carried out interesting work in development of microelectrodes used for probing the neural signals [1.40]-[1.43], and systems for monitoring other kinds of bio-signals [1.44]-[1.46].

Another major activity on neural recording systems is going on at the University of Utah under the direction of R. R. Harrison and R. A. Normann. They have developed some inspiring circuits for modern neural recording systems. The most important work that Harrison's team has contributed to the neural recording area is their low-power low-noise CMOS amplifier design [1.47], in which they presented a topology that used MOS-bipolar pseudo resistor for ultra low frequency high pass control for the neural amplifier. This design has been adopted by many other researchers, and, more importantly, has resurrected a figure-of-merit for noise performance known as the noise efficiency factor (NEF), which is defined as:

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (1.1)$$

where $V_{ni,rms}$ is the input referred rms noise voltage, I_{tot} is the total amplifier supply current, and BW is the amplifier bandwidth in hertz. U_T is the thermal voltage kq/T . k is the Boltzmann constant. T is the absolute temperature. An amplifier using a single bipolar transistor (with no $1/f$ noise) has an NEF of one; all practical circuits have higher values. Using NEF encouraged designers to invent topologies and techniques with successively lower and improved NEFs. In addition, Harrison et al. developed micropower circuits for bidirectional wireless telemetry in neural recording applications [1.48], adaptive threshold spike detection [1.49], low-power FM transmitters [1.50], and floating gate common mode feedback circuit for low noise amplifiers [1.51]. In 2006, R. R. Harrison et al. presented a wireless recording SoC with 100 electrodes [1.52]. It interfaced with a 100 electrodes Utah Microelectrode Array. Its 433MHz FSK wireless link provided 330kbps data rate. Its 2.64 MHz inductive link received power and commands wirelessly. The complete system SoC was implemented in the AMI 0.5 μm 3-metal 2-poly standard CMOS process, measured 4.7×5.9 mm^2 , and consumed a total power of 13.5 mW. However, this system had only 330kbps bandwidth, and could only transfer a signal channel high resolution data at a time, while all other 99 channels were in spike detect mode. Meantime, the transmitting distance was limited to be only 2 cm.

In addition to the aforementioned groups, there are a lot of other groups, which conducted impressive work in recent years. One of them is W. Liu's group, previously in North Carolina State University, now in University of California at Santa Cruz. In 2001, M. Dagtekin et al. presented a 32-site 8-channel fully integrated neural recording system by using chopper modulation technique to reduce the flicker noise and DC offset of the preamplifiers [1.53]. Their system consumed approximately 750 μ W of power. But this system was only in the simulation stage and was not implemented. In 2008, M. Chae and W. Liu et al. developed a 128 channel wireless neural recording system with 6-9 bits of resolution for all channels [1.54]. The 128 channels were divided into 16 groups, each contained 16 neural amplifiers and a 640kSps 9-bit successive-approximation (SAR) ADC. To reduce power dissipation, each group was enabled one by one. In order to handle up to 90Mbps data produced by the system, an ultra-wide-band (UWB) wireless link was implemented in this system. The entire system was implemented in a TSMC 0.35 μ m 4-metal 2-ploy CMOS process, consumed 8.8×7.2 mm² chip area and 6.0mW total power. However, neither bench-top nor *in vivo* recording results from this system have been reported. In 2003, R. Bashirullah et al. presented the simulated performance of an inductively powered bidirectional telemetric system for an implantable retinal prosthetic device implemented in a 1.5 μ m CMOS process that incorporated a smart feedback system via reverse telemetry to compensate for instantaneous changes in power level due to coil misalignment and load

variations [1.55]. At UCLA, in 2003, P. Irazoqui-Pastor et al. reported *in vivo* EEG recordings from un-tethered rodents using an inductively powered implantable wireless neural recording device [1.56]. The disadvantage of that system is it only has one channel. In 2003, G. A. DeMichele et al. reported a 16-channel integrated wireless biotelemetry system dissipating 18 mW of power from a 4.75 V supply in a 1.5 μm BiCMOS process [1.57]. Unfortunately, this system suffered major input referred noise ($\sim 150 \mu\text{V}_{\text{rms}}$) due to the bad design of the ESD structure, which made it incapable for actual neural recording applications. In 2004, E. A. Johannessen et al. reported a microelectronic pill utilizing system-level integration of sensors and integrated circuits in a recording device [1.58]-[1.60]. The system was fabricated in a 0.6 μm CMOS process that consumed 12.1 mW of power, measured $5.5 \times 1.6 \text{ cm}^2$, and weighed 13.5 g including two silver-oxide batteries. However, this system was focusing on temperature, pH, conductivity, and dissolved oxygen monitoring and had only 4 channels. In 2004, C. Chestek et al. developed an 8-channel wireless sensor for neurodynamic studies [1.61]. The sensor was interfaced with a commercially available microcontroller and wireless transmitter. It measured $3 \times 1.5 \text{ cm}^2$, and was powered by a 3 V, 160 mAh lithium-ion battery. The problem with this system was the 5kbps wireless link, which was even not enough to handle a single channel neural data. At Duke University, J. Morizio et al., in 2005, reported a 15-channel wireless headstage for neuroprosthetics that measured $2.5 \times 2.5 \times 1.3 \text{ cm}^3$, and weighed 8.3 g including two batteries [1.62]. However,

it was subject to signal distortion and low fidelity on signal quality due to its analog architecture. At Jet Propulsion Laboratory (JPL), in 2003, M. Mojarradi et al. built a miniaturized neuroprosthesis suitable for implanting into the brain [1.63]. The prosthesis had a heterogeneous integrated circuitry for signal acquiring and a second CMOS integrated circuit for wireless transmission of neural data and conditioning of wireless power. Although they have implanted an intracortical electrode array and 8×8 -element concept front-end integrated circuit for initial evaluations, the wireless transceiver and wireless power integrated circuit was in the early concept stages. And they were still facing the problems of transmitting digital neural information at the required rate and electromagnetic tissue absorption during the wireless power transfer.

Other than the above work produced mainly by engineers, many neuroscientists, such as A. L. Nicolelis and P. D. Wolf in Duke University, J. P. Donoghue and W. R. Patterson in Brown University, and N. Thakor in Johns Hopkins University, have built their own custom wireless neural recording systems for their applications. In 2004, I. Obeid et al. presented a design for a wearable telemetry system [1.64], weighing 235 g, measuring $5.1 \times 8.1 \times 12.4$ cm³, and capable of transmitting up to 12 signals from implanted electrodes. However, the system was not integrated and the total power consumption was very large (4 W). In 2007, Y. -K. Song et al. developed a 16-channel brain implantable microsystem with hybrid RF/IR telemetry [1.65]. This system utilized 13.56 MHz RF for both power and data

forward link. At the same time, it had an infrared (IR) data link employing a very low threshold current IR vertical cavity surface emitting semiconductor laser (VCSEL). The concept of an optoelectronic data link enabled considerable system flexibility for future neural prosthesis applications, including very large bandwidth capability up to 10Gbps. The complete system was assembled on dual-panel flexible liquid crystal polymer (LCP) with a total size of $\sim 2 \times 2\text{cm}^2$. However, the large power dissipation cost by the commercial 1MSps 12-bit ADC (AD7495, Analog Devices, Inc., Norwood, MA) (10.5mW) and the IR VCSEL (8585-1003, Emcore Corp., Albuquerque, NM) (50mW) prevented it from being used in close proximity to brain tissue. In addition, the use of IR link for data transfer required the IR VCSEL and the receiving photodiode to be placed and oriented in a fixed position, which was extremely difficult in *in vivo* freely moving animal testing. In 2008, M. Mohsen et al. presented a 16-channel wireless recording system [1.66]. It was powered by a separate telemetry chip, which harvested power from a 4 MHz inductive link. The telemetry module was also used to transmit low frequency neural data (EEG and ECoG) over the same link back to the base station across 4 cm distance at up to 32 kbps with a BER less than 10^{-5} . Obviously this system was limited by the transmitting distance and data rate.

In addition to systems developed by academic universities or groups, some of the commercially available devices also support multi-channel wideband operation. One example, offered by Triangle Biosystems (Durham, NC) [1.67] provides a 6-hour operation system

with 31 channels. However, it is subject to signal distortion due to its analog FM transmission method, and the battery life is too short to meet the multi-day recording objectives. Neurasytems (Bozeman, Montana) [1.68] offers a large number of channels (128) but uses relatively high power consumption and a battery life of only 4 hours.

In summary, neural recording systems have evolved in the past decades from simple single-channel wired external devices to complex multi-channel bidirectional wireless implantable systems. Utilizing novel methodologies in low-power low-noise ASIC design have brought about many of these changes. However, combining high-performance mixed-signal/RF circuit blocks on the same silicon substrate towards developing a highly integrated, robust, multi-channel, wireless microsystem with effective biological *in vivo* functionality and ease of use still presents numerous technical challenges that are yet to be resolved. This is probably why none of the numerous aforementioned wireless neural recording systems has found a wide application in neuroscience laboratories yet. My Ph.D. research work aims at developing a WINeR system with better performance over the aforementioned works in many ways, such as more simultaneous recording channels, less power, lower noise, longer transmitting range, smaller chip area, and less complexity. Table 1. 1 summarizes the state-of-the-art wireless neural recording system and compared some of the most important specifications for these systems. In the last column of Table 1. 1, I also list the performance of our latest WINeR system [1.69], from which we concluded that our

system is superior to other systems in terms of number of high resolution simultaneous channels, entire system noise, data rate (with traditional wireless schemes), transmitting range, power dissipation, and also chip area and complexity (as shown in the highlighted areas in Table 1. 1). Figure 1. 1 shows their corresponding photographs.

Table 1. 1 State-of-the-art wireless neural recording systems

	Irazoqui-Past or [1.8]	Mohseni [1.36]	Johannessen [1.58]	Yu [1.70]	Harrison [1.71]	Sodagar [1.72]	Song [1.65]	Chae [1.54]	This work [1.69]
No. of Channels	1	1 or 3	4	8	1 (analog) or 88 (spike detect)	4 16-ch chips	16	128	32 + 4 monitoring
Input referred noise	$\sim 8 \mu\text{V}_{\text{rms}}$ Amp only	$7.1 \mu\text{V}_{\text{rms}}$ Amp only	$5.94 \mu\text{V}_{\text{rms}}$ Amp only	-	$5.1 \mu\text{V}_{\text{rms}}$ Amp only	$\sim 8 \mu\text{V}_{\text{rms}}$ Amp only	$9 \mu\text{V}_{\text{rms}}$ Amp only	$4.9 \mu\text{V}_{\text{rms}}$ Amp only	$4.9 \mu\text{V}_{\text{rms}}$ Entire
Telemetry Freq.	3.2 GHz	94-98 MHz	20-40 MHz	50-150 MHz	433 MHz	70-200MHz	IR (infrared) optical	4GHz UWB	915MHz
Data Rate	-	-	1 kbps	2.56 Mbps	330 kbps	2 Mbps	Up to 10Gbps	up to 90Mbps	Equivalently $>5.12 \text{Mbps}$
Comm. Scheme	Analog FM	TDM/Analog FM	TDMA/FSK	TDM/Digital OOK	TDM/Digital FSK	TDM/FSK	Digital IR using VCSEL	OOK/PPM impulse UWB	FSK/ OOK
Power Supply	Ext. Inductive 2-3.2V	Battery $\pm 1.5\text{V}$	Battery 3.1V	Inductive 3.3V	Inductive 3.3V	Inductive 1.5-3V	Battery 3V	Battery $\pm 1.65\text{V}$	Battery $\pm 1.5\text{V}$
Power Diss.	5-8mW	1.66mW or 2.2mW	12.1mW	12.7mW	13.6mW	14.4mW@1. 8V	1.4mW Amp chip only	6.0mW	5.6mW
Trans. Range	0.5 m	0.5 m	1 m	-	-	-	-	-	>1m
Dimension	$0.5 \times 0.5 \times 1$ cm^3	$1.7 \times 1.2 \times 0.16$ cm^3	$1.6 \times 5.5 \text{ cm}^2$	-	-	$1.4 \times 1.55 \text{ cm}^2$	$\sim 2 \times 2 \text{ cm}^2$	-	$3.0 \times 2.4 \text{ cm}^2$
Chip Area	$< 1 \text{ mm}^2$	4.484 mm^2	22.5 mm^2	$4.6 \times 4.7 \text{ mm}^2$	27.3 mm^2	$3.5 \times 2.74 \text{ mm}^2$, $1.9 \times 1.2 \text{ mm}^2$, $4.6 \times 4.6 \text{ mm}^2$	$2.2 \times 2.2 \text{ mm}^2$	$8.8 \times 7.2 \text{ mm}^2$	$3.3 \times 3 \text{ mm}^2$
Total Weight	-	1.1g	13.5g	12g	-	0.275g	-	-	-
External Comp.	-	3	8	-	-	-	-	-	6
Technology	$0.35 \mu\text{m}$ CMOS	$1.5 \mu\text{m}$ CMOS	$0.6 \mu\text{m}$ CMOS	$1.5 \mu\text{m}$ CMOS	$0.5 \mu\text{m}$ CMOS	$0.5 \mu\text{m}/1.5 \mu\text{m}$ CMOS	$1.5 \mu\text{m}$ CMOS	$0.35 \mu\text{m}$ CMOS	$0.5 \mu\text{m}$ CMOS
Implementation	Single chip	Single chip	Hybrid	Single chip	Single chip	Multi chip	Hybrid	Single Chip	Single Chip
Presented Year	2003	2004	2004	2004	2005	2007	2007	2008	2009

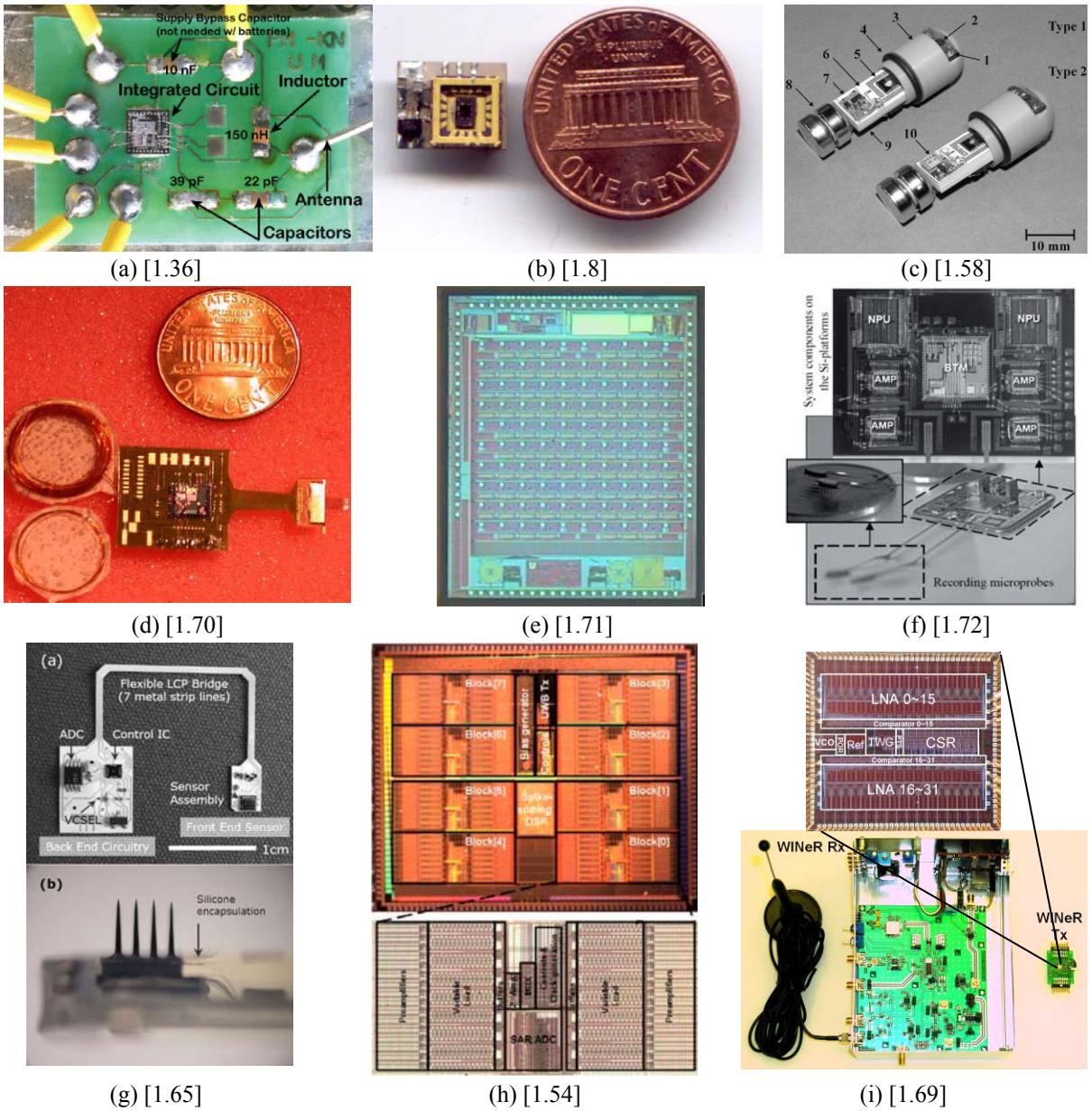


Figure 1.1 State-of-the-art wireless neural recording systems.

1.3 Dissertation Outline

This dissertation has been organized as follows: Chapter 2 gives a brief description

of the pulse-width-modulation time-division-multiplexing WINeR system architecture followed by the developing history of the WINeR system. Chapter 3 describes the latest system-on-chip (SoC) 32-channel WINeR-V transmitter. Chapter 4 details the custom-designed wideband WINeR receiver and its graphic user interface (GUI). Chapter 5 provides detailed noise analysis for the entire WINeR system using the pulse width technique. Chapter 6 demonstrates the *in vivo* testing results for the WINeR systems. Chapter 7 discusses the conclusion and the possible future improvements of the WINeR system.

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CHAPTER 2 WINeR System Architecture

2.1 Challenges of Designing the WINeR System

There are quite a few advantages of the wireless neural recording systems over the hardwired ones according to the discussion in the early part of Chapter 1, however designing multi-channel wireless implantable neural recording system involves quite a few challenges.

1. Very high input impedance

Since the impedance of the probe interface with the brain can be quite high [2.1] (several $M\Omega$), therefore the WINeR front-end preamplifiers with very high input impedances should be used to maximize the amplitude of the captured signals.

2. Low noise, large signal bandwidth, and robustness against DC baseline drifts

Table 2. 1 shows a list of important biopotentials and their wide range of frequencies and amplitudes [2.2]. Extracellular neural action potentials (ENAP) are one of the most challenging ones to record. They contain frequency components from $0.1 \sim 10$ kHz and amplitudes in $50 \sim 500$ μV range with background noise levels of $5 \sim 10$ μV . These signals usually carry DC baselines up to 500 mV due to electrode-electrolyte interactions [2.3]. The low-level signal amplitude, wide frequency range, and large DC baseline are the major

challenges when designing neural recording amplifiers. In addition, robustness of the amplifier in order to guarantee its proper operation in spite of the process and ambient variations is a major requirement. Finally, it would be useful to have a robust amplifier with tunable bandwidth as well as variable gain that could be used for different types of biopotential signals or different components in one type of biological signal.

Table 2. 1 Characteristics of different biomedical signals [2.2]

Biopotential	Frequency Range	Amplitude Range
EEG	0.5 ~ 40 Hz	typically 0.001- 0.01mV
EMG	20~ 2000 Hz	typically 1 ~ 10 mV
ECG (EKG)	0.05 ~ 100 Hz	typically 1~ 5mV
EOG	DC ~ 10 Hz	typically 0.01 ~ 0.1 mV
ENAP	0.1~10 kHz	typically 50 ~ 500 μ V

3. Low power dissipation

Since the SoC WINeR transmitter is intended to be implanted into the animal or human body, and is usually powered with batteries, the entire implant needs to be extremely energy efficient to maximize the lifetime of the internal battery, and minimize its size. We should also minimize the internal power dissipation which can raise the temperature of the tissue surrounding the implant. The exact value depends on the location of the implant inside the body [2.4]. Histopathological studies show that the limits of a 2°C temperature increase,

of 40 mW/cm^2 heat flux, and of 1.6mW/g of specific absorption rate (SAR) are valid for most tissues in the body [2.5]. Because of the limited researches that have been done on the hypothermia on the neural tissues, it is still unclear that if a chronic regional change in temperature on the order of 1 or 2°C , as might be induced by the implants, would cause changes in the brain function that would be reflected behaviorally or psychologically. Therefore, the safe levels of temperature increase for neuroprostheses could be even more restricting [2.5].

4. Small dimensions

Implantable systems should be as small as possible to minimize surgical risks and discomforts to the patients. Depending on the anatomical positions, the exact size limitations are quite different. But for the WINeR system, as a rule of thumb, it should be less than 1cc, which is a feasible size for implanting. In general, the smaller the size of the implant the better it will be.

5. Wireless

A wireless neural recording system can offer major advantages. For instance, it can achieve higher signal-to-noise-ratio (SNR), reduce the tethering effect and allow behavioral neuroscience researchers use multiple animals in their experiments. For clinical applications

on human, it can reduce risk of infection and tissue damage. However, a key challenge for designing such systems is the bandwidth. To handle multiple channels simultaneously and wirelessly send all the acquired information outside for further signal processing, a wide bandwidth is needed throughout the system all the way from the electrodes to the computer.

Table 2. 2 Number of channels vs. minimum required sampling and data rates
(Assumptions: 20kSps/ch, 8-bit resolution, no overhead)

Number of Channels	1	10	32	100	1000
Sampling Rate (kSps)	20	200	640	2000	20,000
Data Rate (Mbps)	0.16	1.6	5.12	16	160

Table 2. 2 shows the number of channels verses the minimum required sampling rate and data rate. In our case, for example, for a 32-channel system, at least 5~7 Mbps is needed, depending on the required resolution. Another issue about the wireless system is the tissue absorption for the radio frequency electromagnetic power. According to [2.6], as RF frequency exceeds 100 MHz, well below the microwave range, the tissue absorption is about 2×10^{-2} mW/cm³ for a 1 mW/cm² plane wave. This is important from two aspects. First it will attenuate the wireless signal and result in a lower SNR. Secondly, the absorption will lead to tissue heating.

6. Implant micro-assembly and packaging

For implantable devices, implantable assembly in a way that is minimally invasive to the body and at the same time provides protection to the implants itself is a major challenge. Biocompatibility and hermeticity are very important for realizing a clinically implantable device.

2.2 WINeR System Architecture

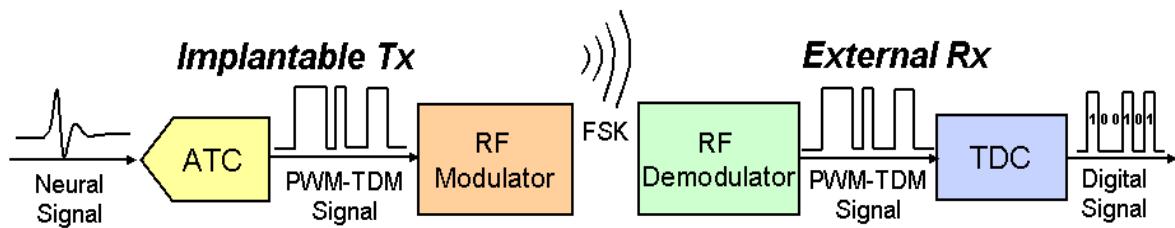


Figure 2.1 PWM-TDM-based WINeR system architecture.

Our philosophy in designing the WINeR system has been to keep the implantable transmitter as simple, small, and low power as possible even at the cost of complicating the external receiver. This would make sense because the size and power are less constraint outside of the body. We have utilized a pulse width modulation (PWM) time division multiplexing (TDM) based technique, which is similar to a single-slope ADC that is made wireless. As shown in Figure 2.1, the idea is to convert analog samples to time by pulse width modulation, transmit the resulting FSK signal across the wireless link, and finally convert time to digital on the receiver side. This approach is simple, robust, and monotonic. Interestingly, it does not even need an on-chip clock, which can contaminate our analog

samples.

2.3 WINeR Developing History

In the journey of developing the WINeR system, we have gone through several versions from WINeR-I to WINeR-V, which involves a transition from smaller number of channels and lower performance to larger number simultaneous channels and better performance. In the following, I'll briefly discuss the precursors (WINeR-I to IV) of the final WINeR-V and the problems they possess. In the next chapter (Chapter 3), I will discuss in detail about the 32-channel WINeR-V transmitter SoC utilizing the aforementioned PWM-TDM architecture.

2.3.1 Two-Channel WINeR-I

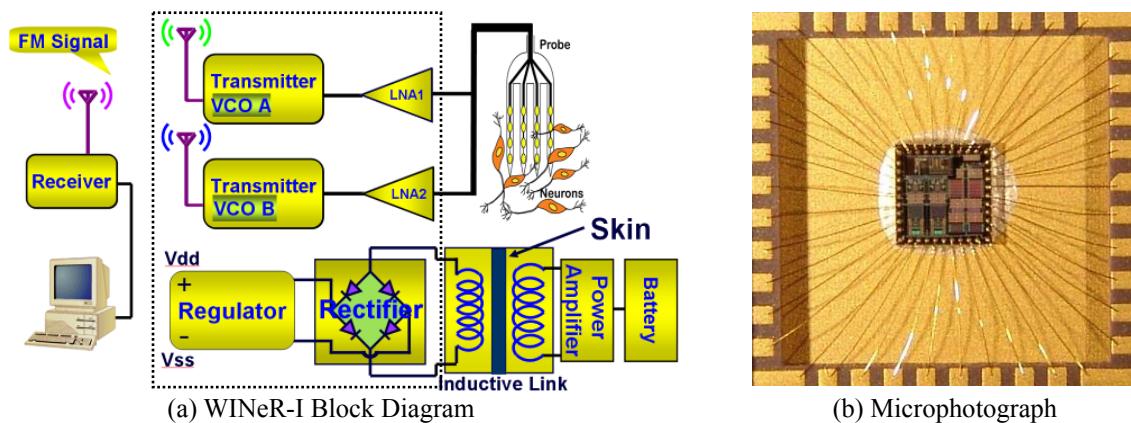


Figure 2.2 WINeR-I system block diagram and microphotograph.

In the first trial, we developed a 2-channel WINeR that was all analog. WINeR-I was fabricated in the MOSIS AMI 1.5 μm 2-metal 2-poly n-well standard CMOS process in a 2.2 mm \times 2.2 mm chip. Figure 2. 2 shows the WINeR-I block diagram and die micrograph. In WINeR-I, each channel had an individual front-end preamplifier/filter and a voltage controlled oscillator (VCO). The preamplifier/filter block had user selectable gains and a 0.1 Hz to 10 kHz bandwidth. The amplified neural signals directly modulated the inductive-capacitive (LC) VCO carrier frequencies around 250 MHz, which could also be modified by changing the off-chip inductor. The transmitted FM signals were received and demodulated by a commercial software controlled radio receiver – WR1550e (WinRadio Communications, Melbourne, Australia). The system test results showed that the smallest pulse that could be detected by the WINeRS-I was \sim 20 μV , which was sufficient for real neural signal recording.

Problems with WINeR-I: Although WINeR-I was functional, it had some problems. First of all, it only had two channels. Secondly, its fully analog design was very sensitive to noise and difficult to ensure good signal fidelity under various channel impairments such as multipath or shadowing. Thirdly, the FM modulation technique required a high linear VCO to achieve low distortion. Finally, having individual VCO for each channel consumed a lot of power. After noticing these issues, we have implemented WINeR-II.

2.3.2 Fifteen-Channel WINeR-II

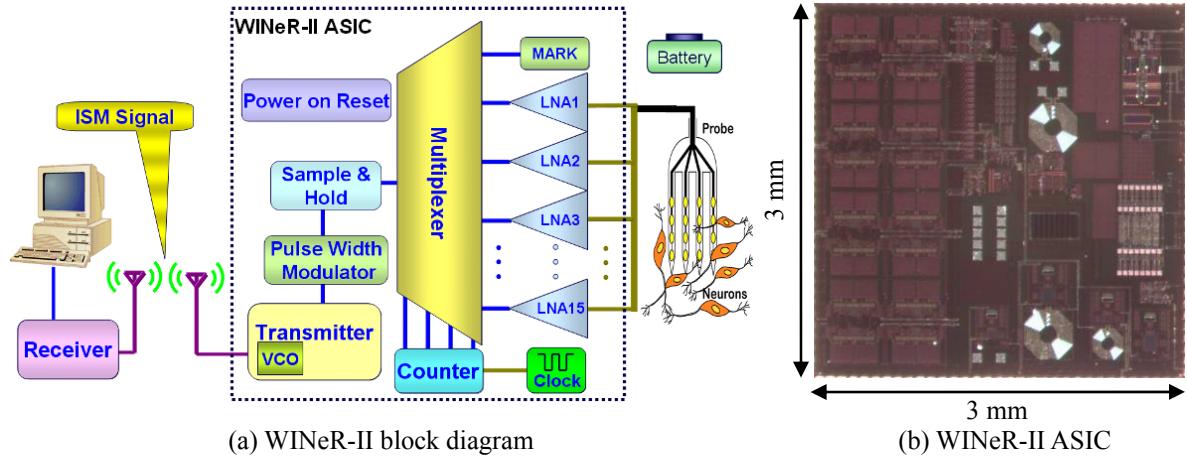


Figure 2. 3 WINeR-II system block diagram and microphotograph.

WINeR-II is a 15-channel wireless neural recording ASIC, which was designed, fabricated, and tested. This system consists of the following blocks that are connected as shown in Figure 2. 3a: a low-noise low-power operational transconductance amplifiers array (LN-OTA), a time division multiplexer (TDM), pulse width modulator (PWM), a transmitter (LC-VCO), a power on reset, and an external commercial receiver (WR1550e). The 3 mm \times 3 mm WINeRS-II ASIC was fabricated in the AMI 0.5 μ m, n-well, 3-metal, 2-poly CMOS process and is shown in Figure 2. 3b. The ASIC was powered by two 1.5 V batteries and drew only 1.5 mA (4.5 mW). For details, please refer to [2.7].

Problems with WINeR-II: WINeR-II was the first WINeR system that utilized the PWM-TDM technique, and we have successfully wirelessly transmitted and received a 20Hz

sine wave by using this system. However there were a lot of problems existing in WINeR-II.

- i. LN-OTA block: 1. Large offset due to the single-ended configuration. 2. Large settling time. 3. Insufficient high pass function and distortion due to the diode PMOS pseudo resistor. 4. Limited control flexibilities over the low-cutoff and gain.
- ii. PWM block: WINeR-II was the first prototype that used the PWM topology. However it did not work properly. The measured on-chip triangular waveform (TW) had uneven amplitudes which never went from rail-to-rail. This is because the frequency fluctuation of the on-chip clock and the cascode configuration of the current source limited the swing of the TW. Furthermore, the on-chip clock injected large noise and interference into the TW signal.
- iii. Wireless link: 1. Limited tunability of the transmitter VCO for compensating temperature and process variation. 2. Limited bandwidth of the receiver. A commercial receiver with only 230 kHz bandwidth was used for both WINeR-I and II. Though it was enough for the 2-channel WINeR-I, it was insufficient for the 15-channel 320 kHz sampling rate WINeR-II. The 230 kHz bandwidth receiver rounded the edge of the received PWM signal and created errors to the system.
- iv. On-chip clock interference: Huge noise was coupled from the 2.93MHz on-chip clock to the sensitive analog front through the substrate, which was mainly due to the compact layout and bad floor plan of the WINeR-II ASIC.

2.3.3 Four-Channel Clockless WINeR-III

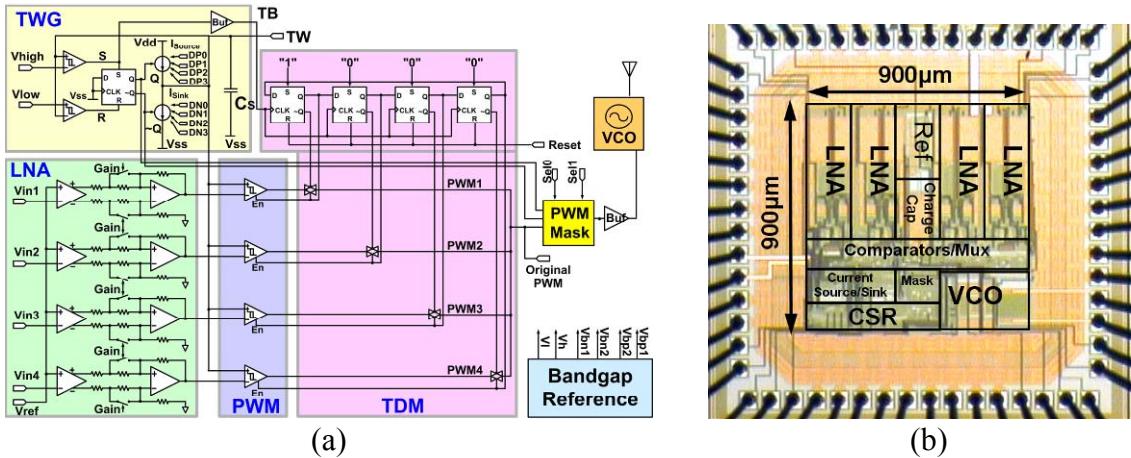


Figure 2. 4 (a) 4-channel WINeR-III system block diagram. (b) WINeR-III chip.

Revisiting the major problem that WINeR-II had, we realized that we needed to minimize or even get rid of the noise coupling from the on-chip clock. Our answer is an asynchronous (or clockless) system. To validate this idea, a 4-channel prototype WINeR SoC (WINeR-III) with a novel architecture based on TDM of PWM samples has been implemented in the AMI 0.5- μm standard CMOS, occupying 0.81 mm^2 and consuming 4.8 mW at ± 1.5 V when all channels are active. The WINeR-III system block diagram, chip micrograph, and floor plan are shown in Figure 2. 4. WINeR-III eliminated the need for off-chip components (crystal), digital buffers, and more importantly, high frequency on-chip clock. Even though only 4 channels have been included in the analog front-end due to the limitation of the chip area, the rest of the system, particularly its adjustable sampling rate and

wireless link, have been designed to handle up to 32 simultaneous channels. The measured input referred noise for the whole system (1~10 kHz) was only $7.3\text{uV}_{\text{rms}}$. For details, please refer to [2.8].

Problems with WINeR-III: Although WINeR-III has achieved unprecedented performance comparing to its precursors, it still has three major problems. 1. The DC coupling topology between the 1st and 2nd stage amplifiers made the entire LNA very vulnerable to the 1st stage offset, which easily saturated the LNA output. 2. The PWM comparators did not have any internal hysteresis, and were very sensitive to noise. 3. The total number of channels was still far below the desired value.

2.3.4 Six-Channel Clockless WINeR-IV with FG LNAs

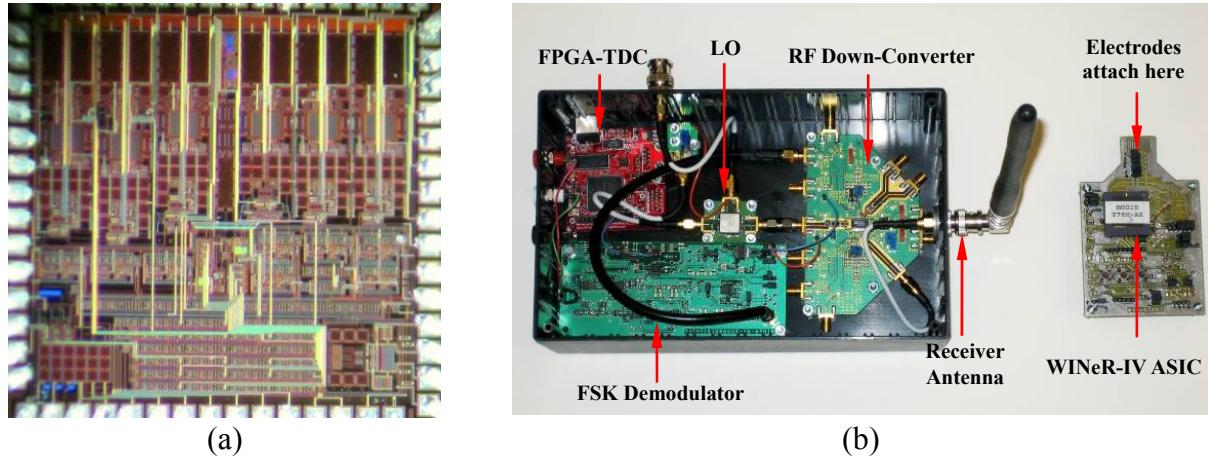


Figure 2.5 (a) WINeR-IV ASIC microphotograph. (b) WINeR-IV transmitter and receiver.

To address the remaining issues of WINeR-III, a 6-channel clockless WINeR-IV was developed in the AMI 0.5- μ m standard CMOS (see Figure 2. 5a), occupying 2.25 mm² and consuming 5.0 mW at \pm 1.5 V when all channels are active. The differences between WINeR-IV and III are the front-end amplifiers and the PWM comparators. We have implemented 6 different amplifier designs in WINeR-IV to address the offset issue left by WINeR-III. The first one had AC coupling for both stages to eliminate the 1st stage offset. The second one also had AC coupling for both stages, but using capacitive averaging common mode feed back (CMFB) topology. The third to the sixth amplifiers used floating gate (FG) offset cancelation schemes. The testing results showed that the first amplifier worked pretty well, the offset at the final output was less than 50mV. The second amplifier with AC coupling and capacitive CMFB also worked. However, because of the capacitive CMFB, its output offset voltage was drifting over time. For those FG amplifiers, although they could be programmed to cancel the offsets, the trial process in programming the FG transistors and their sensitivity to temperature and electromagnetic field made them impractical for *in vivo* wireless neural recording applications. Therefore, we finally chose the first design for our final 32-channel WINeR-V system.

In WINeR-IV, the PWM comparators have also been improved by adding an internal positive feedback hysteresis. The feedback loop transistor pair was sized with a ratio of 1.1:1, therefore created a hysteresis window of \sim 50mV, which offered enough margin for noise

rejection.

Measurement results showed that WINeR-IV was able to wirelessly record and transmit neural signals up to 3.5m. The input referred rms noise of the entire WINeR-IV were 9.8 and $12.7 \mu\text{V}_{\text{rms}}$ at 0.5 and 3.5 m, respectively, which corresponded to the overall system resolutions of 8.2 and 7.9 bits, respectively.

2.3.5 Final 32-Channel WINeR-V

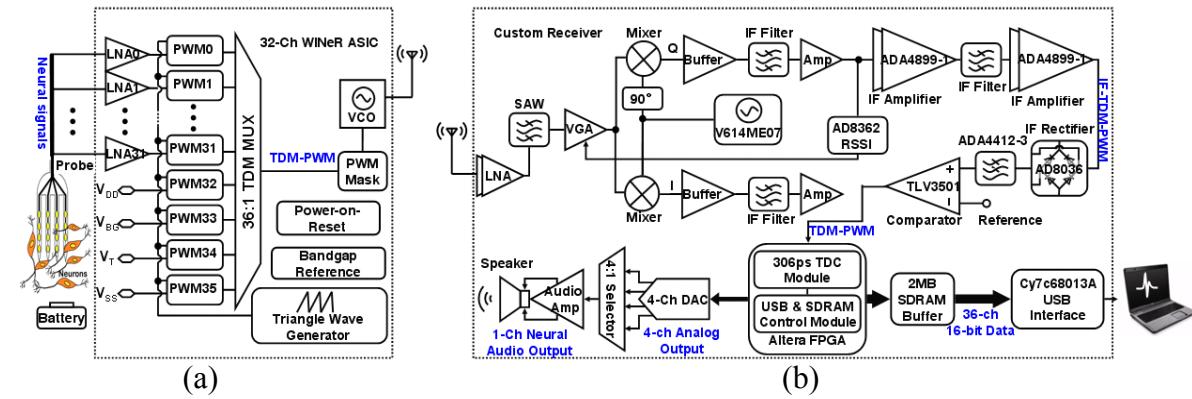


Figure 2.6 Block diagram of the 32-channel WINeR-V system. (a) WINeR-V transmitter.
(b) WINeR receiver.

After all the effects that mentioned previously, a final version of a 32-channel WINeR system, WINeR-V, was developed. The system block diagram of WINeR-V is shown in Figure 2.6, which consists of two parts: a 32-channel transmitter ASIC and a custom designed receiver using off-the-shelf components. In the next two chapters, I will be

discussing details on the WINeR-V transmitter and receiver.

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CHAPTER 3 System-on-a-Chip WINeR-V

Transmitter

3.1 Tissue Interface

The WINeR system is dedicated to recording extracellular neural signals, which need to be acquired by probes before arriving at the WINeR system inputs. There are two types of probes that are frequently used for neural recording applications: the metal microwires and the silicon micromachined electrodes.

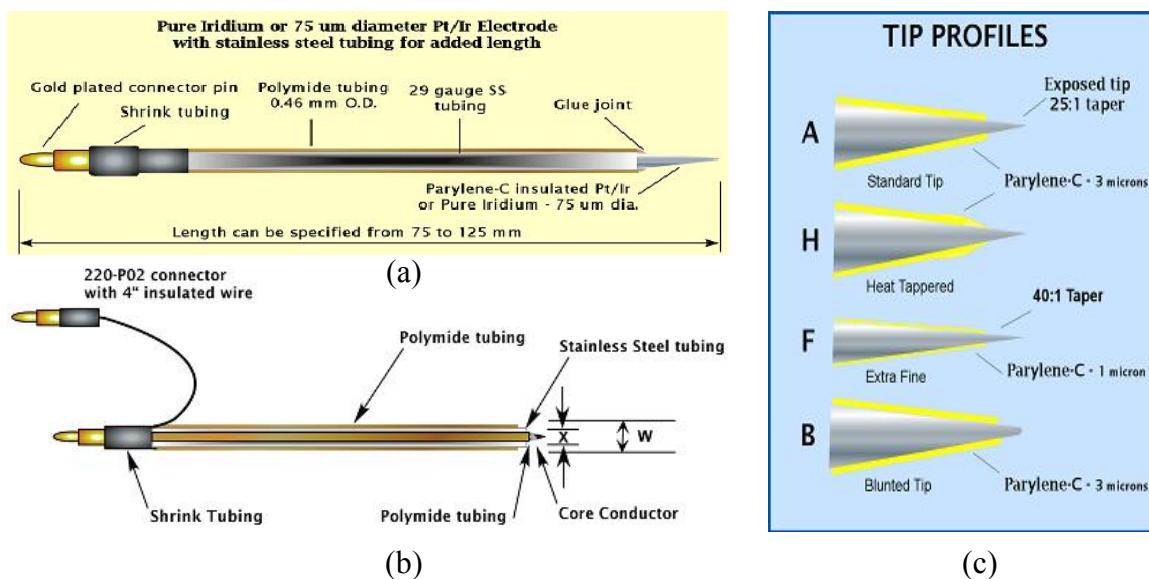


Figure 3.1 Example of commercially available metal microelectrodes [3.1]. (a) Unshielded single electrodes. (b) Concentric electrodes. (c) Tip profiles of the electrodes.

i. Metal microelectrodes (microwires)

Neural recording using metal microelectrodes has been very popular. The metal microelectrode can be handmade or purchased commercially [3.1],[3.2]. Figure 3. 1 shows two types of commercially available metal microelectrodes [3.1],[3.2]. These electrodes are usually formed by electrolytically sharpening a small-diameter metal wire to a fine tip (< 1 μ m). The body of the metal electrode is insulated with Polyimide or Parylene-C (polymer) except at the tip, which is exposed ~3 μ m from insulation. Metals such as tungsten, platinum, iridium, or stainless steel are commonly used for electrode core. Metal microelectrodes form a capacitive interface to the electrolyte (aqueous tissue) and track the variations of the potential field caused by the extracellular ionic currents. Therefore, different types of microelectrodes have fairly similar electrical characteristics and equivalent circuit models.

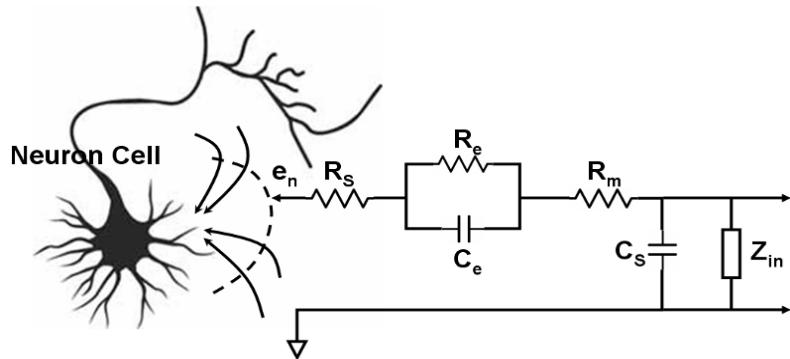


Figure 3.2 The equivalent circuit of a metal microelectrode recording [3.3].

Figure 3. 2 shows the equivalent circuit of the metal microelectrodes [3.3]. Where e_n

is the potential created in the volume conductor with respect to a point at infinity by the extracellular currents flowing around a neuron during an action potential. Z_{in} is the input impedance of the LNA. R_m is the resistance of the metallic portion of the microelectrode. C_e and R_e are the capacitance and leakage resistance of the electric double layer at the interface of the metal tip and the electrolyte solution, respectively. R_s is the spreading resistance of the saline bath. C_s is all the shunt capacitance to ground from the tip to the input of the amplifier. According to this model, for better recording, we need R_s , R_e , and C_s to be small and Z_{in} and C_e to be large. As far as Z_{in} is concerned, for our case, it is the input PMOS pair gate capacitance in parallel with the PMOS-NMOS pseudo resistor. So $Z_{in}=C_{in}||R_{in}$, since C_{in} is in pF range and R_{in} is around $10^{12}\Omega$, then Z_{in} usually exceeds $10\text{ M}\Omega$ in the neural signal frequency range of $0.1\text{ Hz} \sim 10\text{ kHz}$. Consequently, Z_{in} is seldomly a problem for the recording.

The metal resistance R_m can be expressed as: $R_m=\rho 4L/\pi d^2$. Where L is the length of the metal microelectrode, ρ is the resistivity of the metal (usually around $10^{-5}\Omega\cdot\text{cm}$), and d is the diameter of the electrode. Therefore, a 1mm length metal microelectrode with $1\mu\text{m} \sim 10\mu\text{m}$ diameter range results in R_m with a value from 1.3Ω to 130Ω . The small value of R_m can also be ignored. C_e is literally an electrolytic capacitor, using a transmission line distributed model, both C_e and R_e vary with frequency as $1/(\omega)^{1/2}$, and the phase angle of the impedance $Z_e(C_e||R_e)$ is equal to 45° (even empirically). Due to the very small area of the

electrode tip, C_e is small, and R_e is very large, for example a $1\mu\text{m}^2$ area tip results in a capacitive reactance of $785 \text{ M}\Omega$, hence the R_e is also $785 \text{ M}\Omega$, which results in $|Z_e|=557 \text{ M}\Omega$ [3.3]. The huge Z_e results in two problems: the first one is that the microelectrode will be extremely noisy due to the large thermal noise. Second one is since this double layer impedance is comparable or even larger than the LNA input impedance, it could greatly attenuate the signal before it reaches the LNA input. So we need to somehow reduce Z_e to a certain value that could make the metal electrodes to be practical. Platinizing is one of the most commonly used methods to decrease Z_e . By depositing a spongy colloidal layer of platinum on to the tip of the electrode, we could increase the effective recording area while keeping the exposed metallic area to be small. After platinizing, the tip impedance Z_e could be brought down by two or three orders to useful values [3.3]-[3.4]. Finally the saline spreading resistance, R_S , is usually around $10 \text{ k}\Omega$ to $100 \text{ k}\Omega$ range depending on the tip size of the electrodes, which is much smaller than Z_e , and can be ignored [3.3].

ii. Silicon micromachined electrodes

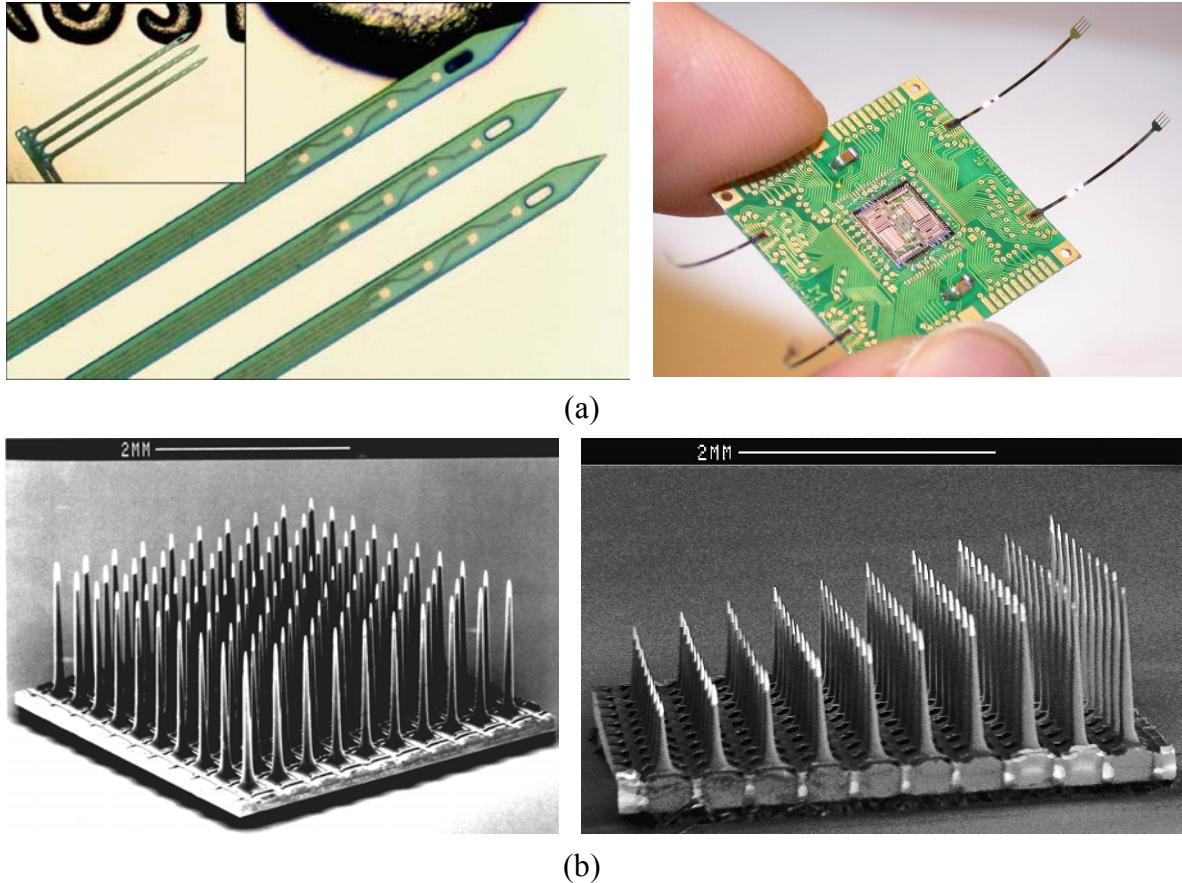


Figure 3.3 Michigan Electrode Array [3.5] and Utah Electrode Array [3.6]. (a) An example of assembly the MEA with silicon ribbon cable on the system PCB. (b) A UEA with 100 electrodes (left) and a slanted UEA with varying depths (right).

Silicon micromachined electrode array is another candidate of the recording probe. They advance the metal microelectrodes in terms of less tissue damage, multiple recording sites along the shank for multi-layered structure recording (Michigan Electrode Array), better homogeneity over handmade metal microelectrodes, and different geometries of the

recording sites depending on the application. Commonly used silicon micromachined electrodes include Michigan Electrode Array (MEA) and Utah Electrode Array (UEA). Figure 3. 3a shows the photograph of the MEA next to the “TRUST” on a U.S. penny. Figure 3. 3b shows a UEA with 100 electrodes and its slanted version with varying depths.

3.2 WINeR-V SoC Circuit Description

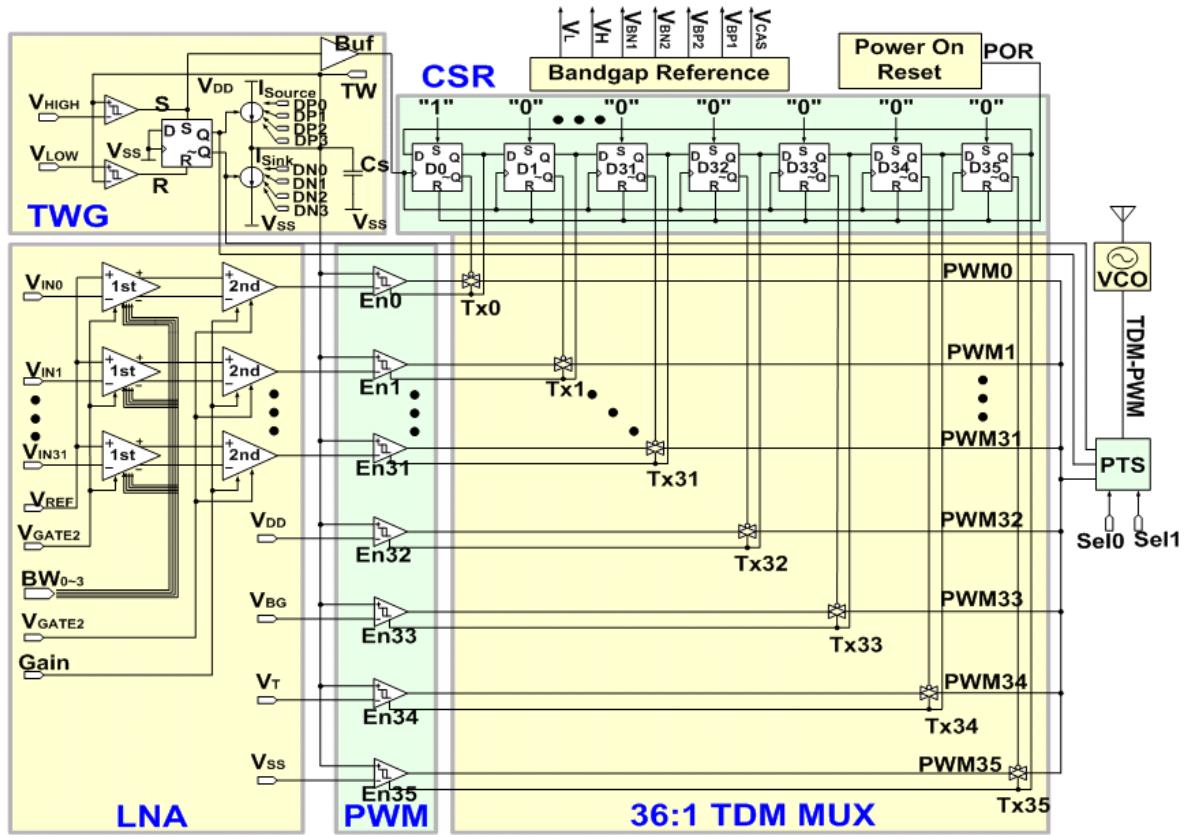


Figure 3. 4 Schematic of the 32-channel clockless WINeR-V ASIC.

Figure 3. 4 shows the schematic of the latest 32-channel WINeR-V SoC, which

consists of 8 parts: front-end amplifier array, pulse width modulator (PWM), precise triangular waveform generator (TWG), 36 to 1 time-division-multiplexer (TDM), pulse trimming and synchronization (PTS) block, voltage controlled oscillator (VCO), bandgap reference, and power-on-reset (POR). In the following section, I will describe the individual blocks.

3.2.1 Neural Amplifier

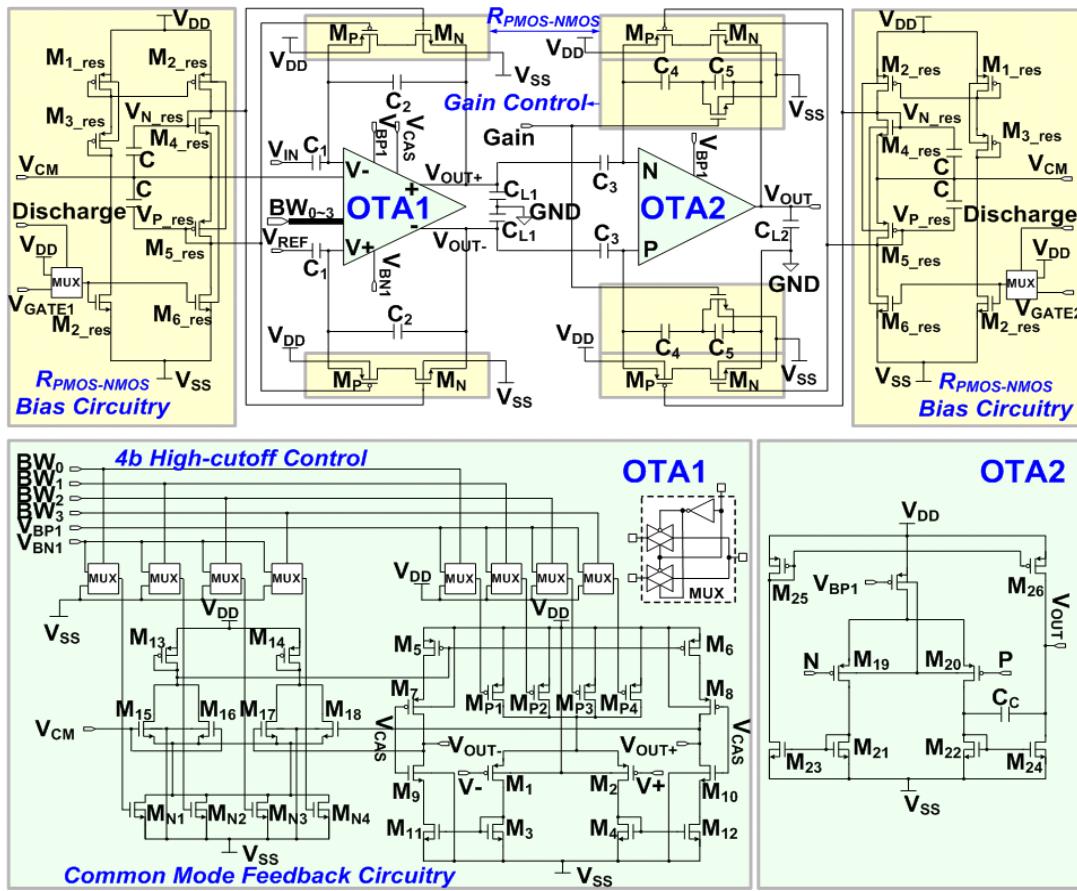


Figure 3. 5 Schematic of the front-end low noise amplifier.

The analog front-end of the WINeR-V ASIC consists of an array of 32 two-stage capacitively coupled low noise amplifiers (LNA), as shown in Figure 3. 5, which have built-in bandpass filtering capability to amplify the neural signals in the desired frequency range of 0.1 Hz to 10 kHz. The 1st stage is fully differential with fixed 40 dB gain and common-mode feedback. It also provides 4-bit control over the amplifier bias current, which offers a programmable high-cutoff frequency. This is because the dominant pole f_H of the OTA1 can be written as:

$$f_H = \frac{1}{2\pi R_{out1} C_{L1}} = \frac{1}{2\pi(g_{m7}r_{o7}r_{o5} \parallel g_{m9}r_{o9}r_{o11})C_{L1}} \quad (3.1)$$

where R_{out1} is the OTA1 ac output equivalent resistance, C_{L1} is the output load capacitor. g_{mi} and r_{oi} are transconductance and output resistance of their associated transistors in Figure 3. 5, respectively. In subthreshold operation, $g_{mi} \propto I_{bias}$ and $r_{oi} \propto 1/I_{bias}$, then $R_{out1} \propto I_{bias}$, therefore f_H changes proportional to I_{bias} . This is realized by using 4 PMOS ($M_{P1}-M_{P4}$) and 4 NMOS ($M_{N1}-M_{N4}$) tail current transistors with gate enable bits (BW₀₋₃), and choosing their W/L ratio to be: 1, 2, 10, and 10. By properly choosing a unit bias current, the high-cutoff frequency can be programmed from 400Hz ~ 10 kHz. With the 10 kHz high-cutoff setting, the 1st stage dissipates 16.4 μ A from a ± 1.5 V supply. To reject the DC offset from the 1st stage, the 2nd stage is an AC-coupled differential to single-ended amplifier with 1-bit adjustable gain (27/37 dB). It draws 8.1 μ A from supplies. The closed-loop gain of the 2nd stage is

programmable and given by (3.2). This yields an in-band gain of $-C_3/C_{feedback}$. $C_{feedback}$ is the feedback capacitor connecting between the input and the output of OTA2, which are implemented by two capacitors, C_4 , C_5 in series. A switch is added in parallel with C_5 . When V_{gate} is low, $C_{feedback}=C_4C_5/(C_4+C_5)$. When V_{gate} is high, C_5 is shorted, and $C_{feedback}=C_4$.

$$A = -\frac{R_{PMOS-NMOS} \cdot C_3}{\frac{1}{j\omega} + R_{PMOS-NMOS} \cdot C_{feedback}} \quad (3.2)$$

Achieving low-cutoff frequency in the sub-Hertz range with small on chip area is a challenge for neural amplifier design. Many researchers have used subthreshold biased MOS resistor or diode-connected MOS resistor to achieve ultra low-cutoff frequency because of its high resistance ($>10^{11}\Omega$) [3.7]-[3.10]. However, these designs suffer high level of distortion for large output, since the resistance of the MOS resistor highly depends on the input and output voltages. To solve this problem, in both stages of the neural amplifier we have used individual voltage control PMOS-NMOS pseudo resistors— $R_{PMOS-NMOS}$ in conjugation with their feedback capacitors C_2 or C_4/C_5 to create a tunable low-cutoff frequency. The idea of this topology is to bias the $R_{PMOS-NMOS}$ transistors with a small bias circuitry, such that it operates as a bidirectional current source, therefore the impedance seen from either ends of the $R_{PMOS-NMOS}$ will remain constant and will be almost independent of the input and output. Hence it can achieve minimum distortion. This can be understood by a

detailed analysis of the $R_{PMOS-NMOS}$ and its bias circuitry shown in Figure 3. 5. In this configuration, an external control voltage $V_{GATE1,2}$ biases M_{2_res} in deep subthreshold region, where its drain current can be found from [3.11]

$$I_{sub} = I_0 \exp[(V_{GS} - V_{TH})/nV_T] [1 - \exp(-V_{DS}/V_T)] \quad (3.3)$$

where $V_T = kT/q$, $I_0 = \mu_0 C_{ox} (W/L)$, V_{TH} is the MOS threshold voltage, and n is the subthreshold slope factor. The same current passes through M_{4_res} and M_{5_res} , which are diode-connected and sized with large W/L . Noting that V_- and V_+ are maintained around V_{CM} by negative feedback and CMFB, it can be shown that M_{4_res} and M_{5_res} keep the current passing through $R_{PMOS-NMOS}$ (M_{n_res} and M_{p_res}) around KI_{DS2_res} , $K=0.1 = (W/L)_{n_res}/(W/L)_{4_res} = (W/L)_{p_res}/(W/L)_{5_res}$, regardless of the output voltage variations. When $V_{out+} < V_-$, KI_{DS2_res} passes from V_- to V_{out+} because M_{p_res} and M_{5_res} have the same V_{SG} . When $V_{out+} > V_-$, current passes from V_{out+} to V_- , the middle node of the $R_{PMOS-NMOS}$ maintains a voltage slightly higher than V_- , and $V_{GSn_res} \approx V_{n_res} - V_- = V_{GS4_res}$. Therefore, the current passing through $R_{PMOS-NMOS}$ will be around KI_{DS2_res} . By varying $V_{GATE1,2}$, I_{DS2_res} and consequently $R_{PMOS-NMOS}$ change and a tunable low-cutoff frequency can be achieved. Figure 3. 6 compares the simulated resistance vs. voltage across $R_{PMOS-NMOS}$ for our design with a few other designs in [3.7]-[3.10]. The results show that our PMOS-NMOS pseudo resistor has the smallest variations ($0.7 \times 10^{12} \Omega \sim 2 \times 10^{12} \Omega$) within ± 1.5 V output range.

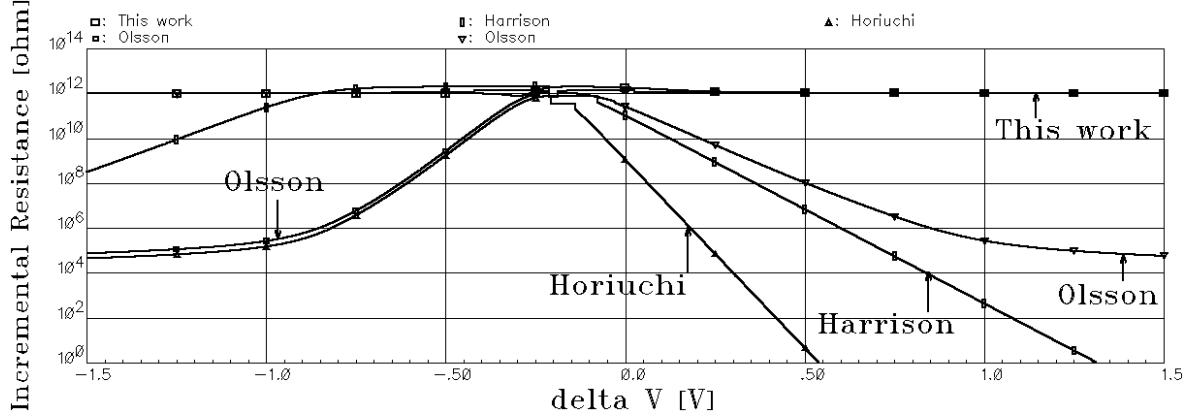


Figure 3.6 Comparison between simulated resistances of different MOS pseudo resistor designs [3.7]-[3.10].

One of the problems with large subthreshold biased PMOS-NMOS pseudo resistors is large settling times in the order of a few seconds. If the amplifier output is saturated, it will take a long time for it to return back to normal baseline. To overcome this problem, discharge switches are added to the external bias nodes to switch them between $V_{GATE1,2}$ and V_{DD} . When saturation is detected by the following signal processing algorithms running on the computer, a discharging pulse is generated that closes the switch and increases current passing through $R_{PMOS-NMOS}$, which shorts $V_{-/+}$ with $V_{out+/-}$ and results in a fast recovery [3.12].

We simulated the LNA recovery performance when using this discharge strategy. As shown in Figure 3.7, the LNA input is given a 10 kHz 400 μ V_{P-P} sine wave overlapping with a high amplitude pulse, which represents the actual neural signal superpositioned with large stimulation artifacts. The high amplitude pulse begins at 1 ms and ends at 3 ms with amplitude of 1.5V. Then the discharge pulse is applied at 2ms, and ended at 3.1ms, 100 μ s

later than the input pulse. According to the simulation, when the input pulse is applied, the LNA is immediately saturated. However, after applying the discharge pulse, the LNA output is forced to 0V even the big input pulse is still applied. After the input pulse goes away, the output of the LNA will stay at 0V until the discharge signal ends, and at that point the LNA output quickly recovers back to normal operational point with in $\sim 100\mu\text{s}$.

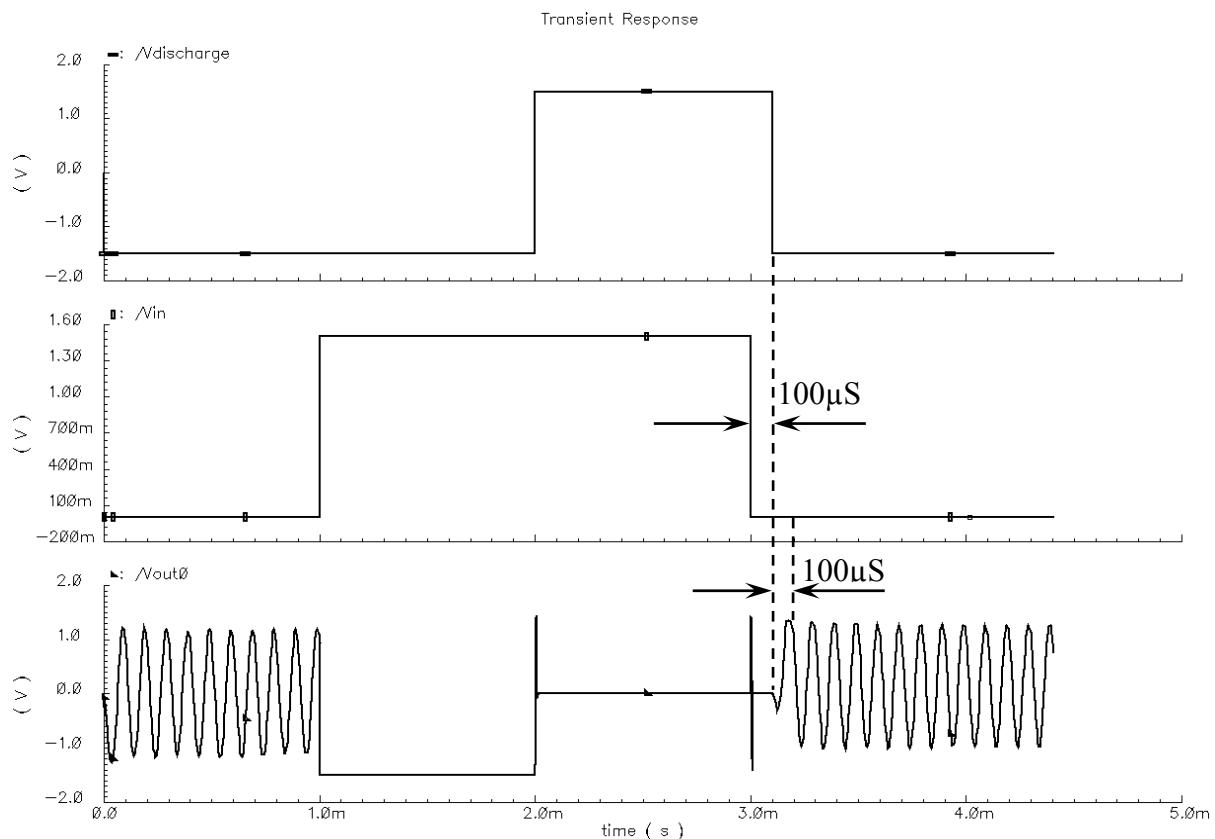


Figure 3. 7 Simulation of the low noise amplifier recovery performance.

3.2.2 Pulse Width Modulator and Time Division Multiplexer

The amplifier outputs are combined with four monitoring signals (V_{DD} , V_{SS} , bandgap reference V_{BG} , and temperature voltage V_T) and fed into the PWM block that consists of 36 rail-to-rail high speed comparators (Figure 3. 4). They are enabled one at a time by circulating a “1” in a circular shift register (CSR), converting the conditioned analog signals into pulses by comparing them with a programmable triangular waveform generated by a precision triangular waveform generator (TWG), see Figure 3. 8. During each comparison, the substrate is entirely quiet and there is no digital transition anywhere on the chip, which reduces the substrate noise and dynamic power dissipation. The monitoring signals provide a unique pattern that can be used to indicate the beginning of each TDM packet on the receiver. In addition, they can also be used for system calibration.

The TDM block consists of a 36-bit CSR running a 36:1 multiplexer (MUX). The CSR receives the buffered timebase signal from the TWG block as its clock. At the global reset, the CSR is loaded with 36-bit binary ‘10...00’. When the system is running, the single “1” circulates in the CSR and connects one out of 36 comparator PWM pulses to the MUX output. The resulting signal is a 36-channel TDM-PWM signal, which is buffered and fed into the VCO after being trimmed and synchronized. This specific design significantly facilitates the extension of the WINeR system from 32 to 64 even 128 channels without

requiring a large number of additional gates.

3.2.3 Precise Triangular Waveform Generator

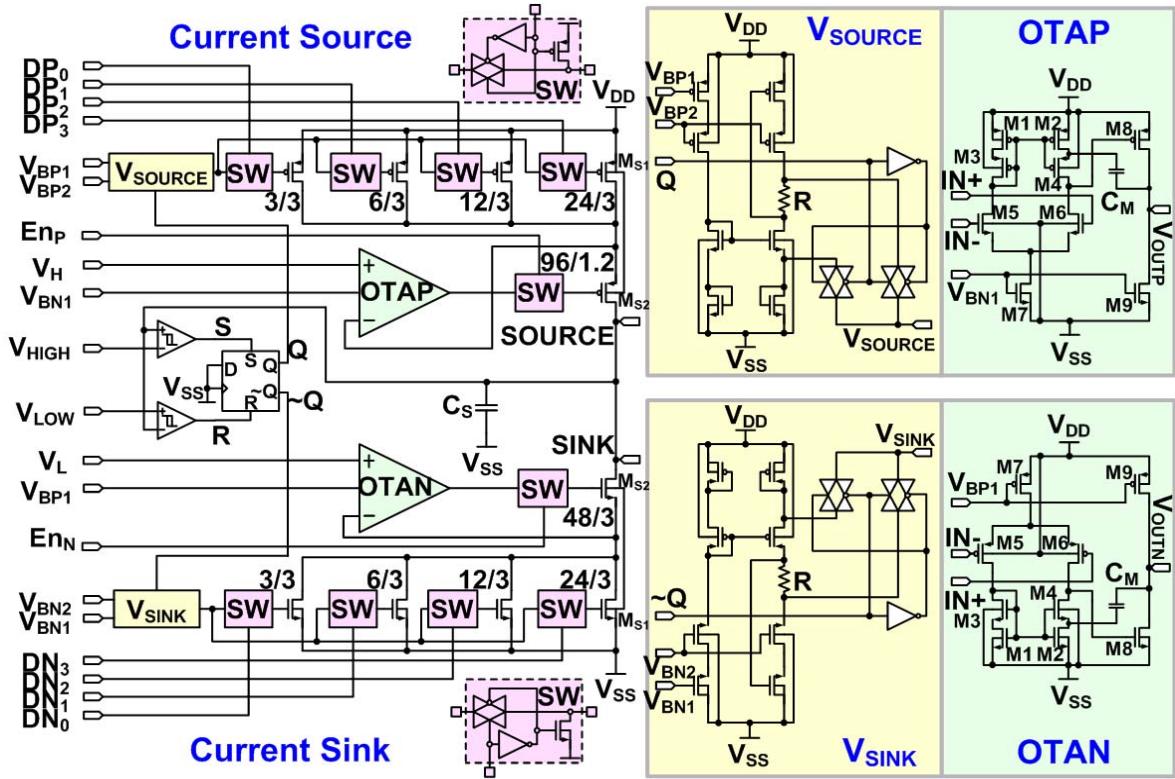


Figure 3.8 Precision triangular waveform generator.

Precision triangular waveform generator (TWG) is a key block in realizing the clockless PWM-TDM (Figure 3.8). Its performance affects noise, accuracy, and resolution of the system. It consists of a binary weighted (DP_{0-3} and DN_{0-3}), high voltage compliance, large output impedance complementary current source/sink (CCSS) pair, which linearly charge/discharge $C_S = 6 \text{ pF}$ and generate the triangular waveform (TW) [3.13]. A detailed

description of the high voltage compliance, large output impedance CCSS circuit that utilizes MOSFETs in deep triode region can be found in [3.14]. By controlling the binary bits, $DP_{0\sim 3}$ and $DN_{0\sim 3}$, I_{Source} and I_{Sink} can be changed in 16 steps. Controlled charge/discharge not only avoids intense substrate charge injection but also provides flexibility over the sampling rate in a wide range.

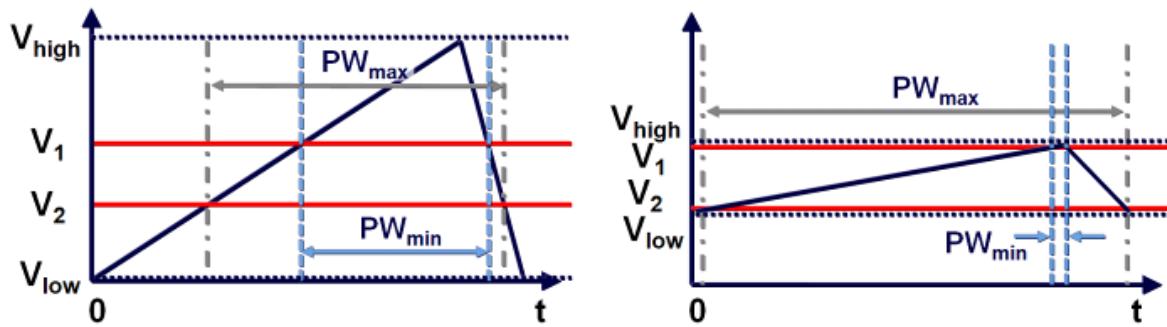


Figure 3.9 System resolution enhancement by limiting the triangular wave upper and lower limits.

A window detector limits the TWG output amplitude and generates the switching signals for the CCSS, CSR, and TDM blocks. The lower and upper limits of the TW, V_{low} and V_{high} , can be either given internally as $V_{SS}+0.1V$ and $V_{DD}-0.1V$ or adjusted externally based on the dynamic range of the incoming neural signals to maximize the system resolution. For instance, as shown in Figure 3.9, if the range of signals at the output of the analog front-end is only from V_1 to V_2 , and TW is rail to rail, the resulting PWM signal will be using only a fraction of its allocated sampling period, T_B . On the other hand if we set V_{high} and V_{low}

slightly above and below V_1 and V_2 , respectively, and also change I_{source} and I_{sink} in the CCSS, the PWM can utilize the entire sampling period (the right figure of Figure 3. 9). It can be shown that variable TW range can improve the system resolution by $\log_2[(V_{DD}-V_{SS})/(V_1-V_2)]$ bits.

3.2.4 Pulse Trimming and Synchronization

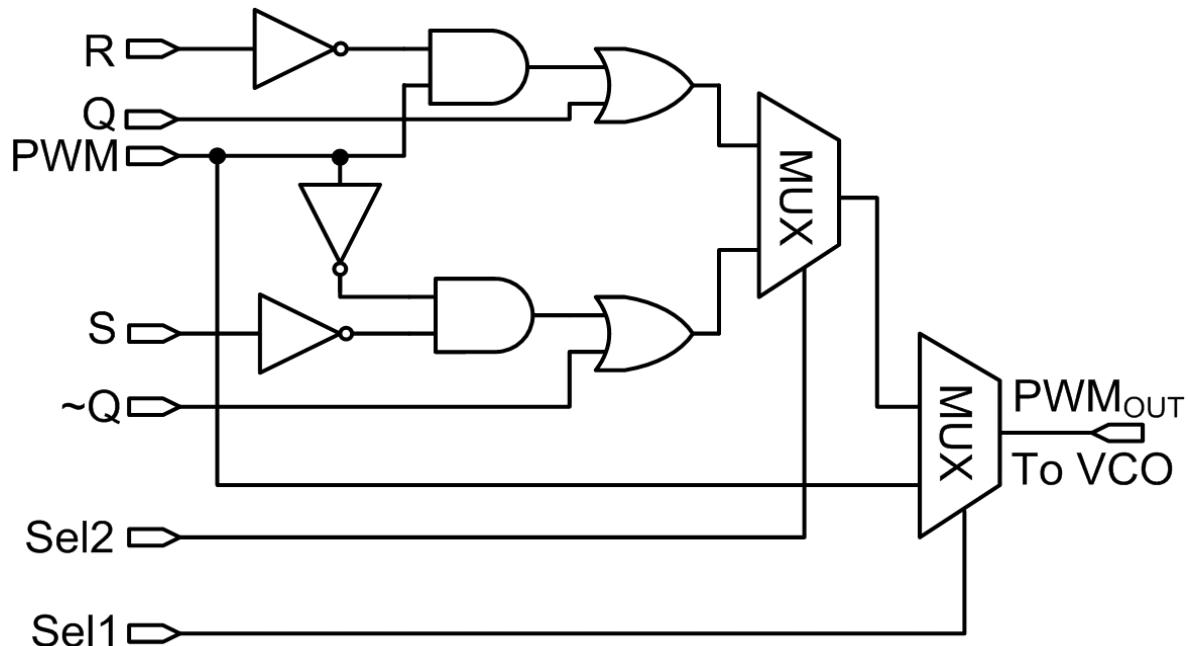


Figure 3. 10 Schematic of the pulse trimming and synchronization.

Following the TDM, there is a pulse trimming and synchronization (PTS) block. The schematic of the PTS is shown in Figure 3. 10. It is responsible for enforcing minimum and maximum widths in the PWM, therefore it can reduce the wireless link bandwidth requirements and increase system accuracy by avoiding transferring extremely narrow pulse

width signals. In addition, it synchronizes the PWM signal at the falling edge of Q or $\sim Q$.

This would facilitate the data recovery on the receiver side.

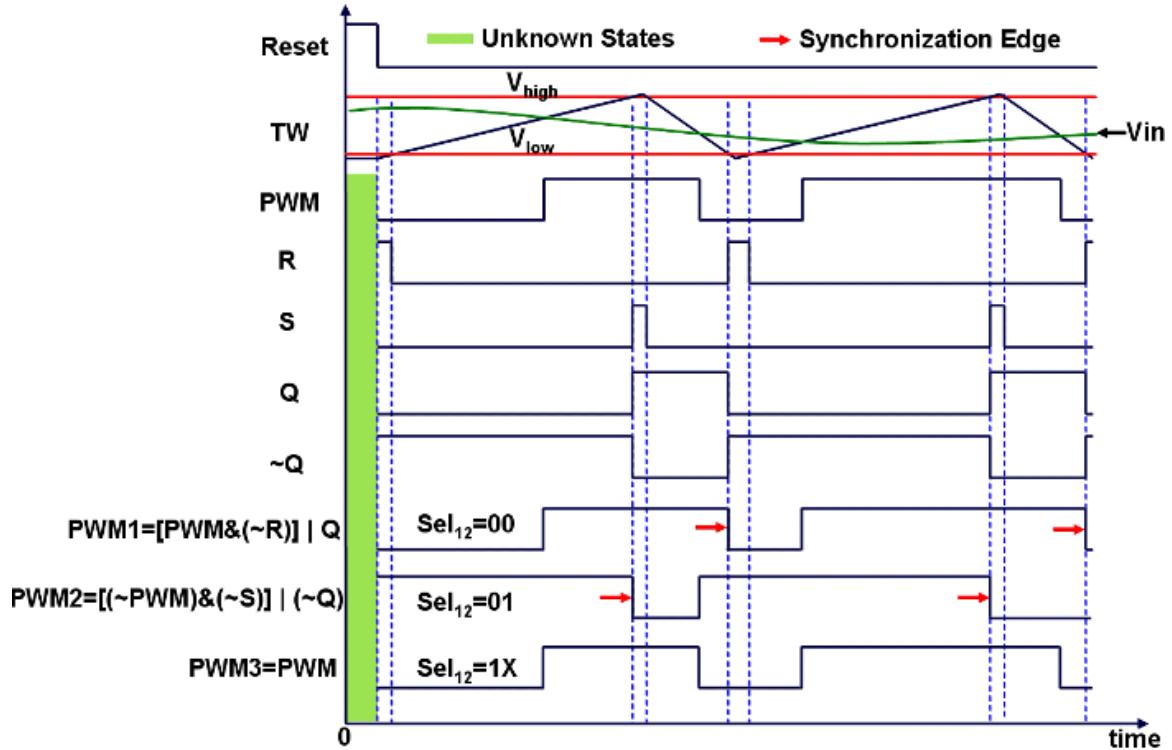


Figure 3. 11 PTS operation.

Figure 3. 11 shows the PTS operation and its associated signals. PWM is the pulse width signal before trimming and synchronization, R, S, Q, and $\sim Q$ are digital inputs from the TWG block (see Figure 3. 8). $Sel_{1,2}$ are selection signals. When $Sel_{1,2}=00$, the output of the PTS will be $PWM_{OUT}=PWM1=[PWM&(\sim R)]|Q$, it will be trimmed and synchronized at the falling edge of Q, and has a maximum and minimum pulse widths equal to $\sim R$ and Q, respectively. When $Sel_{1,2}=01$, the output of the PTS will be

$PWM_{OUT}=PWM2=[(\sim PWM) \& (\sim S)] | (\sim Q)$, it will be trimmed and synchronized at the falling edge of $\sim Q$, and has a maximum and minimum pulse widths equal to $\sim S$ and $\sim Q$, respectively. Finally when $Sel_{1,2}=1X$, $PWM_{OUT}=PWM2=PWM$, the PTS is being bypassed. A detailed description of the PTS can be found in [3.13].

3.2.5 Voltage Controlled Oscillator

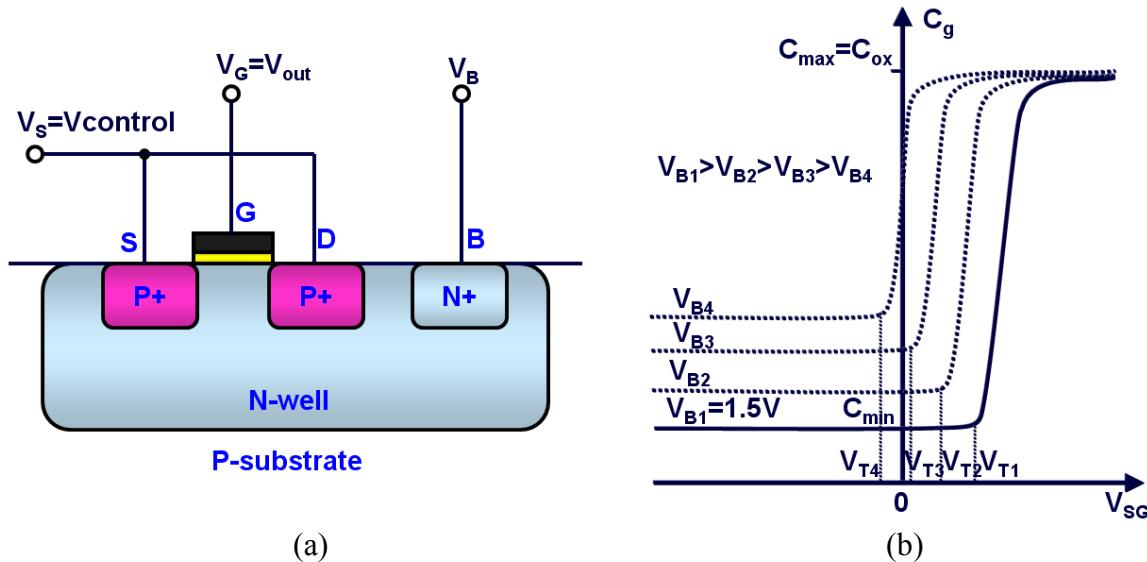


Figure 3.12 (a) PMOS varactor scheme and (b) its C-V curve with different V_B .

Trimmed PWM-TDM signal drives a hybrid VCO with on-chip PMOS varactor and an off-chip SMD inductor. The PMOS varactor (Figure 3.12), which is the heart of an LC-VCO, is a 3-terminal device with the PMOS drain and source terminals shorted and given a voltage, V_s , that can serve as the VCO input signal. The PMOS varactor capacitance, C_g , will be a function of both gate to bulk, V_{GB} , and source/drain to bulk, V_{SB} , voltages. The

gate is usually connected to the VCO output, as shown in Figure 3. 12a, and the n-well bulk voltage, V_B , can be used to tune the VCO. If we connect the n-well to the highest voltage, V_{DD} , the PMOS varactor will operate in the inversion mode, and its $C-V_{SG}$ curve will look like the solid curve in Figure 3. 12b. When $V_{SG} < |V_T|$, where V_T is the extrapolated threshold voltage, this curve is flat and $C_g = C_{min}$, [3.15], because in that range the PMOS varactor works in the depletion region. When $V_{SG} > |V_T|$, the PMOS enters the inversion region and the capacitance starts to increase abruptly. After the PMOS enters in the strong inversion, the capacitance stays at $C_g = C_{max}$, which is almost equal to the gate oxide capacitance C_{ox} . This turning point around $|V_T|$ corresponds to the VCO high gain region. Thus by changing V_T , we can shift the high gain region horizontally [3.15]:

$$V_T = V_{FB} - \phi_0 - \gamma \sqrt{\phi_0 - V_{SB}} \quad (3.4)$$

where V_{FB} is the flat-band voltage and γ is the body effect factor. Φ_0 , in this equation is the value of the “pinned” surface potential of the PMOS in strong inversion with $V_{SB}=0$, which is usually several Φ_t greater than $2|\Phi_F|$. Here, $\Phi_t=kT/q$ is the “thermal voltage” and Φ_F is the Fermi potential of the n-well semiconductor. For real PMOS $2\Phi_F \gg \Phi_t$, so for a good approximation $\Phi_0 \approx 2|\Phi_F|$. To find the turning point of the $C-V_{SG}$ curve, we substitute V_T and V_{SB} by V_{SG} and $V_{SG}+V_{GB}$, respectively. Then (3.4) becomes:

$$V_{SG} = -V_{FB} + 2|\phi_F| + \gamma \sqrt{2|\phi_F| - V_{SG} - V_{GB}} \quad (3.5)$$

Solving for V_{SG} yields:

$$V_{SG} = -V_{FB} + 2|\phi_F| - \frac{\gamma^2}{2} \pm \gamma \sqrt{\gamma^2 + V_{FB} - V_{GB}} \quad (3.6)$$

Noticing that according to (3.5), $V_{SG} > -V_{FB} + 2|\phi_F|$, so for (3.6), the square term should always have a positive sign, which end up with:

$$V_{SG} = -V_{FB} + 2|\phi_F| - \frac{\gamma^2}{2} + \gamma \sqrt{\gamma^2 + V_{FB} - V_{GB}} \quad (3.7)$$

It shows the value of the turning point increases with the increase of V_{GB} . In practice, both V_G and V_S will have large amplitude variations and large signal analysis should be used to extract the actual $C-V_{SG}$ characteristics of the PMOS varactor [3.16]. However, here we only use DC and small signal analyses to demonstrate the influence of V_B . The DC component of V_G is equal to the DC operating point of the VCO output. This is usually designed half way between supply voltages to achieve the widest output swing. With V_G being constant, according to (3.7), the turning point will shift to a lower V_{SG} value with the decrease of V_B . The dashed lines in Figure 3. 12b show this effect. It can be seen that another effect of decreasing V_B is increasing C_{min} . Because when PMOS is in the depletion region, the total

capacitor C_g is the gate capacitor, C_{ox} , in series with the bulk capacitor, C_b , which is the equivalent capacitor formed by the depletion region under the channel, therefore C_{min} can be written as:

$$C_{min} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_b}} = \frac{1}{\frac{1}{C_{ox}} + \sqrt{\frac{2(\phi_0 + V_{SB})}{qN_D\epsilon_S}}} \quad (3.8)$$

where N_D is the donor concentration under the channel and ϵ_S is the permittivity of the silicon. When V_B decreases, the depletion width under the channel decreases, hence the bulk capacitor increases resulting in increasing C_{min} . Overall, by operating the on-chip PMOS varactor array as a three terminal device, the VCO achieves center frequency tunability, shifting of the high gain region, and changing the VCO gain.

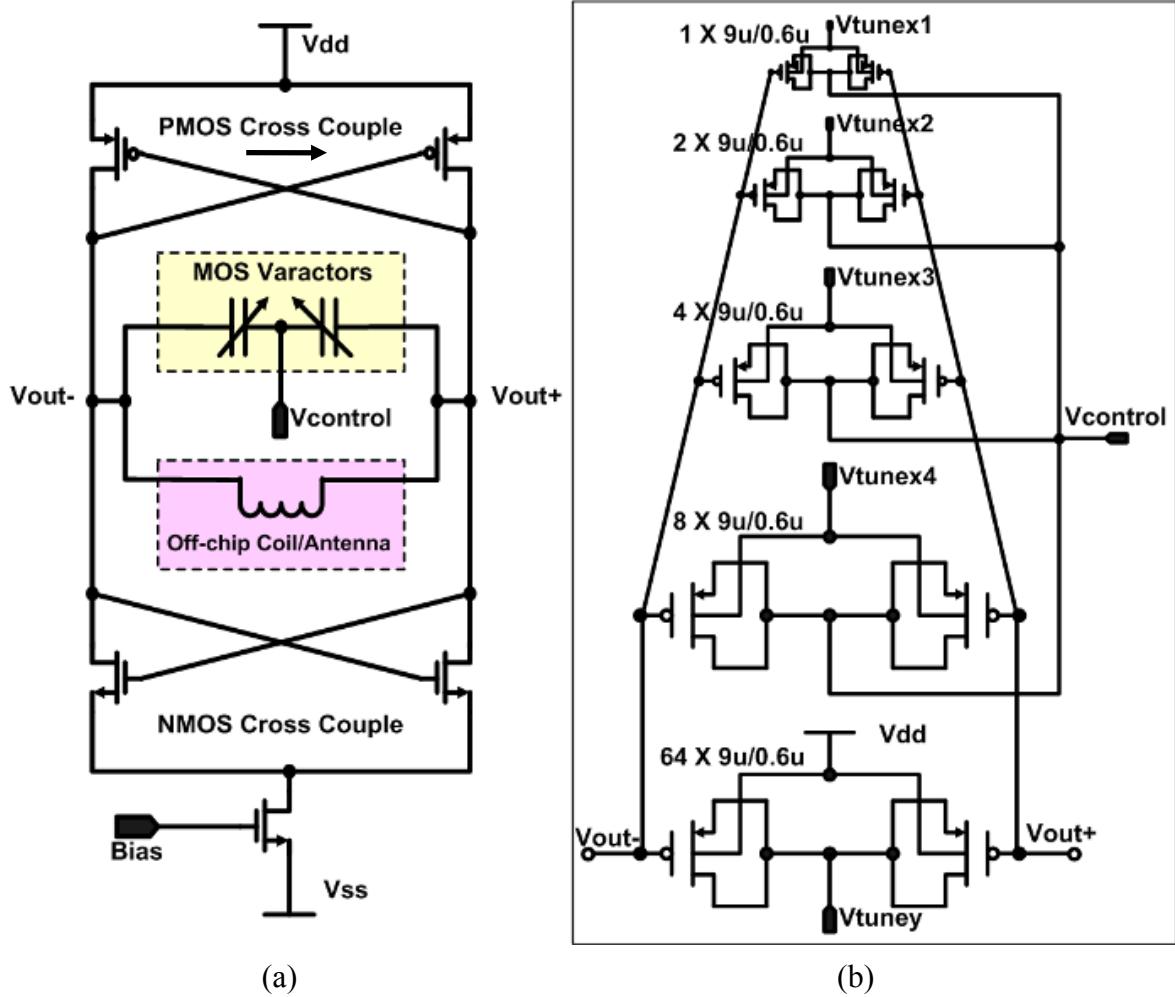


Figure 3.13 (a) Schematic diagram of the hybrid LC-tank VCO. (b) Schematic of the on-chip PMOS varactor.

Considering the above PMOS varactor behavior, we have designed a flexible LC-VCO, shown in Figure 3.13a. The PMOS varactor is shown in Figure 3.13b, the bottom PMOS pair has the largest size ($64 \times 9\mu\text{m}/0.6\mu\text{m}$) and its bulk voltage is always tied to V_{DD} . V_S of this varactor pair is connected to V_{tune-Y} , by changing which we can adjust the VCO center frequency in a wide range. The other four PMOS pairs are smaller and binary

weighted using a unit cell of $9\mu\text{m}/0.6\mu\text{m}$. For this series of varactors, drain/source voltages, V_S , are connected to the VCO input, $V_{control}$, and their bulk voltages are controlled by $V_{tune-X1\sim 4}$. By changing these bulk voltages, we could shift the VCO high gain region and adjust the gain of the VCO. The VCO can also operate in two modes: 1) wideband FSK when the varactor input is driven, 2) wideband OOK when the VCO enable input is driven. In the OOK mode, the VCO power is cut in half at the cost of lower system sampling rate. More detailed description of the VCO can be found in [3.17].

3.2.6 Transmitter Antenna

WINeR system resolution is directly related to the SNR because of the use of PWM-TDM architecture. Therefore to guarantee proper system resolution, enough SNR over the wireless link should be achieved. Due to the scarcity of power on the WINeR transmitter, the on-chip VCO, which is often the most power consuming block, should operate by less than a few mW. This requires a highly efficient antenna for the WINeR transmitter to deliver maximum power. However, there is barely any room available for a decent antenna in the implant. Therefore, a miniature sized antenna with good performance is the best choice. After searching commercially available antennas that meet our requirements in the 900MHz range, we have found that two types of antennas are suitable for the WINeR transmitter, as shown in Figure 3. 14. One is a 915MHz chip antenna from Johanson Technology, Inc. [3.18], the

other is a 916MHz embeddable $\frac{1}{4}$ wave monopole antenna from Linx Technologies, Inc. [3.19]. The chip antenna has a size of $7 \times 2 \times 0.8$ mm 3 , an average gain of -4.0dB, and 8.5dB minimum return loss. The embedded antenna is a little bit larger than the chip antenna with a size of $\varnothing 7\text{mm} \times 14.5\text{mm}$, but since it is a $\frac{1}{4}$ wave monopole, it has better performance than the chip antenna.

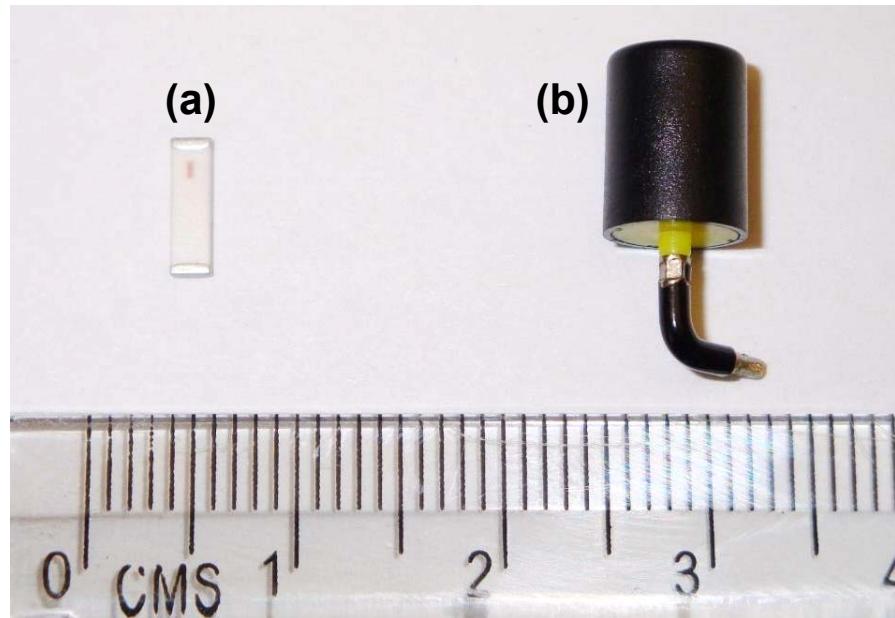


Figure 3. 14 Two types of miniature 900MHz antenna used for the WINeR system. (a) Johanson Technology 915MHz chip antenna [3.18]. (b) Linx Technologies JJB series 916MHz embeddable $\frac{1}{4}$ wave monopole antenna [3.19].

3.3 Measurement Results

3.3.1 32-Channel WINeR-V SoC Implementation

The 32-channel WINeR-V ASIC was fabricated in the AMI 0.5- μm 3-metal 2-poly

standard CMOS process and measures $3.3 \times 3\text{mm}^2$ (Figure 3. 15). When all channels are active, it consumes 5.6mW from $\pm 1.5\text{V}$ supplies in the FSK mode.

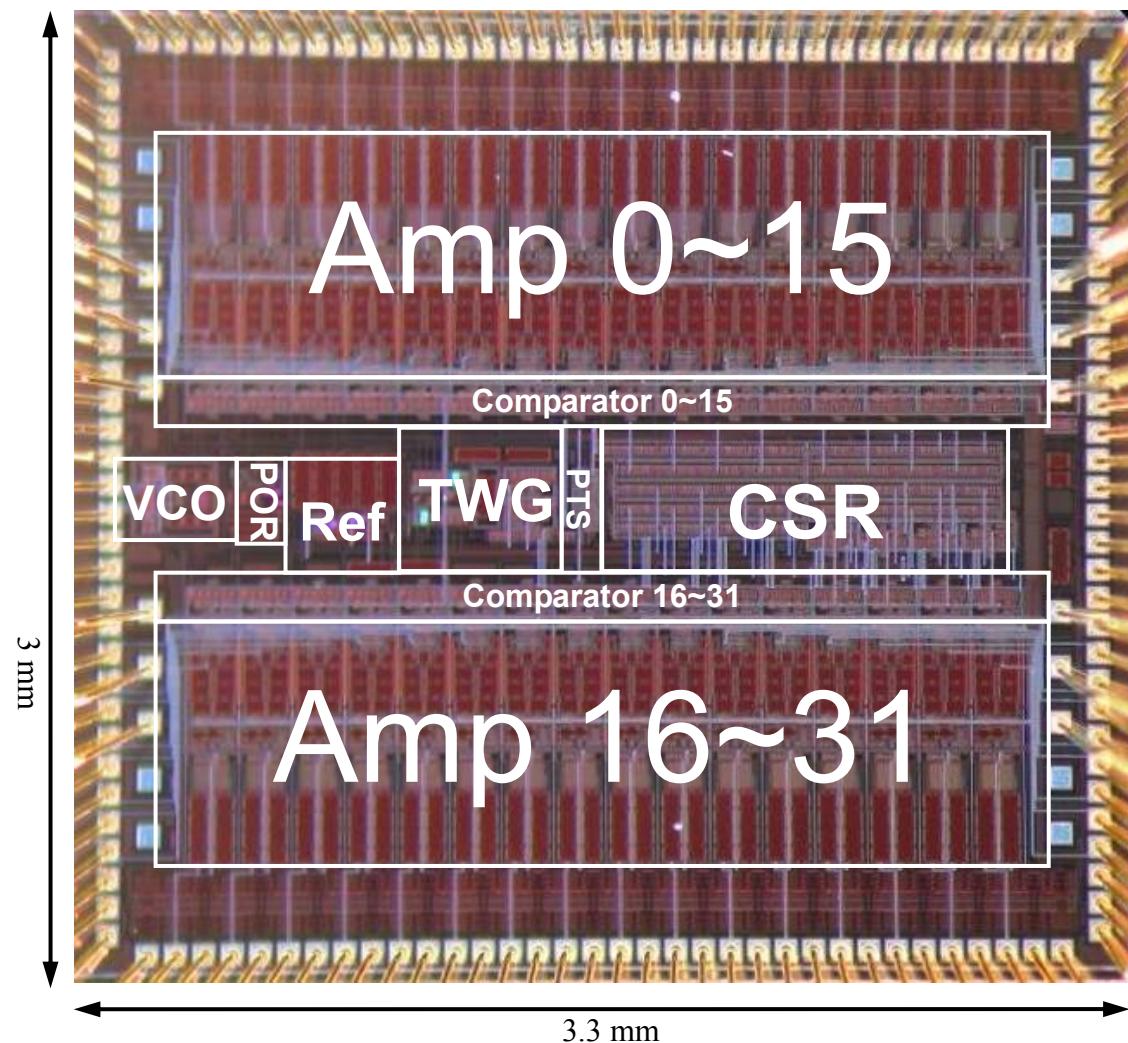


Figure 3. 15 Microphotograph of the 32-channel WINeR-V ASIC.

3.3.2 LNA Measurements

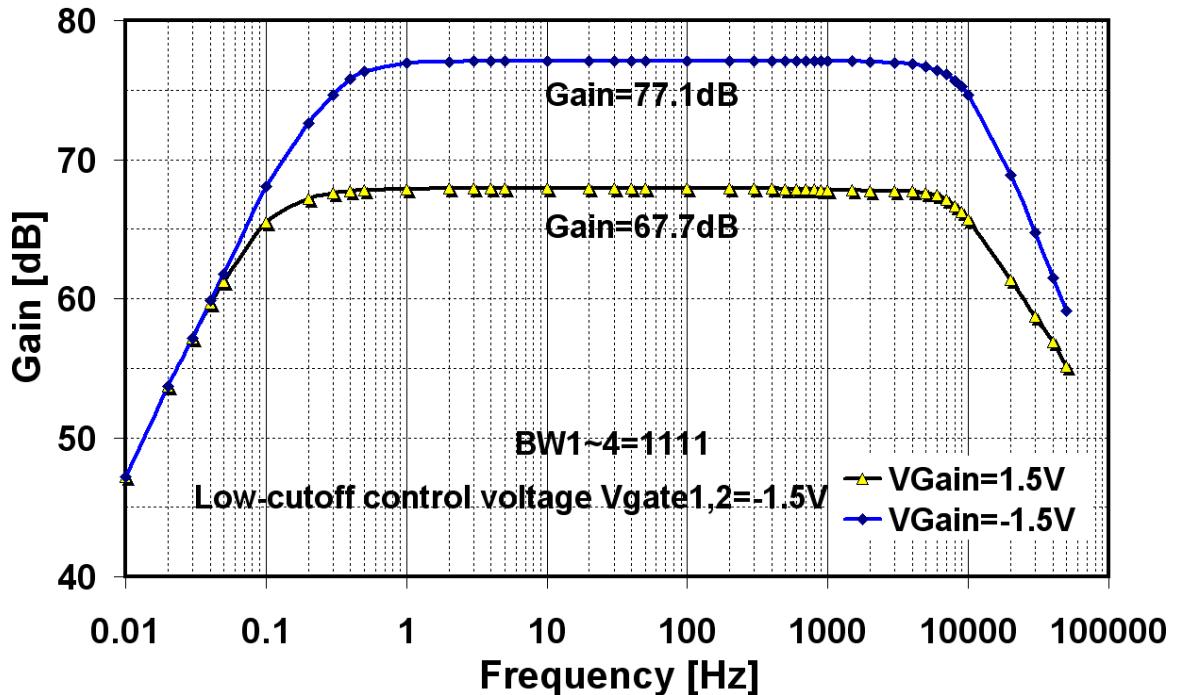


Figure 3.16 Measured LNA variable in-band gain.

The front-end amplifier 1st stage has a measured gain of 40dB and the 2nd stage gain is 27.7/37.1dB, as shown in Figure 3.16. The low-cutoff is continuously tunable from 0.1Hz \sim 1 kHz (see Figure 3.17). The high-cutoff is 4-bit programmable from 0.7~10 kHz (see Figure 3.18). This topology provides 1% THD at 17.4 mV input for the 1st stage and has only $3.9\mu V_{rms}$ measured input referred noise in 10Hz \sim 10 kHz range (see Figure 3.19).

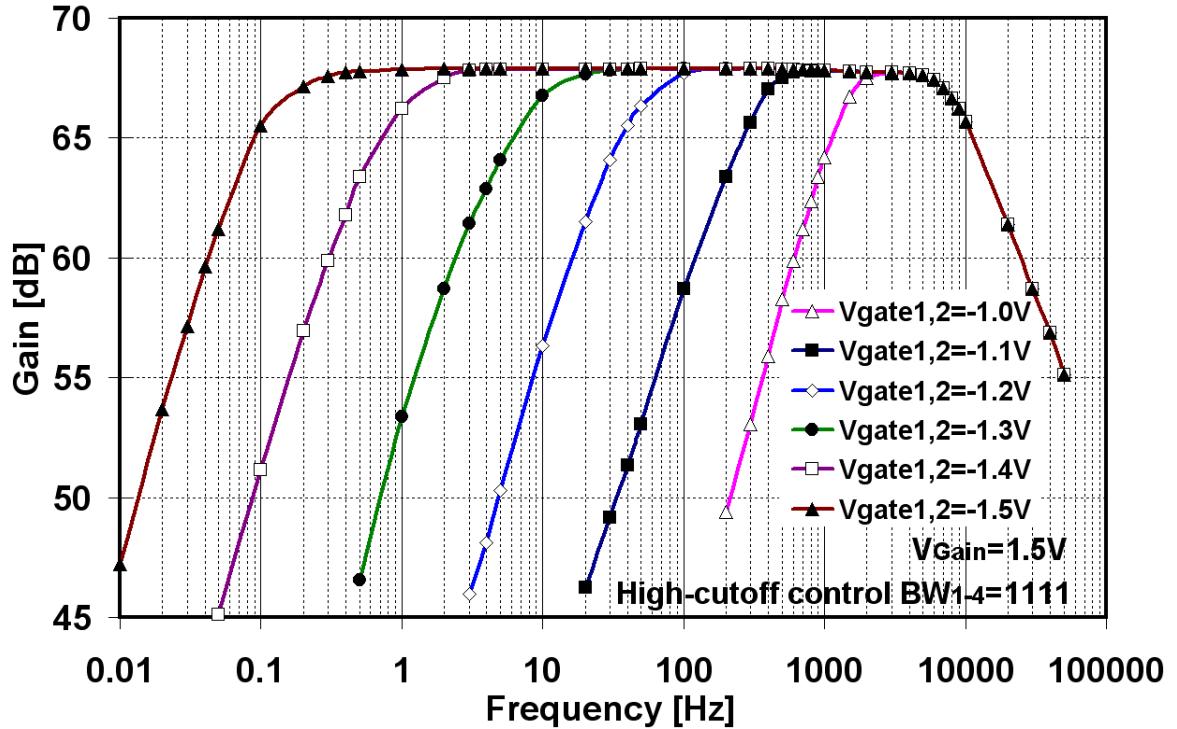


Figure 3.17 Measured LNA tunable low-cutoff frequency response.

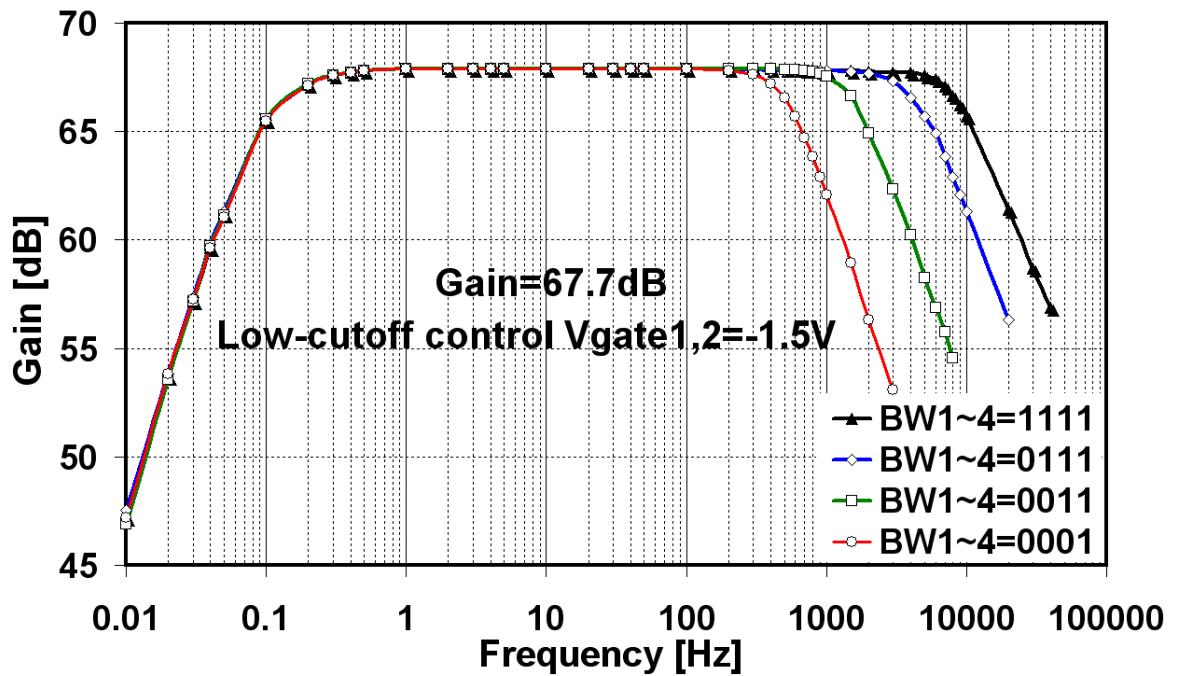


Figure 3.18 Measured LNA programmable high-cutoff frequency response.

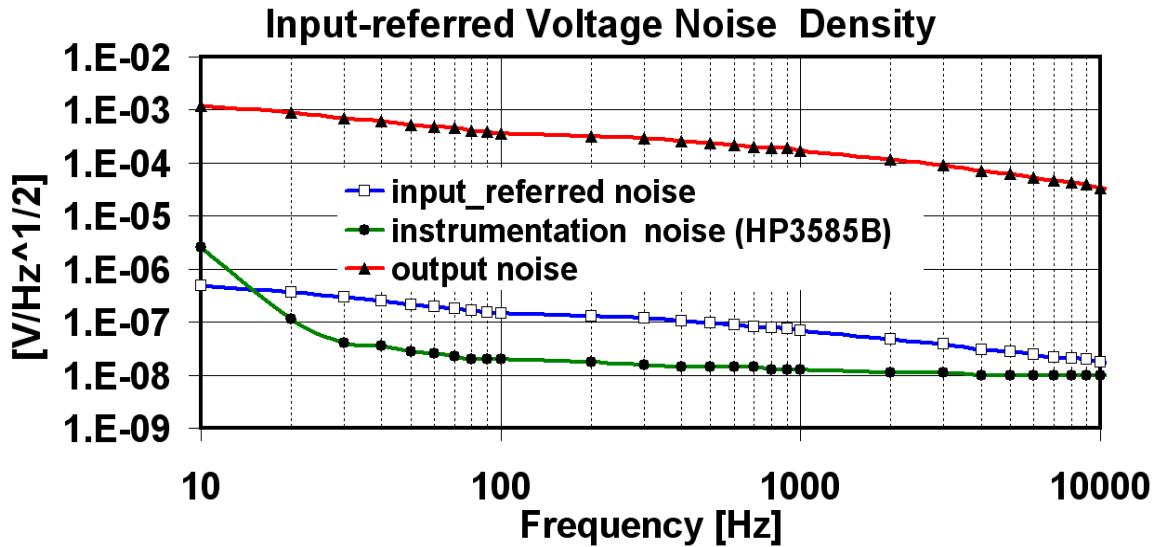


Figure 3. 19 Measured input referred voltage noise density for the LNA with grounded input and 67.7dB gain 0.1~10 kHz bandwidth setting. Integration under this curve from 10 Hz to 10 kHz yields an rms noise voltage of $3.9\mu\text{V}_{\text{rms}}$.

A crosstalk measurement between channels has been conducted all the way from the LNAs to the PC. During this measurement, a $1\text{mV}_{\text{P-P}}$ 1 kHz sine wave has been applied to Channel 15 input, and all other channels are grounded. As shown in Figure 3. 20, the crosstalk between different channels is smaller than -33dB. In addition, since the 2nd stage of the amplifiers also uses AC coupling, the amplifiers are robust against random 1st stage offset.

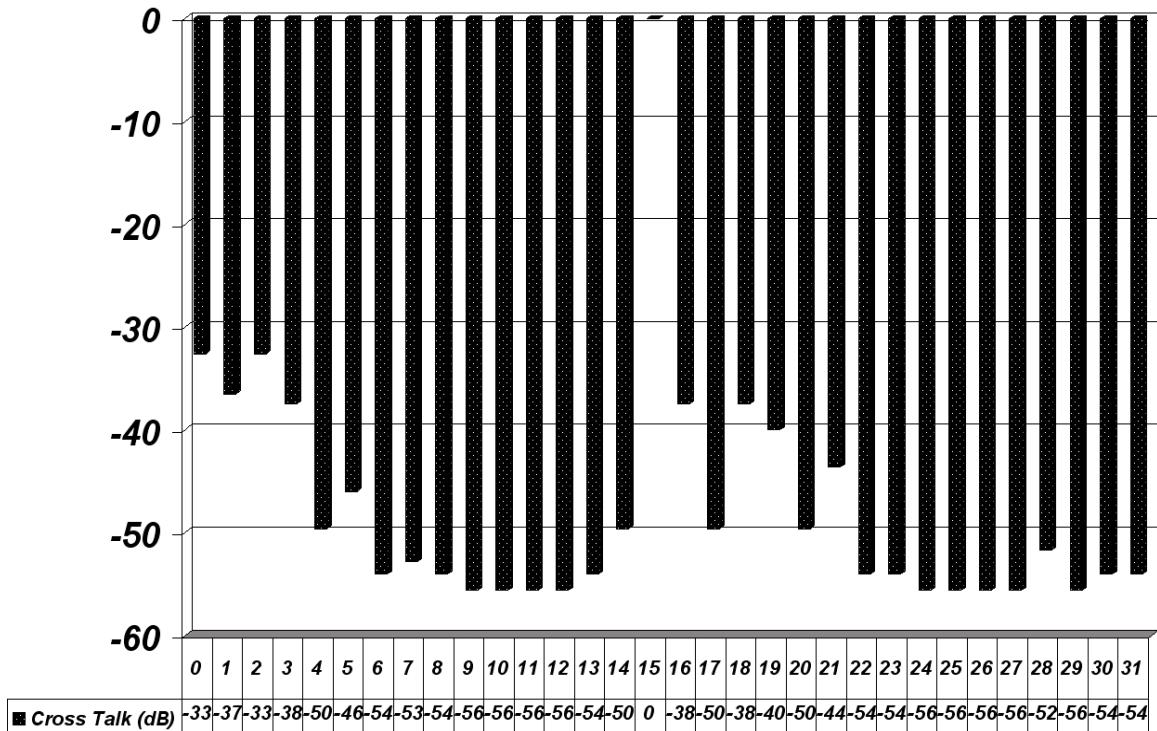


Figure 3. 20 Measured crosstalk from Ch15 to different channels when Ch15 was given 1mV_{P-P} 1 kHz sine wave and the rest of the channels were grounded.

We also measured the LNA recovery performance. We first measured the recovery time for the LNA without using the discharging strategy mentioned in Section 3.2.1. As shown in Figure 3. 21, during this measurement, the LNA input was given a 1 kHz 2mV_{P-P} sine wave superimposed by a high amplitude pulse with 160 ms duration and 1V amplitude. Then we observed the behavior of the LNA output. The results show that the recovery time for the LNA without the discharging strategy is very long, equal to 40.1ms.

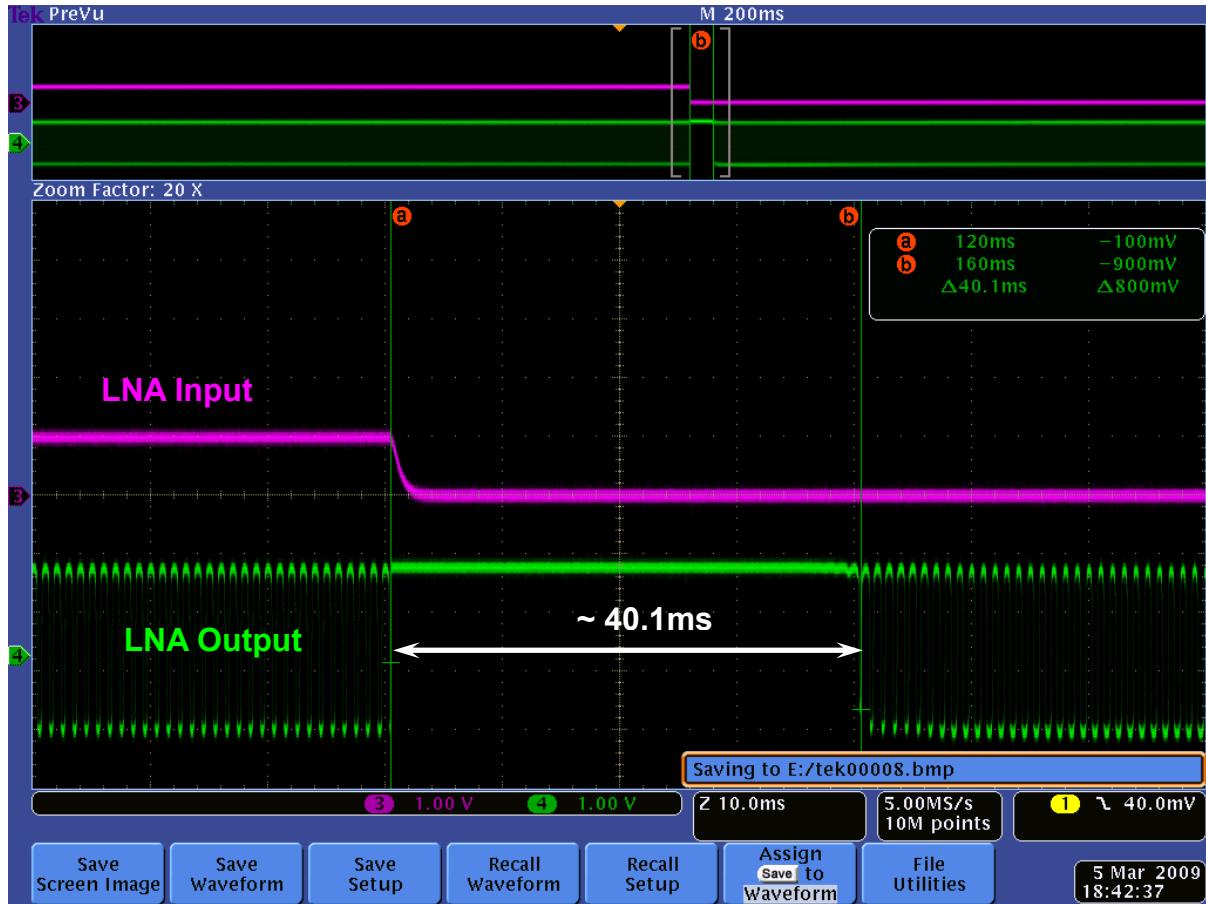


Figure 3. 21 LNA recovery time measurement results without discharge strategy.

After the first testing, we applied the discharge method, and measured the new recovery time. Similar to the simulation, as shown in Figure 3. 22, during this measurement, the LNA input was given a 1 kHz 2mV_{P-P} sine wave superimposed by a high amplitude pulse with 160 ms duration and 1V amplitude. A 100 ms discharge pulse was applied to the discharge pin of the LNA and ended 50 ms after the input pulse. The measurement results in Figure 3. 22 show that the LNA recovery time is $\sim 200\mu\text{s}$, which agrees with the simulation results.

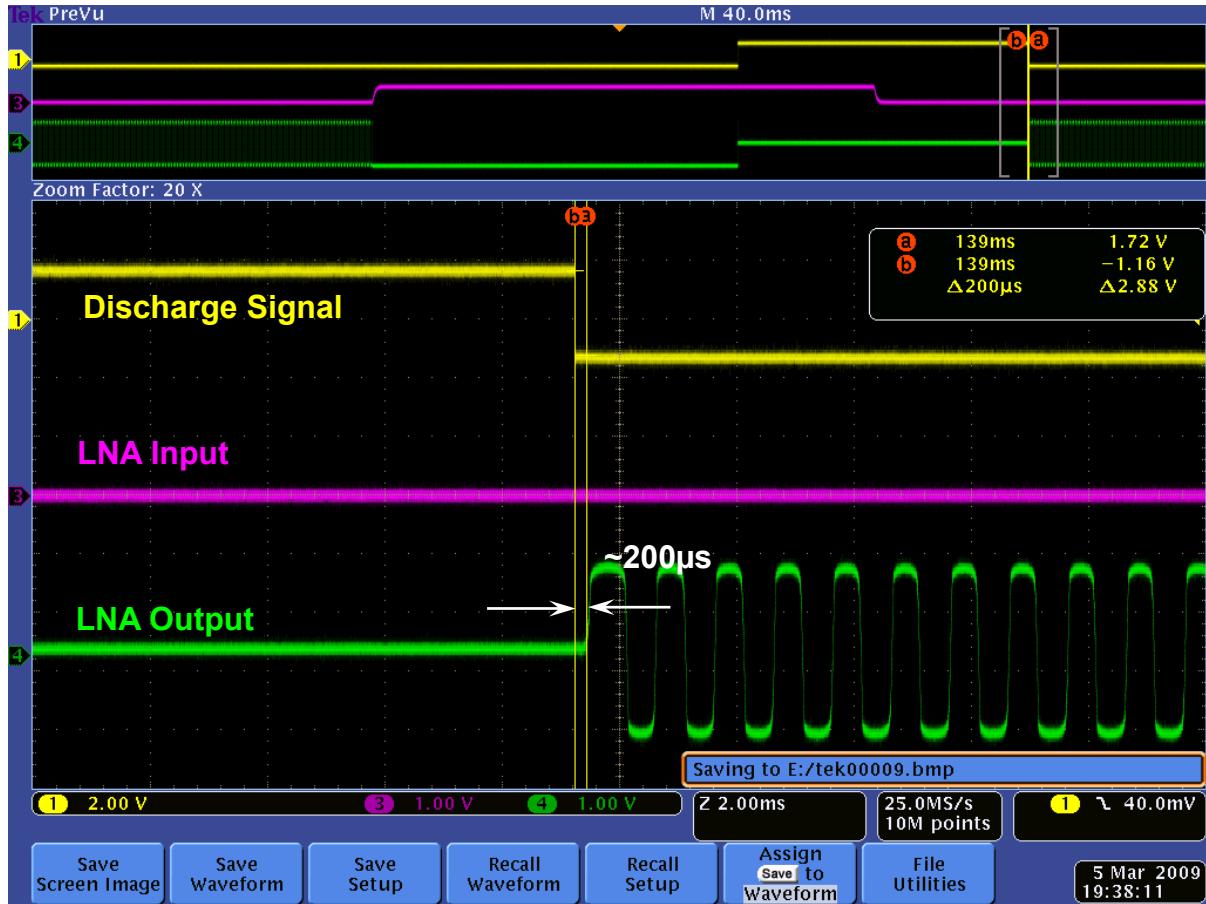


Figure 3.22 LNA recovery time measurement results with discharge strategy.

3.3.3 CCSS Measurements

The complementary current source and sink have maximum I_{Source} and I_{Sink} equal to 34.6 μ A and 123.3 μ A, respectively, and provides voltage compliance from (-1.4V to +1.4V). Measurements show that TWG operated as expected and the TW signal amplitude could vary from 0 to ± 1.4 V. For the maximum TW swing range (2.8 V_{p-p}), the sampling frequency could be adjusted in 225 steps from 58 kHz to 680 kHz using DP_{0~3} and DN_{0~3}. The

measured output impedance of the current source and sink are quite high, equal to $17.6\text{ M}\Omega$ and $26.6\text{ M}\Omega$ at maximum I_{Source} and I_{Sink} values.

3.3.4 VCO Measurements

To measure the performance of the VCO, the transmitter was placed $\sim 1\text{ m}$ away from the receiver. The receiver antenna was placed perpendicular to the transmitter PCB plane for maximum energy pick up. The VCO phase noise was measured as -88.17dBc/Hz at 10 kHz offset using Agilent PSA E4445A 13.5GHz Spectrum Analyzer. We also measured the VCO $F-V$ curve for different V_{tune-Y} and $V_{tune-X4-I}$ values, which are shown in Figure 3. 23 along with the simulation results by using large signal transient analysis. Figure 3. 23a shows the case when V_{tune-Y} is fixed at 1.5V and $V_{tune-X4-I}$ are equally changed from 1.5V to -1.5V . The result was that the VCO high gain region shifted from 1.3 V to 0 V (measured). Meanwhile the $F-V$ curve also shifted down due to the increase in C_{min} as discussed in Section 3.2.5. In Figure 3. 23b, $V_{tunex1\sim 4}=1.5\text{V}$ and we change V_{tune-Y} from -1.5V to 1.5V . The F-V curve shifts horizontally with the maximum frequency from 940MHz to 926MHz (measured). In Figure 3. 23c, $V_{tune-Y} = 1.5\text{V}$ and $V_{tune-X4-I}$ were given different values of -1.5V and 1.5V . As a result, the VCO gain was changed from 1.24 MHz/V to 23.8 MHz/V (measured). The post-layout simulation results of the LC-VCO using transient large signal analysis agreed with the measurement results.

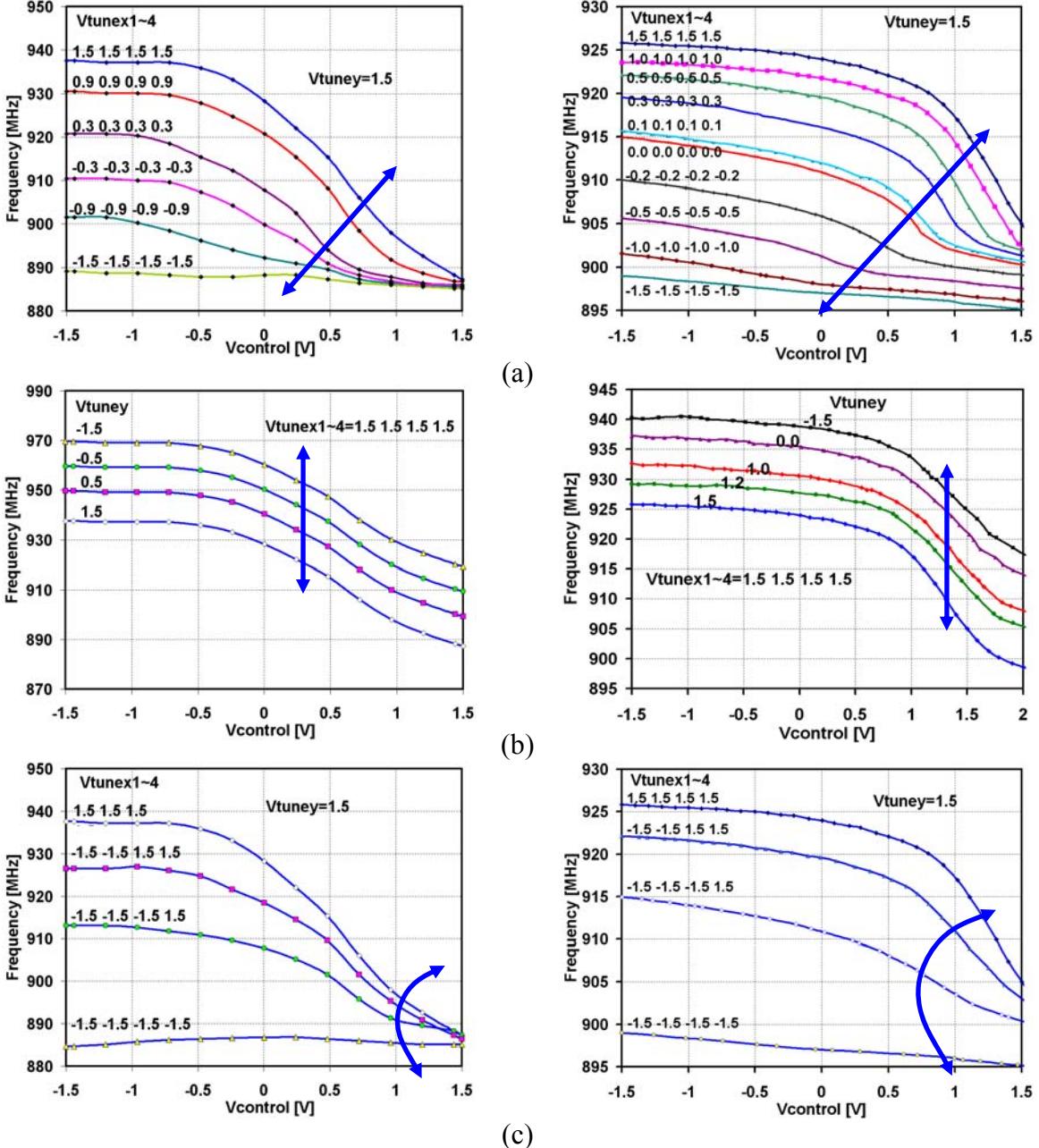


Figure 3.23 Simulation (left) and measurement (right) results of the VCO frequency vs. control voltage curves with different $V_{tune-XI\sim 4}$ and V_{tune-Y} values. (a) Shifting the location of the high gain region along $V_{control}$ axis. (b) Adjusting the VCO center frequency with V_{tune-Y} .

(c) Changing VCO gain using $V_{tunex1\sim 4}$.

Finally we measured the VCO step response by applying a $1\text{MHz} \pm 1.5\text{V}_{\text{p-p}}$ square

waveform with 15 ns rising and falling edges to the input of the VCO. After wirelessly transmitted and received at a distance of 1m, the original square wave was recovered from the received IF-FSK output by a MATLAB code. Figure 3. 24 shows the input square wave signal and the receiver output IF-FSK signal. The results show that the recovered signal has a rising and falling edges of 20ns each, and a delay of 10ns.

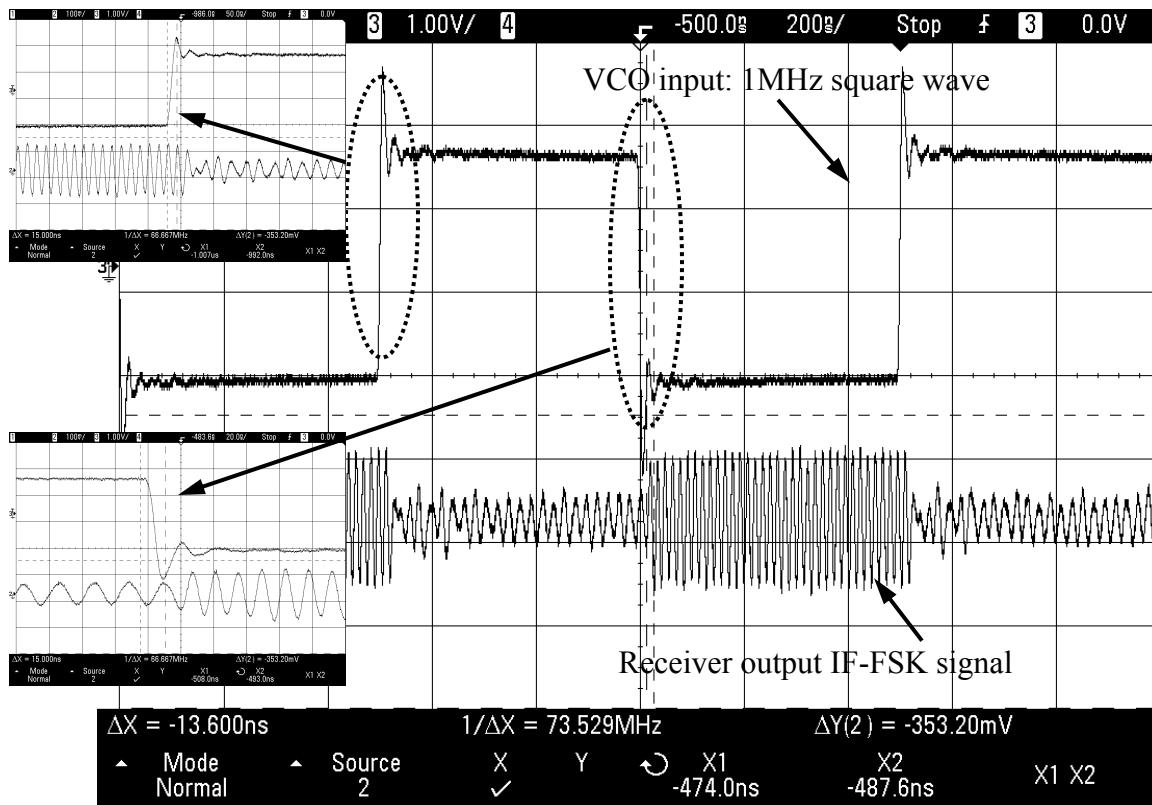


Figure 3. 24 Transmit and receive 1MHz square wave by using the proposed VCO.

3.3.5 32-Channel WINeR-V SoC Full Functionality

The functionality of the entire WINeR-V SoC was bench-top tested using 3 function generators creating a 30Hz cardiac signal, an 80Hz triangular waveform and a 100Hz sine wave, which were further divided down to generate 4 equally spaced voltages below 1mV. 8 out of the total 12 different input signals were used 3 times and given to 24 inputs of the recording channels. The other 4 were used twice and given to the remaining 8 inputs.

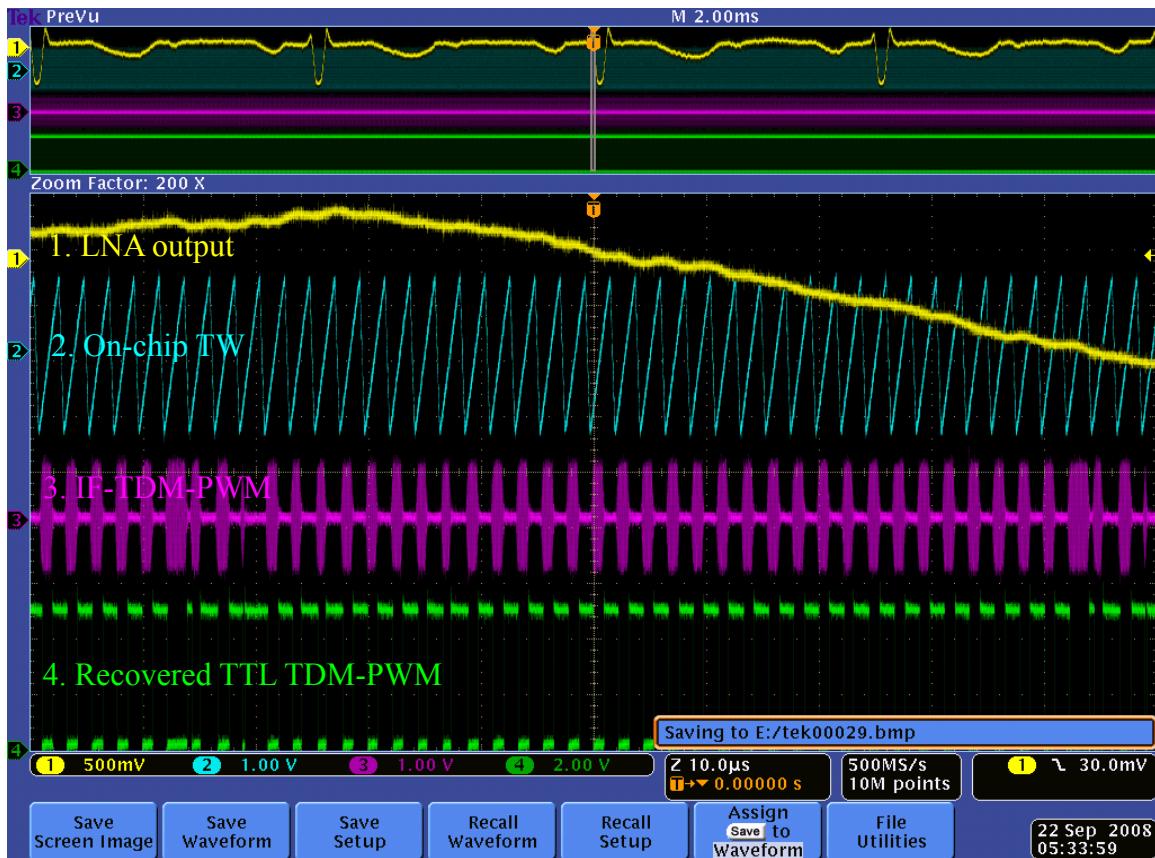


Figure 3. 25 Measured waveforms of WINeR-V. From top: 1. LNA output, 2. On-chip triangular wave, 3. Baseband TDM-PWM, and 4. Recovered TDM-PWM signals at 450 kHz (sampling rate has been reduced from 640 kHz due to probing parasitic effect).

These signals were amplified by 67.7 dB and bandpass filtered at 0.1 Hz ~ 10 kHz by the LNAs. The TWG was set to ± 1.4 V and 640 kHz. The PTS control bits $Sel_{1,2}$ was set to “00”, which trimmed and synchronized the PWM signal at the falling edge of Q , as discussed in Section 3.2.4. The masked PWM-TDM signal drove the hybrid LC-VCO, running at 898/926MHz when in FSK mode and 926MHz when in OOK mode. The off-chip inductor is a 16 nH surface mount device with the size of 1.75mm \times 1.09mm \times 0.86mm and Q=77@900MHz (0603HQ-16NX_L_, CoilCraft, Cary, IL). The FSK-TDM-PWM signal was picked up about 1 m from the WINeR-V transmitter by the receiver. The receiver amplified and down-converted the FSK signal to 42/70MHz IF-TDM-PWM, and further rectified and filtered to baseband TDM-PWM signal with 18MHz bandwidth. It was then translated to TTL level and sent to the FPGA-based TDC for digitization. Figure 3. 25 shows one channel amplifier output, TW, the receiver side IF-TDM-PWM signal, and the recovered TTL TDM-PWM signal. The 16-bit digitized samples were buffered and sent to the PC. The PC ran a VC++ GUI to record and visualize the waveforms in real-time, as shown in Figure 3. 26. The measured characteristics of the 32-channel WINeR-V system are summarized in Table 3. 1.

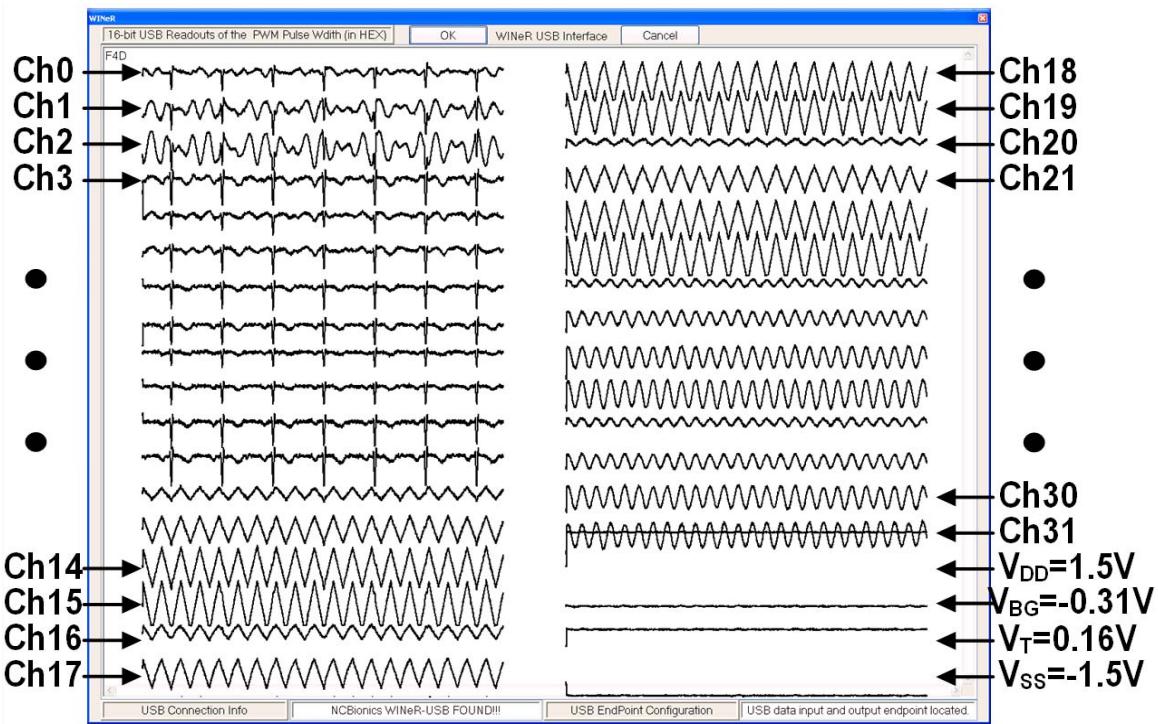


Figure 3. 26 WINeR VC++ GUI showing simultaneously recording from 32 channels wirelessly at 1 meter distance.

Table 3. 1 Summary of WINeR-V chip performance

32-channel Wireless Neural Recording System Performance	
Number of channels	32 recording + 4 monitoring channels
Amplifier gain	67.7dB/77.1dB
Amplifier CMRR	139 dB (simulated)
Amplifier PSRR	65 dB (simulated)
Amplifier input referred noise	3.9 μ Vrms
Amplifier low-cutoff	0.1 Hz~1 kHz (continuous)
Amplifier high-cutoff	700 Hz~10 kHz (4-bit programmable)
Sampling rate	640 kSps
FSK carrier frequency	898MHz / 926 MHz
System resolution (with receiver)	8 bits @1 meter receiving distance
System input referred noise (with receiver)	4.9 μ Vrms@1 meter receiving distance
Total power dissipation	5.6 mW
Power supply	\pm 1.5 V

3.3.6 Sampling Rate, Dynamic Range, and Resolution

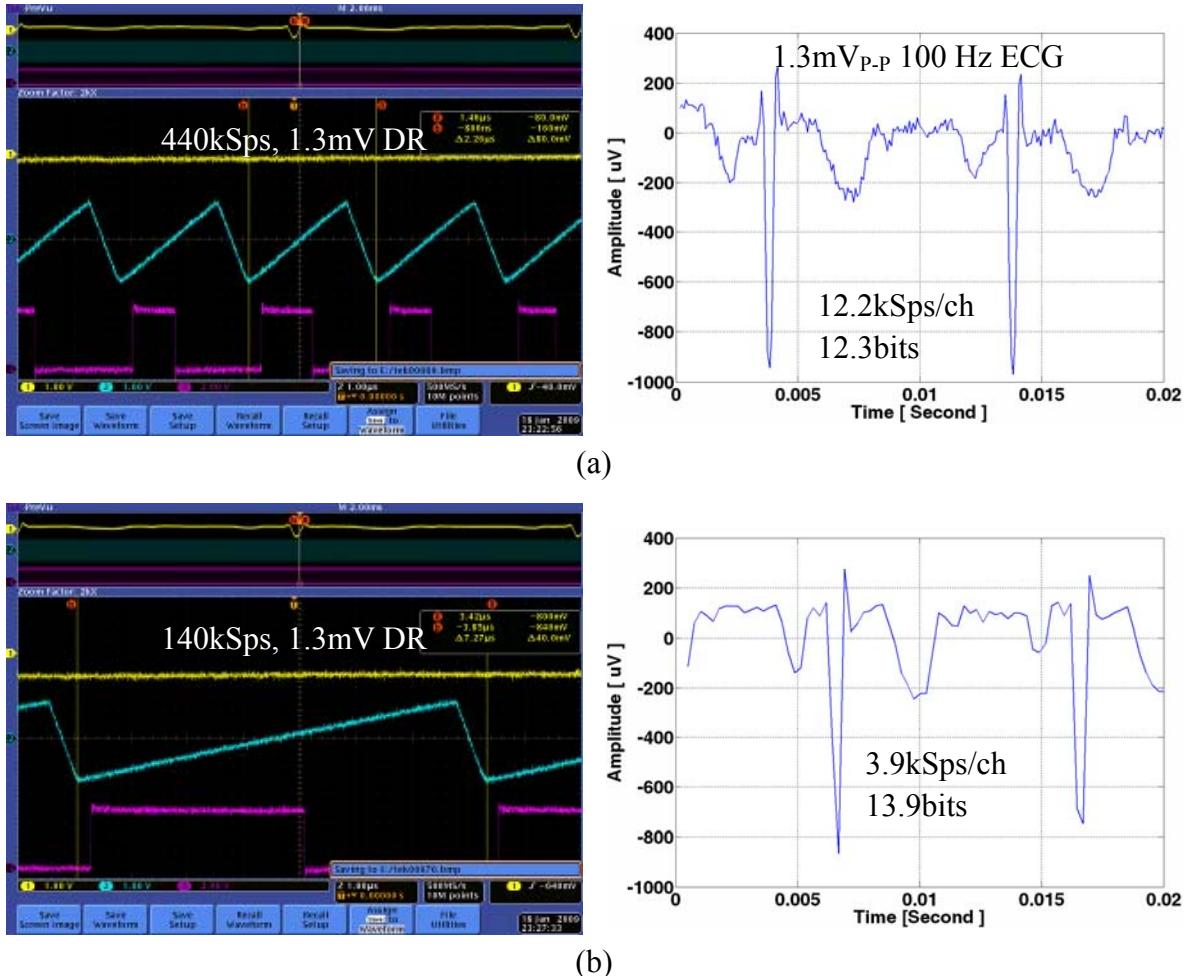


Figure 3.27 Reducing system sampling rate to achieve higher resolution when keeping the input dynamic range to be 1.3mV. (a) 12.2kSps per channel and 12.3bits TDC resolution. (b) 3.9kSps per channel and 13.9bits TDC resolution.

As we have mentioned earlier, the TW frequency and amplitude can be changed by adjusting V_{high} , V_{low} , and the control bits $DN_{0\sim 3}$ and $DP_{0\sim 3}$ in the CCSS. Since the TW frequency and amplitude are directly related to the system sampling rate and input dynamic

range (DR), therefore by changing these parameters we could optimize the system performance based on the input amplitude and signal frequency range of interest. In Figure 3. 27, for example, the input is a 100Hz 1.3mV_{P.P} artificial cardiac signal, and its frequency bandwidth is around 2 kHz. Instead of using channel sampling rate of 12.2kSps (Figure 3. 27a), we could adjust the sampling rate to be its minimum Nyquist rate ~4kSps per channel, therefore we could increase the pulse period from 2.3μs to 7.1μs. Considering our TDC has a time step of 0.304ps, this change will increase the TDC resolution from $\log_2[2300/0.304] = 12.3\text{bits}$ to $\log_2[7100/0.304] = 13.9\text{bits}$.

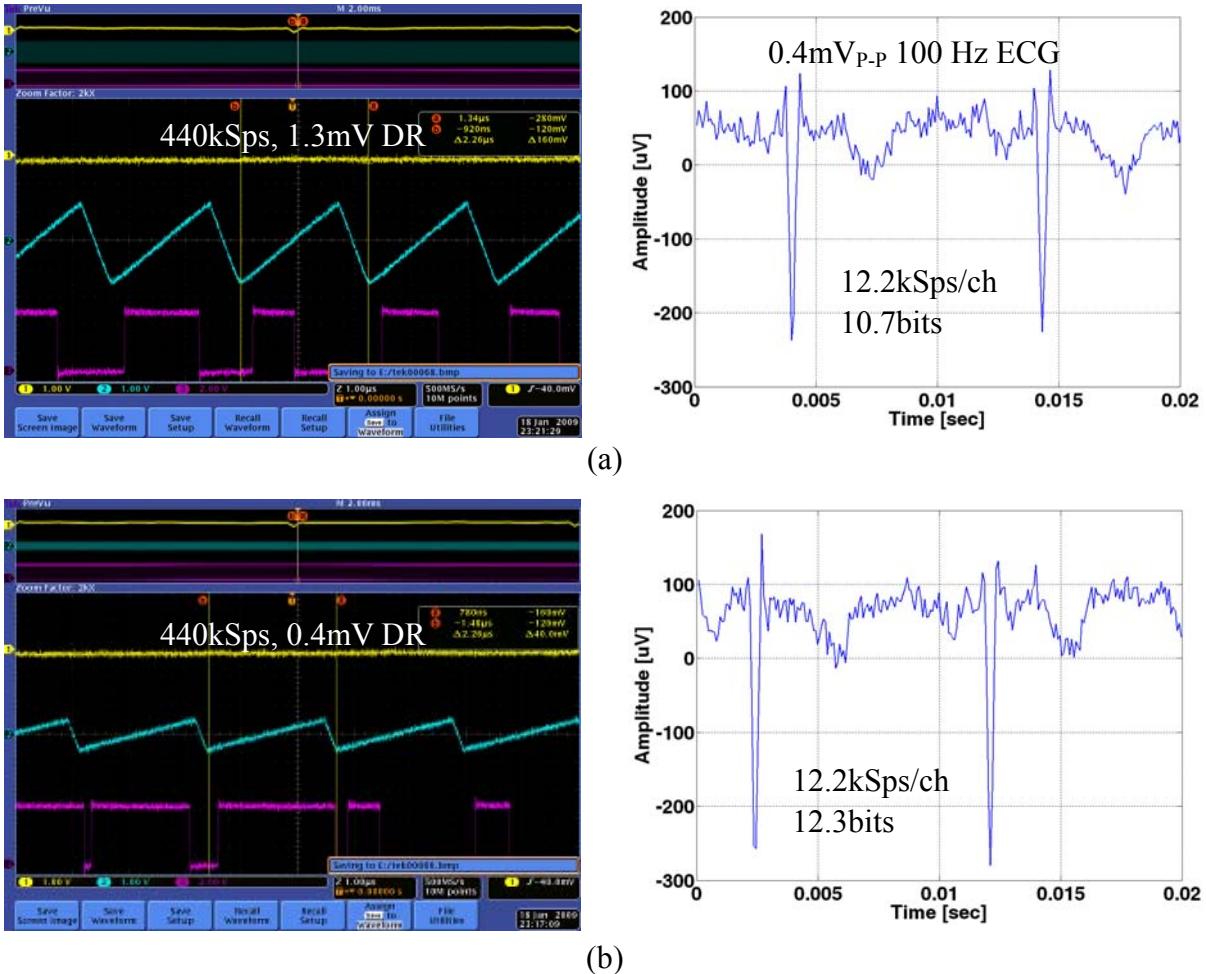


Figure 3.28 Reducing input dynamic range to achieve higher resolution when keeping the system sampling rate to be 440 kSps (12.2kSps/ch). (a) 12.2kSps per channel, 12.3bits TDC resolution. (b) 3.9kSps per channel, 13.9bits TDC resolution.

In another case, as shown in Figure 3.28, if the input signal amplitude is reduced to $0.4\text{mV}_{\text{P-P}}$, and at the same time we want to keep the sampling rate to be constant as 440 kSps (12.2kSps/ch), we can reduce the input dynamic range from $1.3\text{mV}_{\text{P-P}}$ to $0.4\text{mV}_{\text{P-P}}$ to increase the system resolution. For instance, in Figure 3.28a, the input DR is set to $1.3\text{ mV}_{\text{P-P}}$, while the input signal is only $0.4\text{ mV}_{\text{P-P}}$. Therefore the only $1/3$ of the DR is being used. This will lead to

only 10.7 bits of TDC resolution. However, in Figure 3. 28b, since the input DR is equal to input signal range, it will increase the TDC resolution to 12.3bits.

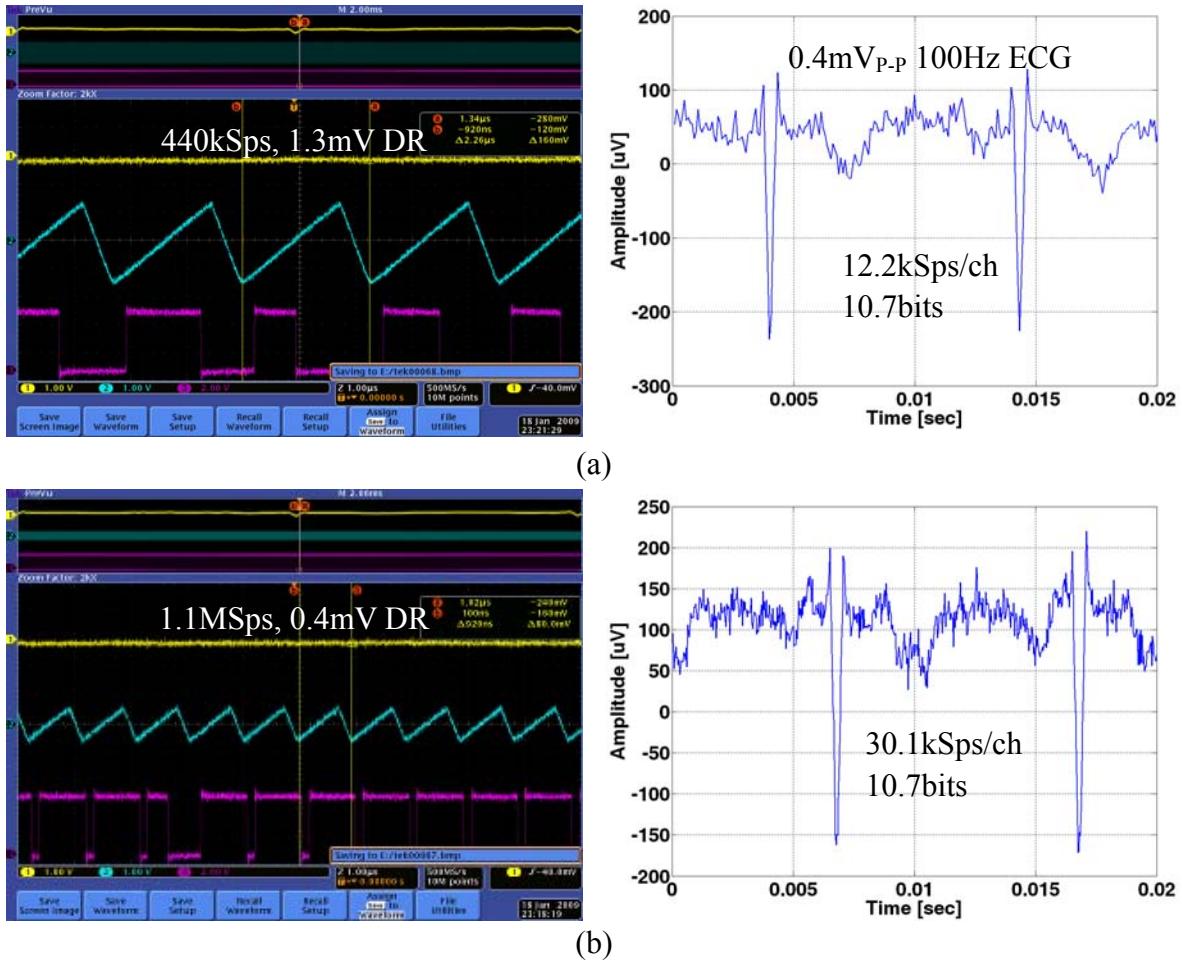


Figure 3. 29 Reducing input dynamic range to achieve higher sampling rate while keeping the TDC resolution be the same (10.7bits). (a) 12.2kSps per channel, 1.3mV_{P-P} DR. (b) 30.1kSps per channel, 0.4mV_{P-P} DR.

Finally, we can increase the sampling rate by trading off the input dynamic range, while still keeping the same TDC resolution. For example, in the previous case, since

1.3mV_{P-P} DR is a waste for 0.4mV_{P-P} input signal range, therefore we can lower the DR to be 0.4mV_{P-P}, while having a higher sampling rate, as shown in Figure 3. 29.

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CHAPTER 4 WINeR Receiver

4.1 Introduction

In the past twenty years, researchers have developed wireless neural recording systems and fulfilled the requirements to a certain extent [4.1]-[4.7]. Most of the research focused on the neural recording on the transmitting side. However, a complete wireless neural recording system includes the implantable recording and transmitting as well as the external receiving and computer interfacing units. The challenges to successfully develop a multi-channel wireless system could come from both sides. For example, as the bandwidth of neural signals can reach above 10 kHz, recording systems with simultaneous recording sites in the order of tens of sites or more yield large amounts of data that makes it very challenging for the wireless neural recording system to allocate enough bandwidth for transferring it across its wireless link. For instance, as shown in Table 2. 2, a 32-channel system at minimum Nyquist rate of 20 kSps/ch and 8 bits of resolution needs a data rate of 5.12 Mbps for the wireless link without considering the overhead. This data rate is quite high especially for the receiver, and is one of the major limitations that prevent the wireless recording systems moving toward the widely used high resolution recording for a large number of channels.

Some analog systems use frequency modulation (FM) scheme for wireless data transmission. P. Mohseni's [4.8] 8-channel system used commercial FM receiver (WR1550e, WinRadio Communications, Melbourne, Australia). Although the analog scheme does not require large RF bandwidth for data transmission, due to the bandwidth limitation (\sim 150 kHz) of the receiver, this system suffered large crosstalk between channels (\sim 37.1%). Besides, the limited bandwidth also required frequency stabilization components such as crystals and phase locked loops (PLL) to reduce the phase noise and ensure good signal fidelity. Increasing the bandwidth of the receiver will alleviate these problems, such as in the 32-channel Triangle Biosystem [4.9], which uses a 3.2GHz custom designed 300MHz bandwidth receiver. However, due to the shortcomings of the analog system, it is subject to signal distortion and signal quality degradation due to analog time-division-demultiplexing for a large number of channels.

Because of the aforementioned disadvantages of the FM scheme, most currently developed wireless recording systems are using digital schemes along with FSK, ASK, OOK, or GFSK modulations for transferring the digital data at ISM band frequencies. In HermesC system, C. A. Chestek et al. [4.10] utilized FSK scheme and 384kbps commercial ISM band transceiver (ADF7025, Analog Devices, Inc., Norwood, MA). M. Rizk et al. [4.11] used a commercial ASK/OOK 1 Mbps RF transceiver (TR1100, RF Monolithics, Inc., Dallas, TX) for their 96-channel system. D. Cheney et al. [4.12] used a commercial 2.4GHz GFSK

1Mbps Nordic transceiver (nRF2401, Nordic Semiconductor, Inc., Trondheim, Norway) for their 16-channel Pico recording system. All these systems used commercial receiver ICs to receive RF signal and demodulated it into digital data. However, these designs suffer from limited wireless data rate. Therefore they either only simultaneously transfer limited number of high resolution channels or need intensive data reduction on the transmitter side. For example, HermesC created one channel 10-bit neural data from the 96 channels, and produced 345.6kbps data over the wireless link, which is the rate that can be handled by ADF7025. In Rizk's 96-channel system, the amplified signal was sampled at 31.25kSps and converted to 12-bit digital value. With the maximum of 1Mbps for the transceiver, fewer than 3 full channels can be transmitted simultaneously. In order to reduce the data rate, automatic bit selection was used to select the 'best' 8 bits to reduce each sample data from 10 to 8 bits. In addition, four data output modes: single channel raw data mode, spike sorting data mode, bincounts data mode, and single channel raw data + spike sort data mode, were implemented to further reduce the data volume. Similar situation happened in the Pico Recording system, in which single channel raw data mode, single channel 20kSps 12-bit data is wirelessly transferred. In its spike reading mode, only the firing rate for each neuron is computed locally and sent over the Nordic transceiver.

When facing the limited transceiver data rate problem, some researchers were seeking different ways to solve it. S. Mandal and R. Sarapeshkar [4.13] have used 25MHz

impedance modulation link with data rate up to 5.8Mbps, which achieved large power saving for the internal transmitter and is sufficient to transmit data for 16 channels with considering the frame overhead bits. However, its impedance modulation scheme limits its range to only 1 or 2 cm. Other researchers were moving to ultra-wide-band (UWB) transceivers for their high data rate (100Mbps~1Gbps), low multipath interference, low power and simplified architecture. M. Chae [4.14] presented a 128-channel system operating at UWB frequency. The UWB link provided maximum of 90Mbps data rate and was able to send all high resolution data from all channels. A custom-designed UWB receiver was built with off-the-shelf components to receive the signal. Another UWB transceiver is commercially available from Neuralynx [4.15] in its Digital Telemetry-128 system. It offers 100Mbps data rate and can support 18-bit 32kSps for all 128 channels. Although UWB technique may offer many advantages, due to the large spread spectrum of the carrierless short pulses, long synchronization time is required for the UWB to achieve high precise signal acquisition, synchronization, and tracking at the receiver. In addition, it requires complex signal processing techniques to recover data from noisy environments.

In addition to the bandwidth issue, another challenge that is often overlooked on the receiver side is the continuous, high throughput data transfer from the wireless receiver to the PC in real-time. For example, a 32-channel system with a minimum of 20 kSps/channel and

16bits/sample produces 10 Mbps raw data. The PC interfacing hardware and software should be designed to continuously acquire such data volumes without any information losses.

To address these challenges, we developed a custom-designed high performance, wideband, and low-noise receiver for the wireless recording systems utilizing PWM-TDM technique. This receiver was evaluated along with the 32-channel WINeR-V transmitter with a small chip antenna attached to the transmitter VCO output, which was described in Chapter 3. The results showed that the WINeR receiver can operate pretty well for a receiving distance of more than 1m. We achieved more than 8 bits of resolution at 640 kHz sampling rate for the entire 32-channel system. The measured input referred noise of the entire system was $4.9 \mu\text{V}_{\text{rms}}$ at 1 meter distance.

4.2 Hardware Description

The WINeR system resolution is determined by the received pulse width error. According to the analysis later in Section 5.3.3, the higher the receiver baseband bandwidth, the less pulse width error we will have. Therefore the WINeR receiver needs high enough bandwidth to receive the FSK-TDM-PWM signal while providing adequate resolution (8 bits or more). Unfortunately, today's commercially available ISM-band FSK receivers only provide up to 600 kHz of baseband bandwidth at 384 kbps data rate [4.16], which is far below what is required for a neural recording system with large number of channels. Hence,

we have implemented a custom designed receiver with up to 75 MHz bandwidth using off-the-shelf components.

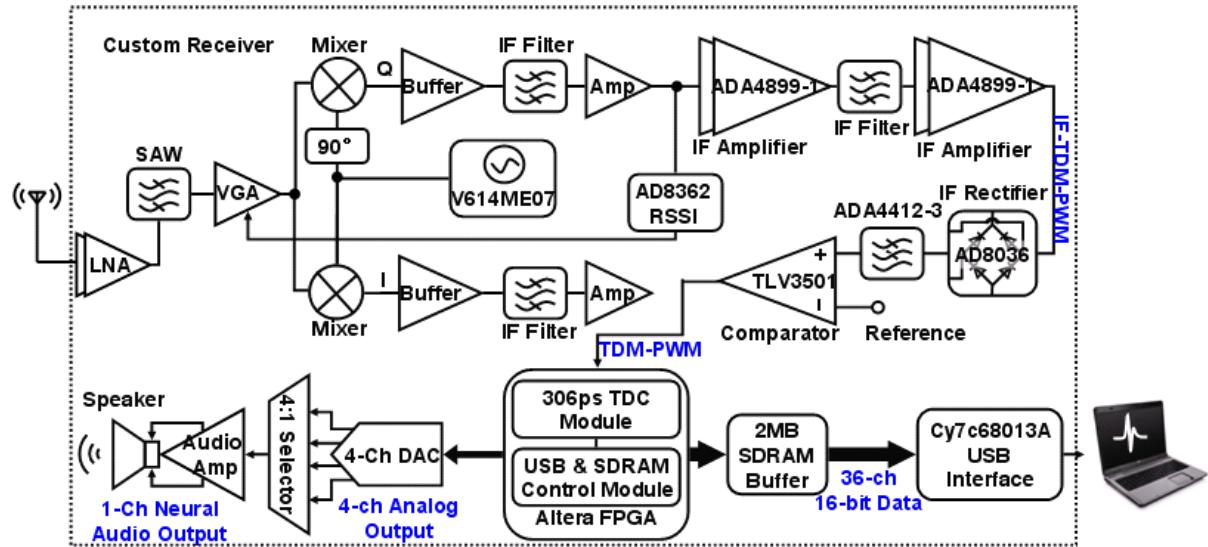


Figure 4. 1 The WINeR receiver block diagram.

The WINeR receiver block diagram is shown in Figure 4. 1. It has four major components: FSK demodulator, time-to-digital convertor (TDC), SDRAM data buffer and USB interface, and the audio block.

4.2.1 Custom Wideband FSK Demodulator

The FSK demodulator consists of the front-end RF low noise amplifier (LNA) (MAX2640, Maxim Integrated Products, Inc., Sunnyvale, CA) with a noise figure of 0.9dB at 900MHz. A 4-stage gain block (BGA2712, NXP Semiconductor, Eindhoven, Netherlands)

is following the LNA, providing a total gain of ~80dB and noise figure of 3.9dB. Since the LNA and gain stage of the receiver provide up to 1.5GHz bandwidth, a 902-928MHz surface acoustic wave (SAW) filter (B3588, EPCOS, Inc., Munich, Germany) with 2.9dB insertion loss is added after the gain block to provide more selectivity for the signal of interest. This SAW filter can be bypassed when larger bandwidth is needed.

The filtered FSK signal is fed into a 50 MHz to 1 GHz quadrature demodulator with 75 MHz bandwidth (AD8348, Analog Devices, Inc., Norwood, MA). The demodulator chip has a built-in variable gain amplifier (VGA) at its front-end and provides $+25.5 \sim -18.5$ dB linear-in-decibel gain control. The output of the VGA drives two (I and Q) double-balanced Gilbert cell down-conversion mixers, which down-convert the amplified signal to intermediate frequencies (IF-TDM-PWM). The IF-TDM-PWM is further filtered and amplified.

Since the transmitter will move with the animal during free moving animal testing, the received signal strength could change by more than 40dB. In order to compensate these variations and stabilize the received signal strength, one of the mixer output (Q) is monitored by a 65dB dynamic range power detector (AD8362, Analog Devices, Inc., Norwood, MA), which output is used to control the VGA gain. This automatic-gain-control (AGC) scheme can stabilize the received signal strength within 0.5dB. To create a tunable local oscillator

(LO) for the down-converter, we have utilized a 1680MHz ~ 2020 MHz VCO (V614ME07, Z-communications, Inc., San Diego, CA) and a divide-by-two balun, which result in receive range of 840 ~ 1010 MHz.

IF-amplifiers and filters are used after the quadrature demodulator to improve the SNR of the IF signal. AD4899-1 (Analog Devices, Inc., Norwood, MA) is chosen as the IF-amplifier for its 300 MHz unity gain bandwidth, ultra low distortion, low noise and unity gain stable characteristics. 4 IF-amplifiers are implemented in two groups. Each group has two IF-amplifiers with their gains setting to 20dB and 6dB and offer a total IF gain of 52dB. Since the RF front-end down-converts all the noise adjacent to the signal spectrum to IF band and feeds it into the IF amplifiers. We found that this noise is quite large especially when the RF carrier frequency is within the busy 900 MHz or 400 MHz ISM bands. The IF amplifiers (ADA4899-1) could get saturated by this noise and create large harmonic distortions in the following IF amplifiers. This could also degrade the SNR and limit the receiving range. To solve this problem, we added passive LC filters between the two groups of IF amplifiers to filter out the out-of-band noise. The filter is implemented as 5th order Chebyshev bandpass with 18 MHz bandwidth from 38~56 MHz and 1.0 dB pass band ripple. The LC values used for these filters are chosen to match 50 Ω at 50 MHz IF frequency. Another important function of the bandpass filter is that it can act as a discriminator. Because of the wide spreading of the two FSK frequencies (28 MHz separation), if one of the IF-FSK frequencies

is tuned at the center of the passband—47 MHz, the other IF-FSK frequency will be located either at 75MHz or 19MHz, which will be filtered out.

The amplified and discriminated IF-FSK signal, which is now more like an on-off-keying (OOK) signal at this stage, as the yellow trace shown in Figure 4. 11, is fed into an IF full-wave rectifier. The rectifier has been realized by a low distortion, wide bandwidth, output voltage clamp amplifier (AD8036, Analog Devices, Inc., Norwood, MA). A video lowpass filter (LPF) (AD4412-3, Analog Devices, Inc., Norwood, MA) follows the rectifier to generate the IF carrier envelope and restore the baseband TDM-PWM signal. This filter is a sixth-order Butterworth video filter with selectable cutoff frequencies at 9, 18, and 36 MHz. The video filter can be replaced with a custom LC filter when a different baseband bandwidth is required. These flexibilities offer more control over the wireless link bandwidth and waveform for achieving better system resolution. Finally, the baseband PWM-TDM signal is recovered and translated to standard TTL levels (0~5V) by a high speed comparator (TLV3501, Texas Instruments, Inc., Dallas, TX) with 4.5ns delay before being fed into the TDC block.

4.2.2 FPGA-Based TDC

TDCs convert sporadic pulses into digital representations of their time indices. A TDC is often used when important information is to be found in the timing of events. To

minimize the TDC error, our 1st and 2nd version of the WINeR receiver used a high speed 16-bit synchronous counter running at 800 MHz in emitter-coupled logic (ECL), which led to a large receiver power consumption of 8.5W.

Another issue with the ECL counters was the random spikes in the recovered signal due to racing when two 8-bit synchronous counters were cascaded and gated with the asynchronous PWM signal. This spiking noise was highly undesirable, since it could be easily confused with the real neural spikes. Even though this issue could be eliminated by synchronizing the incoming PWM with the counters' clock, it would introduce additional pulse width error.

Considering these problems, we replaced the noisy and power consuming ECL counters with a TDC implemented on a field programmable gate array (FPGA). FPGA-based TDCs have been widely used in applications such as high-energy physics because of their low cost, short developing time, and high flexibility. Since J. Kalisz, et al. proposed the first FPGA-based TDC in 1997 [4.17], researchers have achieved resolutions as low as 50 ps [4.18]. Although temperature and power supply compensations are needed to achieve such high resolutions, ordinary FPGA-based TDCs can easily achieve sub nanosecond resolutions that are sufficient for our application.

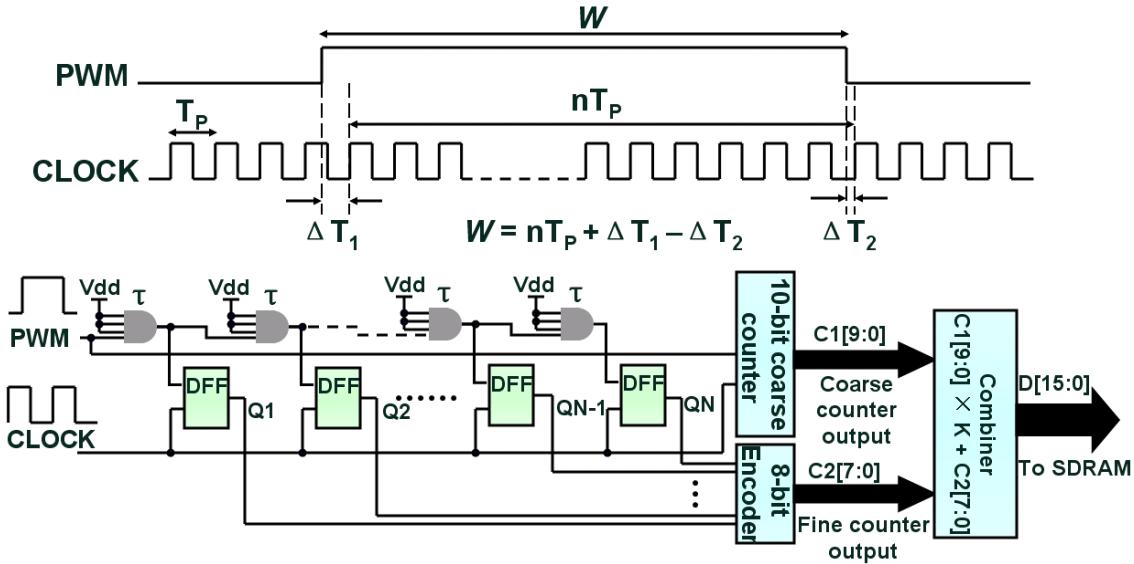


Figure 4.2 FPGA-based high resolution TDC using a logic delay cell chain.

The basic idea of the FPGA-based TDC is shown in Figure 4.2. It consists of two counters, the *coarse* counter and the *fine* counter. The coarse counter is a 10-bit synchronous counter running at the FPGA main clock (period T_P) with the PWM signal as its enable. Considering the fact that PWM pulses are asynchronous with the clock, their falling and rising edges could arrive at any time. If the total pulse width of one PWM sample is w , then

$$w = nT_P + \Delta T_1 - \Delta T_2 \quad (4.1)$$

where ΔT_1 and ΔT_2 are the time differences between the rising and falling edges of the incoming PWM pulse with the rising edges of the clock pulses immediately following those events. When PWM is high, the coarse counter is enabled to provide the most significant bits of the TDC output, $C1[9:0]$. The fine counter is used to measure $\Delta T_1 - \Delta T_2$. It has a chain of

logic delay cells, each with a delay time of τ . Since $\text{Max}(\Delta T_1 - \Delta T_2) = T_P$, the total propagation time of the delay chain should be longer than T_P . This would indicate the time step ratio, $K = T_P/\tau$, and the number of delay cells needed in the chain, $N > K$. The PWM signal is the input to the delay chain. An array of edge-triggered D-flip-flops register delayed versions of the PWM signal along the delay chain at the first rising edge of the clock right after the rising and falling edges of the original PWM. The registered data is sent to an encoder to provide an 8-bit digital value for $\Delta T_1 - \Delta T_2$ which is represented by $C_2[7:0]$. A combiner logic combines the two counter outputs into a 16-bit digitized data $D[15:0]$ based on the following equation

$$D[15:0] = K \times C_1[9:0] + C_2[7:0] \quad (4.2)$$

This architecture resulted in a low power, low-noise, and high resolution TDC with no random spikes.

4.2.3 SDRAM Data Buffer and USB Interface

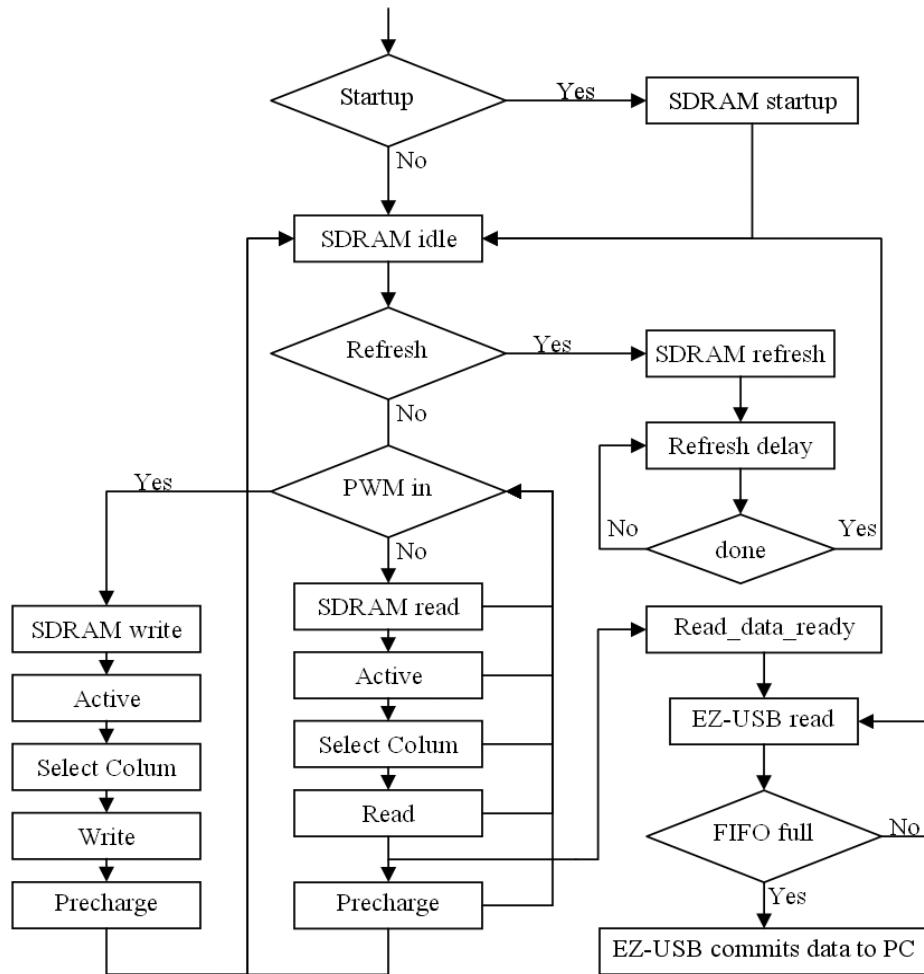


Figure 4.3 FPGA USB/SDRAM control module flow chart.

We included a USB 2.0 interface in the WINeR receiver as the final stage to provide a direct continuous interface to a PC in real-time. Cypress high speed EZ-USB chip (Cy7C68013A, Cypress Semiconductor Corporation, San Jose, CA) was chosen for its programmability, high throughput, reliability, and ease of use. Since PC delays between

successive USB data packets are unpredictable and can vary from 100 μ s to several ms, samples could be lost during these PC delay times. To ensure continuous real-time recording in the receiver without losing any samples, we have used a 2 MB SDRAM between the TDC and the USB interface blocks to buffer the digitized data before they are transferred to the PC. A firmware was developed to enumerate the EZ-USB chip in the slave-FIFO mode (will discuss in detail later), and is controlled by a periphery master module implemented in an Altera FPGA. As shown in the operation flow chart, Figure 4. 3, the FPGA USB/SDRAM control module provides the control signals for the data transfers between the SDRAM and USB blocks. It manages the 16-bit data created by the FPGA-TDC module to be written into the SDRAM on the falling edge of every PWM pulse. The module also controls and maintains the necessary operations of the SDRAM, such as refresh and precharge. When the SDRAM enters the idle state, the control module will initiate a SDRAM read transaction, which makes the EZ-USB to read a 16-bit sample from the SDRAM to its internal 2056 Bytes FIFO. In the meantime, the EZ-USB chip continuously checks its FIFO state, and when it is full, it will automatically commit the data to be transferred to the PC.

4.2.4 Audio Block

To help the neuroscientists and other users to better identify and visualize the neural spikes, the WINeR receiver is equipped with an audio block to offer these convenient

capabilities. The audio block has a 4-channel 16-bit digital-to-analog converter (DAC) with 220kSps update rate (AD5664R, Analog Devices, Inc., Norwood, MA). The clock, data, and enable signals are generated by the same FPGA used to implement the TDC and USB/SDRAM modules. The FPGA can select 4 channels of 16-bit data out of the 36 channels (32 recording+ 4 monitoring), and sends them to the DAC. The DAC converts them into 4 analog signals that can be accessed independently through four SMA connectors on the WINeR receiver box. In addition, one of these 4 analog signals is selected through a 4:1 selector and drives a 1W 8Ω bridge-tied-load (BTL) audio amplifier with DC volume control (TDA7052A, NXP Semiconductor, Eindhoven, Netherlands). Therefore, the user can identify the neural spikes by just hearing the “sounds” of the neurons. This is how most neuroscientists identify whether the recorded neural signals contain real bursts of single-unit spiking activity, as opposed to being the background neural noise only.

4.3 USB Firmware and VC++ Graphic User Interface

To access the WINeR receiver USB interface from the PC, a USB firmware and a VC++ graphic user interface (GUI) were developed.

4.3.1 Cypress EZ-USB Firmware

The first thing to do before using the Cypress EZ-USB is to install the USB driver,

the .SYS file. There are two available .SYS files. Depending on the library that you want to use, different driver should be installed. For our case, since we want to use CYAPI.lib for the VC++ GUI to communicate with the USB, the CYUSB.SYS driver is installed, which can be done by running the CYUSB.inf file.

After installing the USB driver, we need to build the firmware to configure the Cypress USB chip and initialize it. The way to build the firmware is to use “Keil µVision” software, which will come with the Cypress Evaluation Board Kit. You need to first look at the “technical reference manual (TRM)” of the Cypress chip, and find out what kind of operational mode you want the Cypress USB chip to be in, such as “Slave FIFO”, “GPIF”.... Then you can find some built-in examples of “Keil µVision” projects. For example, there is an “FX2_to_extsyncFIFO.Uv2” project under C:\Program Files\Cypress\GPIF Designer\fifo. You can build your own project by modifying the parameters in the source files. The file that needs most of the modifications is the “FX2_to_extsyncFIFO.c” file. For example, the “EPXCFG” value needs to be changed to enable or disable the Endpoints of the USB and configure them either as “in” Endpoints or “out” Endpoints. However, above all, the most important parameter needs to be modified is the VID and PID in the device description file—dscr.A51 (as shown in Figure 4. 4), it should be matched to the VID and PID values of the Cypress EZ-USB chip, as well as those values in the Cypress USB initial file, CYUSB.inf.

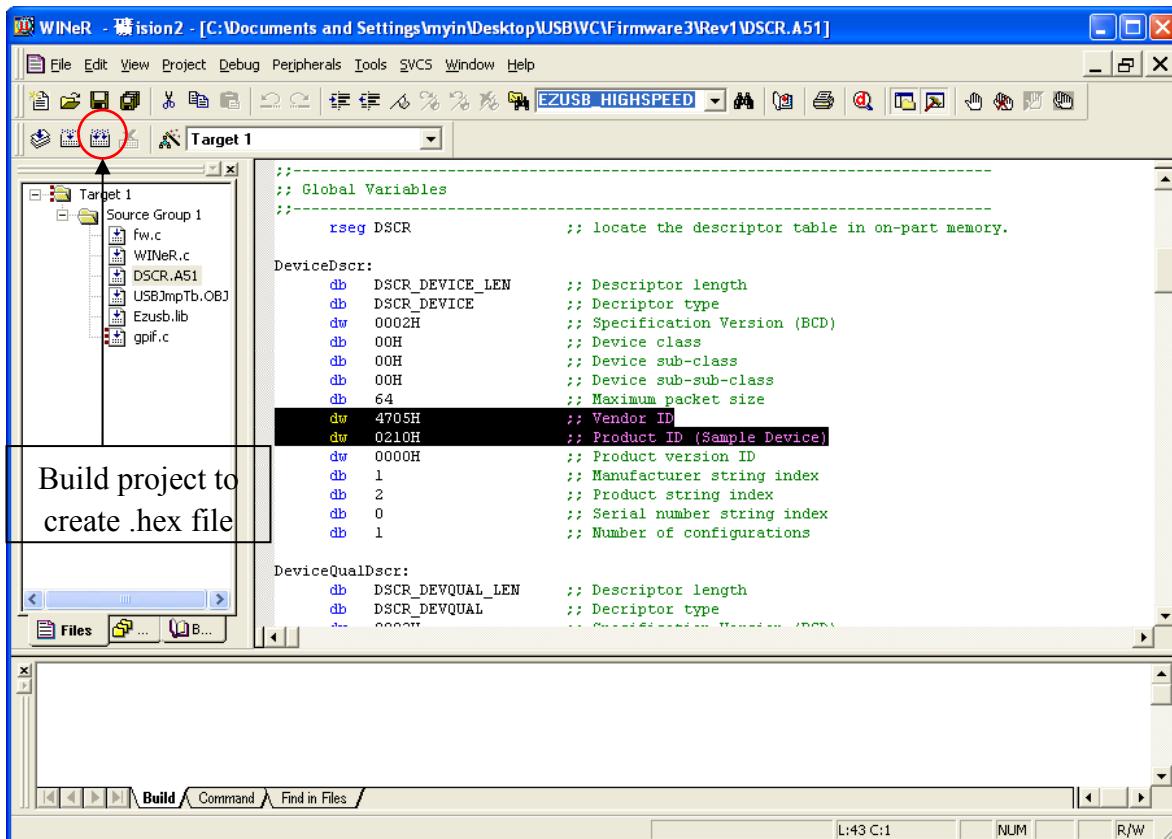


Figure 4. 4 WINeR USB firmware dscr.A51 file (highlighted is the VID and PID for the WINeR Cypress EZ-USB).

In order to configure the USB into a proper mode, gpif.c file should be modified. As mentioned earlier, the USB is configured in “Slave-FIFO” mode. After making all the necessary changes, you can click on the “build all button” at the upper left corner of the Keil μVision window to create the .hex file (Figure 4. 4). Now the firmware is successfully built. Then you need to load the firmware into the USB device.

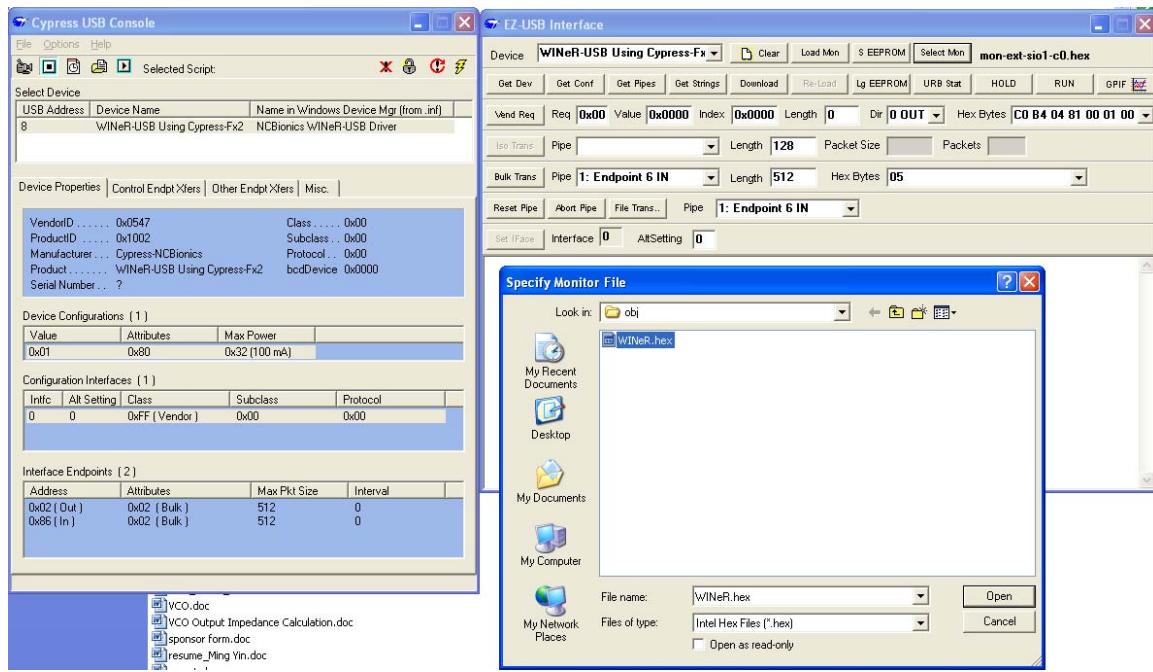


Figure 4. 5 Screenshot of the Cypress USB Console used for loading the firmware to the USB.

The “Cypress USB Console” software is used to load the firmware to the USB. The Cypress USB Console software can be downloaded from the Cypress webpage. In the “EZ-USB Interface” window, as shown in Figure 4. 5, click “Select Mon” to select the .hex file you have just created by using Keil µVision, then click “Load Mon” to load the firmware. After loading the firmware (.hex file), the Cypress USB Console main window will look like the left window shown in Figure 4. 5. It identifies the information of the custom USB that you have configured with the firmware, especially the Endpoints, VID and PID.

One thing the user should note is that if an EEprom is not used, the user needs to load the firmware every time he connects the USB to the PC. A way to avoid this is to have

an off-chip EEprom. But the firmware needs to be burned into the EEprom. To do this, the user needs to convert the .hex into an .iic file. Cypress provides a utility called Hex2bix.exe that converts the hex file produced by Keli µVision into an EEprom file. The method of using Hex2bix.exe is going to “Start”→ “Accessories”→ “Command Prompt”. In the prompt window type command: **hex2bix -i -f 0xC2 -o output.iic input.hex**. Then an EEprom file output.iic is created. Then go back to the “EZ-USB Interface” window of the “Cypress USB Console” software, click the “Seeprom” button and select the .iic file. And then click “OK” to burn the .iic file into the EEprom.

4.3.2 VC++ Graphic User Interface

The last step of communicating with the WINeR receiver Cypress USB interface is to build the VC++ GUI. We used Microsoft Visual Studio 2005 VC++ software to create the MFC Application GUI project, which allowed us to build a dialog mode USB interface. By linking the CYAPI.lib library to this project, we can use the CYUSB.SYS USB driver, which can significantly simplify the code. The most important functions that we need to use are “**CCyUSBDevice()**” and “**XferData()**”. The first one is used to create an Cypress USB class. The second one is used to transfer data with the USB synchronously. For asynchronous data transfer you can use “**BeginDataXfer() / WaitForXfer() / FinishDataXfer()**”.

When the user clicks on the “OK” button in the GUI, the program starts to

communicating with the WINeR USB device. It first looks for the WINeR USB device, and shows the information in the “USB Connection Info” area. Then it checks the Endpoints configuration. If it can find both the “in” and “out” Endpoints from the USB, it shows the “Endpoints founded” message in the “USB EndPoint Configuration” area. Otherwise, it will show an error. After allocating the Endpoints correctly, the program will continuously read in the buffered 16-bit digital data at a data rate that depends on the PWM frequency, for example, if the PWM is 640 kHz, then the throughput data rate will be 10.24Mbps. The GUI can also visualize the data in real-time and store it on the PC hard disk for further digital signal processing. A synchronization algorithm is implemented in the VC++ code. By always looking for the 4 constant monitoring channels (V_{DD} , V_{SS} , bandgap reference V_{BG} , and temperature voltage V_T), the received data can be synchronized and always begin with the 32 recording channels followed by the monitoring channels.

4.4 Measurement Results

4.4.1 WINeR Receiver Implementation

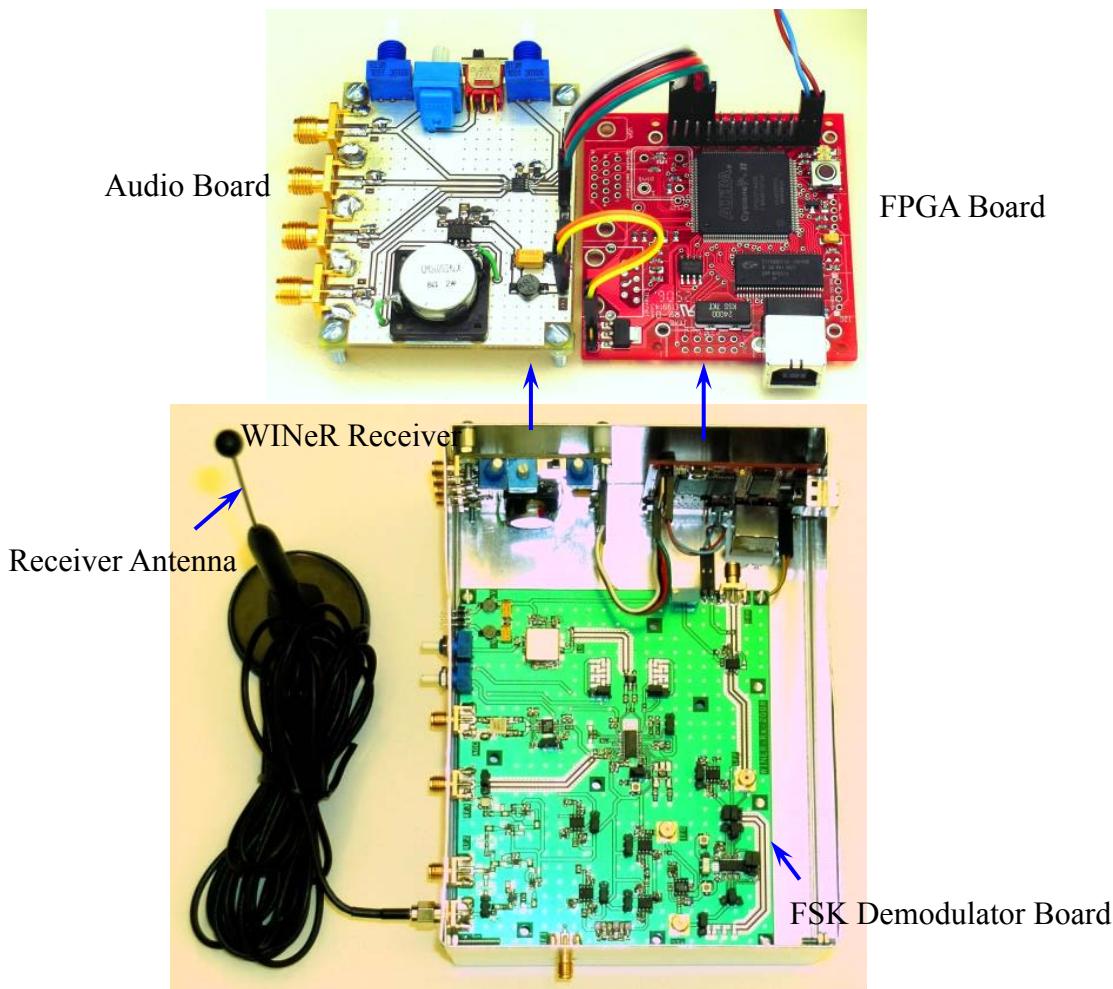


Figure 4. 6 Photograph of the WINeR receiver prototype.

The WINeR receiver FSK demodulator board is implemented in a custom-designed two-layer FR4 printed circuit board (PCB) with the size of $11\text{cm} \times 12.5\text{cm}$ (Figure 4. 6). It contains all the off-the-shelf components for the demodulator discussed earlier in Section

4.2.1. An 824~960MHz 5dBi magnetic base antenna (ANT-ELE-S01-006, Linx Technologies, Inc., Merlin, OR) is used for the WINeR receiver. The demodulator board consumes 100 and 280 mA from -5 and 5 V supplies, respectively, and dissipates a total power of 1.9 W. The TDC, SDRAM/USB, and audio DAC control modules are implemented in a 4608-logic-cell Altera FPGA (EP2C5T144C8, Altera Corporation, San Jose, CA) on a Xylo-EM board (KNJN, LLC, CA), shown in Figure 4. 6. The three modules only consume 928 logic cells (20%), 267 registers and 79pins on the FPGA. The Xylo-EM board also has a 2MB SDRAM and the Cypress EZ-USB chip, which are used for the data buffer and USB interface. The Xylo-EM board is powered through the 5V supply of the USB port and has an on-board 3.3V/5V regulator. The 3.3V output is used to power the audio board. The audio block is also implemented in a custom-designed two-layer FR4 PCB with the size of 5cm × 6.5cm (Figure 4. 6).

4.4.2 TDC Optimization and Measurements

Since the TDC noise directly adds to the overall system noise, therefore optimizing the TDC and its noise are very important for the WINeR system performance. According to the TDC architecture, shown in Figure 4. 2, the resolution of the FPGA counter is mainly dependent on the fine counter, which is further dependent on the delay (IC delay + cell delay) of each delay cell. The delay cells for the TDC were implemented as 4-input AND gates with

3 inputs tied to V_{DD} and one to the PWM signal, as shown in Figure 4. 2. The cell delays are fairly constant and only depend on the process. However, the IC delays can vary depending on the actually implementation of the delay cells. This could introduce noise to the TDC. To minimize the IC delay deviation, and consequently the TDC noise, all the delay cells were arranged in a manner that the deviations of the IC delays between successive delay cells were minimized. As shown in Figure 4. 7, we have managed the delay cells in proximity to each other and arranged them in sequence. Therefore, the IC delay between two adjacent delay cells is almost constant and equal to the minimum IC delay of the FPGA.

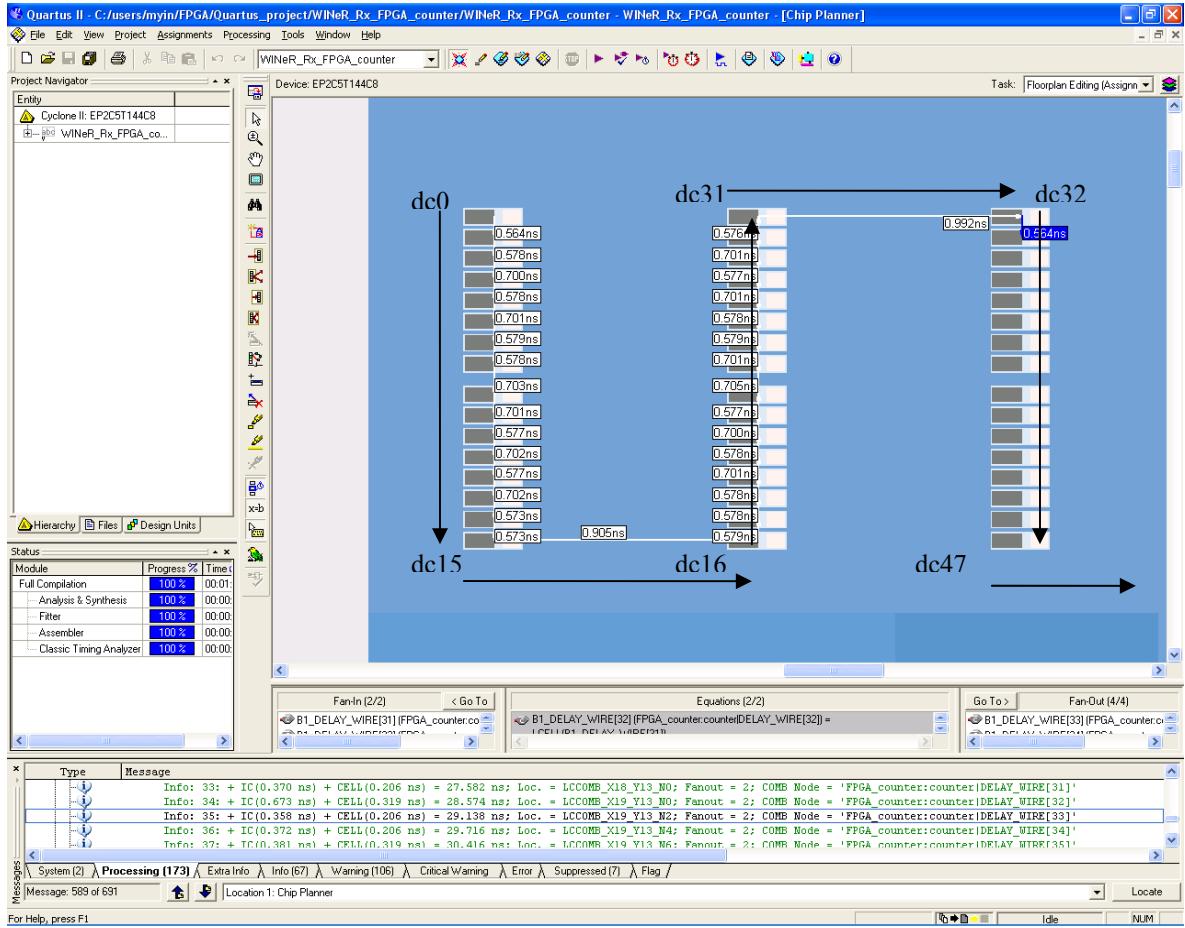


Figure 4. 7 Allocating the delay cell chain in the FPGA in order to minimize the IC delay deviations.

Measured delays at delay chain different taps, shown in Figure 4. 8a, indicate that $\tau \approx 304$ ps. Thus, $K = 68$ for $1/T_P = 48$ MHz. We implemented $N = 80$ delay cells in the chain to make sure that the total delay time was longer than the FPGA clock period. The time interval resolution from a data set of 128,000 measurements is shown in Figure 4. 8b. The time interval standard deviation of 600 ps represents a TDC time interval resolution of $600/\sqrt{2} = 424$ ps.

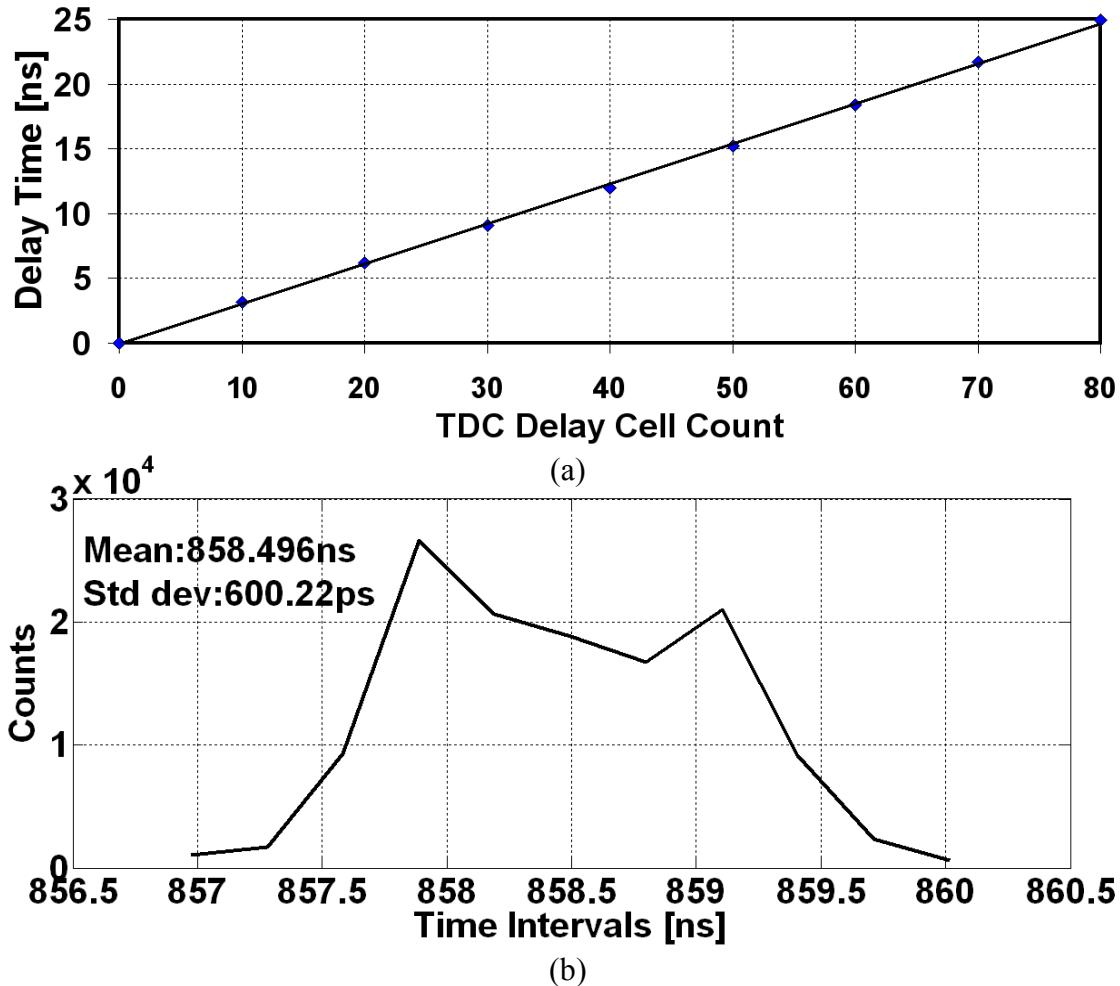


Figure 4.8 Performance of the TDC implemented in Altera FPGA. (a) Delay time as a function of the number of delay cells. (b) Time interval resolution.

4.4.3 WINeR ATC-TDC DNL and INL Measurements

To evaluate the WINeR-V analog-to-time convertor (ATC) and time-to-digital convertor (TDC) block wirelessly, we measured its DNL and INL. In this measurement, a constant voltage generated from a 12-bit Agilent function generator (33250A, Agilent Technologies, Inc., Santa Clara, CA) was used to overwrite Ch31 LNA output. By varying

the constant voltage from -1.5V to 1.5V, the PWM signal generated from that channel was varying according to the value of the constant voltage. Therefore, by receiving the 16-bit digitized value of the pulse width from the same channel on the receiver side, we can evaluate the ATC-TDC block.

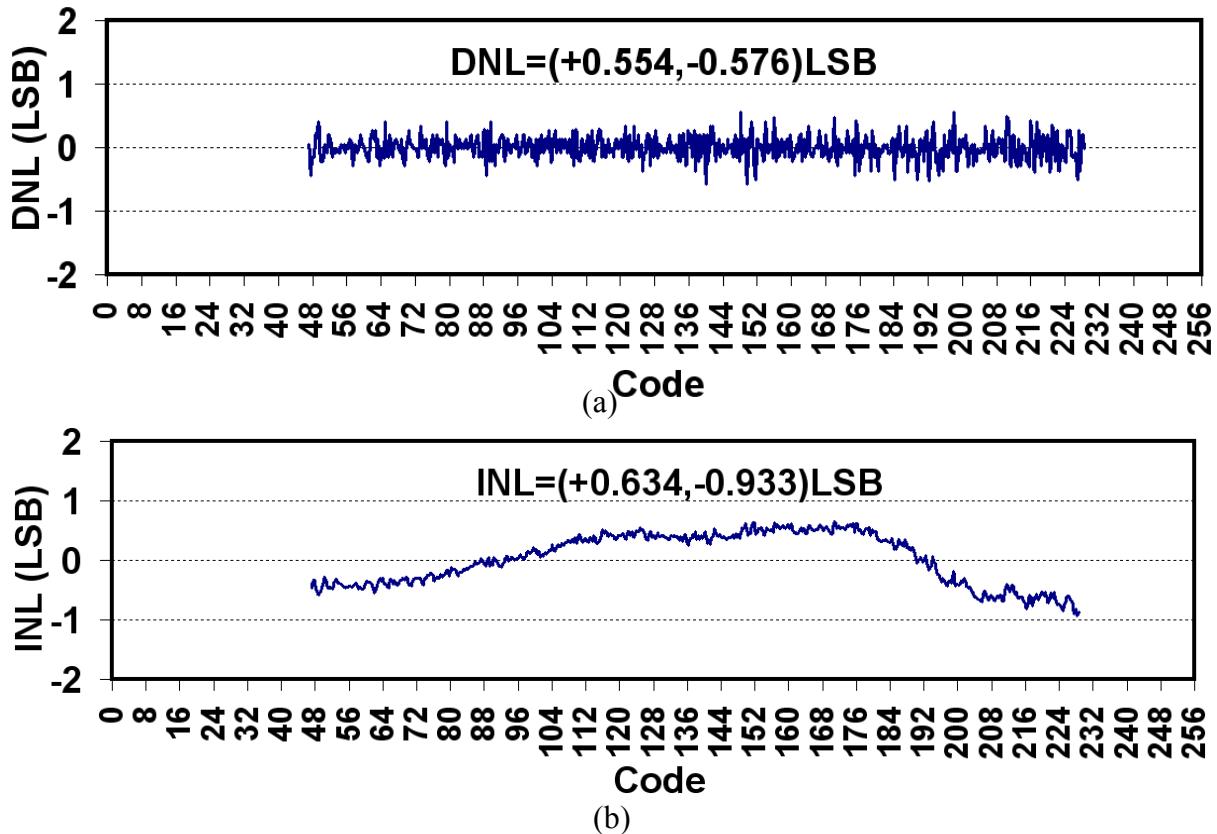


Figure 4.9 DNL (a) and INL (b) measurements for the WINeR-V ATC-TDC block.

As shown in Figure 4.9, the measured DNL and INL for the ATC-TDC block are $(+0.554, -0.576)$ LSB and $(+0.634, -0.933)$ LSB, respectively. The pulse trimming and synchronization (PTS) block will enforce the pulse width having minimum and maximum

values, as discussed in Section 3.2.4. During this measurement, when the constant voltage fell below -1.0V or went above 1.2V, the pulse width will be constant and equal to its minimum and maximum values. Consequently for those codes (<45 or >230), the INL and DNL are not applicable.

4.4.4 WINeR Receiver Bench-top Testing

The WINeR receiver was bench-top tested along with the 32-channel WINeR-V transmitter the same way as discussed in Section 3.3.5. The transmitted FSK-TDM-PWM carrier was picked up at ~1 m from the WINeR-V ASIC by our custom-designed wideband receiver. The received FSK-TDM-PWM spectrum at the receiver mixer input is shown in Figure 4. 10.



Figure 4. 10 Received FSK spectrum around 900MHz at the input of the mixer block.



Figure 4. 11 WINeR-V receiver waveforms. From top: 1. IF-TDM-PWM, 2. Rectified IF-TDM-PWM, 3. Baseband TDM-PWM, 4. Recovered TDM-PWM signals at 640 kHz, 5. LNA output, and 6. Receiver DAC output.

The receiver RF front-end amplified and down-converted the FSK-TDM-PWM signal to 42/70 MHz IF-TDM-PWM (trace 1 in Figure 4. 11), and further rectified (trace 2 in

Figure 4. 11) and filtered it to a baseband TDM-PWM signal (trace 3 in Figure 4. 11) with 18 MHz bandwidth. It was then translated to TTL levels (trace 4 in Figure 4. 11), and sent to the FPGA-based TDC for digitization. The 16-bit digitized samples were buffered in SDRAM and sent to a PC through its USB port. 4 out of the 36 channels for the 16-bit digital data are converted to analog signal, traces 5 and 6 in Figure 4. 11 are the transmitter side LNA output of an artificial cardiac signal, and its corresponding reconstructed signal in the receiver side at the DAC output.

The experiment for measuring the entire system latency was conducted by measuring the delay time between the LNA output and the audio DAC output. As shown in Figure 4. 12, a 2 mVp-p square wave with the frequency of 100Hz is applied to the input. The delay is measured from the LNA output to the receiver DAC output from a same channel (Ch15). According to these results the system latency from the transmitter LNA to the receiver DAC is only $\sim 1\mu\text{s}$.



Figure 4.12 WINeR system latency measurements. (a) Rising edge system latency is around 1 μ s. (b) Falling edge system latency is also around 1 μ s.

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CHAPTER 5 System Noise Analysis

5.1 Introduction

The WINeR system noise level is a key factor in determining its system resolution and accuracy. The noise of the WINeR system is directly related to the total pulse width noise that is seen at the 16-bit digital output on the receiver. In this chapter we will evaluate the wireless PWM technique for wireless neural recording applications by exploring its potential sources of noise and inaccuracy. Our goal is to indicate the SNR on the receiver side as well as the overall WINeR system resolution.

Depending on the location of the noise sources, the WINeR noise can be divided into two major categories: a) the implantable transmitter side noise and b) the external receiver side noise. Transmitter noise includes 3 major sources: 1) the front-end amplifier noise, 2) the PWM block noise, which includes noise in generating the triangular waveform and the PWM comparator noise, and 3) the VCO phase noise. On the receiver side, there are five major noise sources: 1) the thermal noise of the RF stage, 2) the noise due to the receiver bandwidth limitation, 3) LO phase noise, 4) TDC noise, and 5) the received signal strength variation noise.

5.2 Transmitter Side Noise

Since WINeR operates based on TDM-PWM, we express all noise sources in terms of duty cycle error so that we can easily compare them with each other and indicate the dominant sources of noise. The pulse duty cycle can be calculated according to (5.1) base on the pulse width w and pulse period T .

$$D = \frac{w}{T} \quad (5.1)$$

Then the pulse duty cycle error ΔD can be written as:

$$\Delta D = \Delta \left(\frac{w}{T} \right) \approx \frac{\Delta w}{T} = \frac{T_n}{T} \quad (5.2)$$

where T_n is the pulse width jitter due to various sources of noise.

Except for the VCO noise, the rest of the transmitter side noise is similar to the time-base ADC noise that is discussed in [5.1]. In the following, detailed noise analysis for each part mentioned in Section 5.1 will be presented.

5.2.1 Neural Amplifier Noise

As we have shown in Section 3.3.2, the input referred noise of the LNA was $3.9\mu\text{V}_{\text{rms}}$. As stated above, we convert the LNA noise into pulse width noise by using the

following equation

$$\Delta D = \frac{T_{n,LNA}}{T} = \frac{V_{n,input,LNA} Gain_{LNA}}{V_{out_swing,LNA}} = 0.0031 \quad (5.3)$$

where $V_{n,input,LNA}$ is the input referred noise of the LNA, $Gain_{LNA}$ is the total gain of the LNA, $V_{out_swing,LNA}$ is the LNA 2nd stage output swing, T is the PWM period, $T_{n,LNA}$ is the pulse width error due to the LNA noise contribution, ΔD is the PWM duty cycle error caused by the LNA noise.

5.2.2. Pulse Width Modulator Noise

The PWM noise includes both the TWG noise and the PWM comparator noise. The transfer function of the PWM block (Figure 3. 4) is

$$w = CV_{in} \left(\frac{1}{I_{Source}} + \frac{1}{I_{Sink}} \right) \quad (5.4)$$

By taking the derivative of (5.4), and plugging it in (5.2), we can find the pulse duty cycle jitter, which can be expressed as

$$\Delta D = \frac{dw}{T} = \left(\frac{CV_{in}}{T} \left(\frac{1}{I_{Source}} + \frac{1}{I_{Sink}} \right) \frac{dC}{C} - \frac{CV_{in}}{T} \left(\frac{dI_{Source}}{I_{Source}^2} + \frac{dI_{Sink}}{I_{Sink}^2} \right) \right) + \frac{C}{T} \left(\frac{1}{I_{Source}} + \frac{1}{I_{Sink}} \right) dV_{in} \quad (5.5)$$

According to (5.1) and (5.4), we have

$$D = \frac{w}{T} = \frac{CV_{in}}{T} \left(\frac{1}{I_{Source}} + \frac{1}{I_{Sink}} \right) \quad (5.6)$$

At the same time, the pulse period can be expressed as

$$T = C(V_{high} - V_{low}) \left(\frac{1}{I_{Source}} + \frac{1}{I_{Sink}} \right) \quad (5.7)$$

where V_{high} and V_{low} are the upper and lower limits of the triangular waveform, as discussed in Section 3.2.3. By plugging (5.6) and (5.7) in (5.5), we obtain

$$\Delta D = \frac{dw}{T} = D \left(\frac{dC}{C} - \frac{I_{Sink} I_{Source}}{I_{Source} + I_{Sink}} \left(\frac{dI_{Source}}{I_{Source}^2} + \frac{dI_{Sink}}{I_{Sink}^2} \right) \right) + \frac{dV_{in}}{V_{high} - V_{low}} \quad (5.8)$$

where T is the sampling period and $D=w/T$ is the PWM duty cycle. Variations in the TWG capacitor, C , are often very small. dV_{in} is the equivalent input referred noise of the comparator. Since the noise on V_{high} and V_{low} will also affect dw , all comparator noises need to be considered. dI_{Source} and dI_{Sink} are the noise contributions of the CCSS (Figure 3. 8). Although the finite output impedance of the CCSS also contributes to dw , it mostly causes distortion, which can be considered in calibration.

Considering the comparators used for the CCSS and the pulse width modulation are identical, we assume that they have the same input referred noise of $V_{n,comp-in}^2$. Therefore

according to (5.8) the pulse width jitter energy can be obtained as

$$\Delta D^2 = \frac{w_{n,PWM}^2}{T^2} = \frac{D^2 I_{Sink}^2 I_{Source}^2}{(I_{Source} + I_{Sink})^2} \left(\frac{i_{n,Source}^2}{I_{Source}^4} + \frac{i_{n,Sink}^2}{I_{Sink}^4} \right) + \frac{3V_{n,comp-in}^2}{(V_{high} - V_{low})^2} \quad (5.9)$$

where $i_{n,Source}^2$ and $i_{n,Sink}^2$ are the current noise for the CCSS current source and sink, respectively. The factor “3” in the comparator noise is because there are two comparators in the TWG, and one used in the PWM comparison. In order to evaluate the PWM noise quantitatively, we need to look into the transistor level of the PWM block to find $i_{n,Source}^2$, $i_{n,Sink}^2$ and $V_{n,comp-in}^2$.

i. CCSS Noise

For our noise analysis of the PWM block, the $1/f$ noise in the transistors is negligible, since it behaves like a nearly constant offset across each sampling time and is cancelled [5.1]. For the following discussion, we model the MOSFET’s current source thermal noise as

$$I_n^2(f) = 4\gamma k T g_m \Delta f \quad (5.10)$$

where k is the Boltzmann’s constant, T is absolute temperature, g_m is the transconductance of the MOSFET, Δf is the bandwidth, and $\gamma = 2/3$ for above-threshold operation, $\gamma = 1/2$ for subthreshold operation [5.1]. Using (5.10), by reviewing the schematic of the CCSS in Figure

3. 8, we can show that both current source and sink output current noise can be expressed as:

$$i_{n,source/sink}^2 \approx \frac{\gamma kT}{r_o C} \left[\left(\frac{4g_m g_{msl}^2}{g_{m5}^2} + \frac{2g_{msl}^2}{g_{m5}} + g_{msl} \right) \right]_{source/sink} \quad (5.11)$$

ii. Comparator Noise

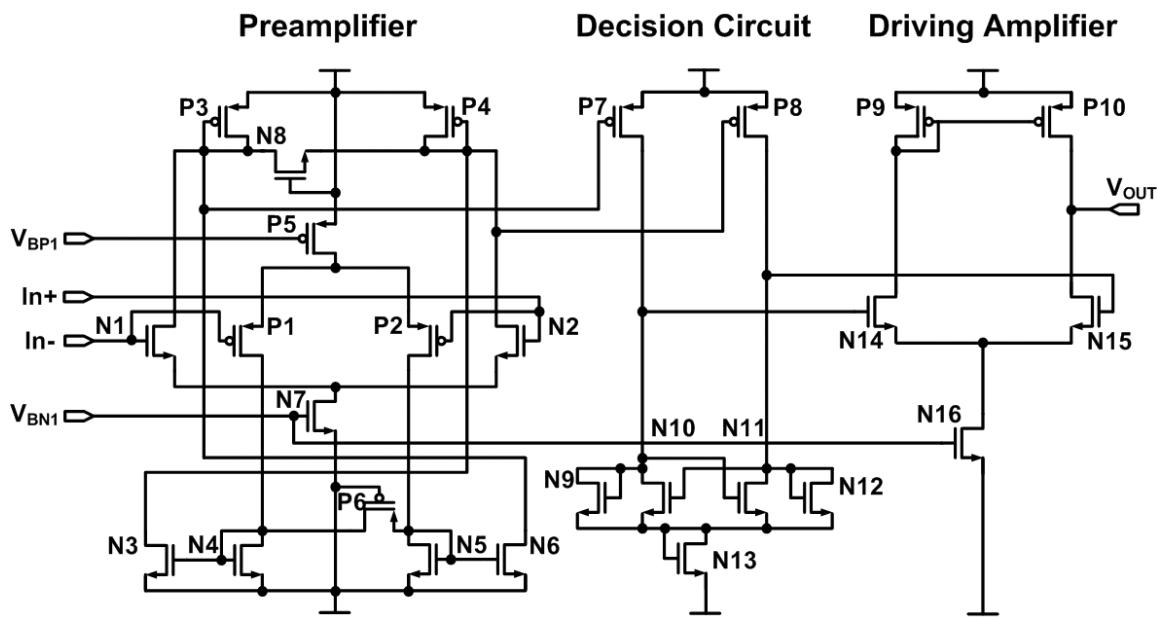


Figure 5.1 Comparator schematic.

The comparator has three stages: preamplifier, decision circuit, and driving amplifier (Figure 5. 1).

(a) Preamplifier

The first stage of the comparator is a fully differential amplifier with nearly rail-to-rail input common mode range. It provides low-gain around 10 and isolation for the

input from the second stage of the comparator. We can obtain the total input referred noise for the preamplifier from:

$$V_{n,pa}^2 \approx \frac{2kT\gamma}{r_{o,pa}C_{L,pa}} \left[\frac{1}{g_{m,p1}} + \frac{g_{m,p3}}{g_{m,n1}^2} + \frac{1}{g_{m,n1}} + \frac{2g_{m,n2}}{g_{m,p1}^2} \right] \quad (5.12)$$

where $g_{m,ni}$ and $g_{m,pi}$ are the transconductances of the associated transistors in Figure 5. 1. $r_{o,pa}$ and $C_{L,pa}$ are the output impedance and load capacitance of the preamplifier, respectively.

(b) Decision Circuit

The decision circuit consists of a positive feedback operational transconductance amplifier (OTA). During operation, only half of the OTA is contributing noise and consuming most of the tail current. The total voltage noise seen at the output of the decision circuit is:

$$V_{n,dc}^2 \approx \frac{kT\gamma}{g_{m,n9}C_{L,dc}} [g_{m,p7} + g_{m,n9} + g_{m,n10} + g_{m,n13}] \quad (5.13)$$

where $C_{L,dc}$ is the load capacitance of the decision circuit. This noise will be added to the input of the driving amplifier stage and contributes to the output noise of the comparator.

(c) Driving Amplifier

The driving amplifier in Figure 5. 1 is a 5 transistor differential to single-ended amplifier. Due to the status of the input signals at the output of the decision circuit, only half of the driving amplifier is on and contributing to the noise. The total output noise presented

at the output of the comparator is:

$$V_{n,da}^2 = \frac{kT\gamma}{r_{o,da}C_{L,da}} \left(\frac{g_{m,n15} + g_{m,p10}}{g_{m,p10}^2} \right) \quad (5.14)$$

where $r_{o,da}$ and $C_{L,da}$ are the output impedance and load capacitance of the driving amplifier, respectively.

Now by summing up the sub-circuit noises in the comparator, we can find the total comparator noise

$$V_{n,comp-in}^2 = V_{n,pa}^2 + \frac{V_{n,dc}^2}{A_{pa}^2 A_{dc}^2} + \frac{V_{n,da}^2}{A_{pa}^2 A_{dc}^2 A_{da}^2} \quad (5.15)$$

where A_{pa} , A_{dc} , and A_{da} are the gains of the preamplifier, decision circuit and driving amplifier, respectively. Since $A_{pa}A_{dc} \gg 1$, then the total comparator input referred noise is almost equal to the preamplifier input referred noise. Then by plugging (5.6) and (5.10) into (5.4), we can calculate the total pulse width noise for the PWM block as:

$$\Delta D = \frac{w_{n,PWM}}{T} = \sqrt{\frac{D^2 I_{Sink}^2 I_{Source}^2}{(I_{Source} + I_{Sink})^2} \left(\frac{i_{n,Source}^2}{I_{Source}^4} + \frac{i_{n,Sink}^2}{I_{Sink}^4} \right) + \frac{3V_{n,comp-in}^2}{(V_{high} - V_{low})^2}} \approx 0.0011 \quad (5.16)$$

5.2.3 VCO Noise

VCO is the only block that should be driven by the PWM comparator to create a FSK-TDM-PWM carrier in the ISM band. In this process, the PWM spectrum is shifted from baseband to FSK frequencies, f_1 and f_2 , as shown in Figure 5. 2.

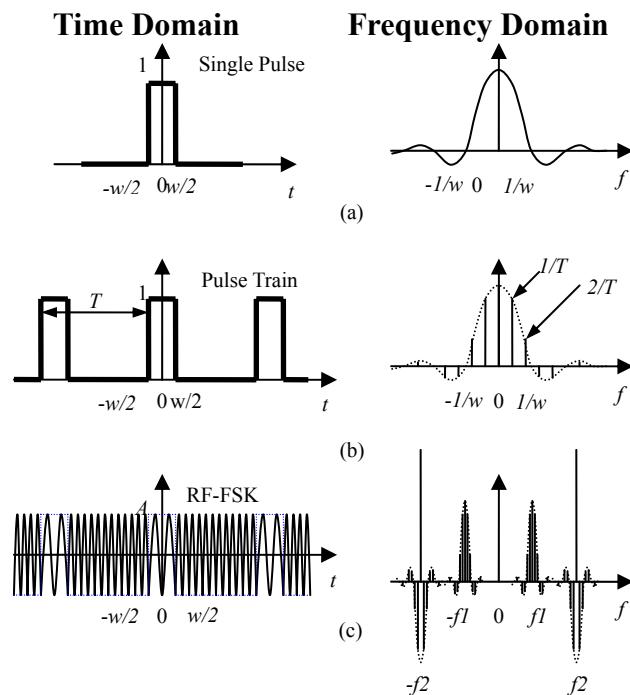


Figure 5. 2 Transmitter side FSK-TDM-PWM signal in time and frequency domains.

A single pulse with width w can be described in time and frequency domains as (Figure 5. 2a)

$$\Pi\left(\frac{t}{w}\right) = \begin{cases} 0, & |t| > \frac{w}{2} \\ 1, & |t| < \frac{w}{2} \\ \frac{1}{2}, & |t| = \frac{w}{2} \end{cases}, \quad F\left[\Pi\left(\frac{t}{w}\right)\right] = \frac{\sin \pi f w}{\pi f}. \quad (5.17)$$

For a simple analysis, let's assume V_{in} is constant and the PWM period is T . The analysis for more complicated PWM signals with variable pulse width can be found in [5.2]. Using (5.17), the PWM pulse train can be written as (Figure 5. 2b)

$$PWM(t) = \sum_{n=-\infty}^{+\infty} \Pi\left(\frac{t-nT}{w}\right) \quad PWM(f) = \sum_{n=-\infty}^{+\infty} \frac{\sin \pi \frac{n w}{T}}{\pi \frac{n}{T}} \delta\left(f - \frac{n}{T}\right) \quad (5.18)$$

where $\delta(f)$ is the delta function. The FSK-PWM spectrum can then be found by shifting (5.18) to $\pm f_1$ and $\pm f_2$ (Figure 5. 2c)

$$FSK - PWM(t) = \sum_{n=-\infty}^{+\infty} \Pi\left(\frac{t-nT}{w}\right) A \cos 2\pi f_1 t + \left(1 - \sum_{n=-\infty}^{+\infty} \Pi\left(\frac{t-nT}{w}\right)\right) A \cos 2\pi f_2 t$$

$$FSK - PWM(f) = \frac{A}{2} \sum_{n=-\infty}^{+\infty} \delta\left(f \pm f_1 - \frac{n}{T}\right) \frac{\sin \pi \frac{n w}{T}}{\pi \frac{n}{T}} - \frac{A}{2} \sum_{n=-\infty}^{+\infty} \delta\left(f \pm f_2 - \frac{n}{T}\right) \frac{\sin \pi \frac{n w}{T}}{\pi \frac{n}{T}} + \frac{A}{2} \delta(f \pm f_2) \quad (5.19)$$

In the frequency domain, the VCO output will be the convolution of (5.19) and the VCO phase noise spectrum, $S_\phi(f)$, at an offset frequency, f , away from the carrier. After receiving, down-converting, and filtering of the FSK-PWM-TDM, if we ignore the bandwidth

limitation for the time being, the restored signal in the time domain will be the ideal PWM pulses in (5.18), shaped by the phase noise function

$$PWM_{Rx}(t) = \sum_{n=-\infty}^{+\infty} \Pi\left(\frac{t-nT}{w}\right) F^{-1}[S_\Phi(f)] \quad (5.20)$$

For white noise sources, frequency stability of the VCO is often characterized by the relative jitter [5.3]

$$S_\Phi(f) \equiv \frac{f_{osc}}{f^2} \left(\frac{\Delta\tau_{rms}}{T_{osc}} \right)^2 \quad (5.21)$$

where $\Delta\tau_{rms}$ is the rms jitter, f_{osc} and T_{osc} are VCO carrier frequency and period. Using (5.21) it is easy to prove that

$$\left(\frac{\Delta f_{rms}}{f_{osc}} \right)^2 = \left(\frac{\Delta\tau_{rms}}{T_{osc}} \right)^2 = S_\Phi(f) \frac{f^2}{f_{osc}} \quad (5.22)$$

The VCO phase noise results in a frequency noise of Δf_{rms} , which after frequency demodulation turns into an rms voltage noise, ΔV_{rms} . Due to the rising and falling slopes of the recovered PWM signal, ΔV_{rms} causes a pulse width error of ΔT_{VCO} , which can be found from

$$\frac{\Delta T_{VCO}}{T_{f/r}} = \frac{\Delta V_{rms}}{V_{pp}} = \frac{\Delta f_{rms}}{f_2 - f_1} \quad (5.23)$$

where $T_{f/r}$ is the sum of rise and fall times and V_{pp} is the peak to peak voltage of the recovered PWM signal. Using (5.22) and (5.23), the pulse width duty cycle error will be

$$\Delta D = \frac{\Delta T_{VCO}}{T} = \frac{f T_{f/r} \sqrt{S_\Phi(f) f_{osc}}}{T(f_2 - f_1)} \quad (5.24)$$

where f is the offset frequency at which VCO phase noise has been measured. It can be seen that increasing the FSK modulation index and reducing $T_{f/r}$ can help reduce the VCO error. Gradual VCO drift does not affect the FSK-PWM signal because it does not affect the pulse width. VCO settling time, however, is an important parameter determined by the VCO bandwidth and phase margin, which in turn depend on the VCO tail current, LC tank quality factor, and loading.

Our measurements showed that the WINeR-V VCO two FSK frequencies are $f_1=898\text{MHz}$ and $f_2=926\text{MHz}$. $f_{osc} \approx 900 \text{ MHz}$ has a phase noise of $S_\Phi(10 \text{ kHz}) = -88.17 \text{ dBc/Hz}$. At the sampling rate of $f_{PWM} = 640 \text{ kHz}$, the PWM period T is equal to $1.5625\mu\text{s}$. When RBW = 18 MHz, $T_{f/r} = 75 \text{ ns}$ for the recovered PWM. Plugging these numbers in (5.24) results in $\Delta D \approx 10^{-5}$, which is far less than the other sources of noise. Therefore, we can

safely conclude that the VCO does not have a dominant effect on the WINeR system accuracy.

5.3 Receiver Side Noise

5.3.1 Thermal Noise

Maximum noise power transfer happens when there is impedance matching between successive blocks. This is usually the case in commercial devices since they are mostly designed for 50Ω . Matching between the receiver antenna and front-end RF LNA results in the transferred noise power of

$$P_n = kT\Delta f \quad (5.25)$$

where Δf is the receiver bandwidth. At room temperature, in dBm, (5.25) becomes

$$P_{n,dBm} = [-174 + 10 \log(\Delta f)] dBm \quad (5.26)$$

Considering the signal path on the receiver side, as shown in Figure 5. 3, every stage has a thermal noise characterized by its noise factor, F , and noise figure $NF = 10 \log(F)$. If several stages with the gains of G_1, G_2, \dots, G_n and noise factors of F_1, F_2, \dots, F_n are connected in series, then

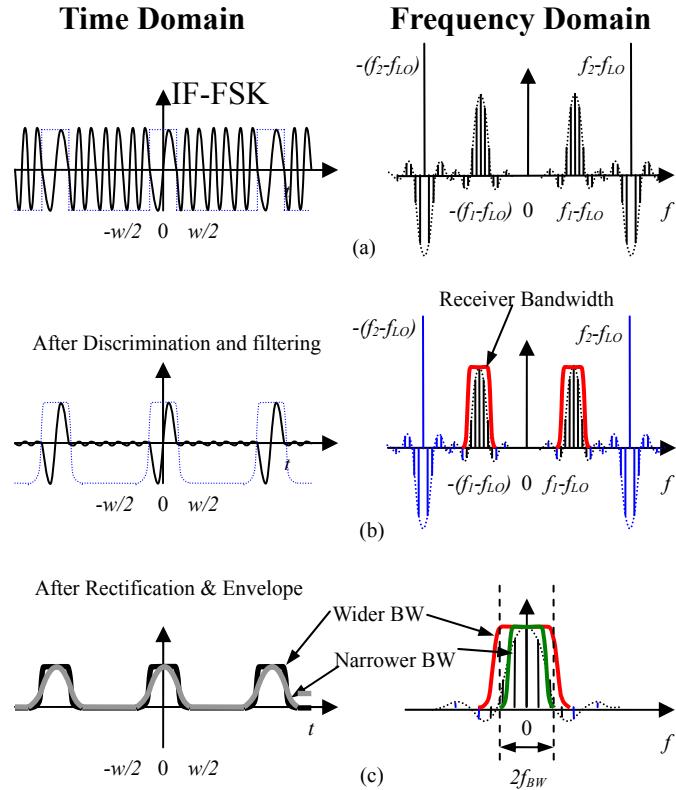


Figure 5.3 Receiver side TDM-PWM signal in time and frequency domains.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_n} \quad (5.27)$$

If the first two stages have a high gain, considering the first 3 terms would be sufficient. The thermal noise received by a receiver with 50Ω input impedance, connected to an antenna with a 50Ω radiation resistance would be

$$P_{n,Rx,dBm} = P_{n,dBm} + 10 \log(F - 1) = [-174 + 10 \log(\Delta f) + 10 \log(F - 1)] dBm \quad (5.28)$$

If the input signal RF power (P_{sig}) is known, we can find the SNR for each stage. For PWM signal, the SNR is the reciprocal of pulse width duty cycle error.

$$SNR_{PWM} = \left(\frac{T}{\Delta w} \right)^2 = \frac{1}{\Delta D^2} \quad (5.29)$$

Hence, the total receiver thermal noise contribution to the pulse width duty cycle error is

$$\Delta D = \sqrt{\frac{1}{SNR_{PWM}}} = 10^{(P_{n,Rx,dBm} - P_{sig,Rx,dBm})/20} = 10^{\left[-174 + 10 \log(\Delta f) + 10 \log \left(F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} - 1 \right) - P_{sig,Rx,dBm} \right] / 20} \quad (5.30)$$

Considering the gains of the RF LNA and gain block are high, the thermal noise of the receiver demodulator will mostly be determined by the RF part. As mentioned earlier, the measured SNR at the receiver mixer input is 57.3dB at 1 meter distance from the transmitter (Figure 4. 10) with 640 kHz PWM frequency. Therefore according to (5.30), the pulse width duty cycle error will be

$$\Delta D = \sqrt{\frac{1}{SNR_{PWM}}} = 10^{-57.3/20} = 0.0014 \quad (5.31)$$

5.3.2 Local Oscillator Phase Noise

The amplified RF-TDM-PWM signal is down-converted to IF-TDM-PWM by multiplication with a local oscillator (f_{LO}). The resulting signal will be similar to (5.19) when

shifting the carrier frequencies from f_1 and f_2 to f_1-f_{LO} and f_2-f_{LO} (Figure 5. 3a), and the error analysis will be similar to the VCO in Section 5.2.3.

The LO used in the WINeR receiver is a commercial Z-Comm VCO, which has a phase noise value of -100dB/Hz (@10 kHz), i.e. $S_\phi(10\text{kHz})=-100\text{dB}/\text{Hz}$. Our two FSK frequencies are $f_1=898\text{MHz}$ and $f_2=926\text{MHz}$. Meanwhile when using 18MHz lowpass filter setting, the measured baseband PWM rising and falling edge, T_{rf} , is 75ns, the PWM period $T_{PWM}=1.5625\mu\text{s}$. According to (5.24), the pulse width duty error will be

$$\Delta D = \frac{T_{f/r} \sqrt{S_\phi(f) f^2 f_{osc}}}{T(f_2 - f_1)} = \frac{75 \times 10^{-9} \times \sqrt{10^{-100/10} \times (10000)^2 \times 915 \times 10^6}}{1.5625 \times 10^{-6} \times 28 \times 10^6} = 5.2 \times 10^{-6} \quad (5.32)$$

The result shows for the WINeR system using a wide band FSK, the LO (even the VCO) phase noise, has minimum contribution to the system noise, and can be safely ignored.

5.3.3 Receiver Bandwidth Limitation

Since edges of the recovered PWM signal become rounded due to receiver bandwidth (RBW) limitation, pulse width error is introduced to the system. We simplify our analysis by considering the receiver as an ideal low pass filter with cutoff frequency of f_{BW} , which truncates the PWM spectrum from $-f_{BW}$ to f_{BW} range. Figure 5. 3 shows the received IF and baseband PWM signal in time and frequency domains. Mathematically, the complete

PWM spectrum in (5.18) is multiplied by the receiver low pass filter

$$PWM_{Rx}(f) = \sum_{n=-\infty}^{+\infty} A \frac{\sin \pi \frac{nW}{T}}{\pi \frac{n}{T}} \frac{\delta\left(f \pm \frac{n}{T}\right)}{2} \Pi\left(\frac{f - f_{BW}}{2f_{BW}}\right) = \sum_{n=-M}^{+M} A \frac{\sin \pi n D}{\pi \frac{n}{T}} \frac{\delta\left(f \pm \frac{n}{T}\right)}{2} \quad (5.33)$$

where $f_{BW}T - 1 < M$ (integer) $\leq f_{BW}T$, and A is the amplitude of the received pulses. To find the pulse width error due to the RBW limitation, we converted (5.33) back to the time domain using inverse Fourier transform

$$PWM_{Rx}(t) = \sum_{n=-M}^{+M} A \frac{\sin \pi n D}{\pi \frac{n}{T}} \cos \frac{2\pi n t}{T} \quad (5.34)$$

By setting a threshold at $A/2$, and solving $PWM_{Rx}(t) = A/2$ for t , we can find the recovered pulse width, $w_{Rx} = 2t$, and duty cycle $D_{Rx} = w_{Rx}/T$. It should be noted that if $M \rightarrow \infty$, i.e. unlimited RBW, then $2t = w$ and $D_{Rx} = D$. From (5.34) we have

$$\sum_{n=-M}^{+M} \frac{\sin \pi n D \cos \pi n D_{Rx}}{\pi \frac{n}{T}} = \frac{1}{2} = \sum_{n=-\infty}^{+\infty} \frac{\sin \pi n D \cos \pi n D}{\pi \frac{n}{T}} \quad (5.35)$$

Subtracting $\sum_{n=-M}^{+M} \frac{\sin \pi n D \cos \pi n D}{\pi \frac{n}{T}}$ from both side yields

$$\sum_{n=-M}^{+M} \frac{\sin \pi n D (\cos \pi n D_{Rx} - \cos \pi n D)}{\pi \frac{n}{T}} = \sum_{|n|>M} \frac{\sin \pi n D \cos \pi n D}{\pi \frac{n}{T}} \quad (5.36)$$

which simplifies to

$$\sum_{n=-M}^{+M} \frac{\sin \pi n D \left(2 \sin \pi n \frac{D_{Rx} + D}{2} \cdot \sin \pi n \frac{D_{Rx} - D}{2} \right)}{\pi \frac{n}{T}} = \sum_{|n|>M} \frac{\sin 2\pi n D}{2\pi \frac{n}{T}} \quad (5.37)$$

Defining $D_{Rx} - D = \Delta D$, and assuming $\pi n \Delta D \ll 1$, where $n \leq M$, then

$$\sum_{n=-M}^{+M} (\sin \pi n D)^2 \Delta D = \sum_{n=-M}^{+M} \frac{1 - \cos 2\pi n D}{2} \Delta D = \sum_{|n|>M} \frac{\sin 2\pi n D}{2\pi n} \quad (5.38)$$

Using (5.38), the RBW duty cycle error can be found from

$$\Delta D = \frac{\sum_{|n|>M} \frac{\sin 2\pi n D}{2\pi n}}{\sum_{n=-M}^{+M} \frac{1 - \cos 2\pi n D}{2}} = \Delta D(M, D) \quad (5.39)$$

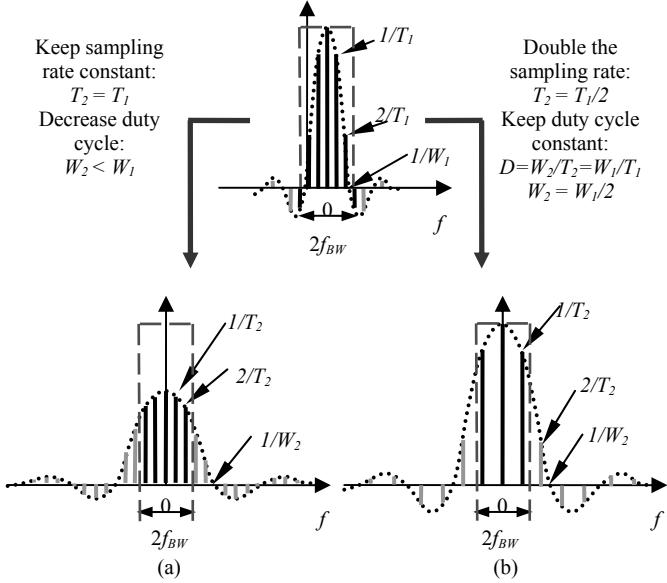


Figure 5.4 Effects of RBW limitation on the spectrum of recovered PWM signal. (a) Constant sampling frequency with reduced PWM duty cycle. (b) Constant PWM duty cycle with increased sampling frequency.

The numerator of (5.39) consists of the even terms of the PWM Fourier series that are left outside of the RBW, and decreases with increasing the RBW (see Figure 5. 3). The denominator of (5.39) increases with M, which is proportional to RBW. Hence, ΔD decreases with increasing RBW. ΔD also depends on D and consequently on T as shown in Figure 5. 4. For a fixed sampling period, T, if D decreases (i.e. $W_2 < W_1$ in Figure 5. 4a), the PWM spectrum spreads further out by a reduction in the amplitude of its in-band components. Therefore, if the RBW is fixed, more terms will be outside of the RBW and ΔD increases. A similar situation can occur if $D \rightarrow 1$. Because in that case, the denominator of (5.39) becomes very small, resulting in higher ΔD . This makes sense because when $D \rightarrow 1$ the “low” pulses in PWM signal become quite narrow. Therefore, we need to limit $0 < D < 1$

from both ends.

Increasing the sampling rate without increasing the RBW can also have a detrimental effect on ΔD even if D is kept constant. This is demonstrated in Figure 5. 4b, where sampling rate is doubled ($T_2 = T_1/2 \rightarrow M_2 = M_1/2$). This means that there will be more terms of the PWM spectrum outside RBW, which lead to a larger numerator in (5.39) and higher ΔD .

In Figure 5. 5, we have plotted ΔD vs. D based on (5.39) for various RBWs from 5 to 75 MHz, and sampling frequencies of 320 and 640 kHz. In order to reduce ΔD , D has been limited to 10~90%. Table 5. 1 summarizes the theoretical worst case ΔD variations with RBW and D for 16-channel and 32-channel PWM-TDM systems, sampled at 20 kSps/ch. It can be seen that ΔD , which will eventually affect the overall resolution of the WINeR system in wireless PWM technique can be adjusted based on the number of active channels and sampling rate per channel. Therefore, unlike digital approaches, depending on the application and the nature of the biological signals, the WINeR user can establish a tradeoff between the accuracy of the system, bandwidth per channel, and total number of active channels, as shown in Table 5. 1. For our WINeR receiver, for example, For the 640 kHz PWM, 18MHz RBW setting, the value for M in (5.39) will be 28. By plugging M into (5.39), for pulse duty cycle as (0.1~0.9) and (1/6~5/6), the maximum duty cycle errors are 0.0006173 and

0.000384, respectively.

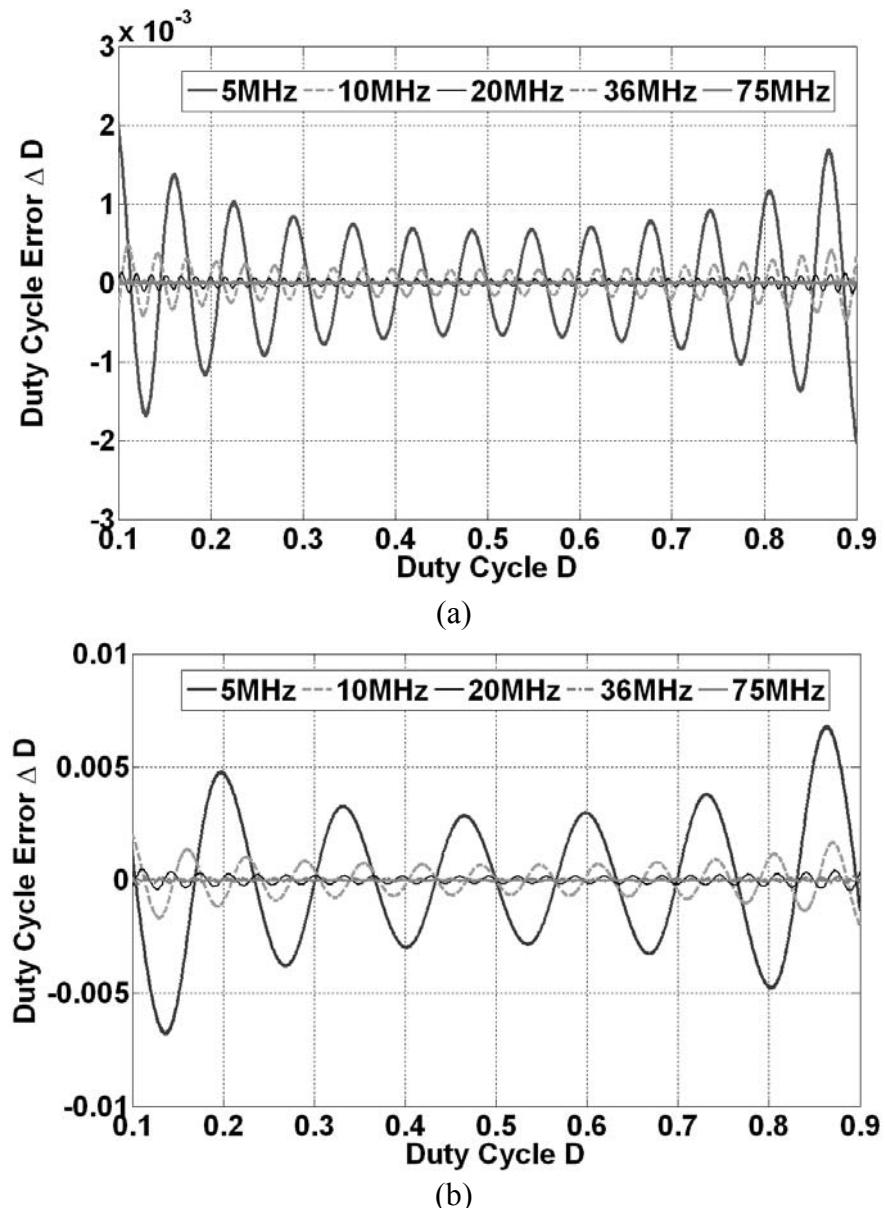


Figure 5.5 Theoretical PWM duty cycle error due to receiver bandwidth limits at RBW = 5, 10, 20, 36, 75 MHz for (a) 320 kHz and (b) 640 kHz sampling rates.

Table 5. 1 Dependence of PWM duty cycle error on sampling rate, PWM duty cycle, and receiver bandwidth.

f_{PWM}	D	ΔD vs. Receiver Bandwidth (RBW)						
		kHz	Range	5 MHz	10 MHz	20 MHz	36 MHz	75 MHz
320	0.1~0.9			2.0×10^{-3}	4.8×10^{-4}	1.3×10^{-4}	4.5×10^{-5}	1.1×10^{-5}
320	0.3~0.7			7.9×10^{-4}	2.0×10^{-4}	5.3×10^{-5}	1.8×10^{-5}	4.3×10^{-6}
640	0.1~0.9			6.8×10^{-3}	1.7×10^{-3}	4.8×10^{-4}	1.6×10^{-4}	3.8×10^{-5}
640	0.3~0.7			3.8×10^{-3}	7.9×10^{-4}	2.0×10^{-4}	6.4×10^{-5}	1.6×10^{-5}

5.3.4 Received Signal Strength Variation (RSSV)

In freely moving animal experiments, the RSSV could easily be introduced by the distance or orientation variations between the receiver and transmitter. It can also be caused by the surrounding environment changes of the transmitter and receiver pair. Although we have already included AGC in our receiver design, its ability to stabilize the signal strength is limited (0.5dB for AD8362). Therefore RSSV still exists. Generally speaking, the phase noise of the transmitter VCO and receiver LO will also introduce RSSV, because any frequency noise will convert into voltage noise, i.e. signal strength noise. But for clarity, we just discuss them separately. The RSSV could introduce noise to the pulse width signal when

the pulse rising and falling times are not zero. This is because according to Figure 5. 6, at the final stage of the receiver FSK demodulator, the baseband PWM signal needs to be compared with a threshold voltage and translated into a TTL level PWM before entering to the TDC. However, all RSSV noise will add to the baseband PWM. As shown in Figure 5. 6a, if the baseband PWM has zero rising and falling times, then as long as the RSSV noise amplitude does not exceed half of the baseband PWM amplitude, there will be no pulse width error introduced. Unfortunately, in real case, as shown in Figure 5. 6b the baseband PWM always has non-zero rising/falling times due to the limited bandwidth of the wireless link. If we assume the signal and RSSV noise amplitude of the baseband PWM are V and $\Delta V_{n,RSSV}$, respectively, and the total rising and falling times of the baseband PWM is T_{rf} , then the total pulse width noise caused by RSSV will be

$$\Delta t_{n,RSSV} = \frac{\Delta V_{n,RSSV}}{V} T_{r/f} \quad (5.40)$$

Therefore the PWM duty cycle error can be calculated as

$$\Delta D = \frac{\Delta t_{n,RSSV}}{T} = \frac{T_{r/f} \Delta V_{n,RSSV}}{TV} \quad (5.41)$$

Since the AGC used in the receiver can stabilize the received signal strength within 0.5dB, therefore for the baseband PWM, $\Delta V_{n,RSSV}/V=10^{0.5/20}-1=0.059$. After plugging this

value in (5.41), we can calculate the pulse width duty cycle error as

$$\Delta D = \frac{T_{r/f} \Delta V_{n,RSSV}}{TV} = \frac{75 \times 10^{-9} \times 0.059}{1.5625 \times 10^{-6}} = 0.0028 \quad (5.42)$$

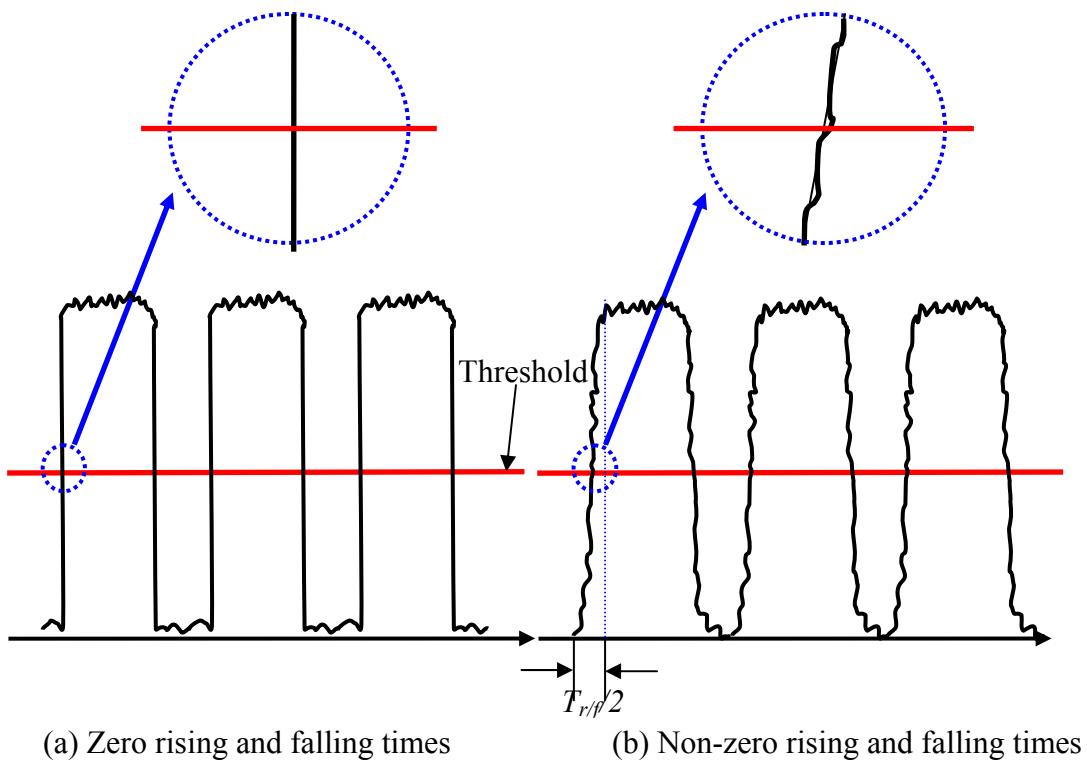


Figure 5.6 Explanation of pulse width noise cause by received signal strength variation for zero and non-zero rising and falling times pulse width signals.

5.3.5 TDC Noise

The estimation of the noise caused by the TDC is quite simple. Assuming that the TDC has a time resolution of $\Delta t_{n,TDC}$, therefore similar to Equation (5.42), we have

$$\Delta D = \frac{\Delta t_{n,TDC}}{T} \quad (5.43)$$

As we have mentioned before, the TDC has a measured time interval resolution ($\Delta t_{n,TDC}$) of 424 ps. Using (5.43), we have

$$\Delta D = \frac{\Delta t_{n,TDC}}{T} = \frac{0.424 \times 10^{-9}}{1.5625 \times 10^{-6}} = 0.00027 \quad (5.44)$$

5.4 Entire System Noise and Resolution

Table 5. 2 summarizes the noise contributions form different parts of the receiver according to the above analysis. In this table, the pulse duty cycle noises are converted to pulse width noise by multiplying the pulse width period $T_{PWM} = 1.5625\mu s$.

Table 5. 2 Summary of the WINeR-V noise contributions at 640kSps, 18 MHz receiver bandwidth, and 1 m receiving distance

Circuit	Transmitter			Receiver					
	TWG	Compa rator	VCO	Duty Cycle		LNA/Mi xer/IF	RSSV	LO	TDC
				0.1~0.9	1/6~5/6				
Pulse width noise	1.3ns	1.05ns	0.024ns	0.97ns	0.60ns	2.13ns	2.08ns	0.008ns	0.54ns
Equivalent SNR	61.5dB	63.5dB	96.4dB	64.2dB	68.3dB	57.3dB	57.5dB	106dB	69.2
Equivalent NOB	10.2	10.5	16.0	10.7	11.3	9.5	9.6	17.6	11.5
Overall System Resolution				8.8					

Direct noise measurement for different blocks of the WINeR system was performed in the laboratory environment and inside a Faraday cage. We conducted this measurement by evaluating the noises on the 16-bit digital outputs from the PC and then refer them back to the input. This measurement was done in 4 conditions: 1. the entire system, which included all the noise sources all the way from the transmitter amplifier to the receiver TDC. 2. From transmitter VCO to PC, which included the wireless link, the receiver, and the TDC. 3. From transmitter PWM to PC, which bypassed the wireless link by directly giving the transmitter PWM to the receiver TDC. 4. From TDC to PC, where only the TDC noise was considered. During all these measurements, the inputs were grounded and the distance between the transmitter and receiver was 1m. The data was collected in 1 s. The input referred noise amplitude and pulse width error for these measurements are shown in Figure 5. 7. Table 5. 3 summarizes the directly measured WINeR system noise contributions from different stages.

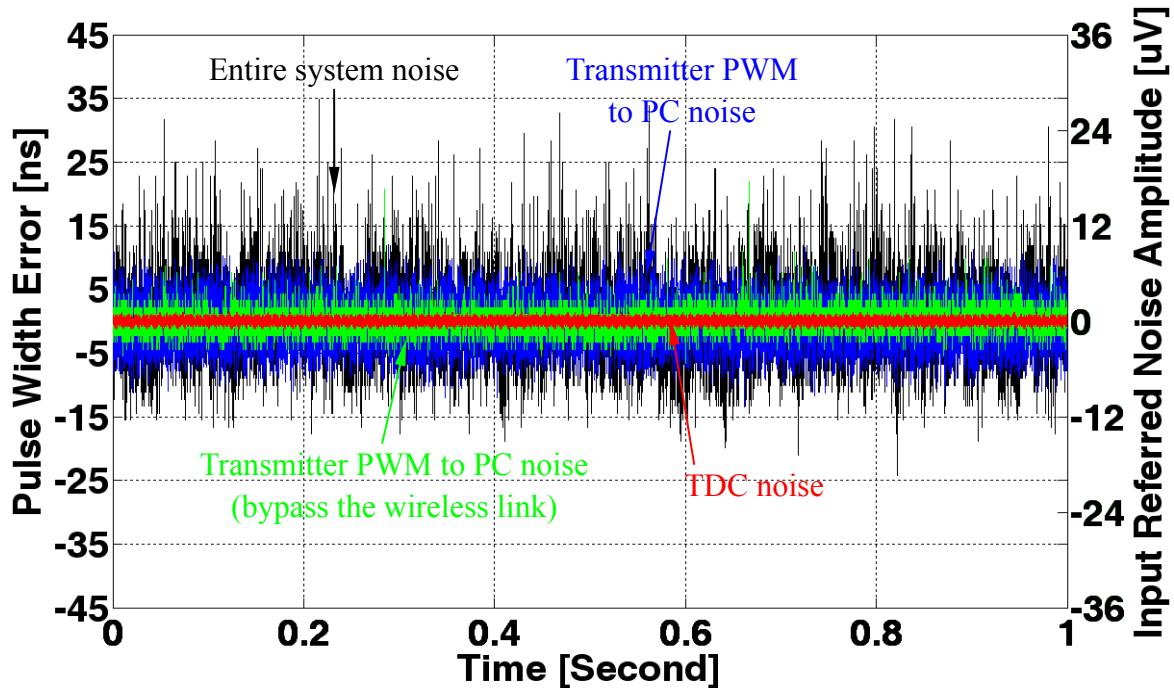


Figure 5.7 Input referred noise amplitude from different stages of the WINeR-V system to the PC at 1 m distance (LNA inputs are grounded).

Table 5.3 Summary of directly measured WINeR-V system noise contributions from different stages at 640kSps, 18 MHz receiver bandwidth, and 1 m receiving distance

Circuit	Input Referred Noise (rms)	Pulse Width Noise (rms)
LNA	$3.9 \mu\text{V}_{\text{rms}}$	4.9 ns
PWM	$1.36 \mu\text{V}_{\text{rms}}$	1.7 ns
Wireless/Receiver	$2.9 \mu\text{V}_{\text{rms}}$	3.6 ns
TDC	$0.43 \mu\text{V}_{\text{rms}}$	0.54 ns
Total	$4.9 \mu\text{V}_{\text{rms}}$	6.1 ns

According to Table 5.3 and the early analysis, for the current 32-channel WINeR-V

system, the noise from the transmitter LNA and the wireless/receiver is the dominant noise.

The later one is further dominated by the receiver thermal noise and RSSV noise.

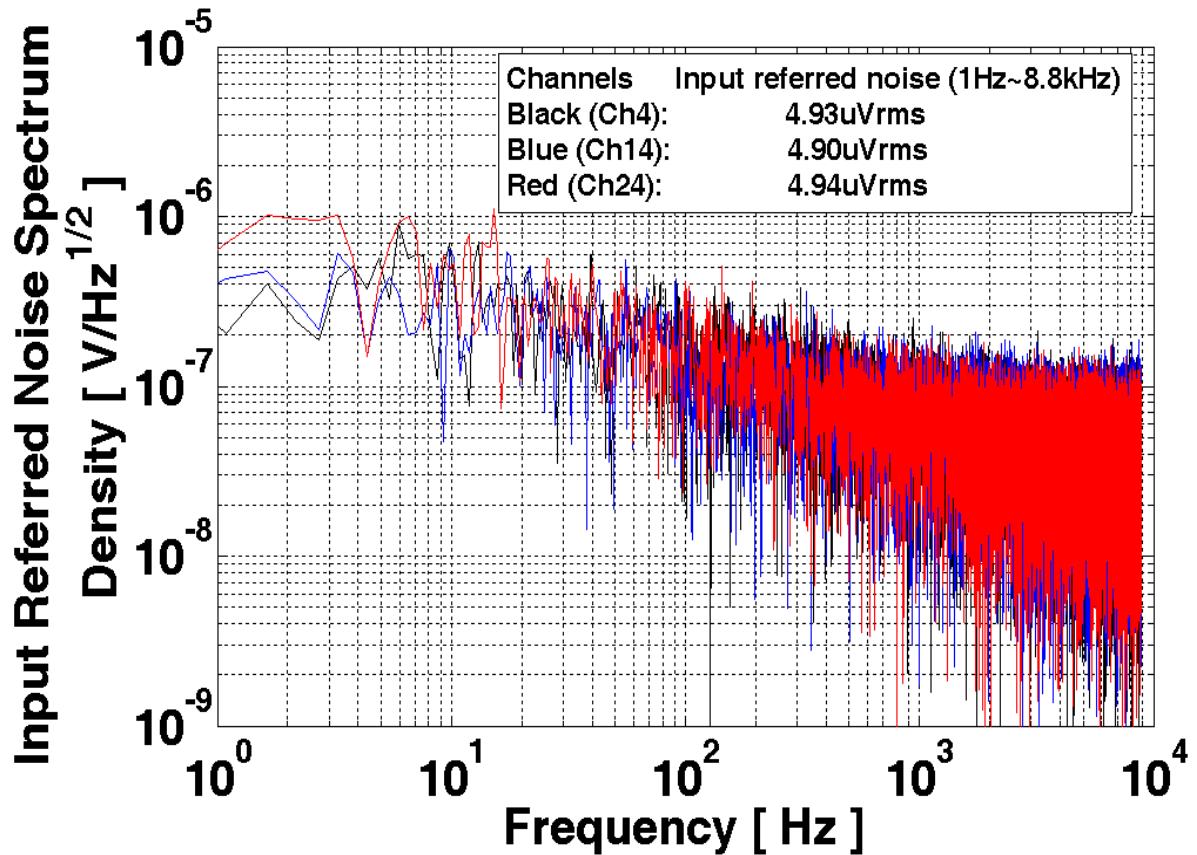


Figure 5. 8 Input referred noise spectrum of the entire WINeR-V system at 1 m distance
(LNA inputs are grounded).

To evaluate the system noise experimentally, the input referred noise of the complete 32-channel WINeR-V was measured by grounding all channels and conducting fast Fourier analysis on the recorded data from three grounded channels (Ch4, Ch14, and Ch24) in 1s at 1m distance. The input referred noise spectrum density had a noise corner around 10 kHz, as

shown in Figure 5. 8. Integration of these curves from 1 Hz to 8.8 kHz resulted in an input referred noise of 4.93, 4.90 and 4.94 μV_{rms} , respectively.

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CHAPTER 6 *In Vivo* Animal Testing

6.1 Introduction

To validate the functionality of the WINeR system in actual neural recording setups, we have tested the WINeR system *in vivo* on rats. The testing was conducted in three steps. In the first step, we validated the capability of the front-end LNA in amplifying and filtering the extracellular neural signals from the metal microelectrodes, as well as the WINeR receiver functionality by using WINeR-IV. In the second step, we verified the *in vivo* functionality of the entire 32-channel WINeR-V headstage on an awake rat being constrained in a plastic container. Finally, we performed *in vivo* testing for the 32-channel WINeR-V headstage on a freely moving rat.

6.2 Trial I: *In Vivo* Testing of WINeR-IV

For this *in vivo* testing, we have collaborated with Dr. Woodward at NC Neuroscience Institute Lab in Winston Salem, NC, USA. The animal model was a Wistar Strain rat. *In vivo* neural recording interface was chronically implanted in the brain stem (Ventral Tegmental Area—VTA) for about 1 month prior to the test as shown in Figure 6. 1. The electrodes were four groups of 50 micron stainless steel with Teflon insulation arranged in a close (2, 3, 3) configuration of eight microwires, making a total of 40 electrodes. The

electrodes were then connected to 4 10-pin Omnetics male micro connectors (A11489, Omnetics, Omnetics Connector Corporation, Minneapolis, MN). These connectors were assembled into two groups and covered with cement. Each group had 20 electrodes, 4 of them were used for references (ground), and 16 of them were recording electrodes making a total of 32 recording channels. The rat was anesthetized with an intraperitoneal injection of a mixture of ketamine, xylazine, and acepromazine and maintained with ketamine updates, as shown in Figure 6. 1.

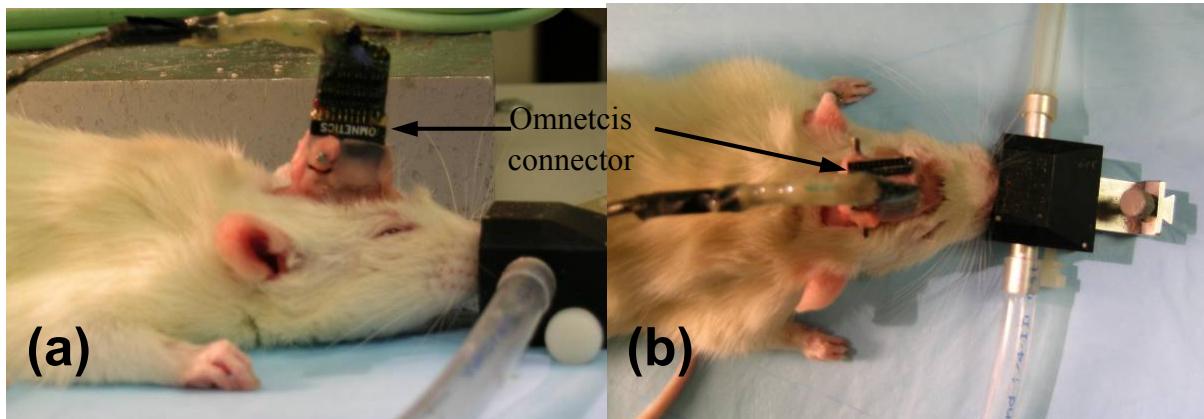


Figure 6. 1 Anesthetized rat with 40 implanted electrodes. (a) Side view. (b) Top view.

During the test, WINeR-IV was used. Although WINeR-IV has 6 channels, only the first channel with AC coupling for both stages and differential difference amplifier (DDA) CMFB (as discussed in Chapter 2) was used. To verify the capability of the LNA, the neural signal picked up by the microelectrode was directly given to the input of the LNA, and the output of the LNA was observed on the oscilloscope. For this experiment, the LNA gain and

bandwidth was set to 60dB and 600Hz \sim 10 kHz, respectively. The recorded neural spikes at the LNA output are shown in Figure 6. 2. This result shows that the LNA design of the first channel in WINeR-IV is capable of acquiring real *in vivo* neural signals. We also noticed that the neural spikes had amplitudes of $50\mu\text{V}_{\text{P-P}} \sim 300\mu\text{V}_{\text{P-P}}$ with a peak to peak background noise of $\sim 50\mu\text{V}_{\text{P-P}}$, i.e. $\sim 8\mu\text{V}_{\text{rms}}$.

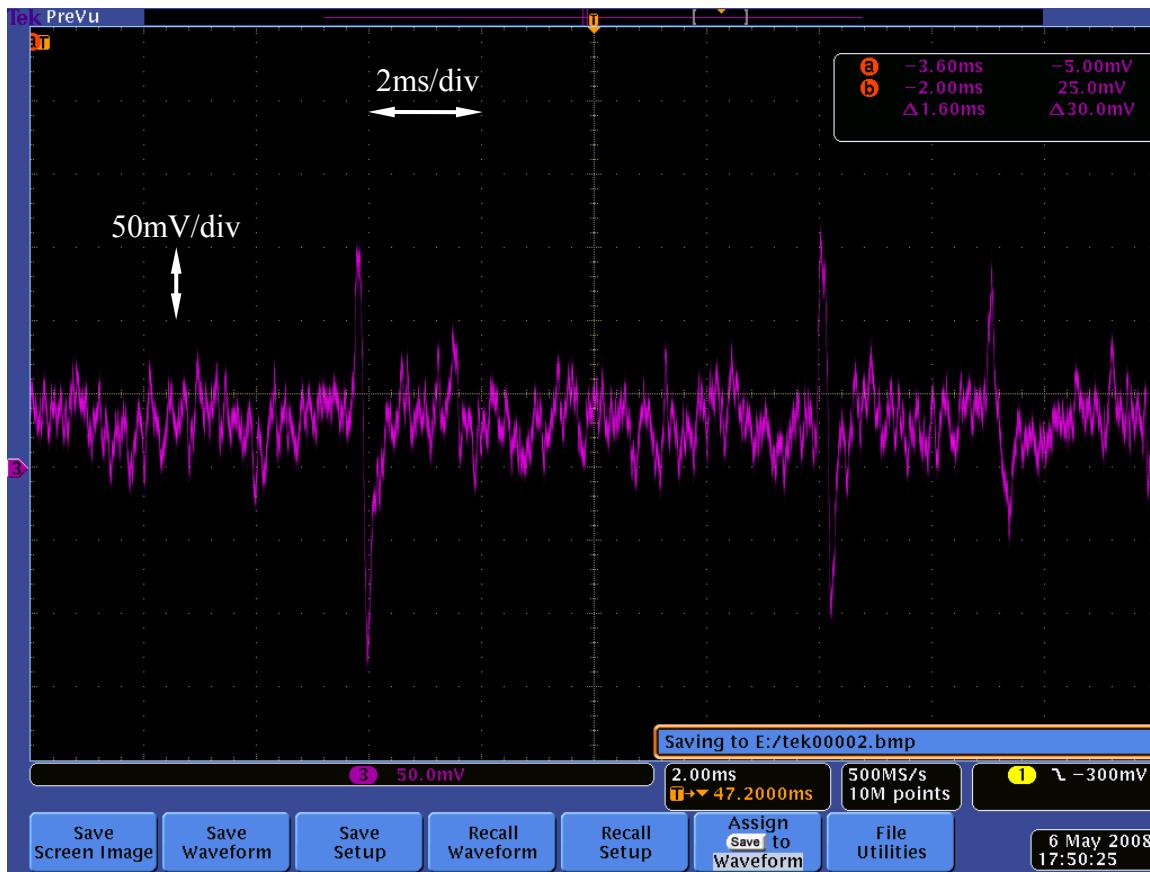


Figure 6. 2 Recorded neural spikes at WINeR-IV LNA output from the anesthetized rat.

We also verified the full functionality of the WINeR-IV along with the WINeR receiver by using the single channel recording while grounding the other channels. During

this experiment, the rat was freely moving in the cage. Since the WINeR-IV was bonded in a bulky package and PCB at that time ($10.5 \times 7.0 \times 1.5\text{cm}^3$) and was not suitable to directly sit on the animal's head during the freely moving test, a unity gain stage was used before the WINeR-IV inputs to reduce the noise picked up by the long wire connection between the probe and WINeR-IV. The receiver was placed ~ 1 meter away from the transmitter (see Figure 6. 3).

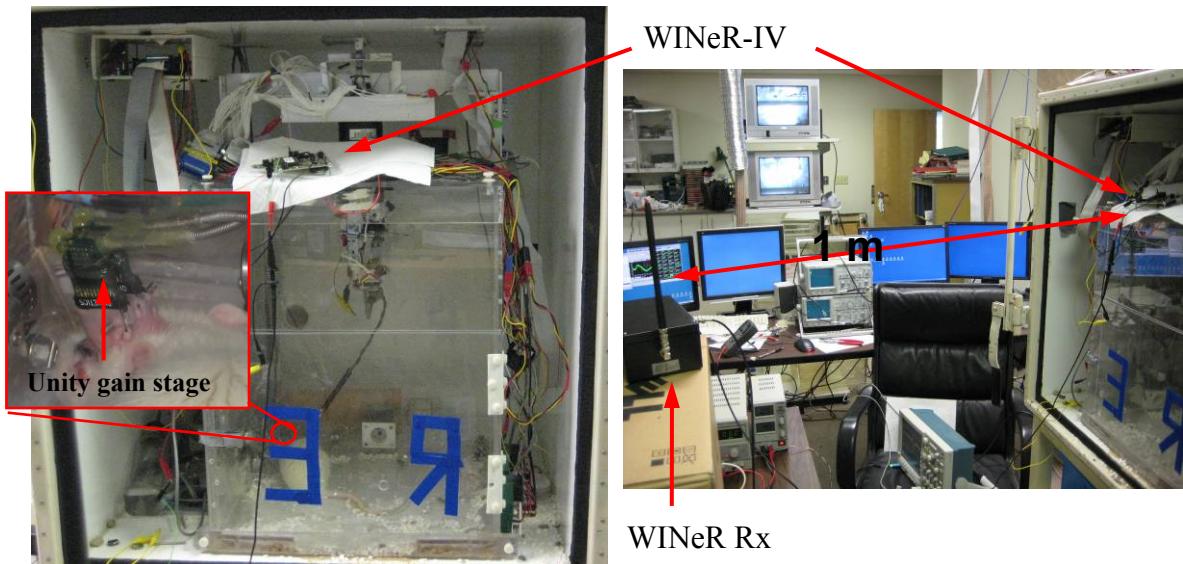


Figure 6. 3 *In vivo* testing setup for WINeR-IV.

The recorded *in vivo* data is shown in Figure 6. 4. According to the recorded neural data, the neural spikes have amplitudes of $100 \mu\text{V}_{\text{P-P}} \sim 500 \mu\text{V}_{\text{P-P}}$, and the spike duration is around $500 \mu\text{s}$. Comparing to the anesthetized testing results, the freely moving animal had larger spike amplitude and much higher rate. The noise level in the later test had a

peak-to-peak value of $60\mu\text{V}_{\text{P-P}}$, i.e. $10\mu\text{V}_{\text{rms}}$, which is consistent with the first testing results.

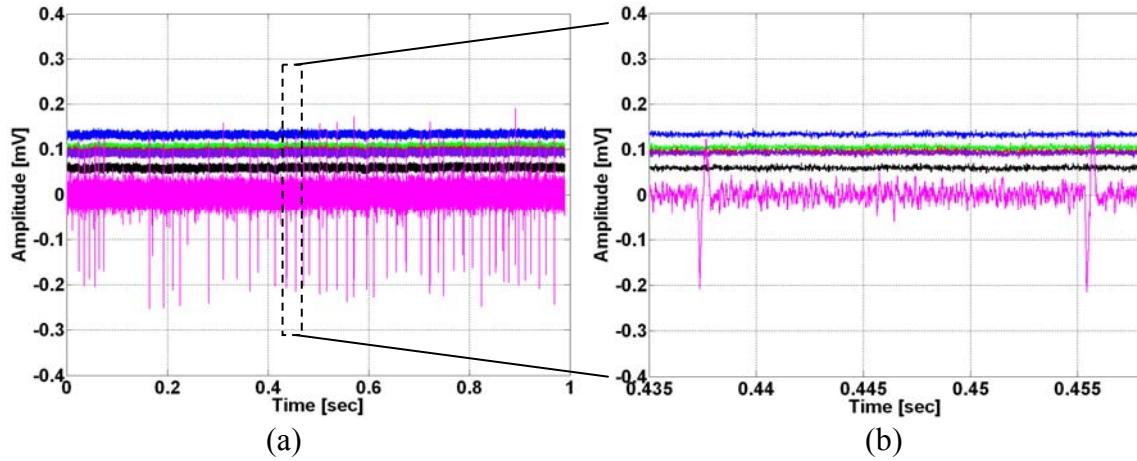


Figure 6.4 Wirelessly recorded neural signals at 1 meter distance from a freely moving rat by using WINeR-IV with unity gain stage before the LNA.

6.3 Trial II: Testing of WINeR-V with Awake Rat

With the experience gained from the first trial on WINeR-IV, we tested the 32-channel WINeR-V on an awake but restrained rat in collaboration with NC Neuroscience Institute. The difference between the animals used in Trial I and Trial II was that the second one had electrodes implanted prior to the test for about 5 months, while the first one was only about 1 month post-surgery. In addition, in the second test, the WINeR-V was stand alone. The LNAs were directly interfacing with the electrodes and no unity gain stage was used. The 32-channel WINeR-V headstage transmitter board is shown in Figure 6.5. This is the first prototype of WINeR-V and it was relatively large ($5.5 \times 4.5 \times 1.5 \text{ cm}^3$) because the

WINeR-V ASIC was packaged in a large 145-pin PGA package.

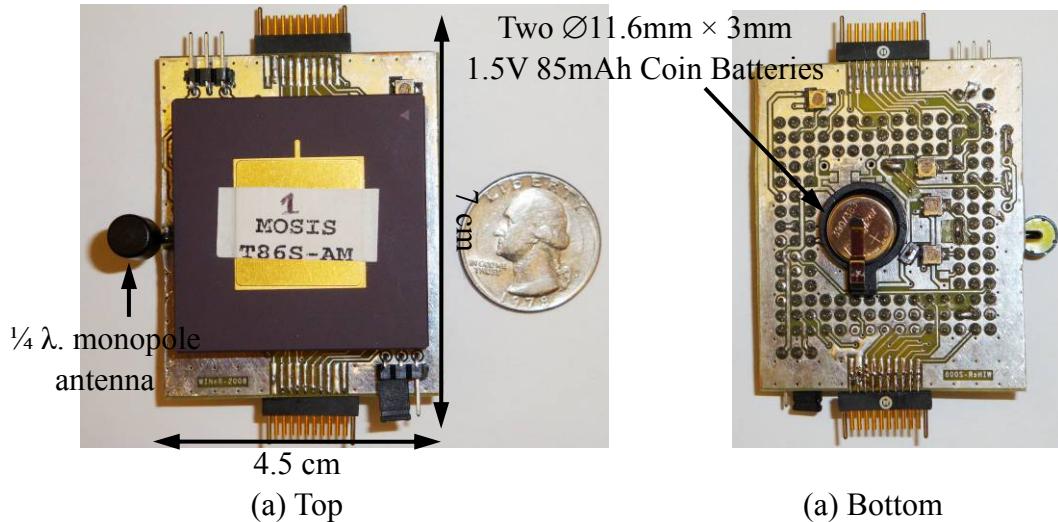


Figure 6.5 32-channel WINeR-V *in vivo* testing headstage prototype I.

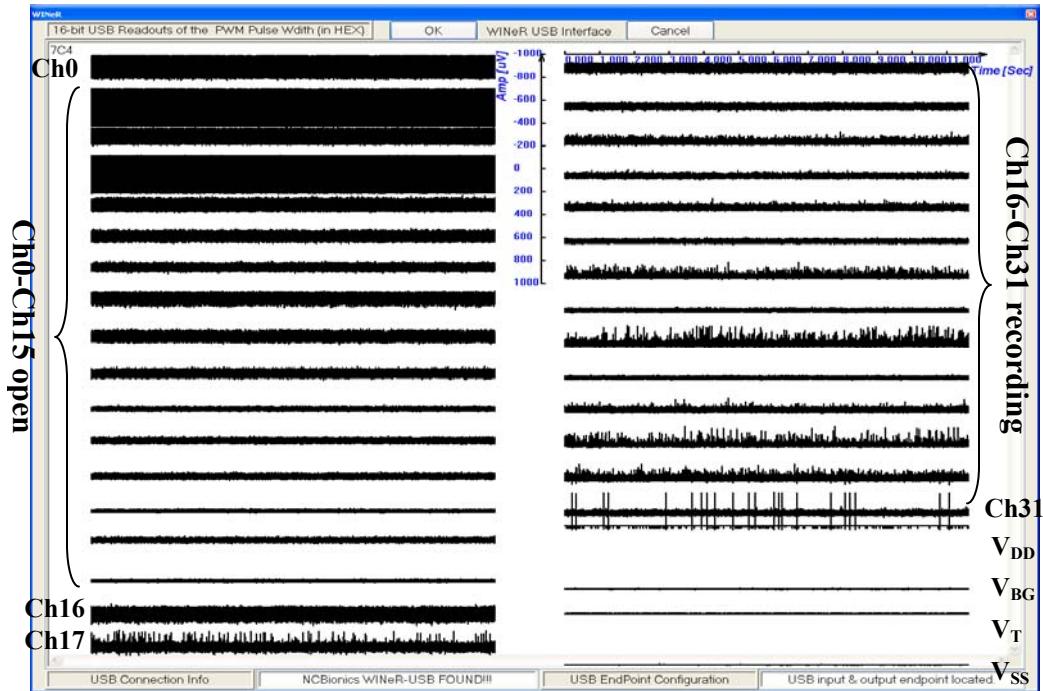
During the testing, the rat was restrained inside a plastic container to avoid the device being bumped to the walls of the cage due to the movement of the rat. The electrode connectors were accessible from out of the restrainer through a small opening on top. The WINeR-V transmitter board has 4 10-pin Omnetics female micro connectors (A11490, Omnetics, Omnetics Connector Corporation, Minneapolis, MN) on both sides of the board, two on each side. Only one side was used in the testing, providing a total of 16 simultaneous recording channels. The other 16 channels were left open. The transmitter board was powered with two \varnothing 11.6mm \times 3mm, 1.55V, 85mAh silver-oxide coin batteries (390-389TS, Energizer Battery Company, St. Louis, MO). The transmitter board used an embeddable $\frac{1}{4}$ wave monopole antenna as discussed in Section 3.2.6. The transmitter amplifiers bandwidth

and gain were set to 600Hz ~ 6 kHz and 77.1 dB, respectively. The system sampling rate was adjusted to 640kSps. The receiver antenna was mounted on the iron wall of the cage and separated by 0.3m from the transmitter (Figure 6. 6).



Figure 6. 6 *In vivo* testing setup of the 32-channel WINeR system on a restrained awake rat (Wistar Strain) in a Faraday cage (the distance between the transmitter and receiver was 0.3m).

The real-time WINeR GUI screenshot for a recording length of more than 11 s is shown in Figure 6. 7a. The GUI waveform begins with 16 open channels and 16 recording channels followed by the 4 monitoring channels. The result shows that one of the recording channels has successfully recorded neural spikes as high as $300\mu\text{V}_{\text{P-P}}$ (Ch31 red). Some other channels recorded signals of $\sim 100\mu\text{V}_{\text{P-P}}$ (Ch17, Ch26, and Ch29), and the rest of the recording channels showed signal amplitude less than $50\mu\text{V}_{\text{P-P}}$. For the open channels, some of them were resting around “0” volts, and a few of them were oscillating.



(a)

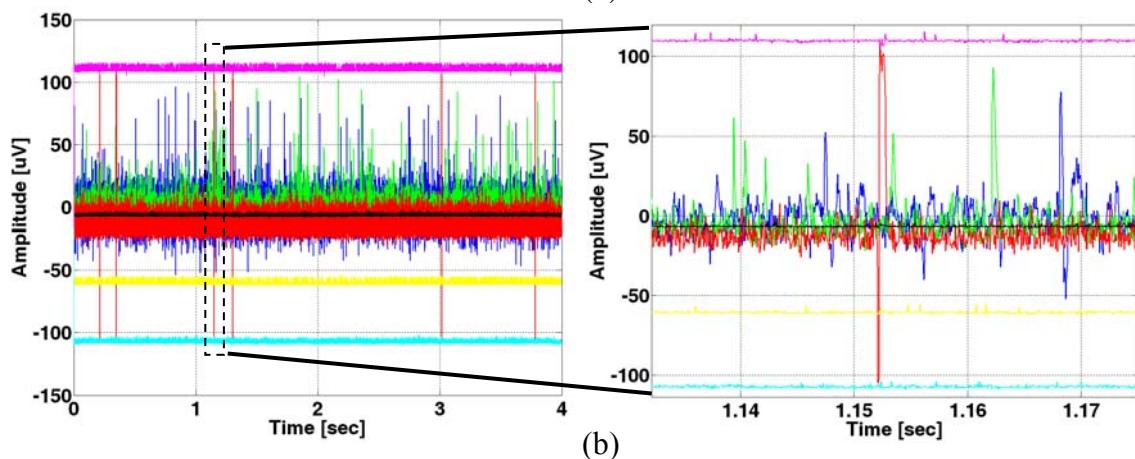


Figure 6. 7 (a) Real-time WINeR GUI screenshot during *in vivo* recording from an awake rat using WINeR-V. (b) Selective plot of 3 channels signals in MATALB using the data shown in (a).

A more detailed view of the recorded signals from Ch31: red, Ch17: blue, and Ch26: green are shown on Figure 6. 7b and c. Background noise showing in the *in vivo* testing are

in the order of $\sim 50\mu\text{V}_{\text{P-P}}$, i.e. $\sim 9\mu\text{V}_{\text{rms}}$.

6.4 Trial III: Testing of WINeR-V with Freely Moving Rat

Finally, we collaborated with Dr. Rainnie at Emory University and tested WINeR-V system on a freely moving rat. For this test, an adult male Sprague-Dawley rat was used. This rat had 20 electrodes implanted in the basolateral amygdala and infralimbic cortex area. The electrodes were connected to two 10-pin Omnetcis male micro connectors (A11365-001, Omnetics, Omnetics Connector Corporation, Minneapolis, MN). These connectors were consolidated with cement. Each connector has 10 pins, 2 of them were used for reference (ground), and 8 of them were recording electrodes.

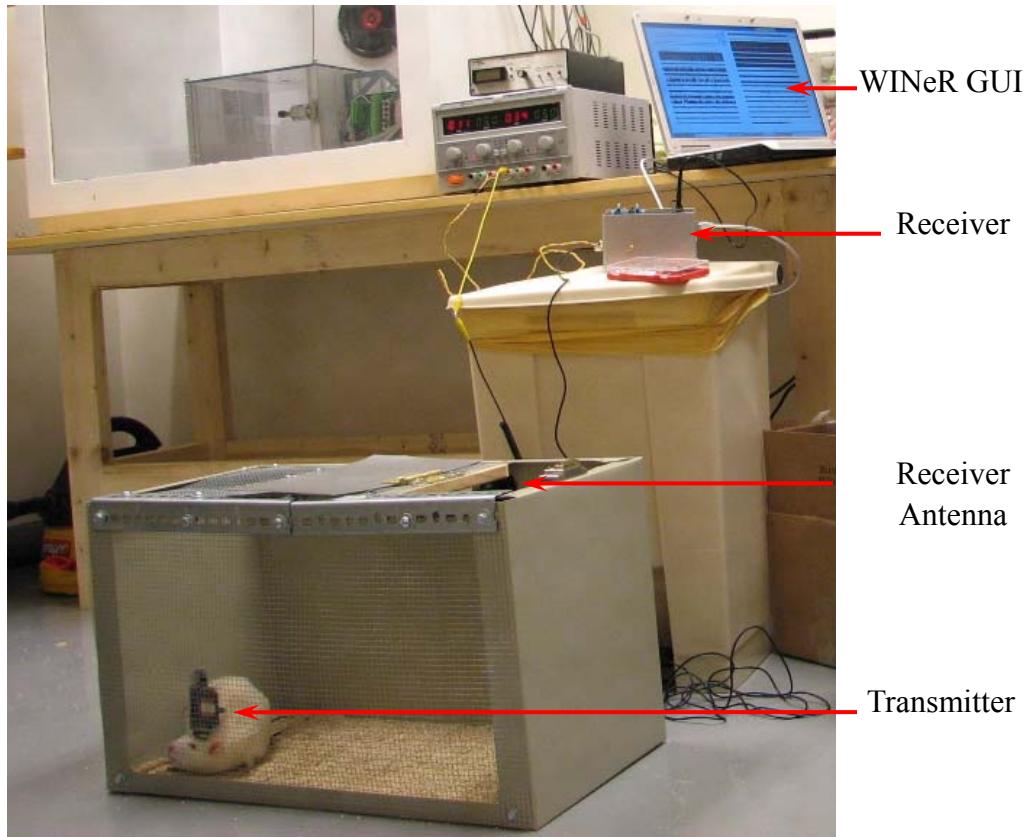


Figure 6.8 *In vivo* testing setup of the 32-channel WINeR-V system on a freely moving rat (adult male Sprague-Dawley) in a Faraday cage (the distance between the transmitter and receiver was smaller than 0.7m).

As shown in Figure 6.8, during the testing, the rat was not constrained and free to move in the cage. The headstage used for this testing was the same as the one used in Trial II, shown in Figure 6.5. Therefore, its size reduced the rat activity. The settings for the transmitter were the same as before, i.e. 600 Hz~6 kHz LNA bandwidth, 77.1dB gain, and 640kSps sampling rate. The distance between the transmitter and receiver was 0.7m.

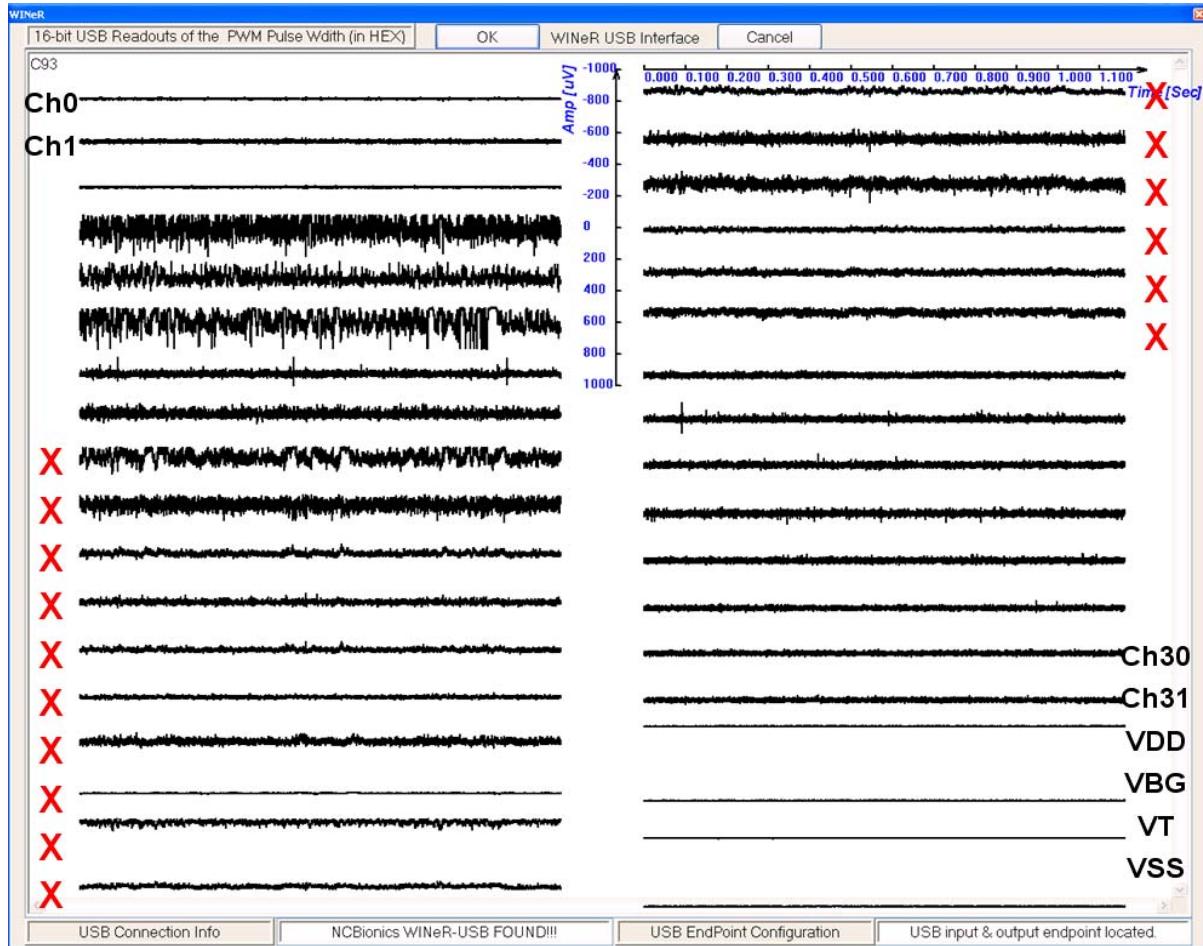


Figure 6. 9 Real-time WINeR GUI screenshot during *in vivo* recording from a freely moving rat using WINeR-V (X are open channels).

The real-time WINeR GUI screenshot for a recording length of more than 1.1 seconds is shown in Figure 6. 9. The GUI waveform begins with 8 recording channels and followed by 16 open channels and then another 8 recording channels. The last 4 are monitoring channels. The result shows that the 32-channel WINeR system has successfully recorded neural spikes. Two of the recording channels carried signals as high as $200\text{--}300\mu\text{V}_{\text{P-P}}$ (Ch6 and Ch25). Some other channels showed signals $\sim 100\mu\text{V}_{\text{P-P}}$ (Ch26 and

Ch27), the rest of the recording channels had signals with amplitudes less than $100\mu\text{V}_{\text{P-P}}$. For the open channels, most of them were rested around “0” volts, and a few channels had large noise on them, which could be the result of oscillation.

To extract more information, 24s of recorded raw data from 4 channels that carried larger signals were fed into two commercial neural signal processing software, NeuroExplorer [6.1] and Plexon Offline Spike Sorter [6.2], for offline signal processing. The high resolution raw data and principle-component-analysis (PCA) classified neuron data are plotted in Figure 6. 10 and Figure 6. 11. The background noise showing in the *in vivo* testing results is in the level of $\sim 50\mu\text{V}_{\text{P-P}}$, or $\sim 9\mu\text{V}_{\text{rms}}$.

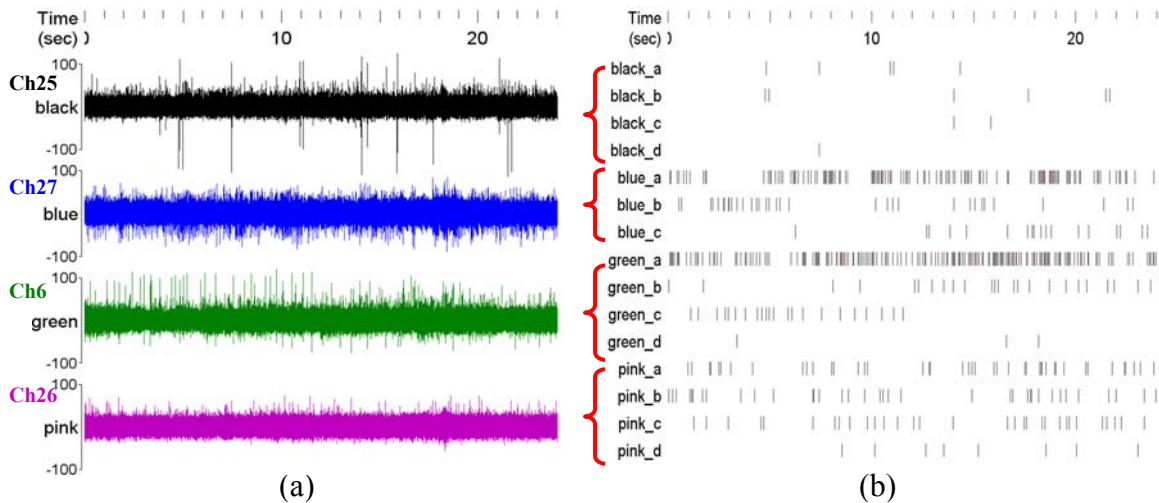


Figure 6. 10 Offline processed neuron data from 4 channels carrying large neural signals (Black:Ch25, Blue:Ch27, Green:Ch6, Pink:Ch26). (a) NeuroExplorer high resolution raw data. (b) NeuroExplorer classified spike sorting data.

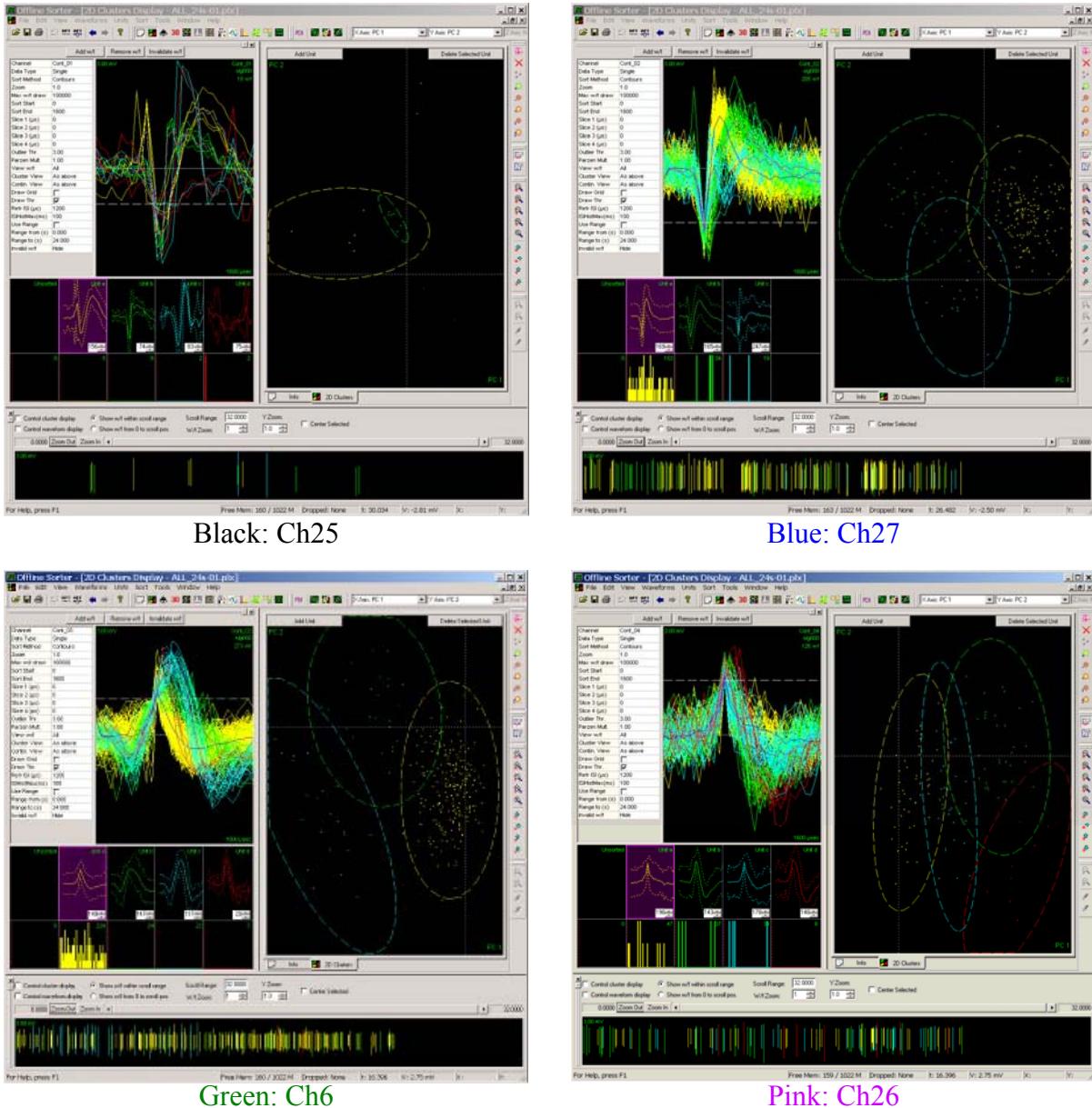


Figure 6.11 Plexon Offline Spike Sorter screenshots for the 4 channels carrying large neural signals (Black:Ch25, Blue:Ch27, Green:Ch6, Pink:Ch26).

In addition to recording neural spikes, we also recorded local field potentials along with the spikes using WINeR-V by setting the LNA bandwidth to 1 Hz ~ 6 kHz. Figure 6.12

shows the *in vivo* measured local field potentials along with the spikes from 8 simultaneous channels of WINeR-V.

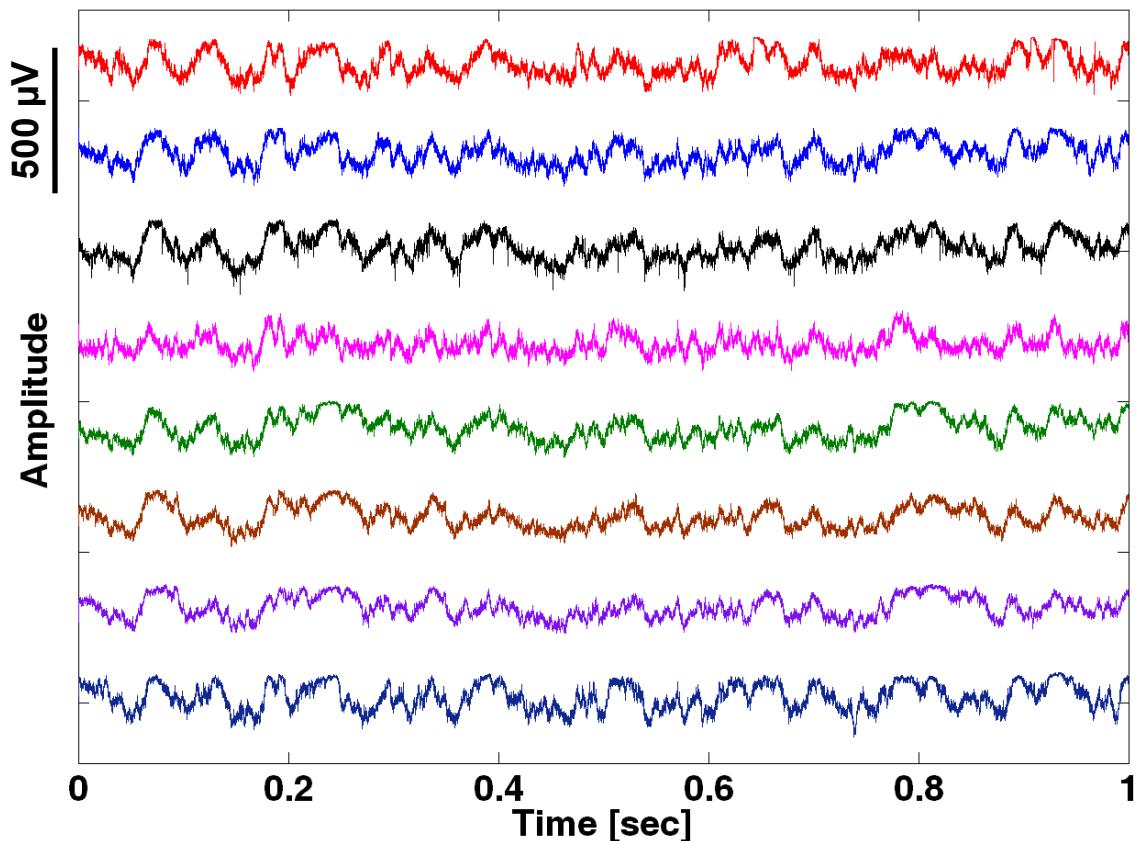


Figure 6.12 *In vivo* measured local field potentials along with the spikes from 8 simultaneous channels of WINeR-V when the LNAs bandwidth was set to 1Hz ~ 6 kHz.

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CHAPTER 7 Conclusion and Future Work

7.1 Conclusion

In this dissertation, we focused on developing a system-on-a-chip (SoC) multi-channel wireless implantable neural recording system with low power, low noise, and miniature size, which can transfer the entire recorded neural activities to the external computer for further signal processing. In designing such a system, we utilized a clockless PWM-TDM architecture, which is similar to a single-slope ADC that is made wireless. This technique is quite robust against noise and interference and at the same time offers unique flexibilities for the user, such as variable sampling rate, dynamic range, resolution, bandwidth, gain, and carrier frequency. After briefly going through the developing history of the WINeR system in Chapter 2, this dissertation discussed in detail the latest 32-channel WINeR-V SoC ASIC and its bench-top and *in vivo* measurements results.

This dissertation also demonstrated a high performance, low noise receiver with up to 75 MHz bandwidth for the WINeR system that utilizes the PWM-TDM technique. Utilization of several IF gain stages, passive LC filters, and a high resolution FPGA-based TDC have significantly enhanced the latest receiver performance compared to its predecessors. It also uses a 2 MB SDRAM buffer to maintain up to 10 Mb/s raw data

throughput at 640 kHz sampling rate for up to 32 parallel channels. A VC++ graphic user interface is developed to record and visualize the recovered neural signal in real-time. The receiver is also equipped with an audio part that picks 4 channels of digitized signals and converts them into analog signals. One of these signals is given to an audio amplifier to drive an audio speaker, which offers the ability of identifying the neural spikes by just hearing the sound of the neurons.

After describing the WINeR transmitter and receiver, we evaluated the wireless PWM-TDM technique for wireless neural recording application by exploring its potential sources of noise and inaccuracy. We have done a detailed noise analysis on the WINeR-V system and indicated the major sources of noise and their contribution to the total input referred noise. The results showed that the LNA, pulse width modulator, and to a lesser extent the VCO phase noise contribute the most to the noise on the transmitter side. The thermal noise of the RF frontend and wireless link, changes in the received signal strength, and the limitation of the receiver bandwidth play the most significant roles for noise on the receiver side. Detailed noise measurements were performed and the results showed that the entire 32-channel WINeR-V from electrodes to the PC has a total input referred noise of 4.9 μV_{rms} at 1 m distance, and it provided more than 8 bits of resolution. This is equivalent to a bandwidth of 5.12 Mbps throughout the WINeR-V system.

In vivo tests have been conducted with the WINeR-IV and WINeR-V. The tests on WINeR-IV verified the functionalities of the front-end LNA and the basic PWM-TDM WINeR system design. We also tested WINeR-V on an awake but restrained rat (Wistar Strain) and a freely moving rat (adult male Sprague-Dawley), from which we successfully recorded both neural spikes and local field potentials from 16 simultaneous channels. These results validated the full functionality of the WINeR-V system and showed a homogenous noise level of $\sim 9\mu\text{V}_{\text{rms}}$ during all the *in vivo* tests.

7.2 Future Work

After all those efforts, there is still room for further improvement.

7.2.1 Transmitter Improvements

i. Miniaturization: As shown in Figure 6. 5, the headstage used for the latest awake and freely moving animal tests was very large and was not practical for long term freely moving animal testing or implantation. In addition, its large size and weight could potentially bias the experiment results and make the animal subjects feel uncomfortable or even harm them. We have assembled two smaller prototypes of the 32-channel WINeR-V headstages (thanks to GT-Bionics lab member, Seung Bae Lee, for wire bonding the chip on the small PCBs), as shown in Figure 7. 1. The testing and validation of these two prototypes are still ongoing

with our collaborators at Emory University, Atlanta, GA.

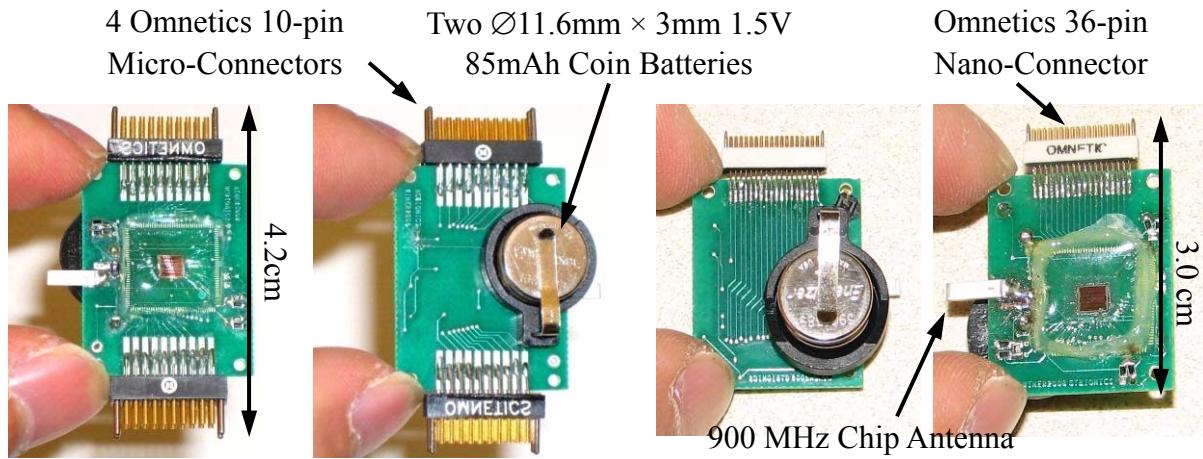


Figure 7.1 Two battery powered small prototypes of the 32-channel WINeR-V headstage.

ii. Power supply of the system: The systems we have discussed so far are suitable for the animal headstage. Because they are all battery powered, and the batteries need to be replaced after a couple of days. As far as implanting is concerned, every part of the system should be minimized in size in order to cause the minimum tissue damage. Also primary batteries need to be replaced with inductive link or rechargeable batteries. An inductive link is a promising choice for these kinds of implantable devices. The block diagram of the inductive link is shown in Figure 7.2 [7.1]. An externally generated RF magnetic field in the megahertz range induces a sinusoidal voltage in the receiver inductive-capacitive (*LC*) tank circuit. The next block should be a wideband rectifier to convert the ac signal to an unregulated dc supply voltage. A regulator always follows the rectifier to provide a constant DC voltage for the

whole implantable system as a power supply. It contains circuitry that continuously holds the output voltage at the desired value regardless of changes in load current or input voltage (this assumes that the load current and input voltage are within the specified operating range for the part). A FSK signal is transferred over the inductive link as well to provide control information to the internal implantable system externally (Figure 7. 2). The project for realizing this idea is already ongoing in our lab [7.1].

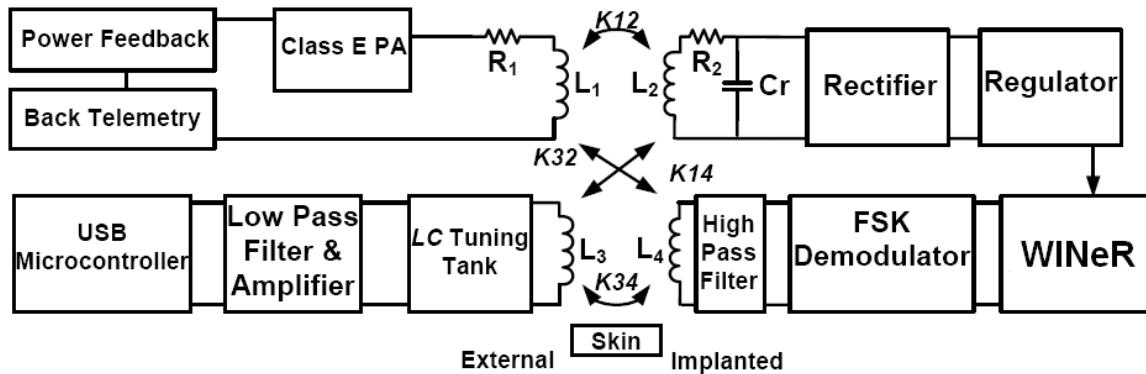


Figure 7. 2 Conceptual block diagram of the inductive link to transmitter both power and data to the implants [7.1].

iii. Adding power amplifier to the transmitter: According to the measurement results the proposed unbuffered flexible hybrid LC tank VCO can work properly in the range of one or two meters. But with new requirements on the WINeR system, users may want to operate it over a longer distance. In that case an RF power amplifier may be needed to increase the transmitted power of the FSK signal as long as this is within the allowed total power consumption range of the WINeR system.

7.2.2 Receiver Improvements

- i. Multiple receiver antennas: The transmitter and receiver antennas do not have perfect omnidirectional radiation patterns. Therefore, during the *in vivo* testing the received signal strength could vary a lot (more than 40dB) because of the movement of the transmitter along with the animal, which could affect the quality of the received signal or even disrupt recording. Although we have already implemented an AGC block to stabilize the signal strength, the input dynamic range of the AGC is only -52dBm ~ +8dBm. In practice, if the received signal strength falls below -52dBm, the AGC will be not helpful. Using multiple receiver antennas can potentially alleviate this problem. The idea is to place multiple receiver antennas at different directions or positions within the recording enclosure, and continuously monitoring the received signal strengths from different antennas by using high speed RF power detectors. Then the receiver can use the outputs of the power detectors to select the antenna that carries the best signal, and control an RF switch to switch to that antenna.
- ii. FPGA-based FSK demodulator module: For FSK demodulation, the current receiver still uses conventional discriminator, rectifier, and low pass filter based FSK demodulation scheme. This method needs many off-chip components for those blocks, which add to the cost and power consumption of the receiver, and their performance is also limited by those commercially available components. We have recently come up with a new idea of building a FPGA-based FSK demodulator.

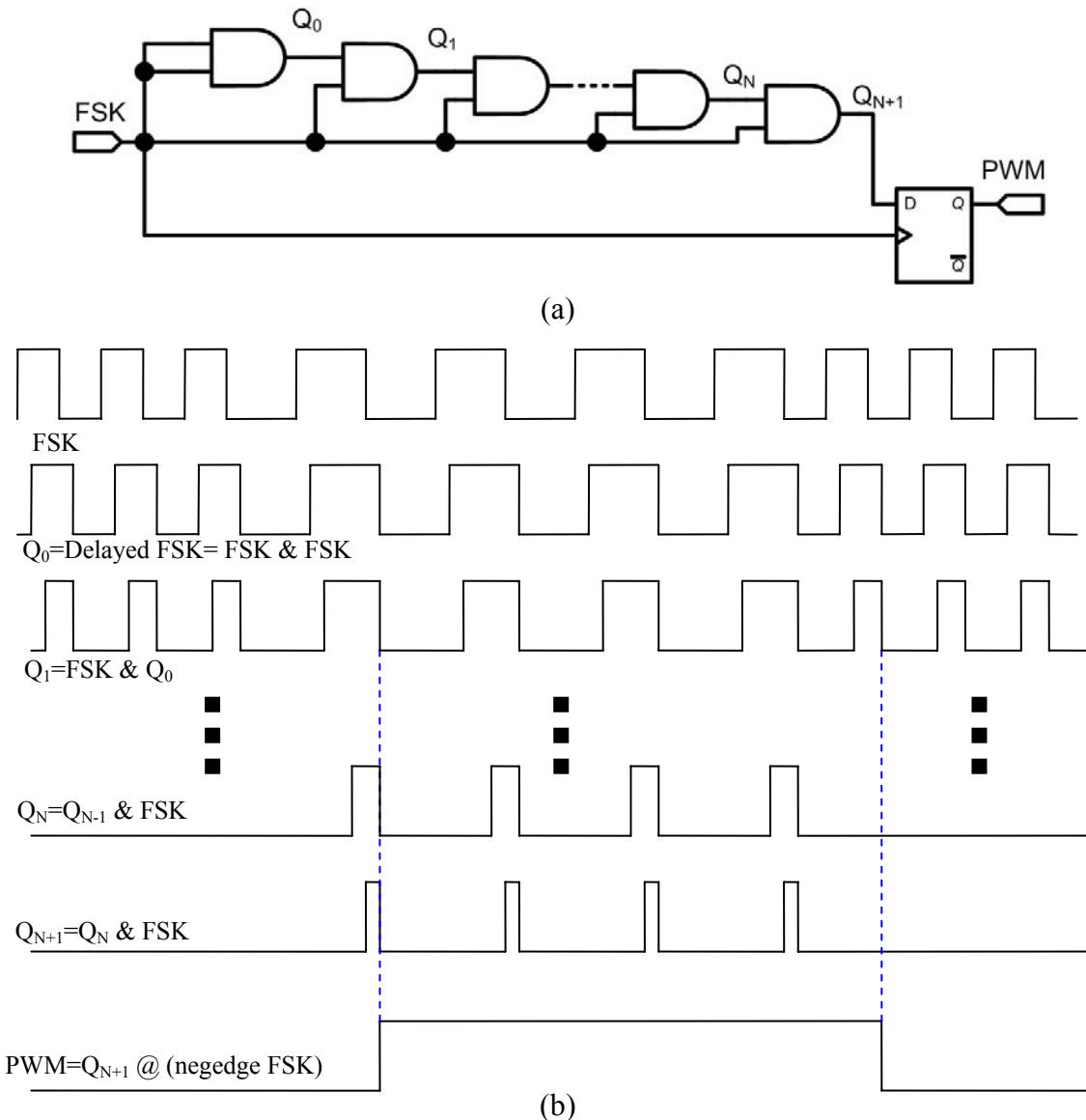


Figure 7.3 FPGA-based FSK demodulator. (a) Conceptual block diagram. (b) Operation and associated waveforms.

The conceptual block diagram of the FPGA-based FSK demodulator is shown in Figure 7.3a. Figure 7.3b shows the FSK demodulator operation and its associated waveforms. We assume the input signal is a true IF-FSK, as shown in the first trace of Figure

7. 3b. We first create a delayed FSK, Q_0 (2nd trace of Figure 7. 3b), then we assign $Q_1=$ FSK & Q_0 (3rd trace of Figure 7. 3b). Because of the delay, the positive pulse width in Q_1 will be slightly narrower than the original FSK signal. By repeating the same logic, we will get a chain of $Q_1 \sim Q_{N+1}$, as shown in Figure 7. 3b. Since the two IF-FSK frequencies are different, there will be an integer, N, from where the positive pulses at the higher FSK carrier will be missing, and only the positive pulses at lower FSK frequency exist. If we assign $PWM=Q_{N+1}$ @ (negedge FSK), then the original FSK modulated PWM signal will be recovered. This module was implemented in a Xilinx FPGA and was validated with a 40/70MHz, 100 kHz modulation frequency IF-FSK signal.

iii. RF carrier frequency tracking: Because of the size and power constraints on the transmitter side, the transmitter VCO does not have any frequency stabilization components, such as PLL or crystal. Therefore its carrier frequency could drift due to temperature variation or surrounding environment. Moreover, the unbuffered transmitter VCO design makes this situation even worse. The drifting of the carrier frequency will greatly reduce the received signal quality and even miss data packages. To avoid this problem, we are planning to add a carrier frequency tracking algorithm on the receiver. By monitoring the down-converted IF signal frequency change, it can automatically retune the receiver LO to stabilize the IF frequency in a certain range.

iv. Hardware synchronization: The current receiver does not have any synchronization

algorithm in its hardware. Only a simple synchronization scheme was implemented in the GUI software, which was not quite robust and may also add large latency to the system. For improving the system fidelity, hardware synchronization should be implemented.

7.2.3 GUI Improvements

The current VC++ GUI is very simple and not quite user friendly. Also, it can only save the data file in an Excel format (CSV) or binary format (BIN), which are not compatible with the widely used industrial neuron data format, such as NeuroExplorer format (NEX) [7.2] or the Plexon format (PLX) [7.3]. The next step for improving the WINeR GUI is to provide enough flexibility in controlling the data recording characteristics based on the user's preferences, as well as making the WINeR data format to be compatible with the industrial standards. We believe this will make the WINeR system more acceptable for the potential users.

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