

The Nordic Electronics Packaging Guideline

Chapter: B. Flip-Chip

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B. Flip-Chip Technology

B1. Level 1. Introduction to Flip-Chip techniques

B1.1 Why flip-chip?

In the development of packaging of electronics the aim is to lower cost, increase the packaging density, improve the performance while still maintaining or even improving the reliability of the circuits. The concept of flip-chip process where the semiconductor chip is assembled face down onto circuit board is ideal for size considerations, because there is no extra area needed for contacting on the sides of the component. The performance in high frequency applications is superior to other interconnection methods, because the length of the connection path is minimised. Also reliability is better than with packaged components due to decreased number of connections. In flip-chip joining there is only one level of connections between the chip and the circuit board.

Potentially flip chip technology is cheaper than wire bonding because bonding of all connections takes place simultaneously whereas with wire bonding one bond is made at a time. In practise, however, this price benefit is not always achieved due to immature processes, e.g. the cost of die bumping with current processes can be significant, especially in low volumes.

Flip-chip joining is not a new technology. The technology has been driven by IBM for mainframe computer applications. Many millions of flip chips have been processed by IBM on ceramic substrates since the end of 60's. At the beginning of 70's the automotive industry also began to use flip chips on ceramics. Today flip-chips are widely used for watches, mobile phones, portable communicators, disk drives, hearing aids, LCD displays, automotive engine controllers as well as the main frame computers. The number of flip chips assembled was over 500 million in year 1995 and close to 600 million flip chips were consumed 1997 [B1].

B1.2 General benefits/disadvantages

Advantages:

- Smaller size: Smaller IC footprint (only about 5% of that of packaged IC e.g. quad flat pack), reduced height and weight.
- Increased functionality: The use of flip chips allow an increase in the number of I/O. I/O is not limited to the perimeter of the chip as in wire bonding. An area array pad layout enables more signal, power and ground connections in less space. A flip chip can easily handle more than 400 pads.
- Improved performance: Short interconnect delivers low inductance, resistance and capacitance, small electrical delays, good high frequency characteristics, thermal path from the back side of the die.
- Improved reliability: Epoxy underfill in large chips ensures high reliability. Flip-chips can reduce the number connections per pin from three to one.
- Improved thermal capabilities: Because flip chips are not encapsulated, the back side of the chip can be used for efficient cooling.
- Low cost: Batch bumping process, cost of bumping decreases, cost reductions in the underfill-process

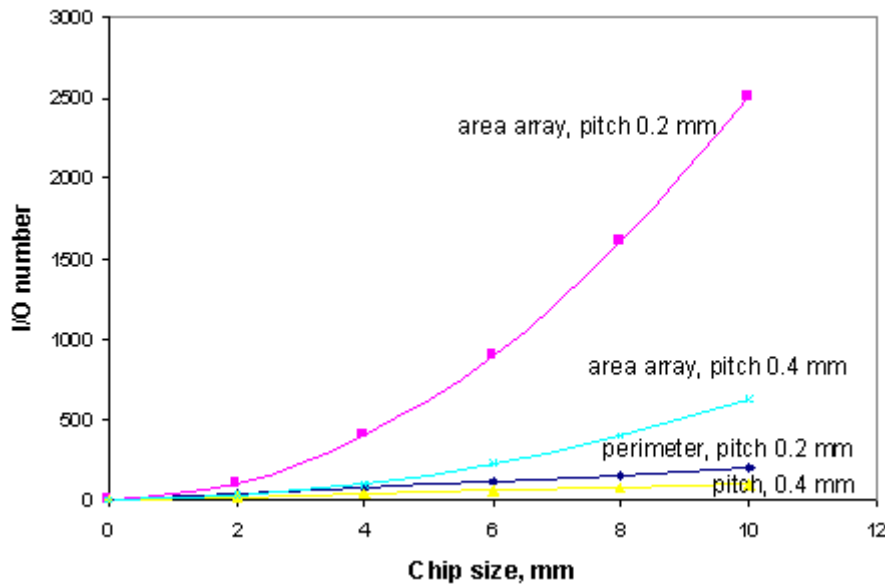


Figure B1. Comparison of the number of I/O vs. chip size between area array and perimeter array pad arrangement for pitches of 0.2 mm and 0.4 mm.

Disadvantages:

- Difficult testing of bare dies.
- Limited availability of bumped chips.
- Challenge for PCB technology as pitches become very fine and bump counts are high.
- For inspection of hidden joints an X-ray equipment is needed.
- Weak process compatibility with SMT.
- Handling of bare chips is difficult.
- High assembly accuracy needed.
- With present day materials underfilling process with a considerable curing time is needed.
- Low reliability for some substrates.
- Repairing is difficult or impossible.

B1.3 Relative cost comparison

The cost of flip chip technology can be divided into bumping cost and assembly process cost. Die bumping costs are dependent on wafer size, number of dies per wafer, wafer yield and volume. The assembly processes for the most common flip chip technology include pick and place together with flux application, reflow and cleaning as well as underfill process and its curing. The cost of the necessary equipment and floor space, the capacity of the equipment and its compatibility with other manufacturing processes are also important factors having influence on the economy of the technology for particular product. The substrate has also an important impact on the packaging costs. The cost of substrate depends e.g. on via sizes, layer count, line width and spaces, die pad pitch, flatness requirements, material type, panelization optimisation and the fabrication process.

In the case of manufacturing of 300 - 400 I/O BGA packages in the volume of 1 million per month the capital cost of flip chip process is less than half of the corresponding cost for wire bonding technology and the floor space needed is also only about one half of that for wire bonding technology

The cost of bumping with solder bumps using common batch processes is practically independent of the wafer size. The costs per die are therefore strongly dependent on the number of good dies obtained from one wafer. An order of magnitude for wafer bumping in high volume production is \$85 per wafer. For the case of 10 mm die on 8 inch wafer and yield of 90% the bumping cost per die is \$0.37.

The cost of wire bonding process increases with increasing number of I/O's while the cost of flip chip process is practically independent of the I/O count. For very high I/O numbers the flip chip process is the only choice.

Wire bonding, which is a mature technology, costs about \$0.03 per pin, based on a 500 I/O device. The cost to bump a 200 mm with the evaporative process is around \$200, sputtering and plating comes in at around \$100, and electroless nickel bumping cost projections are below \$50 [B1].

B1.4 Availability of components

A precondition for using flip chip technique is availability of bumped chips or alternatively known good bare dies when bumping is done separately. The use of solder bumping is the most common process alternative. Many chip houses already deliver solder bumped dies <LINK TO <http://www.imec.be/kgd/>>. Solder bumping which is a wafer level process, needs big and expensive facilities. Therefore it is not convenient to have inhouse processing facilities for solder bumping. There are also specialised companies making services of solder bumping.

The situation with the availability of solder bumped and tested chips for flip chip bonding is still not satisfactory. Flip chip bonding knowledge is spreading slowly and as an additional production step in wafer manufacturing the known good die (KGD) issue is still causing a certain degree of uncertainty on the user side [B2].

B1.5 How mature is the technology?

Although flip chip technology has been used already for about 30 years, it is still in quite limited use. It has many technical variations which have very different levels of maturity and fairly restricted availability. The flip chip technology using solder joining is already in a fairly mature state. The limitations are at least partly related to the limited availability of bumped components and limited compatibility with available SMD processing equipment.

B1.6 Short description of each flip chip process

There are many different alternative processes used for flip-chip joining. A common feature of the joined structures is that the chip is lying face down to the substrate and the connections between the chip and the substrate are made using bumps of electrically conducting material. Cross sections of flip chip joints without and with underfill material are shown in Figure B2. Examples of the different types of flip chip joints are schematically shown in Figure B3.

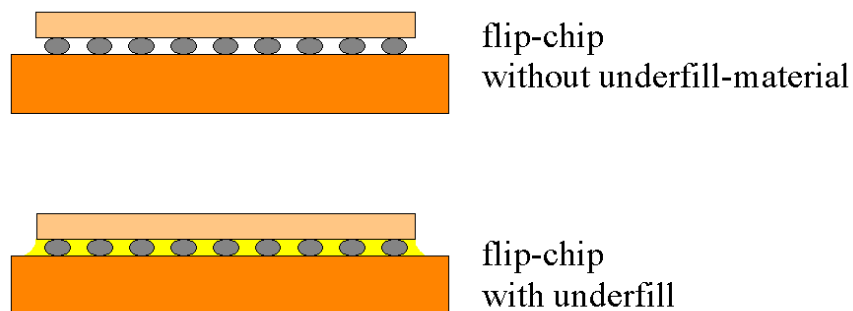


Figure B2. Cross sections of flip chip joints without and with underfill material.

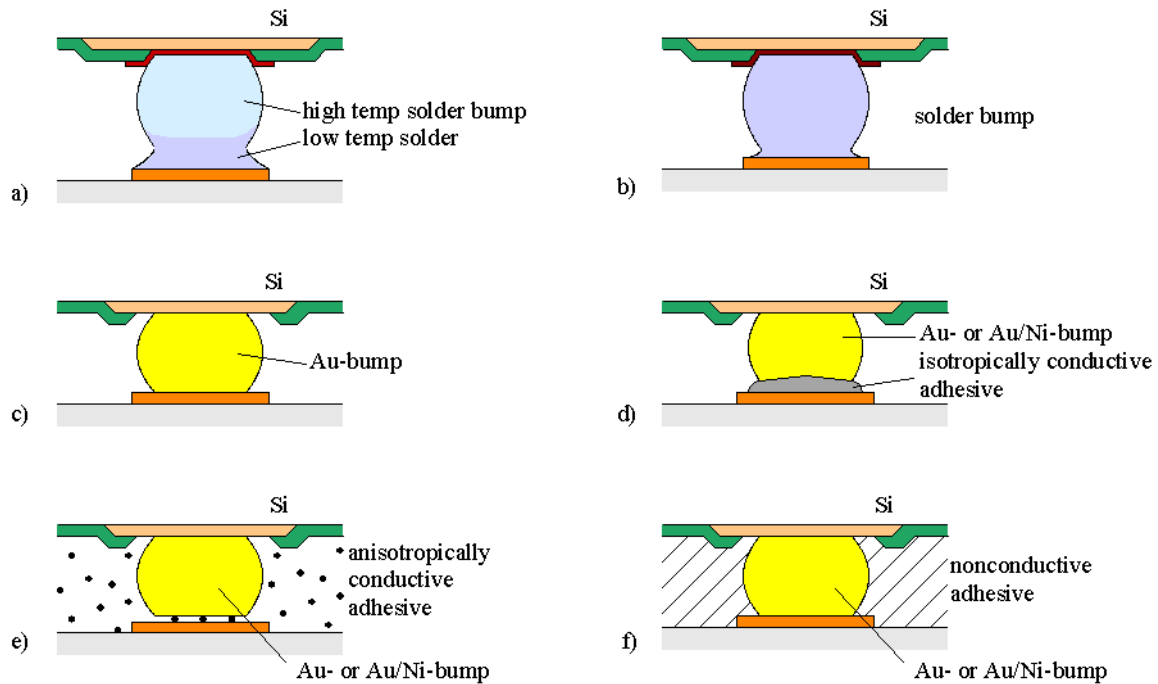


Figure B3. Examples of different types of flip chip joints.

B1.6.1 Flip chip process by solder joining. <LINK TO B2.1>

In flip chip soldering process solder bumped chips are soldered onto the circuit board. Solder is usually, but not always, deposited also on to the substrate pad areas. For fine pitch applications, solder can be deposited e.g. by electroplating, solder ink jet or solid solder deposition. Tacky flux is applied to the solder contact areas either by dipping the chip into a flux reservoir or by dispensing flux onto the substrate. For coarse pitch applications (>0.4 mm) solder paste is deposited on the substrate by stencil printing. The bumps of chips are placed into the tacky paste and they are reflowed in an oven. After the reflow process cleaning of the flux is preferred. The underfill material is applied by dispensing along one or two sides of the chip, from where the low viscosity epoxy is drawn by capillary forces into the space between the chip and substrate. Finally the underfill is cured by heat. Repairing of the flip chip joint is usually impossible after the underfill process. Therefore testing must be done after reflow and before the underfill application. The steps of flip chip soldering process are:

- die preparing (testing, bumping, dicing)
- substrate preparing (flux application or solder paste printing)
- pick, alignment and place
- reflow soldering
- cleaning of flux residues (optional)
- underfill dispensing
- underfill curing.

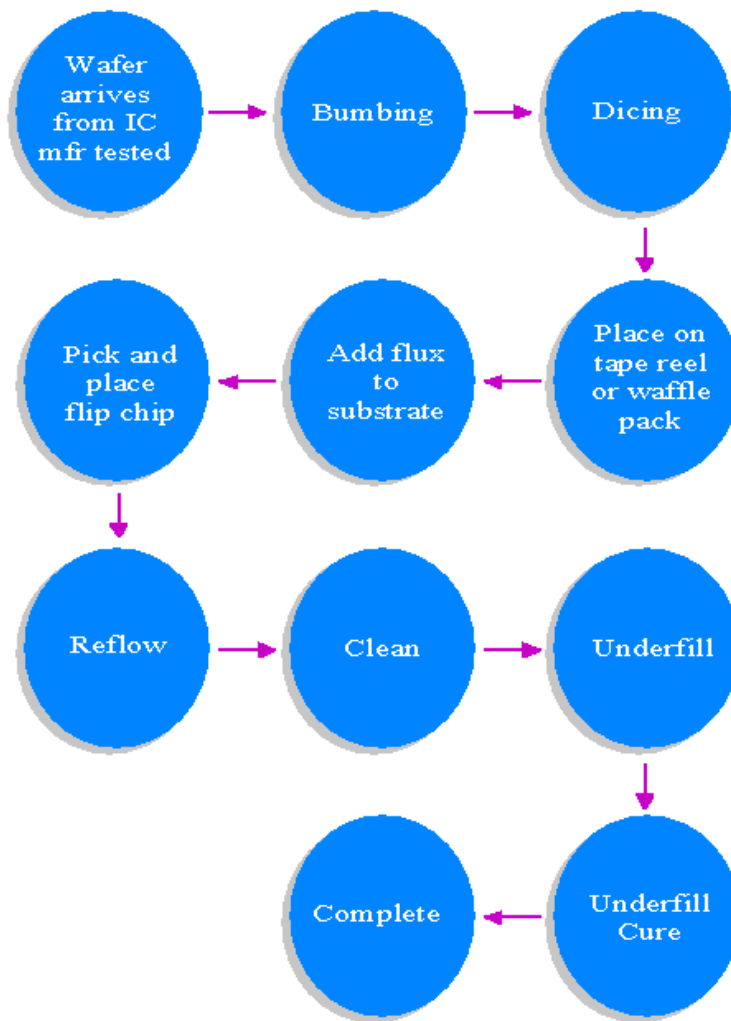


Figure B4. Flip chip soldering process.

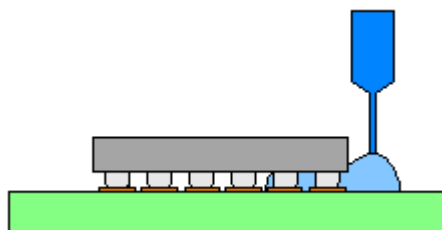


Figure B5. The underfill application by dispensing.

B1.6.2 Flip chip joining by thermocompression. <LINK TO B2.2>

In the thermocompression bonding process, the bumps of the chip are bonded to the pads on the substrate by force and heat applied from an end effector. The process requires gold bumps on the chip or the substrate and a correspondingly bondable surface (e.g. gold, aluminium). The bonding temperature is usually high, e.g. 300 °C for gold bonding, to soften the material and increase the diffusion bonding process. The bonding force can be up to 1 N for an 80µm diameter bump. Due to the required high bonding force and temperature, the process is limited to rigid substrates such as alumina or silicon. Additionally, the substrates must have a high planarity. A bonder with high accuracy in the parallelism alignment is required. In order to avoid pre-damaging of the semiconductor material, the bonding force must be applied with a gradient.

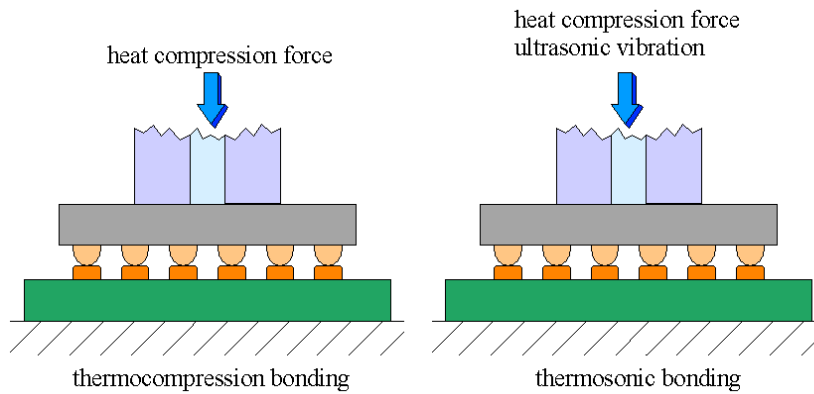


Figure B6. Principles of flip chip joining by thermocompression and thermosonic processes.

B1.6.3 Flip chip thermosonic joining <LINK TO B2.3>

The thermocompression bonding process can be made more efficient by using ultrasonic power to speed up the welding process. Ultrasonic energy is transferred to the bonding area from the pick-up tool through the back surface of the chip. The thermosonic bonding introduces ultrasonic energy that softens the bonding material and makes it vulnerable to plastic deformation. The main benefit of the method compared to thermocompression is lower bonding temperature and shorter processing time. One potential problem associated with thermosonic bonding is silicon cratering. It is generally believed that such damage results from excessive ultrasonic vibration.

B1.6.4 Flip chip joining using adhesives (isotropic, anisotropic, nonconductive) <LINK TO B2.4>

Conductive adhesives have become a viable alternative to tin-lead solders also in flip chip joining. Adhesively bonded flip chip combines the advantages of thin structures and cost efficiency. The advantages of conductive adhesives include ease of processing, low curing temperatures, and elimination of the need to clean after the bonding process. Anisotropically conductive adhesives have also the ability to connect fine pitch devices. Figure B7 shows a schematic drawing of flip chip bonding with isotropically and anisotropically conductive adhesives (ICAs and ACAs). Also nonconductive adhesives can be used for flip chip bonding, in this case the joint surfaces are forced into intimate contact by the adhesive between the component and substrate.

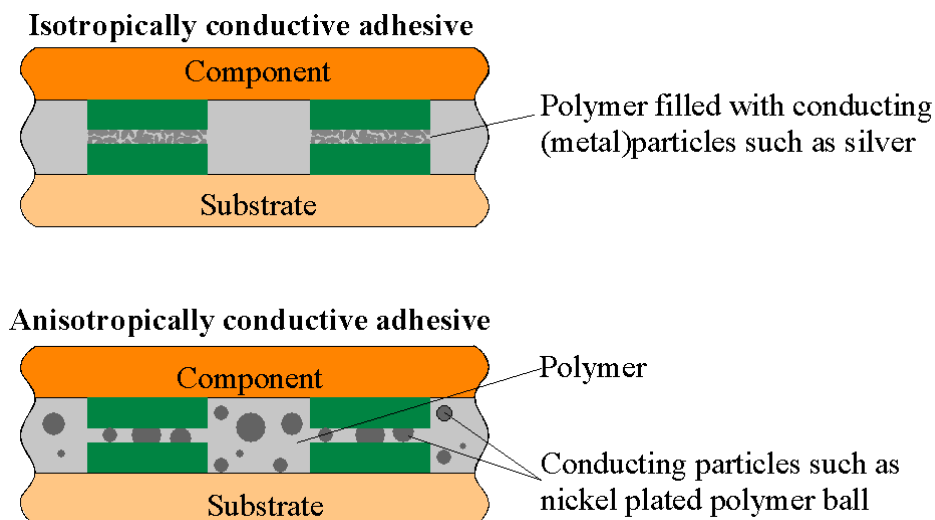


Figure B7. Schematic drawings of flip chip joints made with conductive adhesives.

Isotropically conductive adhesives are pastes of polymer resin that are filled with conducting particles to a content that assures conductivity in all directions. Generally, the polymer resin is epoxy and conducting particles are silver. Anisotropically conductive adhesives are pastes or films of thermoplastics or b-stage

epoxies. They are filled with metal particles or metal coated polymer spheres to a content that assures electrical insulation in all directions before bonding. After bonding the adhesive becomes electrically conductive in z-direction. The metal particles are typically nickel or gold and these metals are also used to coat polymer spheres.

B1.7 Reliability

The different flip chip processes have different aspects concerning the reliability. However, one key factor which has drastically increased the reliability of flip chip structures against temperature variations is the use of underfiller between the chip and the circuit board which, when properly selected and applied, may increase the reliability by more than one decade. The underfill materials, usually filled epoxies, are stiff enough to take part of the forces developed by different thermal expansion coefficients of the chip and substrate. An underfill material also protects the face of the chip against moisture and impurities and makes the structure mechanically stronger.

B1.8 Testing <LINK TO B2.1 TESTING PARAGRAPHS>

The reason for testing is to assure the functionality of the components before and after the flip chip process. The flip chip joined structure should be tested before underfill process when the repairing is still possible

B2. Level 2. Guidelines

B2.1 Flip chip bonding using soldering process

B2.1.1 Design issues

Bumping and UBM processes

Various bumping processes suited for flip chip soldering have been reviewed e.g. by Patterson et al [B3]. The main wafer level bumping processes are evaporated solder bumping, electroplated solder bumping and printed solder paste bumping. Solder ball bumping using slightly modified ball bonder and wire of solder alloy material have also been used.

The deposition of under bump metallurgy (UBM) on to the pad areas of the chip is a very important issue to allow bump formation and to stand the flip chip soldering process. The under bump metallurgy has various functions. It must allow good enough adhesion to the pad metallisation which usually is aluminium. It must act as a diffusion barrier during the soldering process, allow good wettability of the solder material and prevent oxidation of the surface. For different bumping processes different under bump metallurgies are used. Table B1 summarises the features of each solder deposition processes in terms of under bump metallurgy.

Table B1. Under bump metallurgies used for different bumping processes [B3].

UBM	Evaporated (typical of C4)	Plating I	Plating II	Solder paste printing (typ FCT)	Electroless nickel
Adhesion layer	Cr	TiW	CrCu	Al	Ni
Solder diffusion layer	Phased Cr-Cu	Cu stud/mini bump	CrCu	Ni	Ni
Solder wettable layer	Cu	Cu	Cu	Cu	Au
Oxide prevention	Au	Au	Au	Cu	Au
Suitability for 63SnPb	No	Poor	No	Yes	Yes
Use with probed wafers	No	No	No	Yes	Mixed

In evaporated solder bumping process a metal mask (typically molybdenum) is used to make the deposition of UBM layers and the solder alloy onto a silicon wafer with normal passivation as well as polyimide passivation (see Figure B8). The process includes sequential evaporation of chromium, a phased chromium/copper layer, a copper layer and a gold layer to form the UBM. A high lead solder layer is then evaporated on top of the UBM to form a thick deposit of 97PbSn or 95PbSn.

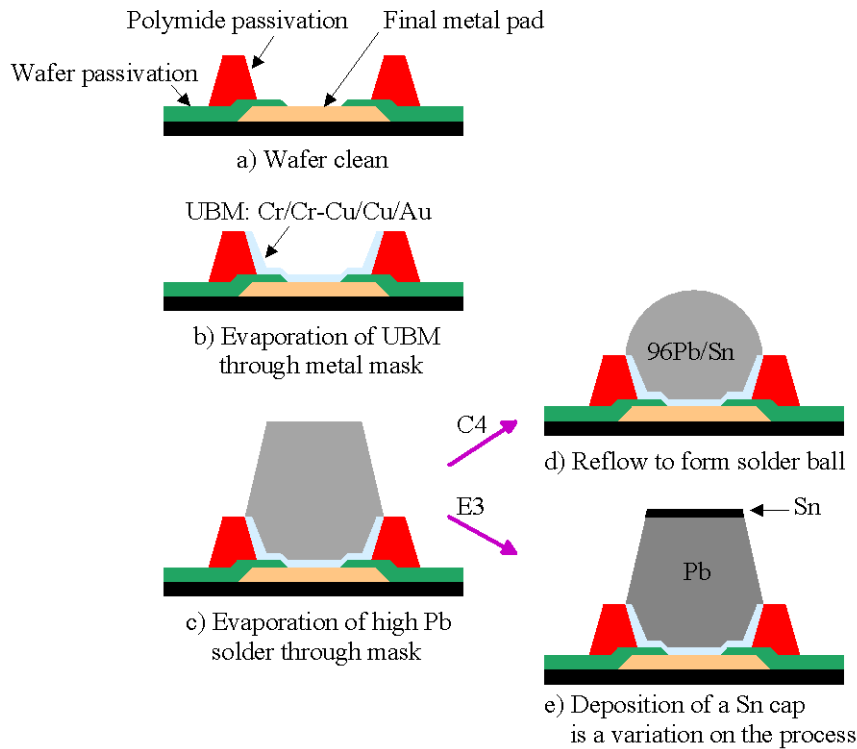


Figure B8. Evaporative solder bumping process [B3].

Electroplating is a popular alternative to the evaporation process because of its lower cost, facility and floor space requirements. One of the various process alternatives is schematically shown in Figure B9. The UBM materials used are typically TiW, Cu and Au sequentially sputtered or evaporated over the entire wafer. The UBM adheres to the wafer passivation as well as to the bond pads. Patterned photoresist is then applied to allow plating of copper minibump onto the UBM metallisation. A second mask allows then the formation of the plated solder bump, after which the photoresist is stripped. The UBM which is on the entire wafer is removed from the areas other than pad areas by wet etching. Finally the bumps are formed by reflow

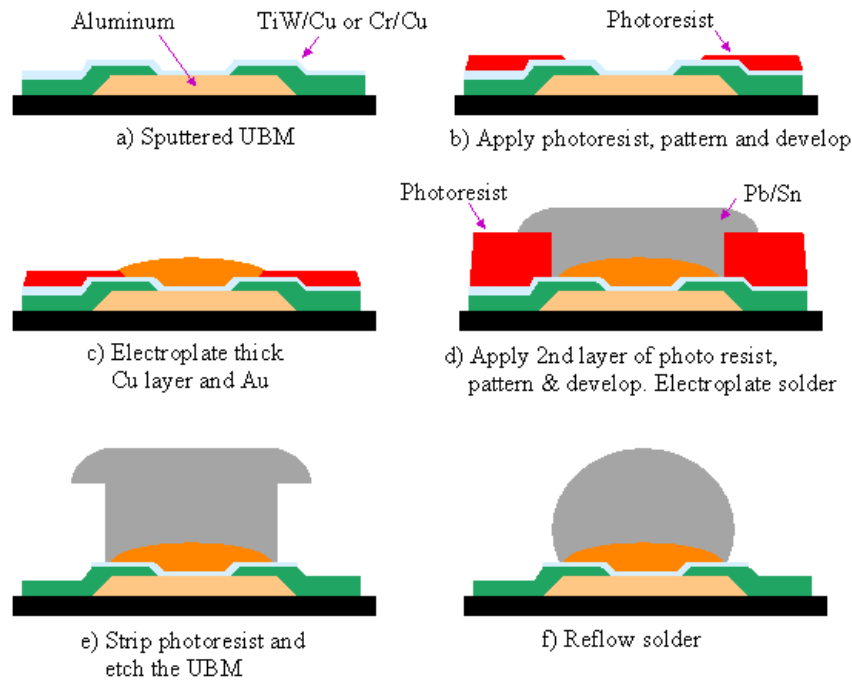


Figure B9. Solder bumping by electroplating process.

The formation of the bump by stencil printing of solder paste is a practical process which is suited for many types of solder materials including 63SnPb. The UBM layers are deposited by sputtering. The first layer is sputtered aluminium followed by sputtered layers of Ni and Cu. A layer of photoresist is applied, patterned and developed. The Al, Ni and Cu-layers are then etched away except over the bond pad passivation openings. The photoresist is removed leaving the UBM over the pad areas. Solder paste is then printed onto pad areas and reflowed to form the spherical bumps.

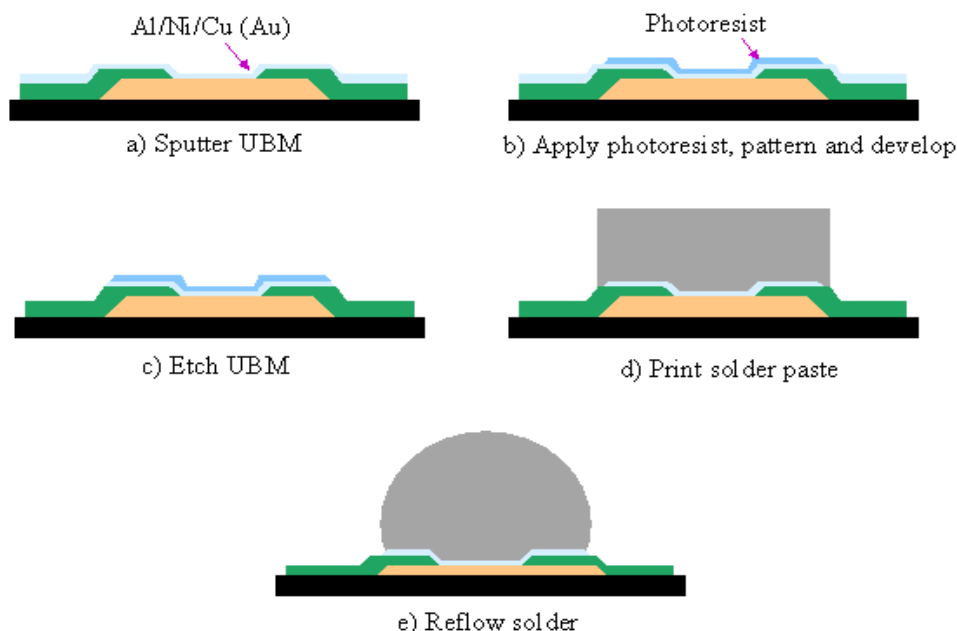


Figure B10. Sputtered UBM and solder paste bumping process..

The company Flip Chip Technologies has design guide <LINK TO <http://www.flipchip.com>>, which gives advice for selecting between available bumping materials, explains the geometrical restrictions and die pad design standards, bump placement, resistance and shear test patterns, alignment key specification and

placement as well as wafer passivation requirements. Various test die (peripheral or array type) and substrates available for evaluation and reliability testing. Compatibility of the solder material with the substrate material is very important. FR4-substrate, for example, can not stand the high temperature reflow temperature of Pb95/Sn5. If high temperature solder is used for bumps, low temperature solder alloy must be applied to the substrate to make possible a low temperature joining process. The minimum pitch obtained for perimeter pad layout is about 200 μm whereas for the area array layout the minimum pitch is about 250 μm .

In almost all dies the pads are peripherally located because of the wire bonding applications. For flip chip bonding the number of I/O can be increased by applying area array pad layout. The redistribution of the pad layout from peripheral arrangement to area array arrangement is possible by doing extra redistribution circuitry onto the die prior to bumping process.

Maximum current density for solder bumps is approximately 4200 A/cm². Typical bump heights are 125 - 140 μm depending of pitch and the bump height tolerance $\pm 15 \mu\text{m}$.

Substrate metallization

The metallization on the substrate must be solderable to the solder material used in the bumps. If the matching lands on the substrate are copper, they are usually plated with tin-lead, tin or gold. If gold is used as the metallization on the substrate, its thickness should be limited to 1 - 2 μm in order to limit the formation of brittle gold-tin intermetallic compound. If bare copper is the metallization, it may be desirable to coat the lands with molten solder by a solder levelling process to improve solderability and increase the volume of solder for a more compliant joint. However if such a process is used, care must be taken to insure uniformity of deposited solder height and volume among all the lands for a given chip, since deviations greater than 50 μm may lead to open circuit conditions after the reflow assembly process step.

Heat

Maximum recommended junction temperature is 140 °C without underfill and 150 °C with underfill. The thermal resistance for one joint is 1000 - 1500 °C/W. The thermal resistance from chip to substrate through the flip chip joints may be roughly obtained by dividing the thermal resistance of one bump by the number of bumps in the chip. This is the worst case situation because there are also other routes of heat flow which may affect the cooling of the chip. Extra dummy bumps increase the cooling efficiency. High thermal conductivity underfills can be used. When efficient cooling is needed like in high power processor packages back side of the chip can be used for thermal management of the package [B4,B5]).

In a 144-pin plastic pin grid array (PGA) package containing a flip chip bonded 10 x 10 mm silicon test die with 82 peripheral bonding pads bumped with 97%Pb3%Sn solder bumps allowable power dissipation in the package was found to be between 1.7 and 6.7 W in free air and between 2.1 and 13.7 W in air flowing at speed of 1.27 m/s. The highest power ratings were possible using a heat sink connected to the lid of the package and a thermal pad between the chip and the lid. The inclusion of underfill material did not enhance the package thermal performance significantly [B6].

Speed

The flip chip assembly is ideal for high frequency applications because of the very short current path between the component and the substrate. For solder joined flip chip connections the joints are metallurgical joints with series resistance of the order of 1 m Ω . The series inductance is very much smaller than that of wire bonded joint or leaded package. For typical leaded package the series inductance is from 5 to 10 nH while that for flip chip solder joint is only about 0.025 nH. Because of the smaller capacitance, smaller inductance and smaller resistance of the flip chip joints compared with wire bonded joints the propagation delay is also considerably smaller in the flip chip structure. In Table B2 there is a comparison of inductance, capacitances, resistance and propagation delay in two types of packages: Pin grid arrays (PGA) with wire bonded chip and ball grid arrays (BGA) packages with flip chip bonded chip. [B7]. The bumps represent the main discontinuity to the signal propagating on the line which results in partial loss, reflection and possibly distortion of the signal. In principle the bump dimensions can be used as impedance matching parameters to achieve minimum losses over a wide frequency band [B8].

Table B2. Comparison of inductance, capacitance, resistance and propagation delay for PGA packages with wire bonded chip and BGA packages with flip chip bonded chip [B7].

Property	Worst case		Best case	
	PGA with wire bonded chip	BGA with flip chip bonded chip	PGA with wire bonded chip	BGA with flip chip bonded chip
Inductance	19.6 nH	7.9 nH	5.6 nH	0.3 nH
Capacitance	15.9 pF	6.2 pF	9.1 pF	2.5 pF
Resistance	21.0 m Ω	2.1 m Ω	20.2 m Ω	1.7 m Ω
Propagation delay	946 ps	243 ps	508 ps	51 ps

Noise

Generally there are good reasons to assume that solder joints used in flip-chip joining do not generate harmful noise. In digital CMOS processor designs the power supply noise is determined by the core and input drivers and by their ability to draw instantaneous current from the supply and on the way how the on-chip power distribution structures interact with the package and board design. As reported by H. Hashemi and D. Herrell [B9] the flip chip connections, when compared to the wire bonded design, improve the power disturb performance by at best a factor of two. This is because the on-chip and on-package power grid distribution inductance can dominate the low inductance of the flip chip connections. They found that on-chip decoupling capacitors in conjunction with a substantial on-chip power grid structure can provide a much lower noise environment for both wire bonded as well as flip chip connected devices.

Reliability

The main reliability factor is thermal fatigue of solder joints. Other possible failure mechanisms are corrosion at the joints or metallisations and migration of atoms caused by electric fields or thermal gradients in the structure. Alpha particles can be a possible cause of failures for memory chips.

Thermal fatigue depends strongly on the solder material, on the thermal expansion difference of chip and substrate, the height of solder joint and on the distance of solder joint from the neutral point of the joined structure as well as on the range of temperature changes in the environment. The underfill material used between chip and substrate increases drastically the reliability of the joints for thermal fatigue. The thermal fatigue behaviour of different solder compositions are compared in table B3. Indium based solders which are fatigue-resistant are, however, not reliable in high-humidity environments.

Table B3. Relative fatigue life of different solder materials [B10].

Solder material	Relative fatigue life
40Pb60Sn	1
95Pb5Sn	3
50In50Pb	6
5In95Pb	10
In	60

Thermal fatigue of solder joints is an important reliability issue for flip chip joining when no underfill material is used. Properly selected underfill material blocks out part of the thermally induced deformation in the joints to such an extent that the fatigue damages are no more clearly dependent on the distance of the joint from the neutral point of the structure. By taking stress into itself the underfill material transfers part of the deformation to deformations in the chip and substrate. In some cases the stress in the chip may become large enough to cause cracking of the chip. The amount of die stress depends mainly on substrate material and on surface quality of the silicon die [B11]. FEM-analysis methods for reliability estimation [B12], empirical reliability modelling equations [B13] or available PC-software tools [B14] can be used to life time estimation of solder joints in cyclic temperature variation. For critical applications comparative accelerated reliability tests are recommended [B15].

Testing

The flip chip bonded components should be tested before the curing of underfill material. Once the underfill material has been cured the removal of a faulty chip is extremely difficult. Testing of the ICs even prior to flip chip bonding is desirable because joining of functional components (i.e. known good die) minimises the need for rework.

There are still some technical and infrastructure obstacles with known good dies which need to be overcome. Traditionally ICs are tested fully and burned-in after packaging since it is much easier to perform final testing of the chip in its package form. From a business standpoint most companies are not interested in selling bare die since part of their profit is derived from the package and it is difficult to guarantee the quality of bare dies. [B16]

There are basically two ways to test and burn-in for the known good dies: (1) at the wafer level and (2) at the individual chip level. Because of the power distribution, cooling and wafer contact problems, test at high speed and burn-in of chip at wafer level poses a technical challenge. Testing of individual dies has several challenges, too. Test at high speed and burn in for individual bare chip using sockets, probe cards etc. may damage the pads on the chip, limit high frequency capability and increase cost. Built-in self testing (BIST) chips and boundary scan test of innerchip connections are under active investigation. [B17]

One solution of producing known good die is to assemble the bare die into temporary "carriers" which serve as temporary single-chip package that allows traditional final test and burn-in infrastructure to be used to achieve quality levels and reliability levels comparable to traditionally packaged ICs. In general, with these methods the die is mounted in a carrier that has the same form as a single chip package. Temporary electrical connection is made at the bond pads and the device is qualified through test and burn-in processes identical to the traditional package part. Once the die is qualified, electrical connections to the bond pads are released and the die is taken from the carrier. [B18] An example of a known good die packaging socket for test and burn-in is shown at the following link <LINK TO <http://www.manudax.fr/WebYamaichi/francais/tb140.htm>>

Maintaining electrical connections to a large array of soft solder bumps can be extremely difficult. Since the mechanisms that cause the connections to fail are accelerated by increased temperature, the connections can be even less reliable than the ICs being tested. The net result is that the data collected from burn-in is contaminated or even dominated by connection failures. One approach to minimise these failures is to use Burn-in and test substrate (BATS) method that has been developed by MCNC Electronic Technologies Division. The BATS method provides a temporary metallurgical connection between the flip chip IC and a reusable carrier. The first generation of BATS is a multilayer ceramic substrate with a cofired thick-film metallurgy that is not wettable by PbSn solders. The top surface is patterned with an array of pads matching the pattern of the IC to be tested. Prior to mounting an IC to the BATS, a thin layer of sacrificial metal is deposited over the nonwetable top surface pads. An IC is then placed on to the substrate and solder reflow is performed resulting a metallurgical joint. Because the connection is a true solder joint, all the requirements for a flip chip testing and burn-in solution are met. After testing and burn-in, the BATS assembly again undergoes the reflow process, at which time the sacrificial metal dissolves into the solder bump, leaving the solder in contact with the nonwetable co-fired metallurgy. This causes the solder to dewet from the substrate surface and the IC can be removed from the substrate. After the IC is removed from the BATS, the sacrificial metal is redeposited and the test substrate is ready for reuse. [B19]

The difficulty in bare die testing and burn-in results in extra cost and therefore known good dies are usually more expensive than packaged components. Some semiconductor manufacturers also offer die products that have been only minimally tested. These dies are offered in volume at prices that are below packaged part's pricing. On the other hand, the manufacturers do not guarantee specific yields for these minimally tested bare dies. [B20]

B2.1.2 Production issues (tools needed, investments, price/performance, training requirements)

In the common flip chip soldering process chips bumped by solder bumps are soldered onto the circuit board. Solder is usually but not always also deposited on to the substrate pad areas. For fine pitch applications, solder can be deposited e.g. by electroplating, solder ink jet or solid solder deposition. Tacky flux is applied to the solder contact areas either by dipping the chip into a flux reservoir or by dispensing flux

onto the substrate. For coarse pitch applications (>0.4 mm) solder paste is deposited on the substrate by stencil printing. Chips are placed into the tacky paste and they are reflowed in an oven. After the reflow process cleaning of the flux is preferred. The underfill material is applied by dispensing and the underfill is cured by heat. Repairing of the flip chip joint is usually impossible after the underfill process. Therefore testing must be done before the underfill application.

For production of circuit boards with solder bumped flip chips the main steps of process are:

- die bumping
- loading of chips and substrates
- pick-up the chip
- flux or solder application
- alignment of chip
- chip placement
- reflow
- underfill-application
- underfill-curing

The assembly of flip chip components needs some special tools compared with normal SMD mounting. The modifications needed are chip handling including flipping the die in the chip loading unit, dispenser flux application or alternatively an extra dipping step and flux reservoir. Underfill-dispensing and curing equipment are also needed. The conventional underfill process is based on flow of underfill material driven capillary forces under the chip. This needs time of several minutes. New more rapid underfill processes and new materials are under development. The accuracy needed in alignment is dependent on the pitch used. The accuracy of modern assembly equipment of $25\mu\text{m}$ (3σ) is sufficient for most applications. Also the self alignment behaviour of solder material lowers the accuracy requirement. For reflow soldering conventional reflow ovens used in SMD process can be used.



Figure B11. Flip-chip assembly line containing a separate flux dispensing unit. (Photo courtesy of Asymtek.)



Figure B12. Underfill process facility. (Photo courtesy of Asymtek)

B2.2 Flip chip bonding using thermocompression

For some applications such as chip-on-glass for displays, soldering might not be a preferred technology, and alternative approaches have been developed. Most of solderless flip chip technologies connect a component to a substrate through adhesive, thermocompression or thermosonic bondings. These technologies possess the following advantages: 1) a simple, fluxless, dry process, 2) a low processing temperature, 3) a high operation temperature, 4) no lead content, and 5) very fine-pitch connections.

B2.2.1 Design issues

Bumping

The preferred bump material for thermocompression flip chip bonding is gold. These bumps can be made using the conventional electrolytic gold plating (used for TAB bumps) or the stud bumping method. The gold ball bumps (see Figure B13) are fabricated with a flexible low cost bumping technique based on the conventional wire bonding procedure. Established wire bonding machines can be used; therefore, expensive bumping process equipment for sputtering lithography and plating is not necessary. The gold wire must be alloyed with 1% Pd to ease the breaking of wire above the bump. During bump formation the wafer/substrate must be heated to 150... 200°C.

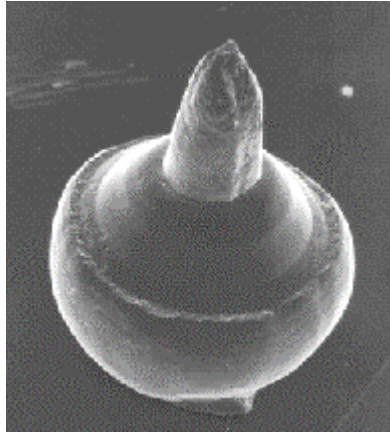


Figure B13. SEM-image of a stud gold bump.

Substrate metallization

The pads on the substrate must have a correspondingly bondable metallization, e.g Au-plating or aluminium (silicon substrates). Additionally, the substrates must have a high planarity.

Heat

See the Flip chip bonding using soldering process/Heat chapter <link to B2.1.1>

Speed

See the Flip chip bonding using soldering process/Speed chapter <link to B2.1.1>

Noise

See the Flip chip bonding using soldering process/Noise chapter <link to B2.1.1>

Reliability

The critical factors determining the reliability of thermocompression bonded chips are similar to bonding with solder joints, e.g. the difference of TCEs between the chip and the substrate, the height of joints and the maximum distance between joints. It is likely that most of the damages (cracks) to the bond area are created during the cooling from the high bonding temperature. The susceptibility to fatigue damage of gold is much lower than that of solder due to its much higher melting temperature, so if the adhesion strengths between the bump and the pads are not exceeded during thermal cycles the reliability would not be a problem.

The underfill material used between chip and substrate increases drastically the reliability of the joints for thermal fatigue. Thermal fatigue of joints is an important reliability issue for flip chip joinings where no underfill material is used.

Testing

See the Flip chip bonding using soldering process/Testing chapter <link to B2.1.1>

B2.2.2 Production issues

A flip chip bonder capable of producing the high bonding temperature of 300°C and force of up to 100cN/bump, and with high accuracy in the parallelism alignment is required (this depends, of course on the pitch). In order to avoid predamaging of the semiconductor material, the bonding force must be applied with a gradient. For brittle GaAs devices an optimal gradient of 5-10 cN/s has been found.

In order to achieve good bonding during thermal compression flip-chip attach a certain amount of ball-bump deformation is necessary. On the other hand, the bonding force and temperature should be as low as possible in order to prevent damage of chip and substrate. For example, for GaAs chips the following parameters have been reported for attaching on silicon substrate: bonding temperature 320°C and bonding force 25-100cN/bump. On GaAs the bonding pads were of Al, on the silicon substrate different type of metallisations were investigated: 1µm AlSi, 0.4µm Au or 2µm electrolytic Au.

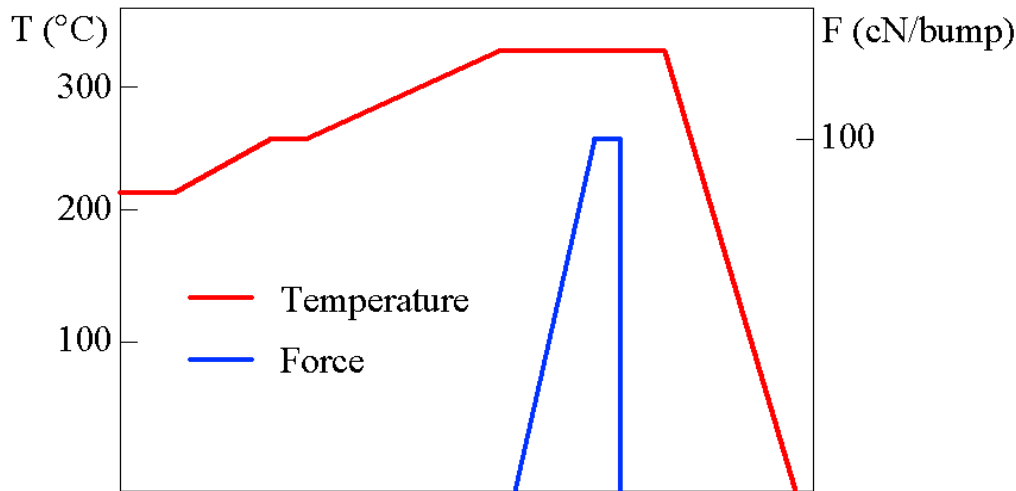


Figure B14. Example of flip chip bonding parameters for TC bonding of GaAs devices.. Stage temperature 320°C, bonding temperature 320°C, max. bonding time 15 s, force gradient 5/10 cN/s.[B21]

B2.3. Flip chip bonding using thermosonic method

B2.3.1 Design issues

Bumping

The preferred bump material for thermocompression flip chip bonding is gold. These bumps can be made using the conventional electrolytic gold plating (used for TAB bumps) or the stud bumping method. The stud bumps are fabricated with a flexible low cost bumping technique based on the conventional wire bonding procedure. Established wire bonding machines can be used; therefore, expensive bumping process equipment for sputtering lithography and plating is not necessary. The gold wire must be alloyed with 1% Pd to ease the breaking of wire above the bump. During bump formation the wafer/substrate must be heated to 150.. 200°C.

Substrate metallization

The pads on the substrate must have a correspondingly bondable metallization, e.g Au-plating or aluminium (silicon substrates). Additionally, the substrates must have a high planarity.

Heat

See the Flip chip bonding using soldering process/Heat chapter <link to B2.1.1>

Speed

See the Flip chip bonding using soldering process/Speed chapter <link to B2.1.1>

Noise

See the Flip chip bonding using soldering process/[Noise](#) chapter <link to B2.1.1>

Reliability

The critical factors determining the reliability of thermosonic bonded chips are similar to bonding with solder joints, e.g. the difference of TCEs between the chip and the substrate, the height of joints and the maximum distance between joints. It is likely that most of the damages (cracks) to the bond area are created during the cooling from the high bonding temperature. The susceptibility to fatigue damage of gold is much lower than that of solder due to its much higher melting temperature, so if the adhesion strengths between the bump and the pads are not exceeded during thermal cycles the reliability would not be a problem.

The underfill material used between chip and substrate increases drastically the reliability of the joints for thermal fatigue. Thermal fatigue of joints is an important reliability issue for flip chip joining when no underfill material is used.

Testing

See the Flip chip bonding using soldering process/[Testing](#) chapter <link to B2.1.1>

B2.3.2 Production issues

Thermosonic flip-chip bonding has a great potential, but it is a high-risk approach. The bonding process involves complicated interactions between pressure, temperature, ultrasonic vibration, and planarity. These interactions make the design of the system end effector challenging.

Compared with soldering and other solderless connection methods, thermosonic flip chip bonding has several advantages:

- 1) simplification of the processing and assembly steps;?
- 2) increase in the number of choices for contact and bonding materials;
- 3) reduction in the levels of assembly temperature, pressure and time;
- 4) enhanced current-carrying capability and high temperature resistance.?

Yatsuda et al. [B22] have reported a bonding temperature of 200°C, force of 60 g/bump and ultrasonic power of 2 - 4 W for 0.5 s for SAW chip bonded on alumina (Figure B9). Results of reliability tests were also reported: no failures during thermal shock cycling between -30 °C...+85 °C (liquid to liquid, 1000 cycles) were observed. The effect of two different bond pad metallisations, 1.5 µm Al and 0.5 µm Au, were also investigated. The gold metallisation was found to perform slightly better in tests, however, the difference in behaviour seems to be of minor practical effect.

The method is currently in production use at Japan Radio Co. [B23], so it is to be considered as a very potential solution for attaching SAW chips on the silicon substrate. The concerns for the application are the lower Al metallisation thickness (0.2µm) and the higher difference between the TCEs of the substrate and the chip.

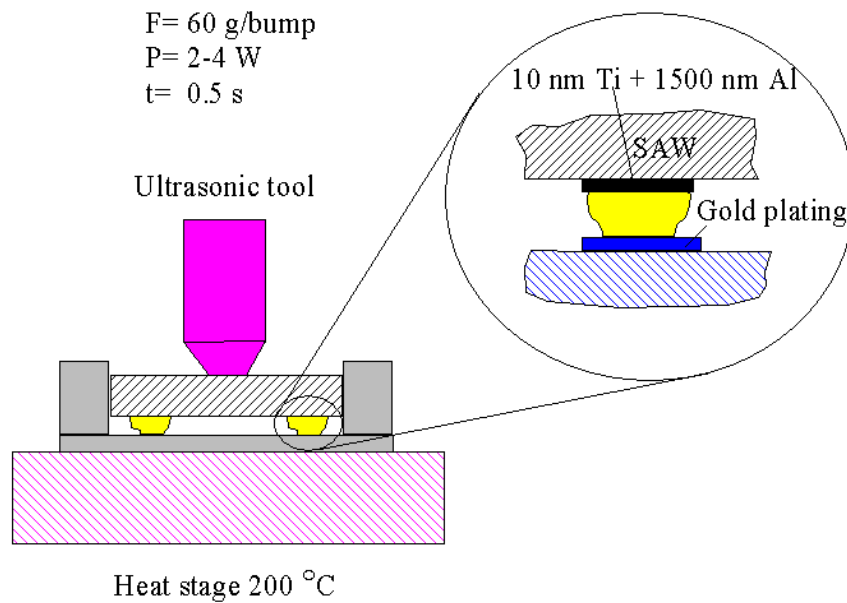


Figure B15. Ultrasonic bonding of SAW as used by Japan Radio Co. [B23].

B2.4 Flip chip joining using adhesives

The adhesive flip chip joining with isotropically conductive adhesives is different from joining with anisotropically conductive adhesives. Therefore the following text is sometimes divided into two parts (ICAs and ACAs). Joining with nonconductive adhesives is not covered because its practical use has so far been very limited. In theory, joining with nonconductive adhesives is very reliable because it decreases the bonding interfaces to a minimum. The situation is different in practice, however. The process is difficult to handle and the joints suffer from reliability problems. For example, the planarity requirements for substrates are much more critical when bonding with nonconductive adhesives than when bonding with ACAs and ICAs.

B2.4.1 Design issues

Bumping

Flip chip technology requires conductive bumps which are added to the contact pads on the semiconductor components. The preferred bump material for adhesive flip chip joining is gold. More information on gold bumping is given in chapters 2.3.1 <LINK TO B2.3.1>. Also isotropically conductive adhesives can be used as the bumping material (Figure B16). With this solution it is important not to apply the adhesive bump onto Al-metallisation because aluminium oxidises easily (even underneath the adhesive) and the joints eventually become nonconducting.



Figure B16. SEM-photograph of a polymer bump made with isotropically conductive adhesive. The bump height is approximately $45 \text{ }\mu\text{m}$.

Heat <link to C2.3.2>

Both ICAs and ACAs are inferior thermal conductors when compared with tin-lead solders. The thermal conductivity of ICAs ranges between 2 and 10 W/m·K. For ACAs the thermal conductivity is around 1 W/m·K. Tin-lead solders have a thermal conductivity between 35 and 50 W/m·K. In practice, however, the thermal resistance of a component is not increased by much if solder flip chip bonding is replaced by adhesive flip chip bonding. Only a small amount of the generated heat in a component is transferred through the flip chip joints and the thermal resistance is governed by other factors such as chip size and substrate material. <LINK TO B2.1.1 HEAT PARAGRAPH>

Speed <link to C2.3.1 and C2.3.13>

The electrical conductivity of ICAs and ACAs is also inferior to tin-lead solders. ICAs have about one magnitude greater volume resistivity than eutectic tin-lead solder ($R_{vol}=170 \cdot 10^{-6} \Omega \cdot \text{cm}$). The studies at VTT Electronics have shown that the resistance of an ICA flip chip joint is in the range of a few milliohms. [B24] There is no literature available on adhesive flip chips joints inductance or capacitance. However, it can be estimated that the use of ICAs will somewhat increase the electrical values in Table B2. <LINK TO TABLE B2>

For ACAs no volume resistivity is given, because the adhesive is not conductive until it has been used to join two surfaces. The use of ACAs has been popular in joining fine pitch heat seals and other such connectors for almost a decade. Such applications do not require minimal electrical resistance. Research has also shown that ACA flip chip joint can have adequate electrical resistance for component joining [B25].

There is ongoing research on the rf-properties of adhesive joints at IVF and some of the results have already been published. For low frequency applications (500 MHz-8 GHz) the results indicated that the ACA flip chip joint and the bridge joint mounted on the FR-4 board or the flexible board can be used. For high frequency applications (1 GHz-40 GHz) the results showed that the ACA flip chip joint and the bridge joint mounted on the high frequency teflon based duroid substrate can be used. [B26]

Noise

The noise properties of adhesive flip chip joints have not been widely researched. Solder joints are low noise joints and it is speculated that the use of adhesives will increase the noise in a flip chip joint. On the other hand, this noise increase may not have any affect on the components performance.

Reliability <link to C2.5, C2.6 and C2.3.13>

Generally, humid conditions cause most reliability problems with adhesive flip chip joints. Typical failure mechanisms are induced by diffusion of water molecules into adhesive layer as well as into the interface between substrate and adhesive. This causes an irreversible decrease of mechanical and adhesive strength, a reversible increase of plasticity, a decrease of glass transition temperature and swelling. Even corrosion of bumps or substrate metallisation can occur. [B27] This will increase the joints electrical resistance which can eventually lead into an open circuit. The use of gold metallisations will decrease failures in humid conditions (Figure B16).

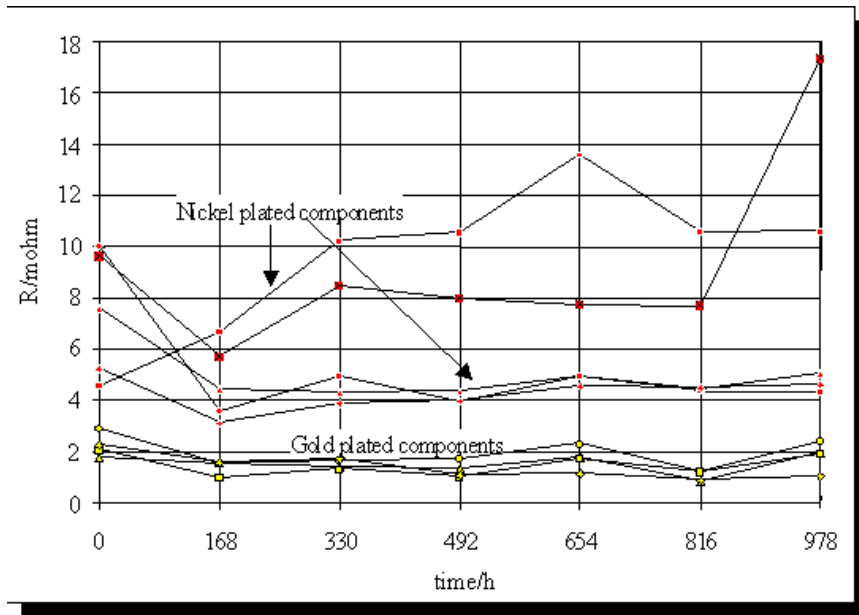


Figure B17. The effects of ageing at 85%RH/85°C on the junction resistance of ICA joints of Au- and Ni-plated components bonded on to thick film Au-metallisation. These results are from die bonded components.

In contrast to ACAs, where most failures are accelerated by humidity testing, temperature cycling is more critical for ICAs. Failures occurring at thermal cycling tests are introduced by component's and substrate's different thermal expansion coefficients. This results shear strain inside the adhesive layer. In case of ICA the stresses may lead to an adhesion failure of single bumps. Fortunately, the use of an underfill material drastically increases the reliability of an ICA flip chip joint (Figure B18).

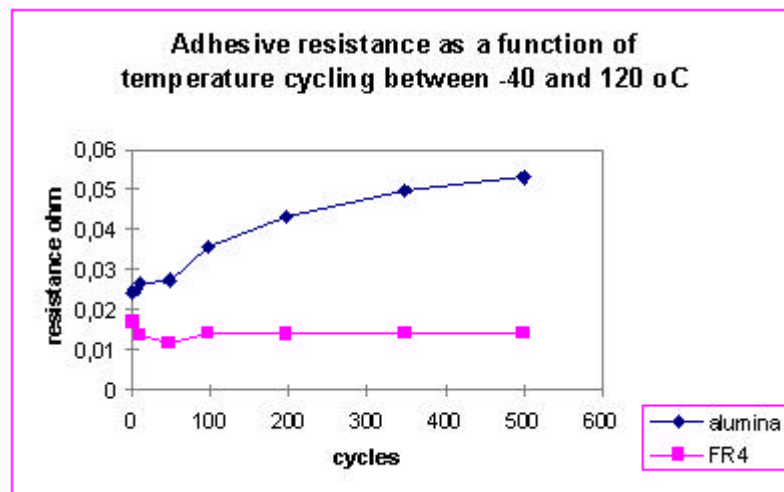


Figure B18. The resistance of adhesive joint as a function of the number of temperature cycles between temperatures -40°C and 120°C . The components have Au-stud bumps. They have been flip chip bonded with an ICA and underfilled.[B28]

Testing

Please, see chapter 2.1.1 and its testing paragraphs. <LINK TO CHAPTER 2.1.1 TESTING PARAGRAPH.>

B2.4.2 Production issues

Flip chip joining with ICAs resembles the production with solders. The isotropically conducting adhesives, however, have no self-aligning but adhesive curing is much more simple than solder reflow. In production the main steps of processes are:

- die bumping,
- loading of chips and substrates,
- pick-up the chips,
- adhesive application and an optional step of thermoplastic adhesive drying,
- alignment and placement of chip,
- adhesive cure (thermosetting) or adhesive bonding (thermoplastic),
- underfill application,
- underfill cure.

The current commercial ICAs have either a thermosetting or thermoplastic polymer matrix and they are usually supplied as a paste. The thermoplastic adhesives have some interesting advantages such as reworkability and a long shelf life (typically 1 year) in one-component package at room temperature. The adhesives can be applied on bumps or on substrate metallisations by dispensing, stencil printing or dipping (Figure B18). Adhesives will wet metallic as well as nonmetallic surfaces and thus adhesive spreading will not be restricted by metallisation pad size on chip or substrate. This can easily lead to short circuiting if preventive measures are not taken. When the adhesives are dispensed high yields are attained with pitches such as 300 μm or 400 μm . Smaller pitches, such as 200 μm , have also been attained with ICAs. The stud bump adhesive joining process in Figure B18 is especially suitable for fine pitch applications.

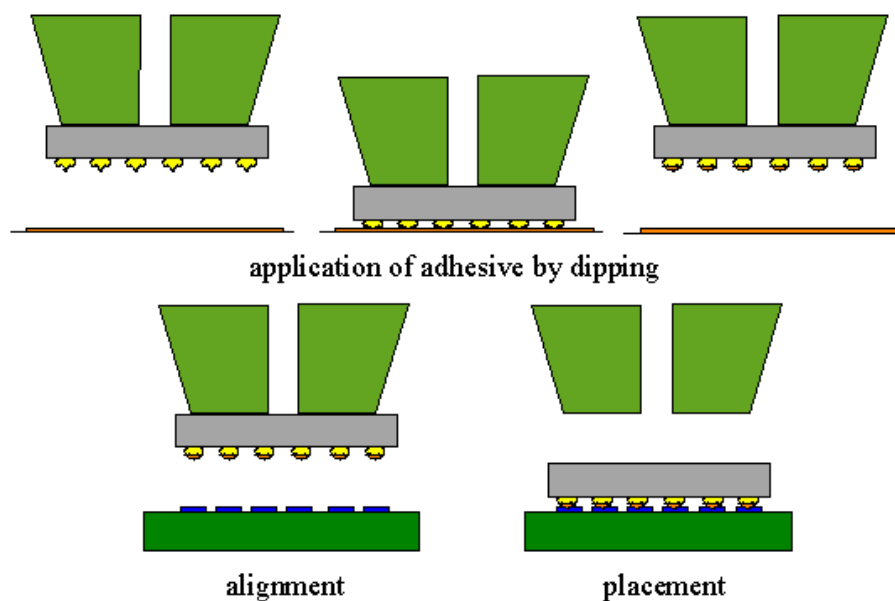


Figure B19. Stud bump adhesive joining process.

The bonding process is a little different for thermosetting ICAs and for thermoplastic ICAs. The thermoplastic polymers consist of long polymer chains and therefore the rheological properties of the adhesives have to be modified with a substantial use of solvents. These solvents often need to be dried after the adhesive has been applied onto the flip chip bump. After drying the adhesive it is possible to store the components or substrates and make the adhesive bonding later, perhaps even in some other factory. When thermosetting adhesives are used the time span between adhesive application and chip placement should be as short as possible.

To cure a thermosetting material a transfer of energy into the polymer is required. This energy is usually supplied by external heat from an oven. During the curing process no pressure is needed to keep the

components in place. The curing temperature ranges typically from 80 °C to 200 °C and the cure time from 5 minutes to some hours. Adhesives usually have many optional cure schedules. A common rule of a thumb is that a decrease of 10 °C or 20 °C in curing temperature doubles the cure time. To cure the adhesives also infrared or ultraviolet energy can be used.

Bonding with a thermoplastic adhesive is a heat/pressure process. Flip chip bonding typically lasts some seconds. The adhesive manufacturers supply instructions of the suitable heat, pressure and time. As the attach temperature rises, the attach pressure and time can be decreased. Thermoplastic adhesives can bond over a broad process window-as low as 100 °C and up to over 300 °C. Bonding limits lie between the glass transition temperature of the polymer and its decomposition point. Applied pressure forces the softened or liquefied polymer into the surface microstructure of the adherents, producing a mechanical link. The time factor, or dwell, allows heat to distribute at the interface and the fluid polymer to penetrate to surface microstructures. The triad key of bonding parameters, temperature, pressure and time are interactive as mentioned earlier, but they are also non-linear. Temperature has the most pronounced effect.

After flip chip joining with ICAs an underfill material can be applied. In practice the use of an underfill material is necessary because the bonding strength of ICA joints is seldom enough to reliably hold the chip in place.

As mentioned earlier, the anisotropically conductive adhesives have been used in pitches down to 100 µm. The risk of short circuiting is minimal because the adhesive joints are conducting only in z-direction. Flip chip joining with ACAs has the following main steps of processes:

- die bumping,
- loading of chips and substrates,
- pick up the chips,
- adhesive application,
- placement of chip,
- adhesive bonding.

Most ACAs have a thermoplastic polymer matrix but there are also thermosetting ACAs. The adhesives are supplied as a paste or as a film. The use of films is more popular because in them the conductive particle distribution is more constant than in paste adhesives. Bonding with ACAs always requires the use of pressure in addition to temperature and it is similar to bonding with thermoplastic ICAs. The ACA also acts an underfill material which simplifies the assembly process.

When flip chip bonding with ACAs, co-planarity between the substrate and the component is critical. Tests with a non-parallel thermode have shown that the yield and die reliability decrease significantly. Additionally, the assembly yield is affected by bump height variations. For large height variation, some of the bumps with low heights might not be pressed for good bonding which results in higher contact resistance. On the other hand, some of the bumps with large heights might be pressed too much and the particles will be destroyed in this region. The top surface of the bump must be as flat as possible, especially when the particle size is small.

B2.5 Environmental issues <link to C1.6.4 and C2.7>

The environmental issues, such as material handling and waste disposal, are governed by the used materials not the technology. The use of flip chip joining has been, however, encouraged with external environmental arguments. With flip chip technology the size of the manufactured devices is decreased which cuts down the use of raw materials. Nevertheless, companies do not change to flip chip technology for purely environmental reasons. The environmental arguments can motivate the use of adhesives in flip chip joining, because adhesives generally provide a leadfree alternative. Leadfree solder bump materials are also available from Flip Chip Technology CASTIN® (Cu/Ag/Sb/Sn).

B3. Level 3. Background information

B3.2 Papers

Technical paper library (<http://www.flipchip.com/flipsec4/library.htm>)

"Reliability of Fine Pitch Solder Bump Flip-Chip-on-Flex: Design and Assembly Techniques, Part 1" by Deborah Patterson, Richard Moraca, Hong Yang, Kate Medlock, Hazel Schofield, Martin Christie, Tony Cowburn and Colin Thompson, GlobalTRONICS 1998, Singapore, October 5-9, 1998.

"Flex-On-Cap Solder Bump for Manufacturability and High Reliability" by Thomas Goodman and Peter Elenius, IMAPS Nordic '98, Stockholm, September 20-23, 1998.

"Wafer Bumping Technologies – A Comparative Analysis for Solder Deposition Processes and Assembly Considerations" by Deborah S. Patterson, Peter Elenius, James A. Leal, INTERPack '97, June 15-19, 1997, EEP-Vol. 19-1, Advances in Electronic Packaging – 1997, ASME 1997, pp. 337-351.

"Flip chip bumping for IC Packaging Contractors" by Peter Elenius, March 1998.

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B3.3 Other links

Bumping Service Design Guide of Flip Chip Technologies (<http://www.flipchip.com>)

Known good die including flip chip literature (<http://www.imec.be/kgd/>)

B4. Level 4. References

B4.1 Recommended reading

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D. Patterson, P. Elenius and J. Leal, "A Comparative Analysis – Solder deposition process and assembly wafer bumping – part II", EPP Printed Circuit Board, May 1998, 30 – 36.

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J. H. Lau, "Solder Joint Reliability of Flip Chip and Plastic Ball Grid Array Assemblies Under Thermal, Mechanical, and Vibrational Conditions," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19 Nov. 1996, 728-35.

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K. Kulojärvi, V. Vuorinen and J. K. Kivilahti, "Effect of Dissolution and Intermetallic Formation on the Reliability of FC Joints," ISHM-Nordic, Oslo (1997).

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B4.3 List of key conferences

Flip Chip Technologies Volume 1, 2 Day Tutorial, Munich, Germany, Nov. 11-12, 1996, Pac Tech - Packaging Technologies GmbH, Fraunhofer - Institut für Zuverlässigkeit und Mikrointegration.

1st Netpack Meeting, December 15 1993, Brussels.

2nd Netpack Meeting, June 7, 1994, Windsor.

3rd Netpack Meeting, October 20, 1994, Berlin.

4th Netpack Meeting, May 17, 1995, Copenhagen.

5th Netpack Meeting, April 2, 1996, Paris.

6th Netpack Meeting, September 18, 1996, Berlin.

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10th European Microelectronics Conference, Copenhagen, 14-17 May 1995.

11th European Microelectronics Conference - EMC '97, 14-16 May 1997.

Area Array Packaging Technologies, Workshop on Flip Chip and Ball Grid Arrays, November 13-15, 1995, Berlin, Fraunhofer- Institute for Reliability and Microintegration

B4.4 Standards

Pending ANSI Approval:

J-STD-012 Implementation of Flip Chip and Chip Scale Technology - Chair, Ray Prasad Concultancy Group, Jan 1996.

New Standards under development as defined in J-STD-012

Std No. 101: Semiconductor Design Standard for Flip Chip Applications.

Std No. 102: Mechanical Outline Standard for Flip Chip or Chip Scale Configurations.

Std No. 103: Performance Standard for Flip Chip/Chip Scale Bumps.

Std No. 104:	Test Methods for Flip Chip or Chip Scale Performance.
Std No. 105:	Flip Chip/Chip Scale Carrier Tray Standard.
Std No. 106:	Bare Dice as Flip Chip or Chip Scale Configuration Management Standard.
Std No. 107:	Design Standard for Flip Chip and Chip Scale Mounting Structures.
Std No. 108:	Qualification and Performance Standard for Flip Chip Organic Mounting Structures.
Std No. 109:	Qualification and Performance Standard for Flip Chip Inorganic Mounting Structures.
Std No. 110:	Test Methods for Qualification and Evaluation of Flip Chip Mounting Structures.
Std No. 111:	Design Standard for Flip Chip/Chip Scale Assembly Configuration.
Std No. 112:	Standard for Flip Chip/Chip Scale Assembly Performance Requirements.
Std No. 113:	Test Methods for Qualification and Evaluation of Flip Chip/Chip Scale Assemblies.
Std No. 114:	Standard for Flip Chip/Chip Scale Assembly Rework and Repair Techniques.
Std No. 115:	Flip Chip/Chip Scale Assembly Reliability Standard.
Std No. 116:	Qualification and Performance of Flip Chip Underfill Materials.
Std No. 117:	Qualification and Performance of Flip Chip Passivation Materials.
Std No. 118:	Qualification and Performance of Flip Chip Encapsulation Materials.
Std No. 119:	Qualification and Performance Standard for Adhesives Used in Flip Chip Assembly.
Std No. 120:	Qualification and Performance Standard for Flux Used in Flip Chip Assembly.

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