A Battery-Powered Activity-Dependent Intracortical Microstimulation IC for Brain-Machine-Brain Interface

Meysam Azin, *Student Member, IEEE*, David J. Guggenmos, Scott Barbay, Randolph J. Nudo, and Pedram Mohseni, *Member, IEEE*

***Abstract*—This paper describes an activity-dependent intracortical microstimulation (ICMS) system-on-chip (SoC) that converts extracellular neural spikes recorded from one brain region to electrical stimuli delivered to another brain region in real time *in vivo*. The 10.9-mm^2 SoC incorporates two identical 4-channel modules, each comprising an analog recording front-end with total input noise voltage of 3.12 μV_{rms} and noise efficiency factor (NEF) of 2.68, 5.9-μW 10-bit successive approximation register analog-to-digital converters (SAR ADCs), 12.4-μW digital spike discrimination processor, and a programmable constant-current microstimulating back-end that delivers up to 94.5 μA with 6-bit resolution to stimulate the cortical tissue when triggered by neural activity. For autonomous operation, the SoC also integrates biasing and clock generation circuitry, frequency-shift-keyed (FSK) transmitter at 433 MHz, and dc-dc converter that generates a power supply of 5.05 V for the microstimulating back-end from a single 1.5-V battery. Measured results from electrical performance characterization and biological experiments with anesthetized rats are presented from a prototype chip fabricated in AMS 0.35 μm two-poly four-metal (2P/4M) CMOS. A noise analysis for the selected low-noise amplifier (LNA) topology is presented that obtains a minimum NEF of 2.33 for a practical design given the technology parameters and power supply voltage. Future considerations in the SoC design with respect to silicon area and power consumption when increasing the number of channels are also discussed.**

***Index Terms*—Activity-dependent microstimulation, brain-machine-brain interface, intracortical microstimulation, neural recording, neurostimulation, spike discrimination, system-on-chip.**

Manuscript received August 24, 2010; revised November 15, 2010; accepted December 15, 2010. Date of publication March 03, 2011; date of current version March 25, 2011. This paper was approved by Guest Editor Ajith Amerasekera. This work was supported by the Department of Defense Traumatic Brain Injury Concept Award Program under Award W81XWH-08-1-0168 and by the American Heart Association under Award 09BGIA2280495.

M. Azin is with the Electrical Engineering and Computer Science Department, Case Western Reserve University, Cleveland, OH 44106 USA.

D. J. Guggenmos, S. Barbay, and R. J. Nudo are with the Department of Molecular and Integrative Physiology and the Landon Center on Aging, Kansas University Medical Center, Kansas City, KS 66160 USA (e-mail: rnudo@kumc.edu).

P. Mohseni is with the Electrical Engineering and Computer Science Department, Case Western Reserve University, Cleveland, OH 44106 USA, and also with the Advanced Platform Technology (APT) Center – A Veterans Affairs (VA) Research Center of Excellence, Cleveland, OH (e-mail: pedram.mohseni@case.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2011.2108770

I. Introduction

In THE PAST decade, significant advancements have occurred in developing engineered devices that bidirectionally interact with the central and peripheral nervous system. Specifically, brain-machine interfaces (BMIs) have been developed for human application that use intrinsic neuronal signals from the brain as input commands to control external devices. Cortical control of the movement of a prosthetic arm or mouse cursor on a computer screen using brain electrical signals have indeed been successfully demonstrated in non-human primates and even in case studies in humans suffering from high-level spinal cord injury [1]–[3]. Other types of BMIs use device-generated electrical signals for stimulation of the nervous system to modulate a particular neural pathway that might be dysfunctional, or to transmit a specific type of sensory information. Deep brain stimulation (DBS), a clinically effective neuromodulation therapy for Parkinson's disease (PD), and neuroprostheses to restore lost sensory functions in blind and hearing-impaired patients fall into this category [4], [5]. Neuroprostheses to restore a lost cognitive function such as memory are also on the horizon [6].

The emergence of BMI technology has been in part enabled by technological innovations in integrated sensor and circuit design over the past few years. Advancements in micro-electro-mechanical-system (MEMS) technology have produced millimeter-sized arrays of microelectrodes containing as many as 100 recording sites that allow long-term, reliable, and stable recording of neural signals [7], [8]. Similarly, novel design methods in application-specific integrated circuit (ASIC) development have recently led to numerous examples of low-power, low-noise, high-performance ICs for recording brain electrical activity [9]–[14], on-chip processing of the recorded neural data [15], [16], and stimulating the nervous system [17]–[21].

While existing BMIs continue to show great promise to improve the quality of life in people suffering from neuropathologies, a new generation of neuroprostheses is now emerging that aims to combine neural recording, signal processing, and microstimulation functionalities in a single device for closed-loop operation. This new category of neuroprostheses can use information extracted from brain neural activity to trigger microstimulation or modulate stimulus parameters in real time, potentially enhancing the clinical efficacy of neuromodulation in alleviating pathologic symptoms or restoring lost sensory and motor functions in the disabled. For example, it has been suggested

that the efficacy of DBS for PD can be increased by optimizing stimulation waveform parameters using a closed-loop global optimization algorithm [22], or that stimulation of the spinal cord directed by cortical neural activity can evoke or facilitate intended movement in the upper limb of paralyzed patients with spinal cord injury [23].

To that end, two discrete board-level devices were recently developed using commercially available hardware to provide refined sensory inputs in closed-loop neuroprosthetic systems [24] and induce neuronal plasticity for functional reorganization in an intact nervous system [25]. Both devices were proven functional in biological tests with awake rodents and primates, respectively. Further, Denison and colleagues have developed an implantable closed-loop microstimulator targeted at titration therapy in DBS [26]. The system incorporates a custom IC for multichannel sensing and analog spectral analysis of local field potentials (LFPs), an auxiliary microprocessor for key biomarker extraction and titration control, and a neurostimulation unit from an existing approved device. Liu and colleagues have proposed another closed-loop microstimulator, incorporating a biomedical multiprocessor system-on-chip (SoC) for real-time spike sorting with principal component analysis and a digitally controlled current stimulating back-end [27]. However, the sensing and digitization front-end is not co-integrated with the rest of the system. Further, neither of these works has yet been tested *in vivo*.

Finally, Flynn and colleagues have reported a 64-channel closed-loop DBS IC, incorporating eight channels of amplification for neural recording and an 8-bit logarithmic analog-to-digital converter (ADC) for digitization [28]. Similarly, Genov and colleagues have recently reported a single-chip 128-channel system that can be configured for fully differential recording and digitization of neural data as well as voltage-mode monophasic or biphasic stimulation on some or all electrodes [29]. However, in the absence of any on-chip neural signal processing unit, the stimulator operation in these works is not dependent on the recorded neural activity, and therefore system operation is not truly closed-loop.

We have previously reported an activity-dependent intracortical microstimulation (ICMS) chip that was limited to single-channel operation [30]. In this paper, we describe a single-chip battery-powered IC with autonomous operation for multichannel brain-machine-brain interface (BMBI) that converts extracellular neural signals recorded on one microelectrode to electrical stimuli delivered via another electrode in real time *in vivo*. The paper is organized as follows. Section II presents the proposed system architecture, whereas Section III discusses the design of major circuitry within the system. Section IV presents detailed benchtop measurement results characterizing electrical performance as well as *in vivo* results from biological experiments. Section V provides a noise analysis for the recording front-end and discusses future considerations in system design. Finally, Section VI draws some conclusions from this work.

II. System Architecture

Fig. 1 shows the proposed architecture for a proof-of-concept system along with its timing operation. There are two identical 4-channel modules per chip, each comprising a recording front-end, monolithic digital signal processing (DSP) unit, and stimulating back-end. The recording front-end provides ac amplification, dc input stabilization, bandpass filtering, and 10-bit digitization to the recorded neural signals with fully programmable gain and bandwidth. The DSP unit provides additional high-pass filtering with an infinite impulse response (IIR) digital filter to remove any residual dc offsets or low-frequency artifacts, and performs real-time spike discrimination based on threshold crossing and two user-adjustable time-amplitude windows for all four channels in a fraction of one ADC conversion cycle. The accepted action potentials trigger the programmable stimulating back-end with a user-adjustable time delay ($<$29 ms) to deliver a charge-balanced asymmetric biphasic stimulus [19] or monophasic stimulus with passive discharge [18] to the neural tissue. Anodic and cathodic current pulse amplitudes can be programmed from 0 to 94.5 μA and 31.5 μA, respectively, with 6-bit resolution.

A decision-making circuitry implemented as a programmable gate array provides any logic combination of the four spike discriminator outputs (SDO 1–4) as a trigger signal for stimulation activation using a 16-bit combination code for each stimulation channel. Multiple recording and stimulation channels in conjunction with the adjustable time delay between spike discrimination and stimulus onset allows various input-output combinations and temporal relationships to be tested to enable *patient-specific* system operation for optimized performance.

The system can operate autonomously from a single 1.5-V battery. An on-chip dc-dc converter generates 5 V from the battery for increased voltage compliance in the stimulating back-end. The dc-dc converter has similar architecture to those in [31], [32] and can provide an output voltage up to approximately $4\times V_{DD}$ to a 1-μF external capacitor for storage. A 735-bit latched shift register provides all programming and control bits for system operation, and a supply-independent relaxation oscillator with similar architecture to that in [33] generates the system clock with 5-bit programmable frequency for timing management.

A radio-frequency frequency-shift-keyed (RF-FSK) transmitter at 433 MHz is shared between the modules and can operate in two modes. In mode I, it transmits the full voltage record (raw or high-pass filtered) on one channel together with the corresponding spike discrimination event. A 3-bit preamble is used in each data stream for synchronization between the on-chip transmitter and an external receiver. Information bits are scrambled within the data stream to reduce the probability of preamble misdetection. In mode II, it transmits the spike discrimination events on all eight channels along with a 6-bit preamble in each data stream.

The system is designed to operate with a nominal clock frequency of 1 MHz. As illustrated in Fig. 1, each ADC conversion cycle takes 28 clock cycles in which 16 clock cycles are dedicated to sampling, 1 cycle to hold, 10 cycles to approximation and 1 cycle to reset, thus providing a sampling frequency of 35.7 kS/s/ch that is adequate for recording extracellular neural spikes with frequency components up to 10 kHz. The extended sampling period helps relax current drive requirement of the preceding ADC driver for low-power operation. The processing of

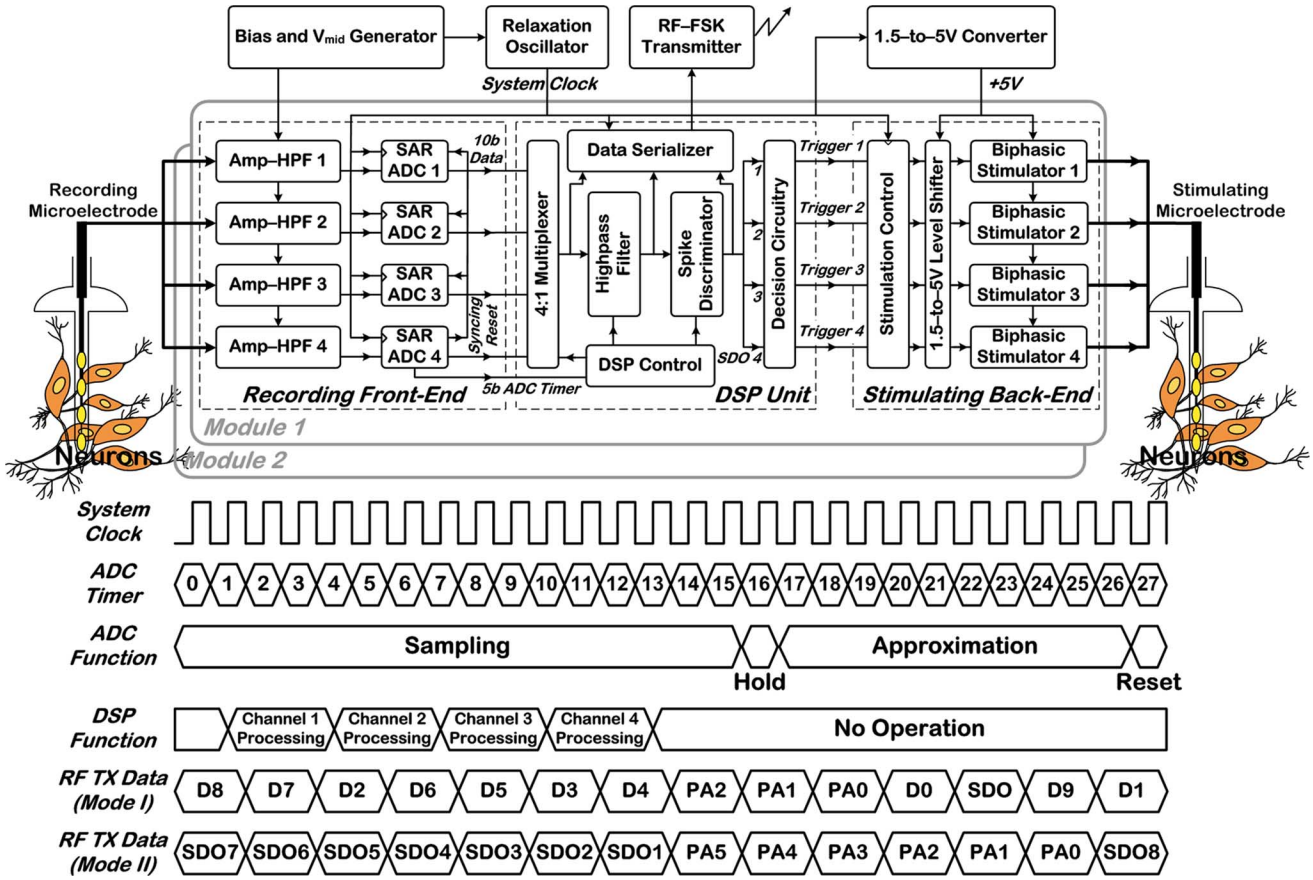

Fig. 1. Proposed architecture and timing operation of a proof-of-concept system for activity-dependent ICMS. There are two identical 4-channel modules per chip powered by a single 1.5-V battery.

each data channel in the DSP unit takes only three clock cycles, enabling the same DSP architecture to handle up to nine neural recording channels per module in any future expansion of system functionality.

III. Integrated Circuit Architecture

A. Recording Front-End

Fig. 2 shows the circuit schematic of the analog recording front-end per channel, operating from 1.5 V and comprising a low-noise amplifier (LNA) with programmable bandwidth, G_m-C high-pass filter (HPF) with adjustable low cutoff frequency, and secondary amplifier with programmable gain and offset. The LNA provides a gain of 32 dB using capacitive feedback in conjunction with a pMOS pseudo-resistor to stabilize the dc input and provide a dc feedback path [14]. Two additional pMOS transistors have been used to short the LNA inputs and output during stimulation and prevent its saturation by large stimulus artifacts, if present. The LNA bandwidth can be programmed from 5.1 to 12 kHz by varying the tail current of the differential input stage. An ultralow-transconductance operational transconductance amplifier (OTA) and a 16.7-pF capacitor form a first-order HPF with an adjustable low cutoff frequency from 0 to 525 Hz by varying the OTA tail current. The analog HPF is intended to attenuate 60 Hz and remove low-frequency LFPs that might be present in the recorded neural data. The secondary amplifier with a resistive feedback provides additional gain of 19.9, 25.4, 27.9 and 33.6 dB, and has a 3-bit offset adjustment mechanism by injecting a small dc current into the feedback path. The secondary amplifier provides a rail-to-rail output voltage swing and drives the ~12-pF capacitor network of the subsequent ADC that converts the amplified neural data to a 10-bit digital code for further processing by the DSP unit.

For analog-to-digital conversion in the recording front-end, a successive approximation register (SAR) ADC is used due to its low power consumption with similar architecture to that in [34]. The ADC design is modified as compared to that previously reported in [35] in order to operate with 1.5 V for lower power consumption.

B. DSP Unit

Fig. 3 shows the architecture of the DSP unit operating from 1.5 V, which is shared among all four channels in each module. Prior to spike discrimination, a first-order IIR filter provides additional high-pass filtering to the multiplexed digitized neural data with a programmable cutoff frequency of 366 or 756 Hz from 1-MHz system clock. Filter coefficients are selected to perform the filtering using arithmetic shifts, subtraction and addition only, with no need for digital multipliers or dividers. The operation of the time-amplitude window discriminator is also shown in Fig. 3 using neural spikes recorded wirelessly by our system from the cerebral cortex of a rat's brain. Once a filtered digitized sample crosses a user-positioned threshold level (L_0), the spike discriminator will check whether the signal waveform

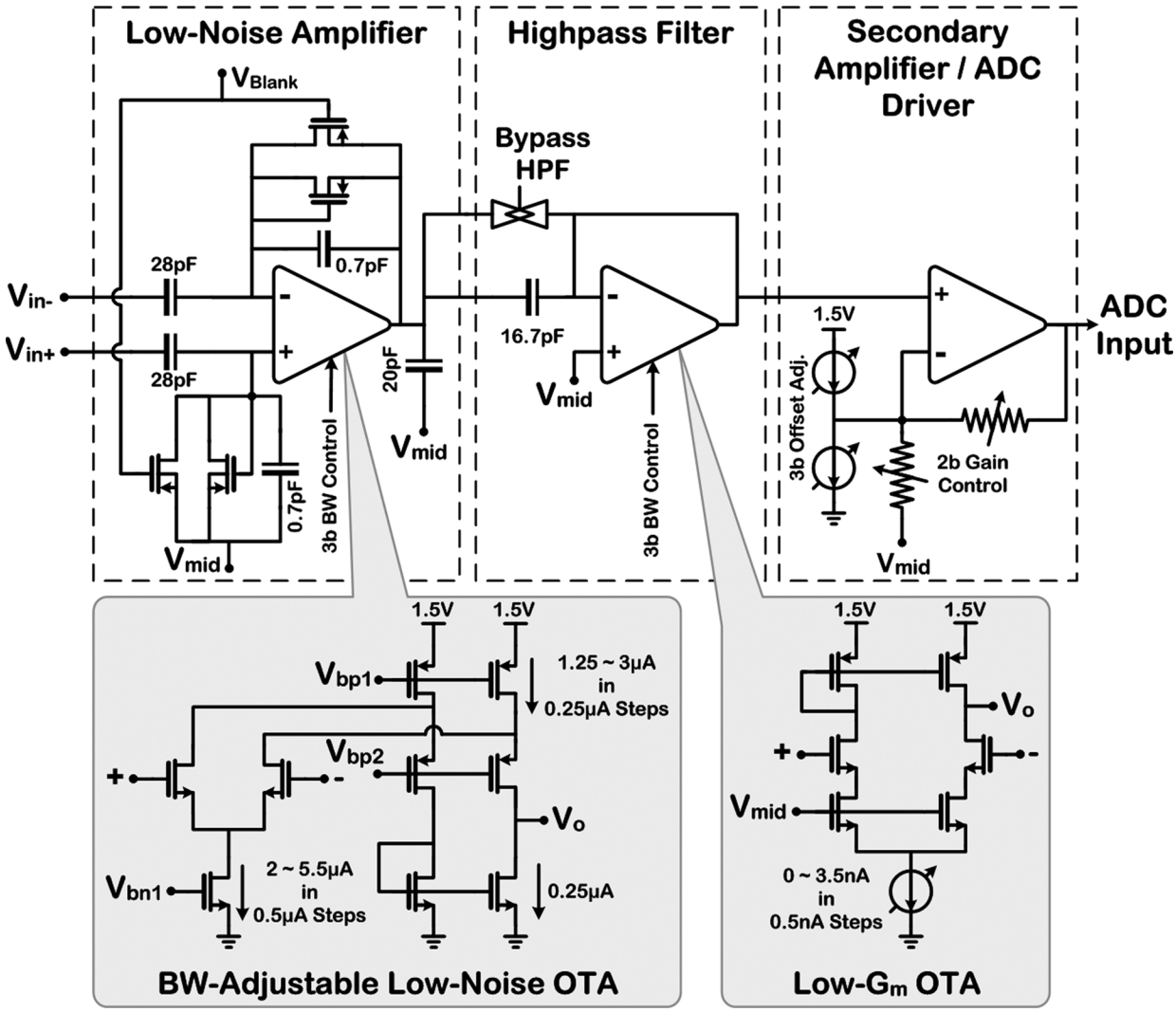

Fig. 2. Circuit schematic of the analog recording front-end per channel.

subsequently passes through two user-adjustable time-amplitude windows (solid red boxes). If a spike event is accepted on any channel, the corresponding SDO is activated after a programmable delay of 0 to ∼28.6 ms for the decision circuitry to generate the stimulus trigger signal. The DSP operation is also blanked to disregard any incoming stimulus artifacts. Spike waveforms crossing the positive threshold level (L_0) are time-aligned and superimposed in Fig. 3. The accepted spikes (dark grey) also pass through the two time-amplitude windows. Waveforms in light grey are rejected by the system (i.e., not used for stimulus triggering). The spike discrimination parameters are determined empirically by the user prior to the experiment and programmed into the chip. As stated previously, the flexibility in adjusting the spike-stimulus time delay is a critical system feature, because the relative timing of spikes and stimulus is known to influence conditioning effects in activity-dependent microstimulation in an intact nervous system [36].

C. Microstimulating Back-End

Fig. 4 shows the circuit schematic of the microstimulating back-end in each module, incorporating four identical stimulation channels with pMOS and nMOS current sources to generate the anodic and cathodic current pulses, respectively, in biphasic stimulation. The stimulation channels also include a dedicated digital control unit for stimulus timing management as well as a 1.5-to-5 V signal level shifter, and share a 6-bit current-based digital-to-analog converter (DAC) and biasing circuitry available in each module.

To maintain a constant stimulus current regardless of the site and tissue impedances, current sources with high output impedance are required [37]. In this work, two feedback amplifiers, $A_{1,2}$, are used to boost the output impedance of the two current sources by maintaining a fixed voltage across drain-source of M_1 and M_4 [38]. Two compensation capacitors at the gates of M_2 (350 fF) and M_5 (150 fF) limit the amplifiers' bandwidth for stability [39].

As stated in Section II, an on-chip dc-dc converter generates a 5-V supply from 1.5 V for the microstimulating back-end. Since the output voltage of the converter is not fully regulated, it is important that the stimulator output current be relatively insensitive to supply voltage variation. Cascode current source architecture with active feedback circuitry as employed herein inherently has low sensitivity to supply voltage variation due to its high output impedance. However, supply voltage variation can also induce output current change through the biasing

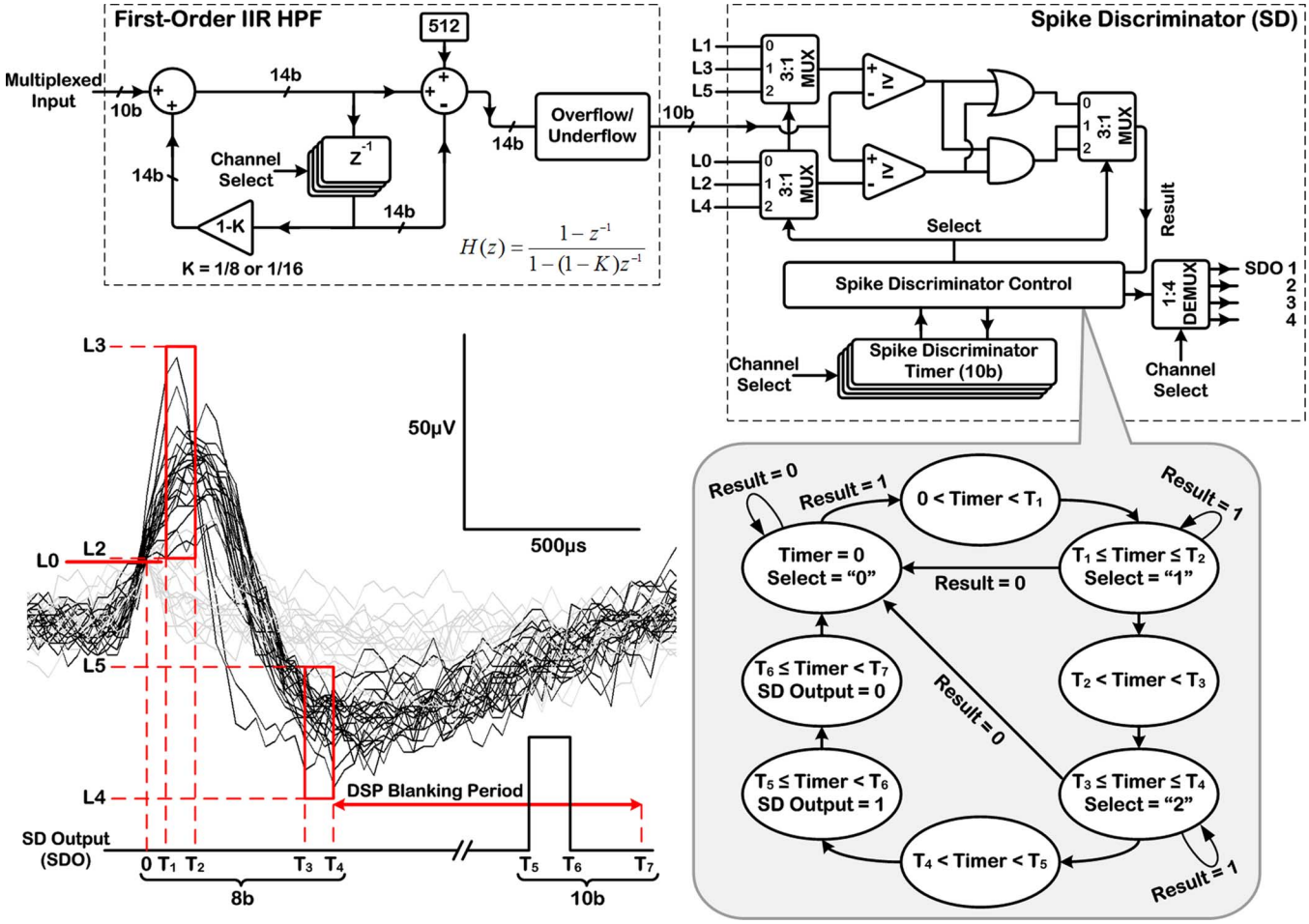

Fig. 3. Architecture of the DSP unit and operation of the time-amplitude window discriminator with neural spikes recorded wirelessly by our system from the cerebral cortex of a rat's brain. The flow chart for spike discrimination algorithm is also shown. Negative threshold level L_1 (not shown in bottom left) is used in the algorithm to discriminate waveforms with reverse polarity (i.e., negative-going initial portion), if necessary.

circuitry. To address this issue for the pMOS current source, M_{b5} is stacked on top of the nMOS current mirror in the current source biasing circuitry to increase the impedance seen from V_{bp} to ground. It should be noted that V_{bn} and V_{dn} for the nMOS current source are generated with circuitry powered by 1.5 V and therefore less susceptible to supply variation.

As previously described in [38], when source-drain voltage of M_5 in the pMOS current source is high (i.e., $|V_{ds}| > \sim 3$ V), a significant portion of the transistor drain current can flow into its bulk due to impact ionization effect [40], greatly degrading the output impedance of the current source. This can be solved by connecting the bulk and source of M_5 together, as also seen in Fig. 4, allowing its drain-bulk current to also flow through M_4 and be controlled by the active feedback circuitry. However, this solution cannot be applied in a standard *n-well* CMOS process to address the same concern for M_2 in the nMOS current source.

Loizou and colleagues have proposed a 3-transistor MOS structure stacked on top of the current source with the purpose of limiting the drain-source voltage across each transistor to a reasonably small value for avoiding hot-carrier effects when the stimulator output voltage is near the supply rail [41]. In this work, this issue is addressed by adding M_{s1-5} to the nMOS current source in each stimulation channel, applying a voltage of $\sim(V_{\rm DD}/2 + V_{GS3})$ to the gate of M_3, instead of $V_{\rm DD}$, during the cathodic phase. In the worst-case scenario of the stimulator output voltage being near the supply rail, the drain-source voltage of M_2 and M_3 is $\sim V_{\rm DD}/2$, not high enough to cause significant drain-bulk current in either transistor. When the output voltage decreases below $V_{\rm DD}/2$, M_3 enters the triode region with a small drain-source voltage, which does not adversely affect voltage compliance.

The microstimulator can be programmed to generate two different types of stimulus current pulses. With timing parameters $T_{1,2,3}$ set to be equal to T_{Anodic} (nominally 192 μs), it generates a monophasic current pulse as shown in Fig. 4 [38]. To control the pulse amplitude, the 6-bit DAC generates a fraction (1/15) of the target output current, which is then amplified by the pMOS current source up to 94.5 μA. This constant-current phase is followed by passive discharge to drain the accumulated charge on the stimulation site using a 2-bit programmable resistor (4.6 to 32 kΩ). During passive discharge, the current DAC and all biasing circuitry are powered down to reduce the static power consumption. In the monophasic mode, the node V_{body} and animal body are tied to the system ground, allowing output voltage headroom of 5 V.

The microstimulator can generate an asymmetric biphasic current pulse as well, as also shown in Fig. 4. In the leading anodic phase, a constant current up to 94.5 μA is generated by the pMOS current source for duration T_1 followed by an interphase delay that lasts until T_2. In the cathodic phase, a con-

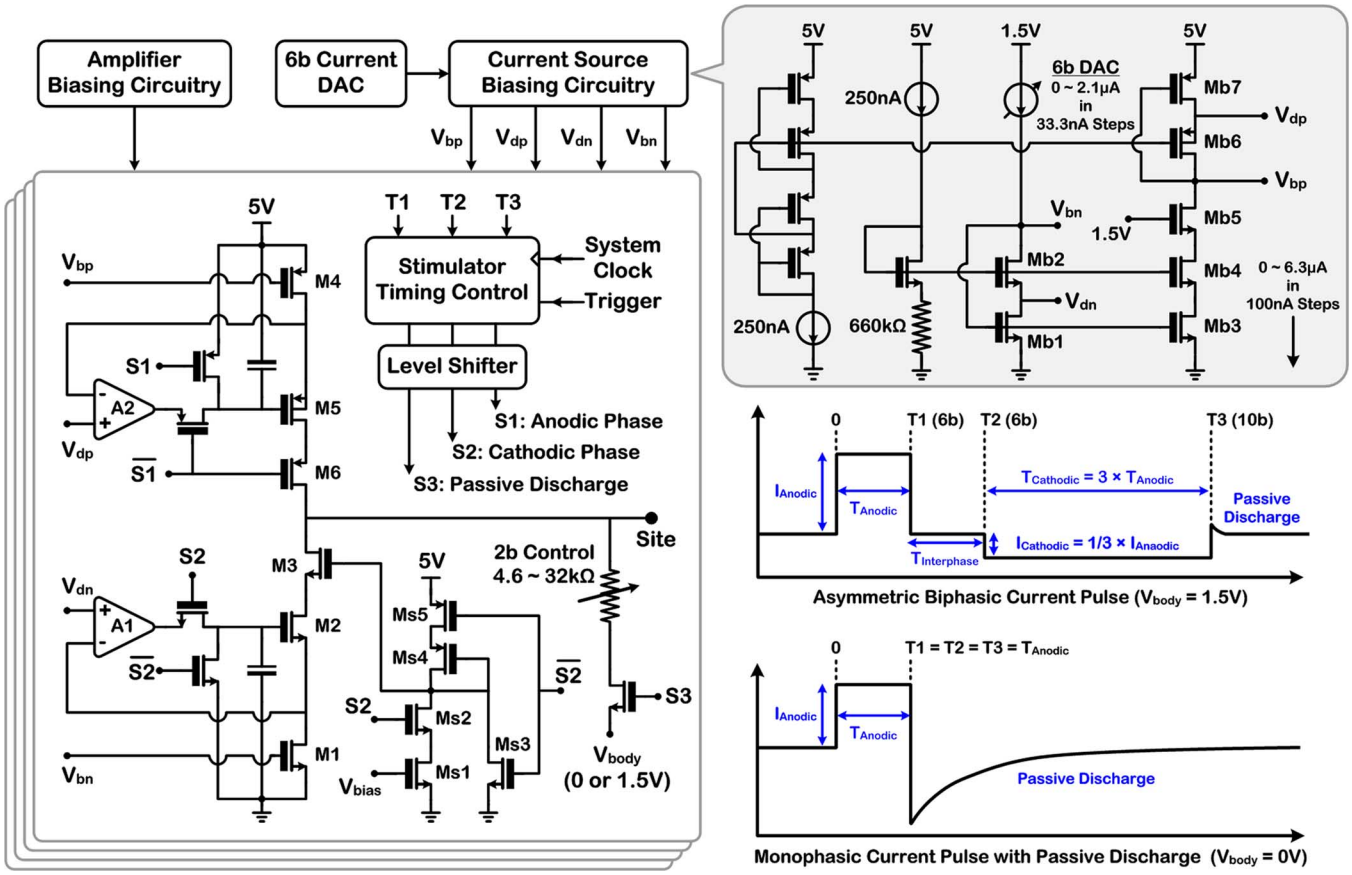

Fig. 4. Circuit schematic of the microstimulating back-end per module, comprising four identical stimulation channels with shared 6-bit current DAC and biasing circuitry. Each stimulation channel incorporates a timing control unit, a 1.5-to-5 V signal level shifter, and a pair of pMOS and nMOS current sources with boosted output impedance via active feedback. All transistors have a thick oxide, except for those in the timing control unit. The two stimulus current waveforms that can be generated by the stimulating back-end are also shown with corresponding time-amplitude parameters.

stant current up to 31.5 μA (always 1/3 of the anodic phase amplitude) is generated by the nMOS current source that lasts until T_3. With a 1-MHz system clock, T_1 and T_2 can be programmed up to 1.008 ms with a resolution of 16 μs, whereas T_3 can be programmed up to 1.023 ms with a resolution of 1 μs. For the asymmetric biphasic current pulse in Fig. 4 to be theoretically charge-balanced, T_3 should nominally be set equal to $3 \times T_1 + T_2$. In practice, however, the ratio of current levels in the anodic and cathodic phases can deviate from 1/3 due to process parameter variation and transistor mismatches. In that case, adjusting T_3 slightly around its nominal value can partially alleviate concerns associated with charge-imbalanced operation.

Passive discharge is also performed after each stimulation cycle to drain any residual charge left from charge mismatch between the anodic and cathodic phases. Further, in this proof-of-concept system with limited number of stimulation channels, external dc-blocking capacitors can also be placed in series with the electrode-tissue interface to prevent any net dc current flow into the tissue arising from charge imbalance or semiconductor failure. An alternative approach to ensure charge-balanced operation would be to employ *active* charge balancing based on monitoring the electrode voltage after each stimulation cycle and maintaining it within a safe predefined voltage range [42]. This technique would be more effective than passive discharge for high-frequency stimulation where there might not be adequate time for the discharge period to achieve sufficient charge balancing. However, this is not expected in *activity-dependent* stimulation given cortical neuronal firing rates of $<$150 spikes per second [43].

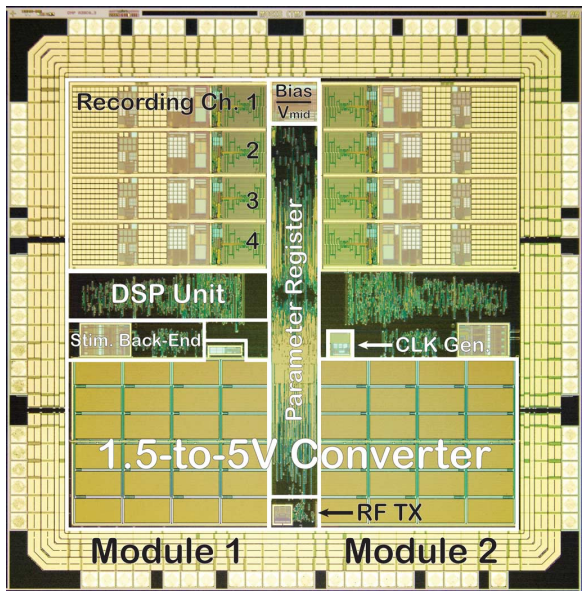

Fig. 5. Die micrograph of the 3.3 × 3.3 mm^2 IC fabricated in 0.35-μm 2P/4M CMOS.

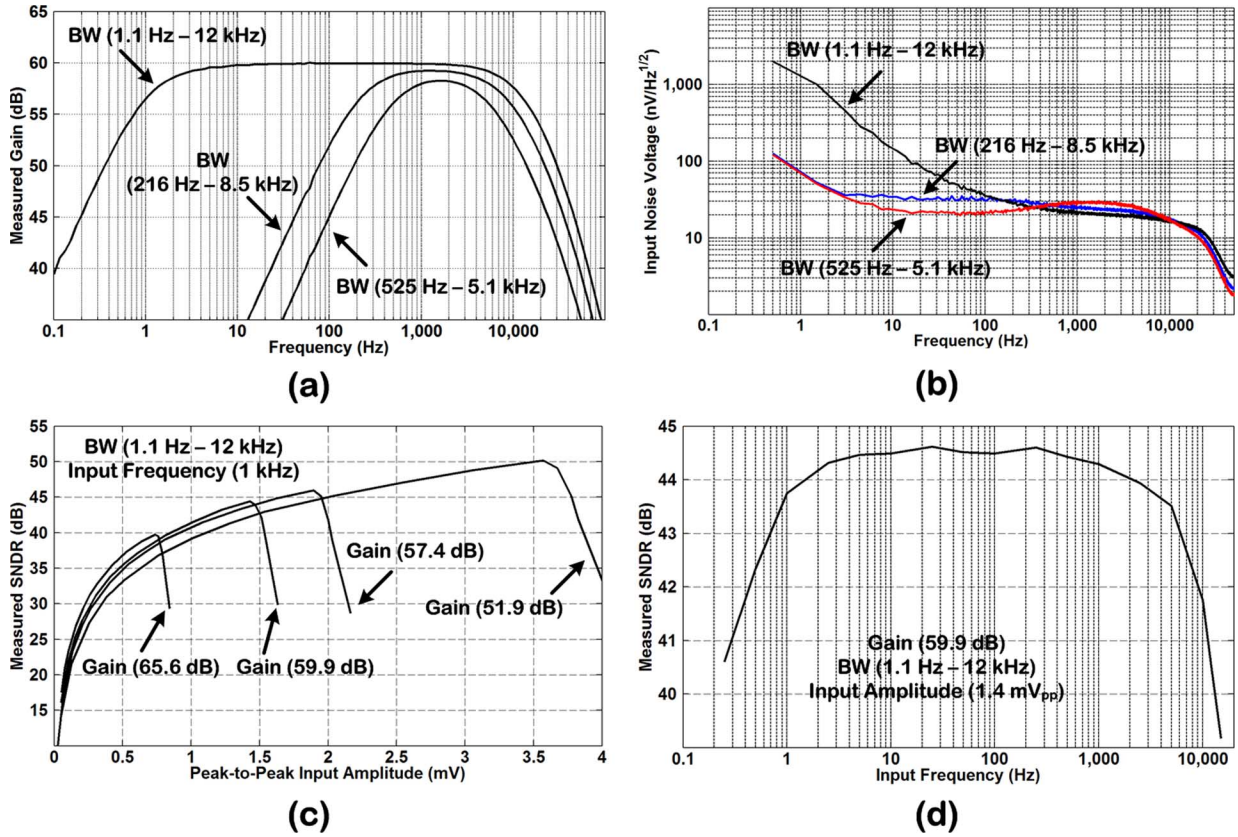

Fig. 6. Measured (a) frequency response and (b) input noise voltage of the analog recording front-end with different bandwidth settings. Measured SNDR of the entire recording front-end at the SAR ADC output versus (c) amplitude and (d) frequency of the input signal.

In the asymmetric biphasic mode, the node V_{body} and animal body are tied to 1.5 V, allowing output voltage headrooms of 3.5 V and 1.5 V for the anodic and cathodic phases, respectively. Therefore, the microstimulator has higher stimulus current drive capability in the monophasic mode due to higher output voltage headroom, but provides higher safety level in the biphasic mode by using a charge-balanced current waveform.

IV. Measurement Results

A prototype chip was fabricated in 0.35-μm two-poly four-metal (2P/4M) CMOS as shown in Fig. 5, measuring 3.3×3.3 mm^2 including the bonding pads. This section discusses the measurement results from benchtop characterization and acute biological experiments with rats.

A. Benchtop Characterization

The top plots in Fig. 6 depict the measured frequency response and input-referred noise voltage spectrum of the analog recording front-end for three different bandwidth settings and with the midband ac gain nominally set to 60 dB. The low cutoff frequency could be programmed from 1.1 to 525 Hz, whereas the high cutoff frequency could be adjusted in the range of 5.1 to 12 kHz. The midband ac gain was measured to be 51.9, 57.4, 59.9 and 65.6 dB when the G_m-C HPF was bypassed. The gain dropped by ∼0.3 dB when the HPF was included in the signal path. With the bandwidth set to 1.1 Hz to 12 kHz, the thermal noise level was measured to be 21 nV/rtHz at 1 kHz. This level increased as the bandwidth decreased, because the LNA input transistors carried less current, increasing their thermal noise contribution. With the same bandwidth setting, the total input noise voltage was measured to be 3.12 μV_{rms} by integrating the noise spectrum from 0.5 Hz to 50 kHz, indicating an increase of only 8.2% due to flicker noise. This led to a noise efficiency factor (NEF) of 2.68 for the LNA. The flicker noise corner frequency was measured to be < 90 Hz for all bandwidth settings, indicating that the G_m-C HPF could largely reduce the flicker noise contribution.

A sinusoidal signal with varying amplitude and frequency was then applied to the LNA input and the SNDR was measured at the ADC output. Fig. 6(c) shows the measured SNDR at 1 kHz versus input amplitude for the four available gain settings. Lower gain values provided higher input dynamic range, whereas higher gain values provided better signal resolution. Fig. 6(d) depicts the measured SNDR versus input frequency. In the frequency range of 100 Hz to 10 kHz for extracellular neural spikes, the recording front-end provided > 41.8 dB of accuracy.

The top plots in Fig. 7 depict the measured microstimulator output current versus its output voltage in the anodic and cathodic phases for four different DAC input codes. The stimulator output voltage could reach at least 4.68 V (going toward 5 V) and 150 mV (going toward 0 V) with a 5-V supply. To further examine the microstimulator functionality, it was interfaced with a silicon-substrate micromachined electrode with stimulus sites of iridium oxide (IrO). Fig. 7(c) and (d) depict the measured monophasic and asymmetric biphasic stimulus current waveforms delivered by the chip to saline via the microelectrode. The power consumption per channel was measured to be 3.5 μW from 5 V, when the microstimulator generated

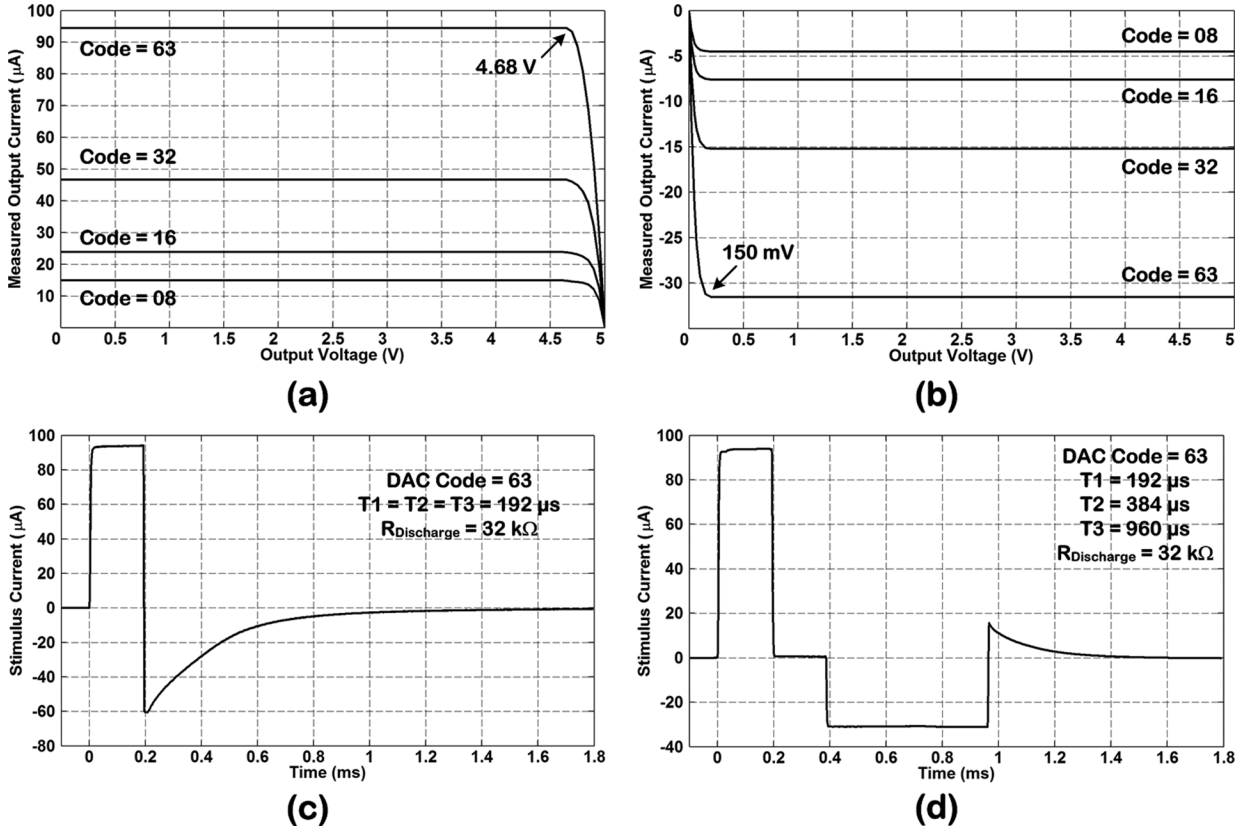

Fig. 7. Top: Measured microstimulator output current versus output voltage for four different DAC input codes in (a) anodic and (b) cathodic phases. Bottom: Measured (c) monophasic and (d) asymmetric biphasic stimulus current waveforms delivered by the chip to saline via a microelectrode. Passive discharge is also performed in each case using an on-chip 32-kΩ resistor.

the biphasic waveform in Fig. 7(d) at a rate of 33 Hz. Table I summarizes the measured performance of major circuitry, and Table II compares the system functionality and its measured performance with that in recent published work.

B. In Vivo Characterization

In the first biological experiment, a silicon microelectrode with recording sites of iridium was implanted in the somatosensory cortex of a rat's brain and externally interfaced with a single channel of the recording front-end on the chip. The left plot in Fig. 8 shows a 4-s snapshot of the extracellular neural spikes recorded wirelessly at the output of the ADC. In another test, a tungsten electrode with impedance value in the range of 50 to 100 kΩ was placed in the cortical motor area and externally interfaced with a single channel of the microstimulating back-end on the chip to stimulate the brain with a train of 13 monophasic current pulses (90 μA, 192 μs, 300 Hz). The right plot in Fig. 8 depicts the evoked electromyogram (EMG) signal recorded from the rat's neck muscle. The largest EMG spike appeared in $<$50 ms from the stimulation onset. The chip was then interfaced with the two implanted electrodes to demonstrate *activity-dependent* ICMS and programmed with the time-amplitude window discriminator parameters determined empirically prior to the experiment. In the first test, the recording and stimulation electrodes were each connected to a single channel of the front- and back-end on the chip, respectively. As the chip operated fully autonomously from a 1.5-V battery, it successfully delivered electrical stimuli to the cortical motor area triggered by neural spikes discriminated on the adjacent electrode in the somatosensory cortex, producing an artificial connection between the two brain regions. Fig. 9 shows the superimposed spike waveforms and corresponding stimulus artifacts from single-pulse stimulation (90 μA, 192 μs) with spike-stimulus delays of 5 and 20 ms. The stimulus artifact rejection mechanism in the recording front-end was de-activated in this test. Hence, artifacts of <4 ms in duration were observed on the recording electrode.

Finally, while the stimulation electrode remained connected to a single channel of the back-end, the *multisite* recording electrode was connected to all four channels of the front-end in one module. The decision-making circuitry was programmed to trigger ICMS whenever neural activity would be present on any two or more data channels. Fig. 10 shows a 300-ms snapshot of the recorded data of each channel at the output of the digital HPF along with the corresponding SDO and the resulting stimulus trigger signal. Two large stimulus artifacts were distinguishable on each channel. The first stimulation was triggered by neural activity on channels 2 and 3, whereas the second was due to neural activity on channels 2 and 4. Some recorded spikes (marked by black arrows) were not discriminated by the DSP unit due to blanking of its operation after discriminating the spikes that immediately preceded them. This can be alleviated by reducing the time duration of DSP blanking.

TABLE I
SUMMARY OF MEASURED PERFORMANCE

Recording Front-End	
AC Gain @ 1 kHz	51.9, 57.4, 59.9, 65.6 dB
Low Cutoff Freq.	1.1 ~ 525 Hz
High Cutoff Freq.	5.1 ~ 12 kHz
Total RMS Input Noise Voltage	3.12 µV (BW of 12 kHz) 3.42 µV (BW of 5.1 kHz)
NEF	2.68 (BW of 12 kHz) 2.9 (BW of 5.1 kHz)
CMRR @ 1 kHz	>56 dB
PSRR @ 1 kHz	>65 dB
Crosstalk	< -72 dB
Max. Sampling Freq.	63 kS/s
INL/DNL	< ±0.8 LSB
ENOB	9.2b (f_{in} = 1 kHz, f_S = 35.7 kS/s) 9.1b (f_{in} = 1 kHz, f_S = 63 kS/s)
Power Consumption*	
Amp-HPF	26.9 µW (BW of 12 kHz) 19.9 µW (BW of 5.1 kHz)
SAR ADC	5.9 µW (f_{CLK} = 1 MHz)
Digital Signal Processing Unit	
HPF Cutoff Freq.	366 / 756 Hz (f_{CLK} = 1 MHz)
Power Consumption	12.4 µW (f_{CLK} = 1 MHz)
Relaxation Oscillator	
Output Frequency	420 kHz ~ 2.5 MHz
Supply Sensitivity	-60 kHz/V
Power Consumption	20.8 µW (f_{CLK} = 1 MHz)

Microstimulating Back-End		
	Anodic	**Cathodic**
Stimulus Waveform	Asymmetric Biphasic & Monophasic w/ Passive Discharge	
Output Current	0 ~ 94.5 µA	0 ~ 31.5 µA
Current Pulsewidth		
Monophasic	0 ~ 1.008 ms	N/A
Biphasic	0 ~ 240 µs	0 ~ 720 µs
Output Impedance	~400 MΩ	~440 MΩ
DAC Resolution	6b	
DAC Linearity	< ±1.6 LSB	
Supply Sensitivity	-70.4 nA/V	-10.4 nA/V
Voltage Compliance		
Monophasic	4.68 (of 5 V)	N/A
Biphasic**	3.18 (of 3.5 V)	1.35 (of 1.5 V)
Current Efficiency	95.6% (I_{out} = 94.5 µA)	N/A
1.5-to-5 V Converter		
DC Output Voltage	4.86 ~ 5.35 V	
Output Ripple	40 mV_{pp}	
Max. Load Current	88 µA (V_{out} = 5.05 V)	
Power Efficiency	31% (V_{out} = 5.05 V)	
RF Transmitter		
Comm. Scheme	FSK @ 433 MHz	
Received Power @ 1 m	-55 dBm (18-cm monopole TX and RX Antennae)	
Power Consumption	200 µW	

Total Power for Two Modules w/o RF TX (Stimulation Rate = 33 Hz, Recording BW = 525 Hz ~ 5.1 kHz) = 375 µW

* Per channel ** See Section III-C.

TABLE II
COMPARISON OF SYSTEM FUNCTIONALITY AND MEASURED PERFORMANCE

	This Work	**[13]**	**[14]**	**[17]**	**[19]**
System Functionality	Neural Spike Recording; Neural Signal Processing; Neurostimulation; Power Conditioning	Neural Recording (Spikes & LFP)	Neural Recording (Spikes & EEG)	Neural Stimulation	Neural Stimulation
Supply Voltage	1.5 V (Battery Powered)	2.8 V	±2.5 V	5 V (Wirelessly Powered)	3.3 V (Logic) 10 V (Stimulation)
RMS Input Noise Voltage	3.12 µV (0.5 Hz – 50 kHz)	3.06 µV (10 Hz – 98 kHz)	2.2 µV (0.5 Hz – 50 kHz)	–	–
Power Consumption*	26.9 µW (BW of 12 kHz)	7.56 µW (BW of 5.32 kHz)	80 µW (BW of 7.2 kHz)	–	–
NEF	2.68	2.67	4	–	–
Stimulus Output Range/Resolution	0 – 94.5 µA/6b	–	–	1 – 255 µA/8b	0 – 735 µA
Stimulus Waveform	Asymmetric Biphasic & Monophasic w/ Passive Discharge	–	–	Symmetric Biphasic	Asymmetric Biphasic
Charge Balancing	Passive Discharge & 220-nF Blocking Capacitor	–	–	Charge Recovery w/ Active Circuit	100-nF Blocking Capacitor
Technology	0.35 µm CMOS	0.5 µm CMOS	1.5 µm CMOS	0.6 µm BiCMOS	0.35 µm CMOS
Experimental Paradigm	*In Vivo*	*In Vivo*	*In Vivo*	*In Vivo*	Benchtop
Publication Year	2011, JSSC	2007, TBCAS	2003, JSSC	2009, TBCAS	2008, TBCAS

* Per recording channel

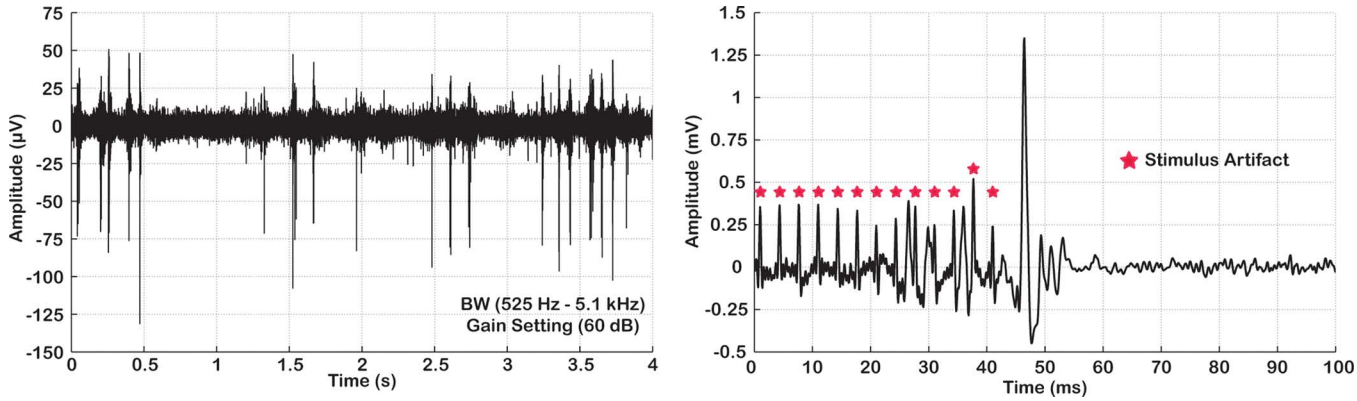

Fig. 8. *In vivo* demonstration of recording and stimulation functionalities of the chip in an anesthetized rat. Left – Extracellular neural spikes recorded wirelessly from the somatosensory cortex of the brain. The data are shown after linear-phase offline filtering (500 Hz to 4 kHz) with spike amplitudes referred to the input. Right – Measured EMG signal from the rat's neck muscle evoked by chip microstimulation of the cortical motor area with a train of 13 monophasic current pulses. The EMG signal is recorded by commercial electrophysiology equipment.

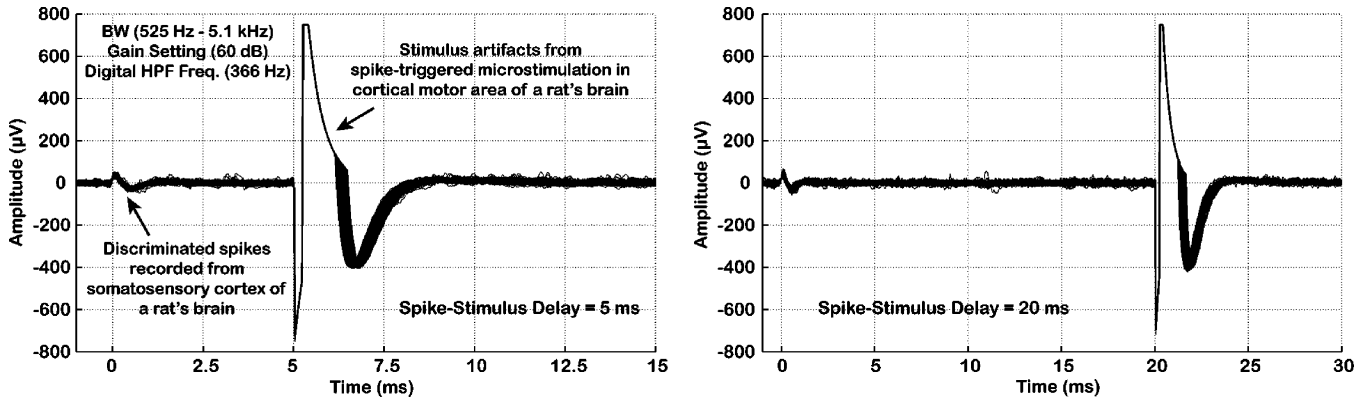

Fig. 9. Stimulation on one microelectrode in the cortical motor area of an anesthetized rat triggered by neural spikes discriminated on an adjacent microelectrode in the somatosensory cortex with spike-stimulus delays of 5 and 20 ms. Stimulus artifacts of < 4 ms in duration are observed on the recording electrode. The data are recorded wirelessly with the amplitude levels referred to the input.

As seen in Figs. 9 and 10, stimulus artifacts are used in this work to show that stimulation is occurring *in vivo*. However, to address the concern of artifacts false-triggering the microstimulator, a time-amplitude window discriminator is used (as opposed to simple spike thresholding) to discriminate between neural spikes and stimulus artifacts by proper adjustment of time-amplitude window parameters. Blanking the DSP operation after spike discrimination also prevents false-triggering the stimulator by the incoming stimulus artifact.Another concern related to stimulus artifacts is that any spike activity that occurs within the duration of the artifact cannot be detected by the system for triggering purposes. This is less of a concern for activity-dependent microstimulation, since we do not foresee a need to use *every* single spike in the system to entrain a neuronal population to another group of neurons. Nonetheless, we are developing an integrated signal-processing solution for real-time stimulus artifact rejection, which affords to retain signal information during each stimulation cycle [44], [45]. Such capability could be added to the DSP unit in the future.

V. Discussion

A. LNA Noise Analysis

This section presents a noise analysis for the selected LNA topology and obtains a minimum NEF for a practical design given our technology parameters and supply voltage. A similar discussion was presented in [13] for a slightly different LNA architecture. Fig. 11 shows a simplified schematic of the LNA and its core OTA for this analysis. We also model the transistor thermal noise current as

$$\overline{i_n^2} = 4KT \times \gamma \times g_m \tag{1}$$

where K is the Boltzmann's constant, T is the absolute temperature, g_m is the transistor transconductance, and γ is 2/3 for a transistor operating in strong inversion (above-threshold) and $1/(2\kappa)$ for a transistor operating in weak inversion (subthreshold) in which κ is the subthreshold gate coupling coefficient with a typical value of 0.7 [40]. The transistor transconductance can be estimated as

$$g_m \approx \frac{\kappa \times I_D}{V_{th}} \quad \text{Weak inversion (subthreshold)}$$
$$g_m \approx \frac{2 \times I_D}{V_{OD}} \quad \text{Strong inversion (above-threshold)} \tag{2}$$

where V_{th} is the thermal voltage, I_D is the transistor drain current, and V_{OD} is the transistor overdrive voltage. Assuming that the overall transconductance of the OTA, G_m, is nearly equal

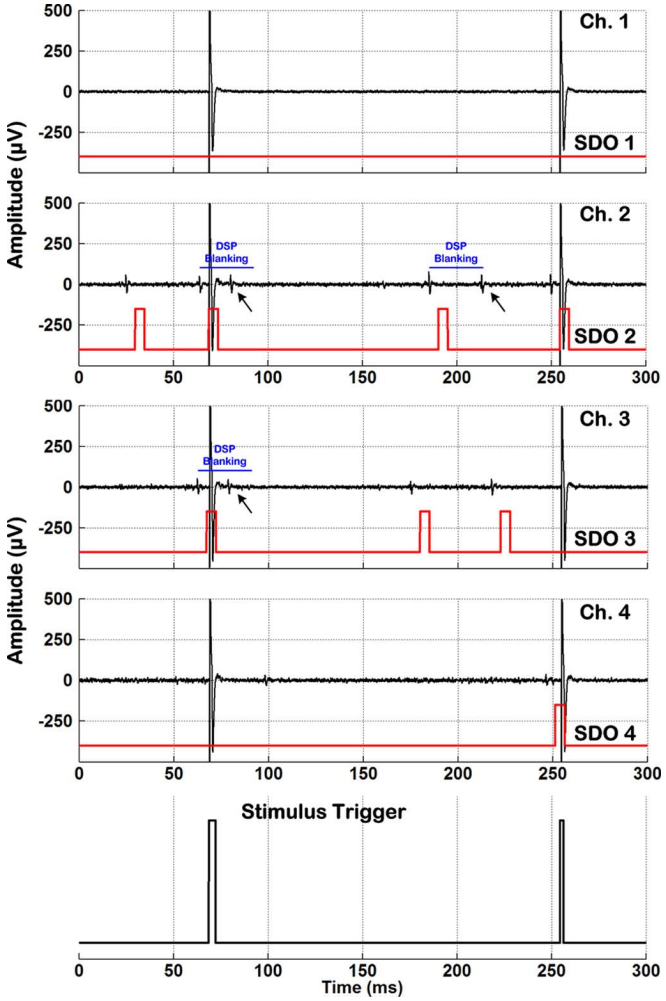

Fig. 10. Stimulation on one microelectrode in the cortical motor area of an anesthetized rat triggered by neural spikes discriminated on multiple recording sites of an adjacent microelectrode. The chip is programmed to trigger ICMS when neural activity is discriminated on any two or more channels of the recording front-end. The timing parameters T_5, T_6 and T_7 in the DSP unit are set to 5, 10 and 28 ms, respectively. Arrows point to neural spikes on channels 2 and 3 that are not discriminated by the system due to blanking of the DSP operation.

to that of transistor M_1, the input-referred noise voltage of the OTA can be estimated as

$$\overline{V_{n,OTA}^2} = \frac{1}{g_{m1}^2}\left(\frac{4KT}{\kappa}\times g_{m1} + \frac{16KT}{3}\times g_{m3} + \frac{16KT}{3}\times g_{m7}\right). \tag{3}$$

To minimize the OTA input noise voltage, $M_{1,2}$ operate in subthreshold to maximize g_{m1} for a given current level, whereas $M_{3,4,7,8}$ operate in strong inversion to reduce their transconductances. Moreover, the drain current of $M_{1,2}$ is selected to be much larger than that of $M_{7,8}$ in the folded branch. This current scaling scheme helps improve the OTA noise performance by further increasing g_{m1} and reducing $g_{m7,8}$. Therefore, neglecting the noise contribution by $M_{7,8}$, (3) can be simplified as

$$\overline{V_{n,OTA}^2} = \frac{1}{g_{m1}} \times \frac{4KT}{\kappa}\left(1 + \frac{8}{3}\times\frac{V_{th}}{V_{OD3}}\times(\beta+1)\right) \tag{4}$$

where $\beta = I_7/I_1$ is the current scaling factor between the input differential pair and the folded branch. Equation (4) suggests that V_{OD3} should be increased to reduce the OTA input noise. However, increasing V_{OD3} means the drain-source voltage of $M_{3,4}$ should be increased too, limiting the OTA output voltage swing. For a peak-to-peak voltage swing (V_{Swing}) of 0.5 V at the OTA output, an upper limit of 0.5 V can be found for V_{OD3} given a supply voltage of 1.5 V. It should be noted that V_{Swing} of 0.5 V allows the LNA to handle input signals as large as $\sim \pm 6$ mV, in case LFPs or other low-frequency artifacts would also be present at the input. In this work, $M_{3,4}$ are sized for V_{OD3} of 0.35 V instead to ensure that they do not enter the triode region in the presence of process parameter variation.

According to (4), the OTA input noise voltage also depends on β, indicating that the current scaling factor should be selected judiciously. To that end, we next investigate the effect of β on the overall OTA transconductance, G_m. The G_m of a folded-cascode OTA with a similar current scaling scheme is thoroughly analyzed in [13]. In a similar way, the analysis of the proposed circuit reveals the G_m to be

$$G_m \approx \frac{g_{m5}}{g_{ds1} + g_{ds3} + g_{m5}} \times g_{m1} \tag{5}$$

where g_{ds} is the transistor drain-source conductance. Since the channel length of $M_{3,4}$ is selected to be much longer than that of $M_{1,2}$, g_{ds3} is much smaller than g_{ds1}, which yields

$$\frac{G_m}{g_{m1}} \approx \frac{1}{1 + \frac{V_{th}}{\kappa \times V_{A1} \times \beta}} \tag{6}$$

where V_{A1} is the early voltage for M_1 (i.e., $1/\lambda_1$) and M_5 is sized to operate in subthreshold. This equation is also plotted in Fig. 11 with a value of 20 V for V_{A1}. According to (4), reducing β helps reduce the OTA input noise voltage, but β cannot be reduced arbitrarily to ensure that G_m is not degraded considerably (i.e., $\beta \geq 0.05$ from Fig. 11).

Another important consideration in selecting β is the sensitivity of bias currents to transistor mismatches in the OTA and associated biasing circuitry. Assume that ΔI_1, ΔI_3 and ΔI_7 are bias current deviations from their corresponding nominal values due to transistor mismatches. If ΔI_1 and ΔI_3 are assumed to be uncorrelated, it can be shown that

$$\frac{\Delta I_7}{I_7} = \sqrt{\frac{\Delta {I_1}^2 + \Delta I_3^2}{{I_7}^2}} = \frac{1}{\beta} \times \sqrt{\left(\frac{\Delta I_1}{I_1}\right)^2 + (\beta+1)^2 \times \left(\frac{\Delta I_3}{I_3}\right)^2}. \tag{7}$$

For example, for a β value of 0.05, a 2% variation in I_1 and I_3 causes a 58% variation in I_7, which might adversely affect the OTA operation and degrade its transconductance. In this work, the minimum value of β (when LNA bandwidth is maximum) is selected to be 0.091 for which G_m is 98% of g_{m1}, and 2% variation in I_1 and I_3 causes only 32.5% variation in I_7. Table III tabulates the dimension, current level, and operating condition of each transistor pair in the OTA for optimum noise performance with the maximum bandwidth setting.

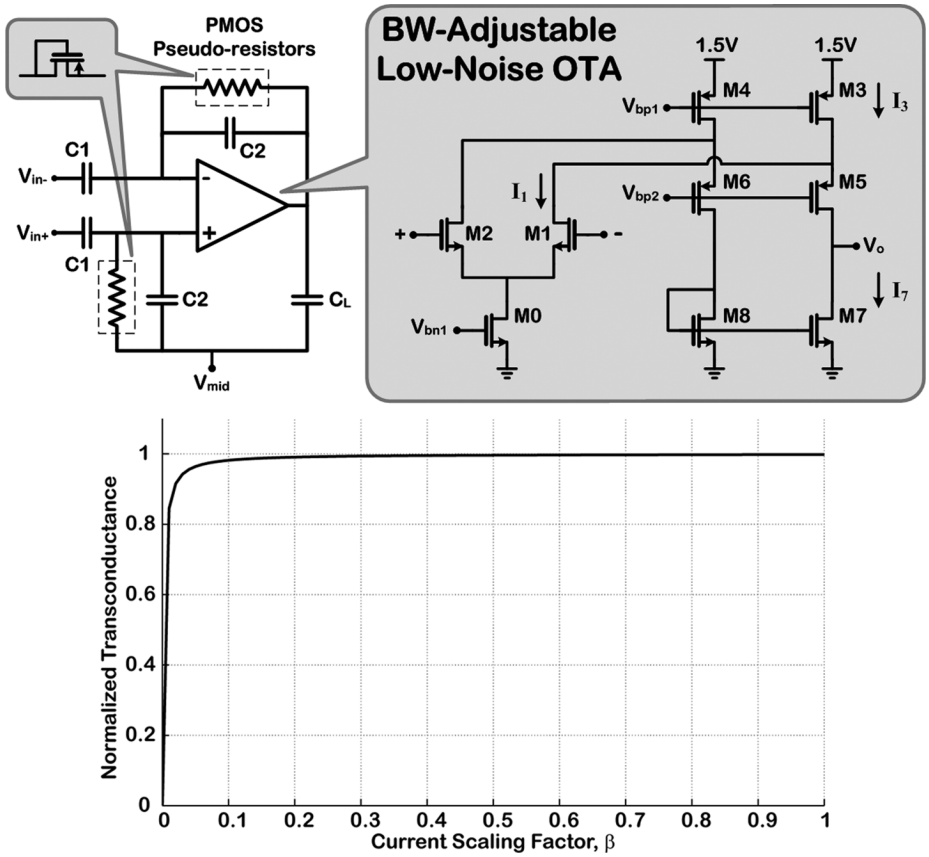

Fig. 11. Simplified schematic of the LNA and its core OTA for noise analysis (top) and a plot of the normalized OTA transconductance G_m/g_{m1} versus the current scaling factor β (bottom).

TABLE III
DIMENSION, CURRENT LEVEL, AND OPERATING CONDITION OF OTA TRANSISTORS

Transistor	Dimension (μm)	Current Level (μA)	Simulated g_m (μS)	Inversion Coefficient*	Operating Condition
$M_{1,2}$	800/2	2.75	76	0.021	subthreshold
$M_{3,4}$	20/20	3.00	16	26.8	above-threshold
$M_{5,6}$	80/1.3	0.25	6.9	0.036	subthreshold
$M_{7,8}$	4/40	0.25	2.5	7.6	above-threshold

* $\mu_n C_{OX}$ = 170 μA/V^2, $\mu_p C_{OX}$ = 58 μA/V^2

To compute the NEF, we should note that the input-referred noise voltage of the LNA is almost equal to that of the OTA given that the parasitic gate capacitance at the input terminals of the OTA is typically much smaller than $C_{1,2}$. The NEF can be calculated according to [46]

$$\mathrm{NEF} = V_{ni,\mathrm{rms}} \times \sqrt{\frac{2 \times I_{\mathrm{total}}}{\pi \times V_{th} \times 4KT \times BW}} \tag{8}$$

where $V_{ni,\mathrm{rms}}$ is the rms input noise voltage of the LNA, I_{total} is the total supply current, and BW is the 3-dB bandwidth of the amplifier. Finally, assuming that the LNA has a single dominant pole in its frequency response and noting that $I_{\mathrm{total}} = 2 \times I_3$, combining (4) and (8) yields

$$\mathrm{NEF} = \sqrt{\frac{2 \times (\beta+1)}{\kappa^2} \times \left(1 + \frac{8}{3} \times \frac{V_{th}}{V_{OD3}} \times (\beta+1)\right)} \tag{9}$$

which results in an NEF of 2.33 for β of 0.091 and V_{OD3} of 0.35 V. Hence, the NEF of 2.68 derived from measured performance of the LNA (when set for maximum bandwidth) is in good agreement with this analysis. This argument also shows that reducing the supply voltage can adversely impact the OTA noise performance for the same output voltage swing, making it challenging to reduce V_{DD} below 1.5 V in this architecture.

B. Future Considerations in System Design

Future applications of the proposed activity-dependent ICMS system might require 16, 32 or even higher number of recording and stimulating channels, resulting in higher power consumption and larger silicon area. Fig. 12 shows a breakdown of the area and power consumption for the entire SoC, including both modules. The core area of the SoC excluding I/O pads is 2.6×2.6 mm^2, of which 34% is occupied by the 1.5-to-5-V converter. In this work, the converter can provide a maximum dc load current of $\sim$ 88 μA for an output voltage of 5.05 V, which allows an average stimulus rate of >500 Hz for simultaneous stimulation on all eight channels with maximum stimulus current, given that the microstimulator dissipates 3.5 μW per channel for such stimulation at a rate of 33 Hz.

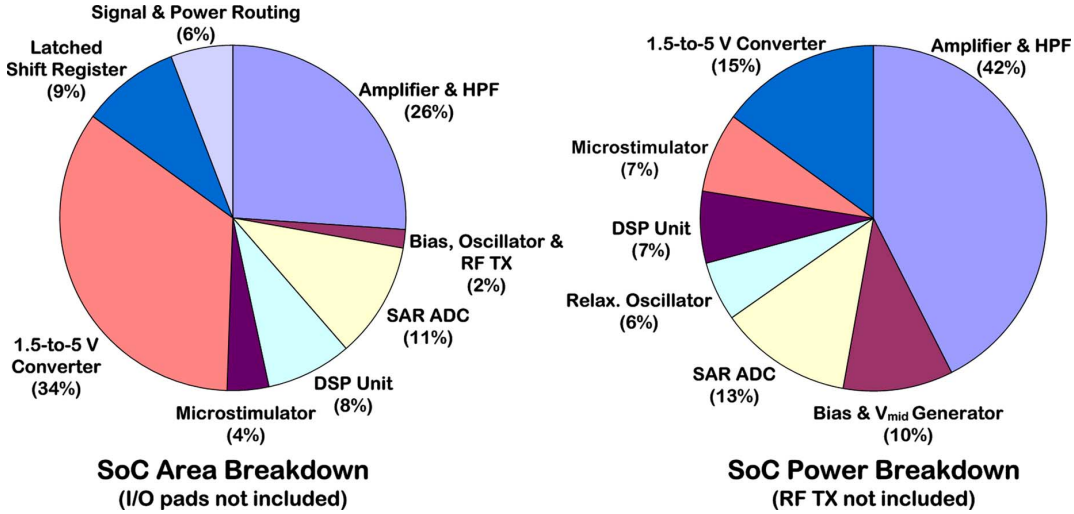

Fig. 12. SoC area and power breakdown.

However, with cortical neuronal firing rates of $<$150 spikes per second [43], the silicon area of the proposed converter can be reduced by $\sim$63%.

The power pie-chart is generated assuming biphasic stimulation at a rate of 33 Hz (anodic: 94.5 μA, 192 μs; cathodic: 31.5 μA, 576 μs) and recording bandwidth of 525 Hz to 5.1 kHz. Excluding the FSK transmitter, the total power consumption is measured to be 375 μW for two modules with the analog recording front-end being the most power-hungry circuit block. Based on simulation results, if we reduce the LNA bias currents to half their current values (all transistors and capacitors should also be sized down accordingly to maintain the same bandwidth), we can save up to 29% and 20% in silicon area and power consumption of the analog recording front-end, respectively. Although this would increase the LNA total input noise by $\sim$41% to 4.8 $\mu\mathrm{V_{rms}}$, it is still less than the background noise of the recording site (5 to 10 μV) [47]. Another effective approach to reduce the front-end power consumption and silicon area is to reduce the SAR ADC resolution to 9 bits. In the proposed design, the input-referred quantization noise of the SAR ADC ($V_{\mathrm{DD}}/(\sqrt{12} \times \mathrm{Gain} \times 2^{\mathrm{ENOB}})$) is $\sim$ 0.8 $\mu\mathrm{V_{rms}}$ for a nominal gain of 60 dB, which is much less than that of the LNA ($\sim$3 $\mu\mathrm{V_{rms}}$). Therefore, reducing the SAR ADC resolution by one bit would not degrade the performance considerably. Further, the power consumption of the secondary amplifier ($\sim$17% of the total system power) driving the capacitive network of the ADC can be significantly reduced as well by decreasing the ADC resolution.

VI. Conclusion

Brain-machine-brain interfaces (BMBIs) are a new generation of neuroprostheses that use information extracted from brain neural activity for titration control of neuromodulation in real time, potentially enhancing their clinical efficacy in restoring a lost motor or sensory function in the disabled. In this paper, we reported on the design, implementation, performance characterization, and *in vivo* testing of a battery-powered IC for activity-dependent ICMS. The single-chip system integrated recording and digitization front-end, neural signal processing unit, 1.5-to-5 V converter, and microstimulating back-end to convert extracellular neural spikes recorded from the somatosensory cortex of a rat's brain to electrical stimuli delivered to the cortical motor area in real time with user-adjustable spike-stimulus time delay, when operating autonomously from a single battery. This system is envisioned to offer a novel *device-based* approach to repairing damaged neural pathways directly within the brain with future rehabilitative applications in behavioral recovery from traumatic brain injury (TBI) [48].

Acknowledgment

The design, implementation, testing, and characterization of the integrated circuit were performed at Case Western Reserve University. The biological experiments were conducted at Kansas University Medical Center. The chip fabrication costs were generously supported by the Advanced Platform Technology (APT) Center – A Veterans Affairs (VA) Research Center of Excellence, Cleveland, OH.

References

[1] D. J. McFarland and J. R. Wolpaw, "Brain-computer interface operation of robotic and prosthetic devices," *Computer*, vol. 41, no. 10, pp. 52–56, Oct. 2008.

[2] M. Velliste, S. Perel, M. C. Spalding, A. S. Whitford, and A. B. Schwartz, "Cortical control of a prosthetic arm for self-feeding," *Nature*, vol. 453, pp. 1098–1101, Jun. 2008.

[3] L. R. Hochberg, M. D. Serruya, G. M. Friehs, J. A. Mukand, M. Saleh, A. H. Caplan, A. Branner, D. Chen, R. D. Penn, and J. P. Donoghue, "Neuronal ensemble control of prosthetic devices by a human with tetraplegia," *Nature*, vol. 442, pp. 164–171, Jul. 2006.

[4] J. D. Weiland and M. S. Humayun, "Intraocular retinal prosthesis," *IEEE Eng. Med. Biol. Mag.*, vol. 25, no. 5, pp. 60–66, Sep./Oct. 2006.

[5] J. P. Rauschecker and R. V. Shannon, "Sending sound to the brain," *Science*, vol. 295, no. 5557, pp. 1025–1029, Feb. 2002.

[6] T. W. Berger *et al.*, "Restoring lost cognitive function: Hippocampal-cortical neural prostheses," *IEEE Eng. Med. Biol. Mag.*, vol. 24, no. 5, pp. 30–44, Sep./Oct. 2005.

[7] R. J. Vetter, J. C. Williams, J. F. Hetke, E. A. Nunamaker, and D. R. Kipke, "Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex," *IEEE Trans. Biomed. Eng.*, vol. 51, pp. 896–904, 2004.

[8] P. K. Campbell, K. E. Jones, R. J. Huber, K. W. Horch, and R. A. Normann, "A silicon-based, three-dimensional neural interface: Manufacturing process for an intracortical electrode array," *IEEE Trans. Biomed. Eng.*, vol. 38, pp. 758–767, 1991.

[9] M. Yin and M. Ghovanloo, "Using pulsewidth modulation for wireless transmission of neural signals in multichannel neural recording systems," *IEEE Trans. Neural Syst. Rehab. Eng.*, vol. 17, no. 4, pp. 354–363, Aug. 2009.

[10] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower CMOS-integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 1, pp. 1–10, Feb. 2009.

[11] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 200 μW eight-channel EEG acquisition ASIC for ambulatory EEG systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3025–3038, Dec. 2008.

[12] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 μW 100 nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[13] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, Jun. 2007.

[14] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[15] A. M. Sodagar, G. E. Perlin, Y. Yao, K. Najafi, and K. D. Wise, "An implantable 64-channel wireless microsystem for single-unit neural recording," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2591–2604, Sep. 2009.

[16] M. S. Chae, Z. Yang, M. R. Yuce, L. Hoang, and W. Liu, "A 128-channel 6-mW wireless neural recording IC with spike feature extraction and UWB transmitter," *IEEE Trans. Neural Syst. Rehab. Eng.*, vol. 17, no. 4, pp. 312–321, Aug. 2009.

[17] B. K. Thurgood, D. J. Warren, N. M. Ledbetter, G. A. Clark, and R. R. Harrison, "A wireless integrated circuit for 100-channel charge-balanced neural stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 6, pp. 405–414, Dec. 2009.

[18] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking capacitors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 231–244, Sep. 2008.

[19] T. G. Constandinou, J. Georgiou, and C. Toumazou, "A partial-current-steering biphasic stimulation driver for vestibular prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 2, pp. 106–113, Jun. 2008.

[20] M. Ortmanns, A. Rocke, M. Gehrke, and H. J. Tiedtke, "A 232-channel epiretinal stimulator ASIC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2946–2959, Dec. 2007.

[21] J. J. Sit and R. Sarpeshkar, "A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 nA dc error for 1-mA full-scale stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 172–183, Sep. 2007.

[22] X. J. Feng, B. Greenwald, H. Rabitz, E. Shea-Brown, and B. Kosut, "Toward closed-loop optimization of deep brain stimulation for Parkinson's disease: Concepts and lessons from a computational model," *J. Neural Eng.*, vol. 4, pp. L14–21, 2007.

[23] A. Jackson, C. T. Moritz, J. Mavoori, T. H. Lucas, and E. E. Fetz, "The neurochip BCI: Towards a neural prosthesis for upper limb function," *IEEE Trans. Neural Syst. Rehab. Eng.*, vol. 14, no. 2, pp. 187–190, Jun. 2006.

[24] S. Venkatraman, K. Elkabany, J. D. Long, Y. Yao, and J. M. Carmena, "A system for neural recording and closed-loop intracortical microstimulation in awake rodents," *IEEE Trans. Biomed. Eng.*, vol. 56, no. 1, pp. 15–22, Jan. 2009.

[25] J. Mavoori, A. Jackson, C. Diorio, and E. Fetz, "An autonomous implantable computer for neural recording and stimulation in unrestrained primates," *J. Neurosci. Methods*, vol. 148, pp. 71–77, 2005.

[26] A. T. Avestruz, W. Santa, D. Carlson, R. Jensen, S. Stanslaski, A. Helfenstine, and T. Denison, "A 5 μW/channel spectral analysis IC for chronic bidirectional brain-machine interfaces," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3006–3024, Dec. 2008.

[27] T. Chen, K. Chen, Z. Yang, K. Cockerham, and W. Liu, "A biomedical multiprocessor SoC for closed-loop neuroprosthetic applications," in *IEEE Int. Solid State Circuits Conference (ISSCC'09) Dig. Tech. Papers* , San Francisco, CA, Feb. 8–12, 2009, pp. 434–435.

[28] J. Lee, H. G. Rhew, D. R. Kipke, and M. P. Flynn, "A 64-channel programmable closed-loop neurostimulator with 8-channel neural amplifier and logarithmic ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1935–1945, Sep. 2010.

[29] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. L. Carlen, and R. Genov, "The 128-channel fully differential integrated neural recording and stimulation interface," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 149–161, Jun. 2010.

[30] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, "An activity-dependent brain microstimulation SoC with integrated 23 nV/rtHz neural recording front-end and 750 nW spike discrimination processor," in *IEEE Symp. VLSI Circuits Dig. Papers*, Honolulu, HI, Jun. 16–18, 2010, pp. 223–224.

[31] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 410–416, Mar. 1998.

[32] C. Boffino, E. Bonizzoni, O. Khouri, G. Pollaccia, C. Resta, and G. Torelli, "A low-ripple voltage tripler," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'06)*, Island of Kos, Greece, May 21–24, 2006, pp. 2753–2756.

[33] M. Paavola, M. Laiho, M. Saukoski, and K. Halonen, "A micropower 2MHz CMOS frequency reference for capacitive sensor applications," in *Proc. Eur. Conf. Circuit Theory and Design*, Aug. 2005, vol. 3, pp. 425–428.

[34] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy ADC for smart dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, Jul. 2003.

[35] M. Azin and P. Mohseni, "A 94-μW 10-b neural recording front-end for an implantable brain-machine-brain interface device," in *Proc. IEEE Biomed. Circuits and Systems Conf. (BioCAS'08)*, Baltimore, MD, Nov. 20–22, 2008, pp. 221–224.

[36] A. Jackson, J. Mavoori, and E. E. Fetz, "Long-term motor cortex plasticity induced by an electronic neural implant," *Nature*, vol. 444, pp. 56–60, Nov. 2006.

[37] M. Ghovanloo and K. Najafi, "A compact large-voltage-compliance high-output-impedance programmable current source for implantable microstimulators," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 1, pp. 97–105, Jan. 2005.

[38] M. Azin and P. Mohseni, "A high-output-impedance current microstimulator for anatomical rewiring of cortical circuitry," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'08)*, Seattle, WA, May 18–21, 2008, pp. 2502–2505.

[39] M. M. Ahmadi, "A new modeling and optimization of gain-boosted cascode amplifier for high-speed and low-voltage applications," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 3, pp. 169–173, Mar. 2006.

[40] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York, NY: Oxford Univ. Press, 1999.

[41] S. Guo, H. Lee, and P. Loizou, "A 9-bit configurable current source with enhanced output resistance for cochlear stimulators," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC'08)*, Sep. 2008, pp. 511–514.

[42] K. Sooksood, T. Stieglitz, and M. Ortmanns, "An active approach for charge balancing in functional electrical stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 162–170, Jun. 2010.

[43] M. A. L. Nicolelis, A. A. Ghazanfar, B. M. Faggin, S. Votaw, and L. M. O. Oliveira, "Reconstructing the Engram: Simultaneous, multisite, many single neuron recordings," *Neuron*, vol. 18, pp. 529–537, Apr. 1997.

[44] K. Limnuson, H. Lu, H. J. Chiel, and P. Mohseni, "VLSI implementation of a template subtraction algorithm for real-time stimulus artifact rejection," in *Proc. 32nd Annu. Int. IEEE Eng. Med. Biol. Conf. (EMBC'10)*, Buenos Aires, Argentina, 2010, pp. 2939–2942.

[45] M. Azin, H. J. Chiel, and P. Mohseni, "Comparisons of FIR and IIR implementations of a subtraction-based stimulus artifact rejection algorithm," in *Proc. 29th Annu. Int. IEEE Eng. Med. Biol. Conf. (EMBC'07)*, Lyon, France, Aug. 23–26, 2007, pp. 1437–1440.

[46] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1163–1168, Dec. 1987.

[47] K. Guillory and R. A. Normann, "A 100-channel system for real-time detection and storage of extracellular spike waveforms," *J. Neurosci. Methods*, vol. 91, pp. 21–29, 1999.

[48] R. J. Nudo, "Mechanisms for recovery of motor function following cortical damage," *Curr. Opin. Neurobiol.*, vol. 16, pp. 638–644, 2006.

Meysam Azin (S'06) was born in 1980. He received the B.S. degree in electrical engineering from Amir Kabir University of Technology, Tehran, Iran, in 2002, and the M.S. degree from Sharif University of Technology, Tehran, Iran, in 2004. In 2004, he joined KavoshCom Asia, a private R&D company in Tehran, where he was directing a design team to develop a low-cost WiFi IP phone. Since 2006, he has been working toward the Ph.D. degree at Case Western Reserve University, Cleveland, OH. His research interests include analog and mixed-mode integrated circuits for advanced biomedical microsystems, low-power wireless sensors and high-performance data converters.

David J. Guggenmos was born in 1983. He received the B.S. degree in psychology from Iowa State University, Ames, in 2005. Since 2005, he has been working toward the Ph.D. degree at the University of Kansas Medical Center, Kansas City, KS. His research interests include motor cortical plasticity and the effects of electrical stimulation on neural tissue.

Scott Barbay was born in 1957. He received the B.S. and M.S. degrees in experimental psychology from University of Louisiana, Lafayette, in 1980 and 1989, respectively, and the Ph.D. degree in 1994 from Texas Christian University, Fort Worth, concentrating on behavioral neuroscience.

He has had postdoctoral training at the Laboratory of Systems Neuroscience at the National Institute of Mental Health, Poolesville, MD, in 1994–1996 and at the Department of Neurobiology and Anatomy at the University of Texas Health Science Center, Houston, TX, in 1996–1997. Presently he is a senior scientist in the Cortical Plasticity Laboratory in the Department of Molecular and Integrative Physiology and Landon Center on Aging at the University of Kansas Medical Center, Kansas City, KS. His primary research interests are in translational models of stroke recovery that emphasize neurophysiological and neuroanatomical reorganization within the cerebral cortex associated with recovery of motor function after stroke.

Dr. Barbay is a member of the Society for Neuroscience and the Association for Psychological Science.

Randolph J. Nudo was born in 1953 in Uniontown, PA. He studied electrical engineering at the University of Notre Dame, South Bend, IN, before completing the B.S. degree in psychology at Pennsylvania State University, University Park, in 1977. He then received the M.S. and Ph.D. degrees in psychology from Florida State University, Tallahassee, in 1980 and 1985, respectively.

He completed a postdoctoral fellowship in physiology at the University of California at San Francisco in 1987. He joined the faculty of the University of Texas Health Science Center in Houston, TX, as a tenure-track Assistant Professor in 1988, and was promoted to Associate Professor with tenure in 1996. Since 1997, he has been on the faculty of the University of Kansas Medical Center, Kansas City, KS, now holding the titles of Professor of Molecular and Integrative Physiology, Marion Merrell Dow Distinguished Professor in Aging, and Director of the Landon Center on Aging. He has published his work in numerous high-profile journals in the field of neuroscience, including *Science*, *The Journal of Neuroscience*, *Journal of Neurophysiology*, *Cerebral Cortex*, and *Nature Medicine*. His research focuses on translating basic science research into more effective clinical interventions for neurological disorders that accompany aging. He is recognized internationally for his work on the effects of rehabilitative training on functional plasticity after stroke. His research activities are currently funded by the National Institutes of Health, the US Army, and the American Heart Association.

Dr. Nudo is on the editorial boards of *Neurorehabilitation and Neural Repair*, *Restorative Neurology and Neuroscience*, and *Neuroscience and Biobehavioral Reviews*. He is also deputy editor of Brain Stimulation, Basic, Translational and Clinical Research in *Neuromodulation*. He is a member of the board of directors of the American Society of Neurorehabilitation. In 2007, he received the prestigious Javits Investigator Award in Neuroscience.

Pedram Mohseni (S'94–M'05) was born in 1974. He received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1996 and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1999 and 2005, respectively.

He joined the faculty of Electrical Engineering and Computer Science Department at Case Western Reserve University, Cleveland, OH as a tenure-track Assistant Professor in August 2005 with a secondary appointment in the Biomedical Engineering Department starting in 2009. His research interests include analog/mixed-signal/RF integrated circuits and microsystems for neural engineering; wireless sensing/actuating systems for brain-machine interfaces; biomedical microtelemetry; and assembly/packaging of biomicrosystems. He has authored numerous papers in refereed IEEE journals and conferences, and has served as a technical reviewer for a number of the IEEE publications.

Dr. Mohseni is a member of the IEEE Solid-State Circuits, Circuits & Systems, and Engineering in Medicine and Biology Societies. He is currently an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II and IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and also serves on the Analog Signal Processing (ASP) and Biomedical Circuits and Systems (BioCAS) Technical Committees of the IEEE Circuits & Systems society. He is a recipient of the 2008 EECS Faculty Research Award for Exceptional Achievement at Case Western Reserve University and the 2009 National Science Foundation CAREER Award.