The Nordic Electronic Packaging Guideline

Multi Chip Module Chapter

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1 INTRODUCTION to Multi Chip Modules

This chapter covers the different varieties of multichip modules. Chapter 1.1 to 1.7 is an introduction to the subject and is intended for those who want an overview of the technology. Part 2 cover each of the substrate technologies in more detail. The attachment and encapsulation technologies are covered in other parts of this guideline. Most of the material in the chapters; 2.2.1.1 to 2.2.1.5, 2.2.2.1 to 2.2.2.5 and 2.2.3.1 to 2.2.3.5 is with the authors permission taken from the book "*Electronic Components, Packaging and Production*" [1] by Leif Halbo and Per Øhlckers.

1.1 What is Multi Chip Modules

A Multi Chip Modules, abbreviated "MCM", is described as a package combining multiple ICs into a single system-level unit. The resulting module is capable of handling an entire function. An MCM can in many ways be looked upon as a single component containing several components connected to do some function. The components are normally mounted un-encapsulated on a substrate where the bare dies are connected to the surface by wire bonding, tape bonding or flip-chip. The module is then personated by some kind of plastic moulding. The module is then mounted on the PCB in the same way as any other QFP or BGA component. MCMs offer an astounding variety of advantages instead of mounting packaged components directly on the PCB:

- Performance improvements, such as shorter interconnect lengths between die (resulting in reduced time of flight), lower power supply inductance, lower capacitance loading, less cross talk, and lower off-chip driver power
- Miniaturization, since MCMs result in a smaller overall package when compared to packaged components performing the same function, hence resulting I/O to the system board is significantly reduced
- Time-to-market, making them attractive alternatives to ASICs, especially for products with short life cycles
- Low-cost silicon sweep, allowing integration of mixed semiconductor technology, such as SiGe or GaAs
- Configuration as hybrids, including surface mount devices in the form of chip scale or micro-ball grid array (BGA) packages and discrete chip capacitors and resistors
- Simplification of board complexity by sweeping several devices onto one package, thereby by reducing total opportunities for error at the board assembly level, as well as allowing for a cheaper PCB
- Improved reliability by decreasing the number of interconnects between "components" and boards
- Adding new functions to a fixed footprint
- Capability of accommodating a variety of second-level interconnects. While BGA are the most popular, lead-frame solutions can be employed for plugability, enabling modularity for upgrades.

Although there is many good reasons for using MCMs, there are also some difficulties and disadvantages. The most important problem that hinders a more widespread use is the availability of components in "Bare Die" form. Although the market is improving, there is still a long way to go before most components are available as "Bare Dies". The other concern is cost. Although the newer MCM-L technologies have a low cost potential, cost is rarely the sole reason for going into MCMs.
There are three separate technologies involved in the manufacture of MCM:

1. Substrate technology
2. Die attach and bonding technology i.e. Wire-Bond, TAB or Flip-Chip
3. Encapsulation technology

Normally these items can be addressed separately.

1.2 MCM marked forecast

U.S. has been the primary consumer of MCMs, Figure 1 shows regional growth is shifting away from the U.S. and into Europe and Asia over the next five to seven years. This is primarily due to the growing telecom

need in Europe and the drive for miniaturisation in consumer products coming out of Japan. Both of these drive the need for lightweight solutions that are conservative on real estate consumption. Another significant trend is the migration to flip chip MCMs. Flip chip MCMs are expected to grow at 108% CAGR to comprise 18% of the MCM opportunity by 2001 [1]. These are indicators that known good die and an infrastructure for flip chip bumping are becoming a realisation.

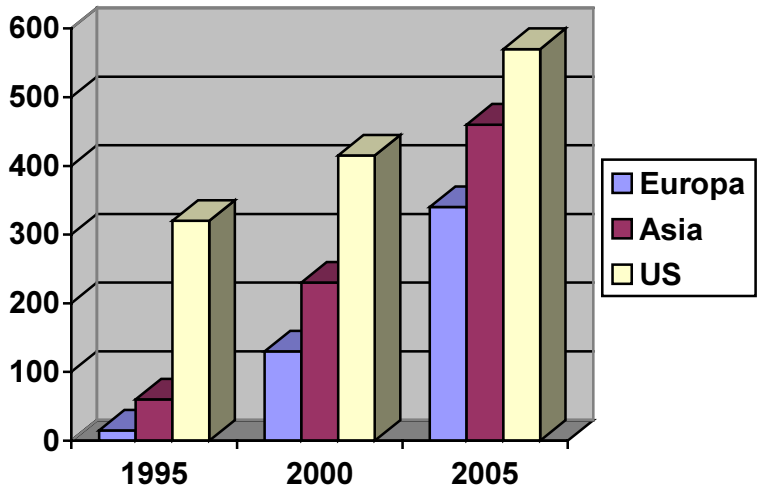

Figure 1. The data for MCM and MCP regional growth by revenue show that grow is shifting away from the U.S. and into Europe and Asia over the next five to seven years. Source: BPA Associates and Electronic Trends.

1.3 Choice of right technology

There are several aspects to consider when choosing the right technology for a multi chip technology. Below follows a discussion of some of them.

1.3.1 MCMs vs. ASICs

MCM designs are very practical when integration of mixed silicon technology is required. Silicon germanium is an enabler of high-frequency applications, such as global positioning systems and satellite systems operating in the GHz frequency range. For these designs, MCMs provide the integration required plus the benefit of a smaller overall package combined with performance. The best argument for using MCMs over ASICs, though, is time-to-market. MCMs can enable functional products to enter the marketplace several times faster than comparable ASIC designs. This is significant for prototype designs or products for competitive low-cost demand.

For products with longer life cycles, the total cost scenario must be analysed. Assembly yield considerations become significant for high-volume applications. Although MCMs have a low up-front cost compared with ASICs, factors such as die yield and assembly yield can keep costs high over the life of the product. The advantage of ASICs in this scenario would be the opportunity to spread the up-front engineering cost over the piece price and leverage the resulting high yield. In the case of an existing product where mature die is being utilised and product shrink is required, an MCM might make more sense. In many cases, the optimum solution might dictate the use of MCM technology to achieve acceptance, followed by an ASIC to support production volumes. Integration of silicon sometimes enables incorporating ASICs onto an MCM to combine memory and clock drivers to overcome the challenges of the speed limitations at the board level.

1.3.2 High frequency

The electrical performance of a package is mainly determined by the geometries and materials used in the package. If high frequency properties are important, a technology must be chosen that offers dielectrics with both low dielectric constant and low dielectric loss. The metal system must have high specific conductivity to minimise the conduction losses. At high frequency, the skin effect means that only the surface of the conductor contributes to the conduction. To obtain well-controlled characteristic impedance the technology must allow precisely defined conductor edges. This means that substrate and the added dielectric layers must have a smooth surface. Water absorption in organic dielectrics will cause a significant change in dielectric constant, changing the impedance of a line. In a harsh environment, this might imply that a circuit with organic dielectric has to be packaged in a hermetic package.

1.3.3 Thermal properties

For some applications, the thermal properties are important. The first way to improve the thermal properties is to choose a substrate with a good thermal conductivity, like certain ceramic materials (beryllium oxide or silicon nitride), silicon or metal based substrates. If the substrate itself is not able to cope with the power, alternative heat paths have to be found. This can be to attach the chips to some type of heat sinks, and use natural or forced convection priciples to bring the die-temperature to the specified level.

1.3.4 Miniaturisation

If miniaturisation is the main goal, parameters like line width, line spacing and via-hole dimensions become very important. The type of electrical connection between the die and the substrate will also play a role, as both wire bonding and TAB needs certain spacing along the chip for the connection. Flip Chip technology on the other hand requires no extra area.

1.3.5 Cost

In many applications, cost is the main constraint. When discussing cost it is very important to consider the production volume, as some technologies will have a substantial “start up” cost. The way the total circuit is divided (or partitioned) into different sub modules will be very important for the total cost. Production yield and reparability will also have a mayor influence on the cost, as well as the problems associated with known good die (KGD).

The cost can be divided into substrate cost, which covers both the mechanical carrier as well as the conductor pattern. Both material cost and processing cost must be considered. The choice of encapsulation also has a big influence on the cost, and must be considered in connection with the environment in which the circuit is going to operate. Another important factor to consider is the test issue. This must be taken into account right from the module design.

1.4 Substrate Technology overview

The substrate forms the basis of the MCM and is the technology, which gets most attention. There exist an overwhelming amount of different technologies, each with its own set of advantages and disadvantages. To classify the different technologies, a division in the groups is often used based on the fabrication technique. The three techniques are Lamination, Deposition and Ceramic sintering.

1.4.1 MCM-L

Lamination based MCM’s is today a very promising technology for many applications. Although greatly modified in some respects the MCM-L technologies is much based on the traditional printed circuit board technique where several layers of conductors and organic dielectrics are laminated together with pressure and heat cured. Several of the MCM-L technologies today are actually very fine-line printed circuit boards. Since these technologies have potential for low cost and high density, numerous variations of the technology are developed.

Advantages
- Low cost
- Medium to high packaging density
- Through visa for direct backside termination

Disadvantages
- Relative high coefficient of thermal expansion may cause problem when attaching large silicon chips.
- High moisture absorption put requirements on encapsulation.
- Low thermal conductivity implies more complex cooling design for power hungry IC's.

1.4.2 MCM C

Ceramic multichip modules are much of a classic in the MCM world. There are three main types; Thick Film, High Temperature Cofired and Low Temperature Cofired. All three are based on patterning by screen-printing where a ceramic or metal paste is pressed through a screen onto a substrate or a ceramic tape. The screen itself is manufactured with a photolithographic process from a film generated from the design data.

1.4.2.1 Thick Film

The thick film layers of conductors or dielectrics are added one at a time. After each layers is printed onto the ceramic base substrate, the substrate go through a drying stage, where the binder in the paste is burned off. The last stage is the firing which takes place at approximately 800 ^{0}C.

The main advantage of the thick film process is the relative simple process and cheap materials. Since this is a screen printing process, the minimum line width that can be printed is in the area of 100um. If narrower lines and spaces are needed, a combination of screen-printing and photolithography is used. The relative low firing temperature also allows a variety of metal pastes with a wide range of conductivities.

Advantages
- Low tooling cost implies acceptable prices, also for low volumes.
- Relative low coefficient of thermal expansion that is compatible with silicon.
- Medium to high thermal conductivity allows a simpler thermal design.

Disadvantages
- Low to medium packaging density
- Vias through base substrate are relatively large and must be pre-cut with a laser.

1.4.2.2 High Temperature Cofired Ceramic (HTCC)

As the name implies in this technology all the layers is fired at the same time under high temperature (approx. 1600^{0}C). This is probably one of the most used ceramic technology and its main use today is in single chip packaging where high I/O IC's is mounted in a Pin Grid Array (PGA) or a Ball Grid Array (BGA). There are not many metals that survive 1600 ^{0}C firing so the chosen conductor material is Tungsten. This is however, a metal with relative low electrical conductivity, and therefore not too well suited for the inter-chip interconnect in MCMs. The high shrinkage during firing also makes small vias difficult.

The conductor patterns is added to a dielectric tape by screen printing after the via-holes are punched in the tape. The via-holes are also filled with conductive paste in the printing process. The layers are then stacked up, laminated under pressure and temperature, and at last fired in an oven at 1600 ^{0}C.

Advantages
- Low price at medium to high volumes
- Relative low tooling cost for low volume production, where a numerical punch can punch one via on one layer at a time
- At higher volumes a punch that punch all vias on one layer can be used
- High number of layers possible (>50)
- Easy to terminate with PGA, BGA or CQFP
- Very good thermal performance ($\lambda \approx 30$ W/mK)

- Chip cavities for later hermetic sealing is possible
- Relative low coefficient of thermal expansion that is compatible with silicon

Disadvantages
- High dielectric constant of dielectric material (ε_r~10)
- Low conductivity of conductors
- Very difficult to make solid ground-planes due to problems with warpage
- High tooling cost
- High weight

1.4.2.3 Low Temperature Cofired Ceramic (LTCC)

As the name implies that this is the same process as the HTCC except that in this technology all the layers is fired at the same time under a relatively low temperature (approx. 800 ^{0}C). The low firing temperature enables the use of precious metals in the conducting layers. The dielectric has somewhat lower dielectric constant.

Advantages
- Low price at medium to high volume
- Relative low tooling cost for low volume production, where a numerical punch can punch one via on one layer at a time
- At higher volumes a punch that punch all vias on one layer can be used
- Easy to terminate with PGA, BGA or CQFP
- High number of layers possible (>50)
- Chip cavities for later hermetic sealing is possible
- Relative low coefficient of thermal expansion that is compatible with silicon

Disadvantages
- Medium to high dielectric constant of dielectric material
- Impossible with solid ground-planes due to warpage
- High tooling cost
- High weight
- Difficult shrinkage control result in poor dimensional control
- Low to medium thermal performance ($\lambda \approx 3$ W/mK)

1.4.3 MCM D

Deposited MCMs are MCMs where the conducting layers are deposited on some sort of carrier, usually ceramic but also on silicon. The metal deposition is normally done by sputtering or evaporation in vacuum. After the deposition process the metallized surface is patterned by applying a photosensitive resist that after exposing and developing function as an etch resist. All metal not covered by the resist is removed.
After the patterning of one layer, a dielectric coating can be applied. For organic dielectrics this are often done by spinning or spraying, whereas non-organic dielectrics are deposited by Chemical Vapour Deposition (CVD). Holes in the dielectric are opened by a similar photolithographic process and new layers can be added.

1.4.3.1 Classic thin-film

Classic thin-film hybrid technology is an example of a technique that fall into this technology. This technology is based on one thin gold signal layer on top of an alumina substrate. Crossovers are made by wire bonding. The backside of the substrate can be gold coated for the use as a ground plane.

Advantages
- Narrow lines possible.
- Low dielectric loss tangent ($\approx$ 0.0001)

- Resistors and small capacitors can be integrated in the wiring
- Trimming of resistors is possible
- Good - very good thermal performance, depending on the substrate ($\lambda \approx$ 30-200 W/mK)

Disadvantages
- One layer may cause routing problems.
- Long bond wires for crossovers may be too inductive for some applications.
- 50 ohm lines will be as wide as the thickness of the substrate.
- High dielectric constant ($\approx$ 7-10)
- Medium cost

1.4.3.2 Silicon thin film

Silicon thin film technology is a simpler version of the VLSI process, where conducting layers of aluminium, separated by layers of silicon dioxide is placed on top of a silicon wafer. Often older process lines designed for semiconductor fabrication is converted to MCM lines. Often one or two layers of polymer thin film is deposited on the top aluminium layer. The low thickness of the silicon dioxide compensates for the low thermal conductivity.

Advantages
- Very narrow lines is possible on the aluminium layers (<2um)
- Narrow lines possible on additional polymer layers (<10um)
- Small via holes, especially on the aluminium layers.
- Perfect thermal match to silicon semiconductors
- Very good / Good thermal performance (The low thickness of the silicon dioxide compensate for the low thermal conductivity of SiO_2.

Disadvantages
- No through vias, all contact pads must be at the top.
- Thin metal layers may force the use of wide lines due to high resistance.
- If topside ground planes are used, wide lines will have a very high capacitance due to the thin silicon dioxide layers.
- High cost substrate

1.4.3.3 Polymer thin film

Polymer thin film a technology where thin (<15um) polymer dielectric films is deposited on a stable base substrate such as silicon or alumina. Thin (2-5um) conductor films, usually copper, is then deposited and processed photolithographically. The lower dielectric constant of the polymers (Polyimide, BCB, etc) together with the 10-15um thick dielectric make 50 Ohm lines more practical.

Advantages
- Narrow lines is possible ($\approx$ 10um)
- Small to medium via holes.(10-50um)
- Better suited for 50 Ohm lines.

Disadvantages
- No through vias, all contact pads must be at the top.
- Poor thermal conductivity of the polymer limits the applicability for higher power devices.
- Difficult to go above two layers.
- High cost

1.5 Module Assembly Techniques

1.5.1 Wire Bond

Wire bonding is currently the dominant chip to substrate connection method. The chip is attached to the substrate with the bonding pads facing away from the substrate. Connecting wires (bond wires) made of gold or aluminium are then attached by welding on the chip pads, pulled to the substrate pads and again attached by welding. Details can be found in the wire-bond guide.

Advantages

- Well proven method with good yield
- Low cost for low to medium production volumes
- No special chip metallization required, chips are normally designed for wire bond
- Can also be used if a few extra crossovers is needed on the substrate
- Function well down to a pad-pitch of approximately 80μm

Disadvantages

- Relatively slow, one bond at the time
- The size and movement of the bond-head may restrict how closely chips can be placed
- Inductance of bond-wires may limit the use in extreme high frequency devices
- Bondable (pure) gold is normally required on the substrate

1.5.2 Tape Automated Bonding (TAB)

Tape Automated Bonding is a technique where the chip is attached to a polyimide tape prepared with copper conductors. This attachment called the inner lead bond is normally done at the wafer “Fab”. The copper wires are connected to the pre-bumped chips by thermocompression bonding, typically all in one go (gang bonding). This, however, may cause cracks in the chip passivation and sometimes one and one lead is connected at the time to allow better control of the bonding. The chips are normally distributed on rolls.

In the assembly plant, the tape is cut in such way that the outer part of the conductors (leads) is exposed. The chip/film assembly is then aligned and soldered or glued to the substrate using conductive adhesive. Normally the cutting and bonding is done in one operation with a tool specially designed for the chip/film assembly. In some applications, a technique called “flip-TAB” is used. In this case, the chips are faced towards the substrate before bonding. This allows much shorter wires and therefore increased high-frequency properties as well as increased packaging density.

Because of the high tooling investments, this technique is mostly used in very high volume products such as watches and LCDs.

Advantages

- Well suited for very high volume production; all bonds in one operation and the chips is delivered on rolls or in cartridges.
- Good electrical performance especially if a tape with a separate ground plane is used.
- Fan-out on the tape makes it possible to mount chips with fine pad pitch on a substrate with a much larger pad pitch.

Disadvantages

- Different bonding tools must be used for different outer lead area dimensions
- Bonding tools are expensive
- TAB film must be specially designed for every chip type
- Normally the chips need special bumping and metallurgy, which prohibit the use of off the shelf chips
- Cross-talk may occur in single layer film at high frequency, especially if the length of the conductors on the film is large
- Inductance of long conductors on single layer films may cause problems in the power supply of power hungry chips

1.5.3 Flip-Chip (FC)

Flip Chip is a very interesting chip attachment technique that will be one of the dominant techniques. The chips are then placed upside down on the substrate, which have the same pad pattern as the chip. This technique requires the formation of bumps onto the chip pads. These bumps can be solder alloy balls or copper bumps in case of solder connections. A lot of effort is currently put into the use of adhesive flip-chip technology. When solder or isotropic conductive adhesive is used, an underfill typically of epoxy is applied on two of the edges of the chip and flows under the chip by the capillary force. This will significantly improve the reliability of the joint. In case of solder flip-chip, the whole process, including the underfill can be done in a modern SMT line.

Advantages

- Very high IO count possible by covering the whole chip area with pads
- Ultimately cheap when infrastructure is settled
- Self alignment under reflow ease registration requirements
- Ideal for high frequency applications due to very low contact inductance
- Work with modern SMT lines equipped for Flip-Chip

Disadvantages

- Require extra metallization on chips
- Difficult to get chips with bumps in low quantities
- Fine pad pitch will require fine pitch boards
- The underfill of epoxy is slow
- Big chips mounted on polymer substrates require underfill to survive thermal cycling
- Bear dies is difficult to test

1.6 Module Encapsulation Techniques

When using bare dies on a substrate the chips must normally be protected from the environment. The most common dangers for the bare chips are mechanical damage and moisture related corrosion. A flip chip with a proper underfill does not normally require extra encapsulation. A few of the most popular techniques is described below.

1.6.1 Dam Moulding

Dam moulding is a encapsulation technique where a high viscosity encapsulant is dispensed as a dam and then the dam is filled with a low viscosity encapsulant. The dam and contents is then cured.

Advantages

- Simple and easy adaptable
- Almost no tooling cost
- Low thermal stress under production
- Well suited for BGA type packages

Disadvantages

- Slow, not suited for very high production volumes
- High thermal resistance, cooling depends very much on substrate

1.6.2 Transfer Moulding

Transfer moulding is the high volume choice for encapsulation. A special moulding tool is designed for each module type. One or more modules are mounted on a contact-lead frame. The moulding tool is then clamped around each module only exposing the leads. A plastic mould is the injected under high temperature and pressure. The tool is cooled and the modules are ejected.

Advantages
- Fast, good for high volume production
- Cheap materials

Disadvantages
- Expensive tooling prohibit the use in low production volumes
- Expensive moulding equipment
- High thermal stress for the modules
- Best for modules with low to medium lead count
- High thermal resistance

1.6.3 Hermetic Casing

Hermetic casing is to put the chip inside a box with a welded lid. The box is welded in nitrogen atmosphere, to fill the box with nitrogen. To prevent leakage in the pin feed-throughs, hermetic glass sealing is used for every pin. The box (package) is normally made of gold plated Kovar. Traditionally this has been the only way to guarantee total hermeticity.

Advantages
- Guaranteed hermeticity
- Medium - low thermal resistance, depending on the substrate
- Good shielding properties

Disadvantages
- High cost
- High weight
- Only suited for low to medium pin-count modules

1.7 Testing issues

The strategy of testing of multi chip modules must be considered carefully before starting the design of a multi chip module. Because of the dense packaging, placement of test probes can be difficult.

1.7.1 Boundary scan

IEEE 1149.1 "Test Access Port and Boundary Scan Architecture" is a scan method for printed circuit boards. The memory elements which make the scan chain, are placed in the bonding pads of the integrated circuits (IC). Each IC also contains a small controller with which the user may control what to test. The intended use of B-Scan was interconnect test where a test pattern is imposed on the outputs of one IC, and the response is received at the input of another IC. The concept is also useful for other features like checking correct placement, starting and receiving results from component self-test, etc.

Advantages
- "Virtual pins" simplifies the in-circuit test fixture
- Gives easy access to confined areas on printed circuit boards
- Gives easy control of which part to test
- May be used to load programs into FPGA and Flash components

Disadvantages
- Not useful for testing complex components on the board
- Runs at low speed

- Requires long time to shift in and out test patterns and responses
- Requires that the used components have B-Scan integrated

1.7.2 Built-In Self Test (BIST)

BIST is mainly used on integrated circuits, but is also useful for printed circuit boards. The method solves the problem of testing isolated parts of the circuit, which otherwise is difficult to access for testing. The concept is to use linear feedback shift registers (LFSR) as a pseudo random pattern generator (PRPG) and a signature analyser (SA). The pattern generator requires a starting "seed" to generate the desired sequence of patterns. This may be loaded through a shift sequence, for instance by using B-Scan. The purpose of the signature analyser is to compress the response into one single word that is shifted out, for instance through B-Scan.

Advantages

- May be the only way to test embedded RAM, ROM, etc.
- Runs at system speed

Disadvantages

- Requires large space in IC's
- Requires extra components on printed circuit boards

1.8 Acronym list

The world of MCM's sports more acronyms than most other technology. Below is a table of the most used acronyms together with a short explanation.

Table 1 Acronym list MCM

Al_2O_3	Aluminium Oxide, also called Alumina
AlN	Aluminium Nitride
ASIC	Application Specific Integrated Circuit
BCB	Benzocyclobutene (photoimageable dielectric)
BeO	Beryllium Oxide also called Beryllia
BGA	Ball Grid Array,
BIST	Built-In Self Test,
FC	Flip Chip,
HTCC	High Temperature Ceramic Carrier
KGD	Known Good Die, naked chips (dies) that is fully tested before shipment from factory
LCD	Liquid Crystal Display
LTCC	Low Temperature Ceramic Carrier
MCM	Multi Chip Module, a way of mounting several dies on one substrate and packaging it as a single component
MCM-C	Multi Chip Module using Ceramic materials
MCM-D	Multi Chip Module using Deposition technique
MCM-L	Multi Chip Module using Lamination technique
MCP	Multi Chip Package
PCA	Printed Circuit board Assembly, a PCB with mounted components.
PCB	Printed Circuit Board, a single or multilayer interconnection board for components
QFP	Quad Flat Pack,
SBU	Sequential Build Up
TAB	Tape Automated Bonding,
WB	Wire Bond

2 CONCLUSION / GUIDELINE

There exist an increasing number of different MCM technologies. New processes and materials are continuously introduced, and many smaller or larger alterations are made to existing processes. Mixing of different technologies means that to some extent, the borders between different technologies are erased. One example is the introduction of the “Combi film” technology where thick and thin film techniques are mixed on the same circuit. In addition, the border between multi chip modules and PCB technology is to some extent wiped out with the new fine line (Sequential Build-Up, SBU) laminates.

2.1 MCM L

With over 16 million units being produced worldwide in 1997, multichip modules on laminate (MCM-L) are the fastest growing component of overall MCM sales. MCM-Ls are projected to comprise almost 70% of all MCMs produced by 2001. Initially popular in telecommunications, MCM-Ls are expected to grow in the automotive and office areas at greater than 25% compound annual growth rate (CAGR) over the next four years [1]. According to Technology Forecasters, MCM-L units produced in 1997 outweigh all other MCMs by about two to one.

Clearly the infrastructure for ceramic MCMs has been in place long before laminates. In the mid-1970s, ceramic MCMs were capable of integrating over 100 chips on a single substrate. MCM-L solutions, however, are beginning to span a wide array of applications once reserved only for ceramics. A significant factor in this trend is the introduction of low-melt flip-chip processes. Flip-chip die can now be connected to laminate carriers using slightly modified surface mount processes. Advances in laminate structures, such as high-density Microvia substrates, have accommodated line widths and spacings down to 50 µm and vias down to 90 µm. This is significant for enabling the escape of the dense I/O grid of flip-chip die. The smaller vias and fine lines allow more signal lines to be routed between the pads, thereby reducing the overall number of layers required. Advancements in moisture sensitivity coupled with new underfill formulations have lead to robust designs. These designs can withstand factory conditions of 30°C and 60% relative humidity for up to one week and suffer no adverse effects during the subsequent second-level assembly processes.

These advancements have afforded MCM-Ls the opportunity to fill requirements in mobile computing, automotive and RF applications. Microprocessors with L2 cache on laminate carriers are being used in laptop computers. In the last twelve months, three suppliers of automotive applications have developed MCM-L packages capable of surviving the harsh under-the-hood environment. With respect to RF packaging, the Semiconductor Industry Association (SIA) roadmap indicates the performance basis for selecting ceramic over plastic laminate will be reduced as improvements in high-performance plastics exhibit cost advantages over ceramics [3].

2.1.1 Sequential Build Up Process

The additive process of the SBU technology avoids the limitations inherent in the subtractive process that is used with the traditional laminates (pre laminated with copper foils). There is either any need for all the process chemistry involved in the plating of high aspect ratio through-holes in the traditional prosess. The different process steps are discussed in this section.

2.1.1.1 Via holes

The main limitation to increased density of conventional circuit boards is area needed for via generation. In the SBU techniques, both the hole diameter as well as the annular ring diameter may be significantly smaller. The reduction in hole diameter is partly because of the thin dielectric layer and the hole forming techniques. The latter because there will be no miss-registration as it is with the conventional stacking of prepregs. A 250 µm drilled hole in a multilayer board will typically require a 625 µm via pad with a minimum hole to hole pitch of 750 µm. For SBU technology an inner layer hole diameter of less than 50 µm is currently in production.

Three different techniques are used for creating the via-holes. These are photo-defined vias, laser-drilled vias and plasma-etch vias, each described underneath.

2.1.1.1.1 Photo defined via

- Mass formation technique
- Established equipment
- Few process steps
- Compatible with all circutization techniques
- High productivity
- 25 μm via capability
- Limited range of approved materials
- Clean-room handling

2.1.1.1.2 Laser drilling

- Can be used on:
- Non filled resins
- Coated foils
- Glass laminates (Nd-YAG laser only)
- Faster, cheaper and smaller then conventional drilling
- Compatible with many resin systems
- Good alternative for few vias / small substrates
- < 25 μm via capability
- High capital investment
- Low productivity for large area or high via density
- Limited choice of dielectrics (mostly non filled)
- Requires photo-process an etching on copper coated dielectrics

Table 2: Laser parameters

Laser type		**CO_2**	**UV-YAG**	**Excimer**
Wave length		9 μm	0,25 / 0,35 μm	0,15 – 0,25 μm
Processibility	Resin	Good	Good	Good
	Glass	Fair	OK	No
	Copper	No	Good	No
Masking		Copper	Copper / none	Copper / photomask
Productivity (holes per minute)		9000 – 18000	1800 - 7200	

Figure 2. A laser drilled via in polyimide dielectric

2.1.1.1.3 Plasma etch

- Mass-via forming
- Use conventional lamination process
- Compatible with most resin systems

- Needs special coated foils
- Non-value added steps
  - Photo-process to open Cu windows
  - Etch back of overhangs
- Via size limited to 75 μm

Table 3: Properties for different via-hole techniques

Items	Photo via	Laser drill (bare resin)	Laser drill (Cladded lam.)	Laser drill (coated foil)	Plasma etch
Productivity (panels / hour)	High 60 – 120	Medium 10 – 20	Low - medium 2 – 10	Low – medium 2 – 20	Low – medium 6 - 12
Initial investment	Medium Coater (liquid) Printer Developer	Low – medium Coater (liquid) Laser system	Medium Laser system	Medium Laser system	Medium Plasma unit
Material used	Liquid photoresist / Dry film	Liquid photoresist / Dry film	Single cladded laminates	Coated foil	Coated foil
Dielectric cost	High	Low - medium	Medium	High	High
Consumables	Photo resist Developer	Photo-tool Photo resist	Photo-tool Photo resist	Photo-tool Photo resist	Photo-tool Photo resist Gases
Technical challenge	Cleanliness Material dev.	Productivity Process dev. Cost	Cost Productivity	Cost Productivity	Cost Productivity
Via size capability	25 – 50 μm	25 – 50 μm	50 – 80 μm	50 – 80 μm	75 – 100 μm
Total cost	Very low	Low	Medium	High	Medium - high

2.1.1.2 Flexible base materials

Conventional flexible base materials are made by bonding the copper layer to the polyimide dielectrics with an adhesive. However, the use of an adhesive layer increases the z-axis thermal expansion of the laminate which can cause cracking of the through hole metallisation during thermal cycling. Eliminating the adhesive using adhesive-less flexible base material is the best way to minimise the cracking tendency. This can be obtained in three ways:

2.1.1.2.1 Chemical deposition

The surface of the polyimide is prepared before a Ni and Cr is electroless deposited. Copper is then electrolytically plated up to the desired thickness. The nickel, which is used as an adhesive promoter, has to be removed in a second etching process after the copper when patterning. In addition, the nickel is quite brittle.

2.1.1.2.2 Vacuum deposition

In vacuum deposition (evaporation or sputtering) a thin seed layer (adhesion promoter) of chromium is deposited on the foil, followed by copper. To obtain the wanted copper thickness, the additional copper is plated electrolytically. A typical problem with this technique is a drop in copper adhesion after thermal and pressure treatment.

2.1.1.2.3 Casting

A not yet polymerised polyimide (in liquid form) is poured onto the copper foil, which is joined with the polyimide film. After polymerisation a single-sided flexible base material is formed. More layers are obtained by sintering together single sided sheets. There is no metallic adhesion promoters used in this process. Physical parameters like peel-strength, dimensional stability and dielectric constant are equal or better than for conventional flexible laminates. The homogenous dielectric material is well fitted for both plasma and laser drilling.

Typical properties of adhesive flexible base material are shown in the table below.

Table 4: Typical properties of adhesive flexible base material

Adhesion	> 1,4 N/mm
Dielectric constant	3,2 (1 MHz)
Loss factor (tan δ)	0,002 (1 MHz)
CTE (z-axis)	Approx. 150 ppm/K
Dimensional stability	0,05 %
Moisture absorption	0,8 %

2.1.1.3 Resin filled Aramid-Paper base material (Thermount, Du Pont)

Aramid is an organic compound, which can be produced in form of long filaments. In the woven form it is known as Kevlar. Filled with various resins like epoxy or polyimide it can be used as base material for PCB's. The main properties is the negative expansion coefficient of aramid, which together with the resin gives a base material with a CTE which can be tailored to 4 – 8 ppm/K. This makes it a very good match to silicon. When the aramid is in the form of long fibres, it is very difficult to drill du to the strong fibres. This type of material has therefore disappeared from the market. However, in the non-woven form the material is very promising. As the material is pure organic, processing methods like laser and plasma can be used.

Table 5: Comparison of different substrate materials for MCM-L

Reinforcement/ Resin	Tg [^{0}C]	X–Y CTE [ppm/K]	Z CTE [ppm/K]	ε_r MHz	Loss Factor	Dimensional stability [%]	Water absorption [%]	Cost Vs. FR4
E-glass/epoxy	125	14 – 18	80	4,,7	0,02	0,04	0,15	1x
E-glass/polyimide	250	12 – 16	60	4,5	0,009	0,05	0,35	2x
Woven kevlar/epoxy	125	6 – 8	105	3,9		0,06	0,85	6x
S-glass/cyanate ester	230	8 – 10	40	3,6	0,004	0,03	0,08	6x
Quarts/polyimide	250	6 – 8	34	4,0		0,04	0,35	9x
Thermount/HiT$_g$ epoxy	180	7 – 9	110	3,9	0,015	0,03	0,44	1,5x
Thermount/polyimide	230	7 – 9	80	3,6		0,03	0,81	2,2x
Thermount/cyanate ester	220	8 – 10	75	3,1		NA	NA	8x
PTFE (RT-Duroid 5880)	NA	30 - 50	240	2,2	0,001	NA	0,015	> 10x

2.1.2 Wire bonding on SBU

The MCM-L and MCM-Flex have significantly softer dielectrics than most other MCM technologies. This means that a careful design of the bond pad and careful specification of the metallisation system. Also the bonding process is important.

- Gold thickness on the substrate is defined by the type of bond process used and the bond strength.
- Secondary metal finishes may be required to provide a rigid bonding surface at high temperature
- The substrate T_g is critical in determining the bond strength and reliability. If the wire bonding process takes the board above the T_g, then localised deformation and sinking of the bond pad area will occur.

Wire bonding typically requires between 100 and 1250 nm of soft gold on the bond pad. For thin layers (100 – 200 nm) immersion gold can be used. This process is self-limiting, and gold is plated on all exposed surfaces, after the solder mask has been applied. Once a complete gold coverage of the surface is achieved, the plating process stops. Immersion gold is the least expensive gold finish available. This coating is commonly used for ordinary surface mount assembly, and provides excellent solderability and coplanarity without a significant cost increase compared to other finishes. This means that the same finish can be used for both wirebonding and soldering.

If higher gold thickness is needed (500 – 1000 nm) for gold wire bonding, electroless gold can be used. The electroless process means that all exposed metal surfaces will be plated. The process will continue as long as it immersed into the plating bath. However, this amount of gold will have a negative effect on the solder, causing a brittle joint.

If thicker gold is needed, electroplating has to be used. Electroplated gold is selectively added onto the metal surfaces that are included in the external electrical circuit. This means that all wire bonding pads must be connected together in a bus. The electroplating is a more costly process, and the required bussing can cause some design (layout) problems

The gold thickness influences on the wire bond pull strength. A study by McDermott[1] is shown in the table below. In this study a 25 μm gold wire has been bonded onto different gold surfaces. In all cases a 5 μm nickel layer underneath the gold.

Table 6: Typical wire bond strengths for different metallisation systems

Gold Finish	Thickness [nm]	Average bond strength [g]	Standard deviation [g]
Immersion gold	110	8,01	1,31
Immersion gold	125	9,60	1.30
Electroless gold	530	9,77	1,66
Electroless gold	900	9,93	1,24

During the bonding process, under pressure and high temperature above the glass transition temperature the PCB will deform under the bond area often called cupping. This cupping effect will dissipate the ultrasonic energy, reducing the bond yield. However below Tg, the PCB is hard and rigid and gives few problems in the wire bonding process.

The use of nickel under the gold finish increases the stiffness of the pad. In addition, the nickel acts as a diffusion barrier between the copper and gold. If the gold thickness is more than 1,25 μm, there is no need for the diffusion barrier. Other options to increase the stiffness and hardness is to use thin coatings of tungsten or titanium (30-50 nm).

Higher T_g materials allows increased bond temperature (increased ultrasonic energy) without exceeding the glass transition temperature. Also a larger bonding pad will help dissipate the heat from the bond area and therefore reduce the localised temperature of the substrate under the bonding pad. The use of thinner wires will allow bonding with lower pressure and reduced cupping effect.

[1] B. McDermott, “Shifting the Paradigm”, Circuitree, March 1996

2.1.3 Dielectrics for SBU

The dielectric material used in sequential build up technology has to fulfil several requirements. These are

- Provide a suitable surface for metal plating, with good adhesion and stress compliance
- Good adherence to different substrate materials
- Simple processing
- Good dielectric properties (low dielectric constant and low dielectric loss)
- Low moisture absorption
- Allow deposition with a well controlled thickness onto the substrate
- Glass transition temperature above 150 ^{o}C
- Low thermal expansion coefficient

Table 7: Comparison of dielectrics used for SBU technology

Factors	Epoxy	Acrylate	Polyimide
Cost	Excellent	Excellent	Poor
Processibility	Excellent	Excellent	Poor
Dielectric constant	Fair	Fair	Good
Glass transition temperature	Fair - good	Poor	Excellent
Thermal expansion	Good	Poor	Excellent
Moisture absorption	Good	Good	Poor
Adhesion to copper laminate	Excellent	Good	Poor
Adhesion to deposited copper	Good	Good	Poor
Overall rating	**Very good**	**Good**	**Fair**

2.1.3.1 Deposition of dielectrics

The dielectric can be applied to the substrate in different ways[2]. One is to move the substrate on a conveyor through a sprayed “curtain” of the dielectric. This method gives high transfer efficiency, however the thin layer of dielectric falling through the air gives a significant loss of solvent. Typically, thickness in the 25 to 60 μm can be obtained in this way.

Spin coating is another option for deposition of dielectrics. This gives thinner layers, less than 20 μm. The transfer efficiency is however low. Nevertheless, this is the method of choice for high cost polyimide solutions, since the equipment is well characterised from the semiconductor industry.

Spray coating has a potential efficiency in between curtain and spin coating. With a proper design of the equipment and the use of low pressure high volume spray, good coatings can be obtained. There is neither a need for high solvent dilution.

Roller coating is an interesting approach, where both sides of the substrate can be coated in the same process.

The application of the dielectric in the form of dry films has significant drawbacks as poor conformity to varied surface topography, loss of possibility of customised thickness and high cost.

The use of photoimageable dielectrics causes a significant reduction in the number of process steps. The result is also less waste and increased throughput.

[2] P. D. Knudsen, R. L. Brainard and K. T. Schell, “A Photoimageable Dielectric for Sequential PWB Fabrication”, Circuit World, Vol. 21, No. 3, 1995

2.1.3.2 Metallisation

The conventional metallisation process is based on electroless copper plating. A temporary plating resist is used to define the conductor tracks. Often a “swell and etch” adhesion promotion system is used to increase the adhesion between metal and polymer as well as increase the ability to comply with mechanical stress. A palladium/tin colloidal is typically used as a catalyst for the deposition of copper. With electroless process, the plating can be done on many panels in a batch process. The plating is uniform, and it will conform to the substrate and provide a coplanar surface regardless of the topography or features.

Adhesion to the substrate is often measured by a peel testing, where the metal is peeled normal to the substrate

Figure 3: Cross-section of metalised laser-drilled via

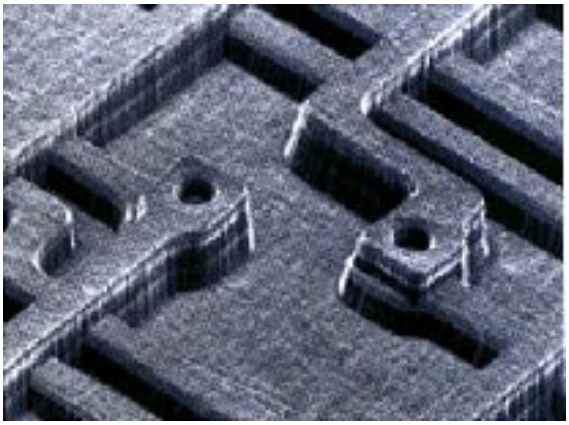

Figure 4: “Cutaway” of two-layer metallisation

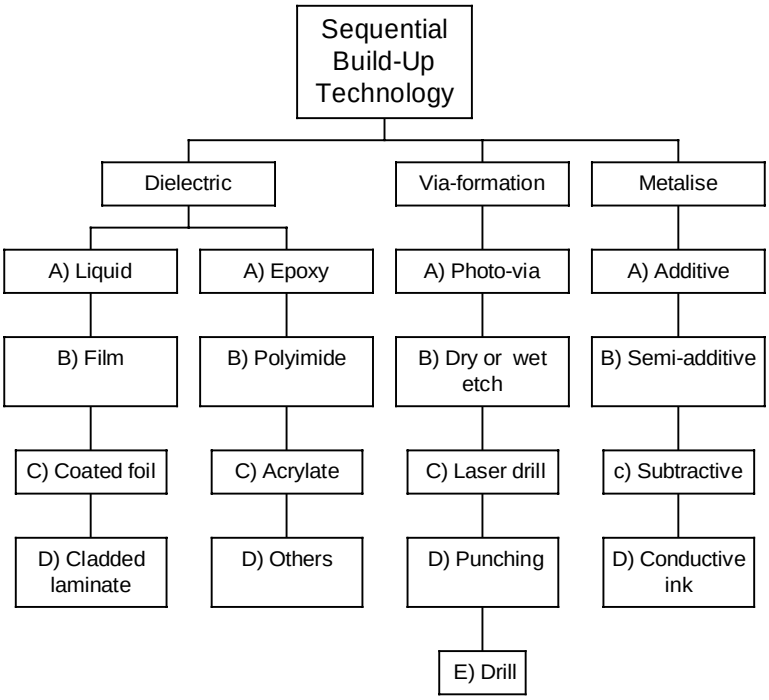

Figure 5: Different technology choices available for SBU

Table 8: Overview of different Build Up technologies, with type of dielectrics and minimum feature sizes.

Technology	Dielectric	Line / Space (µm)	Via / Land dia. (µm)
Microfilled Vias (MfVia)	Epoxy, Polyimide	75 / 75	125 / 250
Photo-via Redistribution Layer	Epoxy, Polyimide	100 / 100	125 / 380
Conductive Adhesive Bonded Flex	Epoxy, Polyimide	100 / 100	125 / 380
Plasma Etched Redistribution Layer	Epoxy	75 / 75	100 / 300
Sequential Bonded Film (Dycostrate)	Polyimide film	75 / 75	100 / 300
Surface Laminar Circuits (SCL)	Epoxy, Polyimide	75 / 75	125 / 250
Build-Up Structure System (IBSS)	Epoxy, PES	75 / 75	125 / 250
Carrier Formed Circuits	Epoxy acrylate	100 / 100	150 / 400
Roll Sheet Build-Up	Epoxy	100 / 100	150 / 450
Sheet Build-Up	Epoxy	75 / 75	100 / 450
Sequential Bonded Solid Vias (ALIVH)	Epoxy aramid	100 / 100	100 / 400
High Density Interconnect (HDI)	Polyimide film	25 / 50	25 / 200
Buried Bump Interconnect (B_2IT)		100 / 100	125 / 250
Microwiring	Polyimide film	100 / 100	125 / 250
Co-Lamintaion Adhesive Build-Up	Polyimide film	75 / 75	125 / 125

2.1.4 Examples

In the example below, IBM designed[3] a MCM-L to improve the performance of two four-port SRAMs by reducing the interconnection length. The result was a 25 % performance increase by reducing the processing time from 20 to 15 ns.

Figure 6. IBMs MCM-L SRAM

This MCM-L incorporates a wire bond die and surface mount capacitors and resistors onto a 27 mm, six-layer laminate substrate. The 262 I/O at the first-level interconnect are reduced to 169 I/O for interface to the system level board, resulting in real estate as well as I/O reductions. The final package required over-moulding for protection of the fragile wires connecting the dies. To include the surface mount devices to be in the over-mould as well, an innovative solution was proposed whereby the pad surface finish was converted to silver palladium and a conductive epoxy was used to attach the discrete components.

The design shown in this figure is an example of the potential for significant space saving by sweeping several ASICs into one package. The original system board design required an area of 125 mm x 125 mm to contain five banks of four ASICs each. Rather than growing the system, board size to accommodate more devices currently packaged in 160 I/O plastic quad flat packs, the solution of sweeping four bare die ASICs onto a laminate carrier was used. The 37,5 mm, eight- layer package represents a 10x savings in total system board real estate required, thus allowing up to a 4-to-1 density improvement for the increased ASIC count.

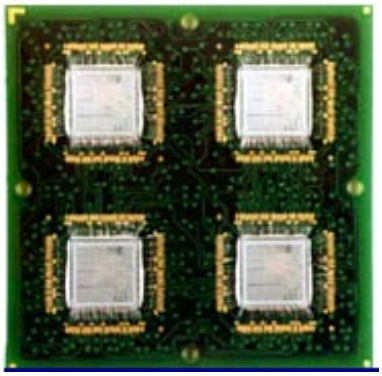

Figure 7. Packaging multiple ASICs in bare die format results in significant real estate savings.

[3] Giuseppe Vendramin and Mike Weller, “MCM-L Rethinking Electronic Packaging”, IBM Corporation

The module shown in Figure 4 is a sweep of four 1Mb x 72 SRAM die. The package features lowtemperature flip-chip processing onto Microvia laminate. Die pitch is 225 µm, and the interface to the system board is a full array of 474 I/O eutectic balls on 1,27 mm pitch. The full array allows each die to be tested individually if desired. Advantages of flip-chip are shown here by allowing die to be placed in close proximity to each other. The backside of the silicon is available for heat spreaders if desired.

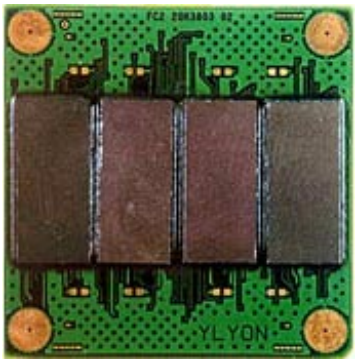

Figure 8. MCM-L combining flip-chip technology on Microvia substrate.

2.1.4.1 Matsushita "ALIVH" technology

Matsushita has developed an alternative to "conventional" SBU technology called ALIVH (Any Layer Inner Via Hole). The board is based on Aramid (non-woven) epoxy prepregs, forming the dielectric layers. A laser is used to drill the via-holes, which are then filled with conductive paste. A copper foil is laminated, and patterned by etching. The different layers are than stacked on top of each other and laminated together, and the pattern on the outer layers is formed.

The ALIVH board allows for via holes from 50 to 200 µm in diameter to be fabricated between any layers. Most importantly, parts can be mounted over the via-holes, since they are filled with electrically conductive paste. This new technology therefore allows increased area for mounting parts and more freedom in the circuit design. The new ALIVH board reduces weighs by a factor of three compared to boards in the older design. In addition, it actually costs ten percent less.

This technology is currently in use for mobile phones. The technology allows more than 80 contact pads per cm^2.

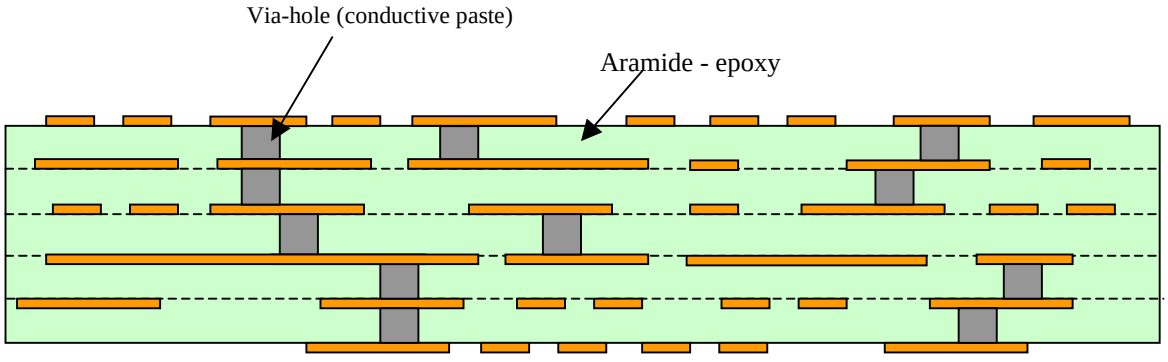

Figure 9: A schematic drawing of the ALIVH technology from Matsushita.

Table 9: The design rules for Matsushita ALIVH technology

Line width	90 µm
Line spacing	60 µm

Via hole diameter	50 - 200 μm
Land diameter	400 μm
Copper thickness (inner layer)	18 μm
Copper thickness (outer layer)	18 or 35 μm

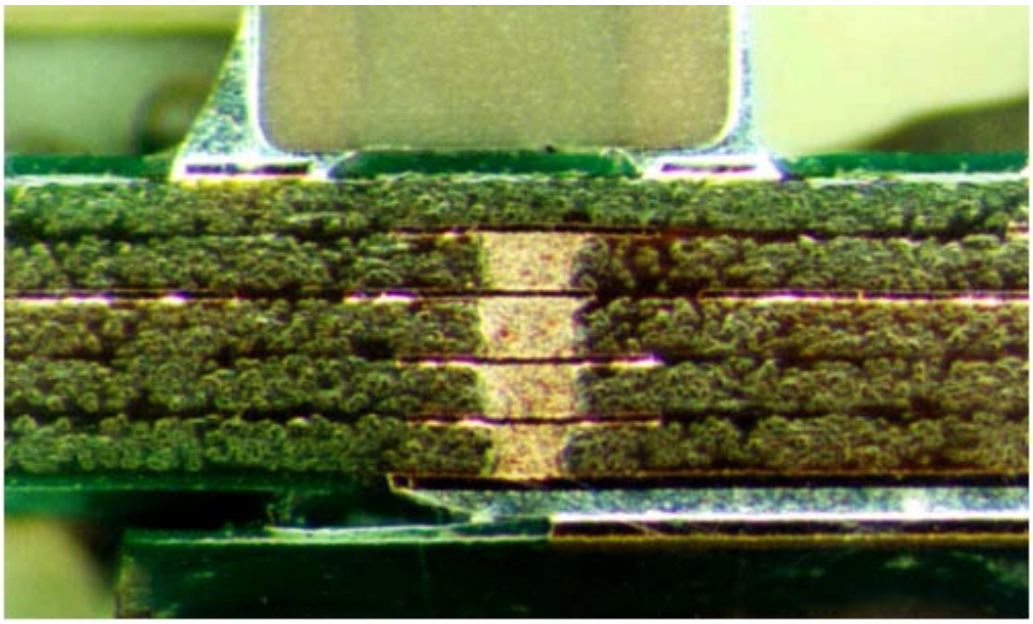

Figure 10 Cross section of an ALIVE circuit board used in the NTT P201 Hyper Digital Phone.

2.1.4.2 Casio MR-80 radio

The Casio radio contains three printed circuit boards. Of primary interest is the flip chip board or multichip module, a photo-via built-up multilayer board with five flip chip die as well as numerous packaged components. The flip chip die include extensive test patterns for a built-in self test (BIST) at wafer level, and the die pads are electroplated with gold.

An anisotropic conductive adhesive film is placed onto the substrate. Casio temporarily mounts the die and performs a functional test based on a test pattern stored in ROM. If the test is negative, the faulty die and the conductive adhesive film are peeled off and replaced. Only once the test is positive is the anisotropic conductive adhesive film cured through pressure and heat.

Anisotropic conductive adhesive film has long been used for chip-on-glass in LCD driver applications. A bare driver IC is mounted onto the LCD glass panel as a flip chip, whereby a conductive adhesive film (or paste) provides the connection between the die's gold bumps and the ITO traces on the LCD glass. This application requires an adhesive-based connection, because the temperature sensitivity of the LCD makes soldering impossible. Due to the superior planarity of the glass, and the CTE match between the glass and the silicon die, such connections achieve high yields and high reliability. Organic substrates, on the other hand, are neither planar nor do they match the CTE of the silicon.

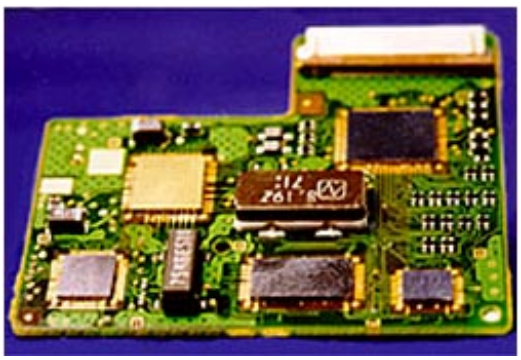

Figure 11 The SBU board used in the Casio MR-80 radio

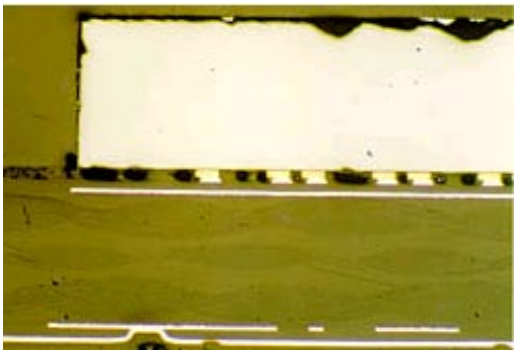

Figure 12 A cross-section of the SBU board and the flip chip die attach used by Casio.

2.1.4.3 Sony DCR-PC7 Camcorder

Inside SONYs Camcorder there is one special CSP-package. This near wall-to-wall CSP package is assembled to both sides of the main board. The technology pushes the board interconnection density to new heights. The board is an eight-layer surface laminar circuit (SLC) supplied by IBM Yasu. Two built-up layers are required on each side of the four-layer core, which contains power, ground and two etched signal layers. Line widths and vias are nominally 75 and 125 microns, respectively. This board supports an attachment pad density of 95 pads per square centimeter. This is astonishingly high and is what can be expected with future near wall-to-wall silicon packaging. This is four times as high as most of today's leading edge boards of conventional manufacture.

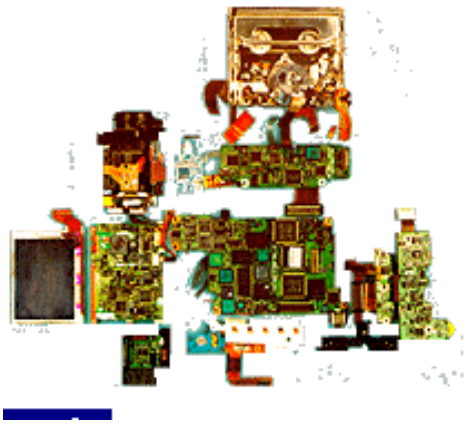

Figure 13 The SBU boards used in the Sony DCR-PC7 Camcorder folded out.

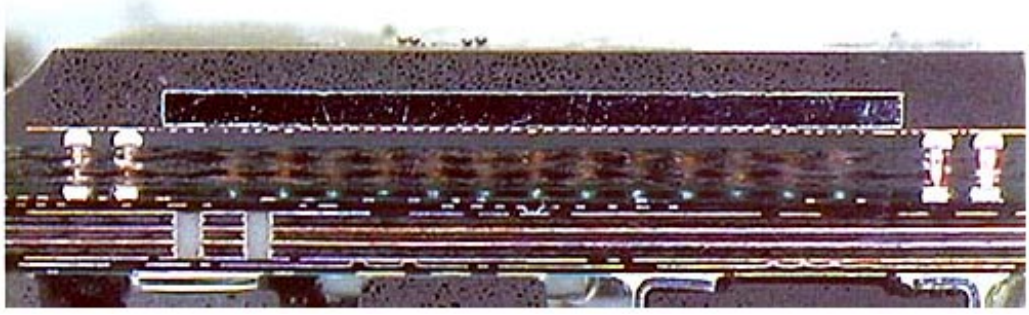

Figure 14 A cross section of the SBU board and a BGA component.

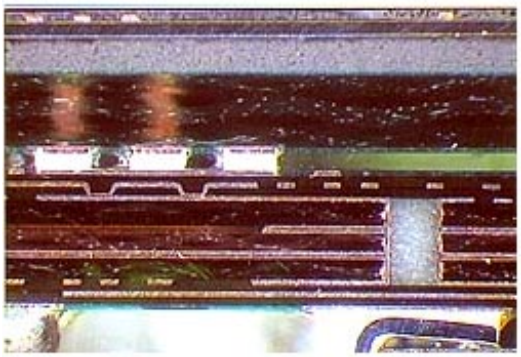

Figure 15 A close up of the cross section of the SBU board. The board has four core layers, and two build up dielectric layers at each side.

2.1.4.4 Processor module from Kongsberg Ericsson Communication

The Norwegian company Kongsberg Ericsson Communicatoin ANS has together with Amitech AS developed a processor module using sequential build-up technology. The module, shown in figure 16, integrates 12 bare dies on a 6-layer MCM-L substrate. Dimensions are 42.5 x 42.5 mm, and the module is terminated with a 314 pin BGA-package with plastic encapsulation. Design rules for the SBU-board are 100 µm conductors, 200 µm pitch, 250 µm pad diameter and 80 µm via. The viaholes are laserdrilled. A schematic drawing of the SBU-board is shown in figure 17. This module combines several technologies to achieve high-density packaging and a cost-effective solution. A modular design of the total system gives the opportunity to flexible solutions using new technology.

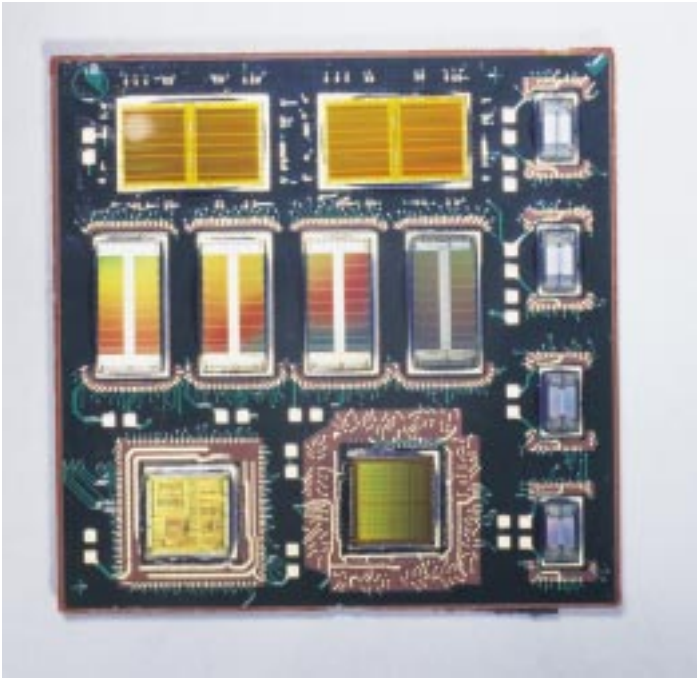

Figure 16 MCM-L module from Kongsberg Ericsson Communication.

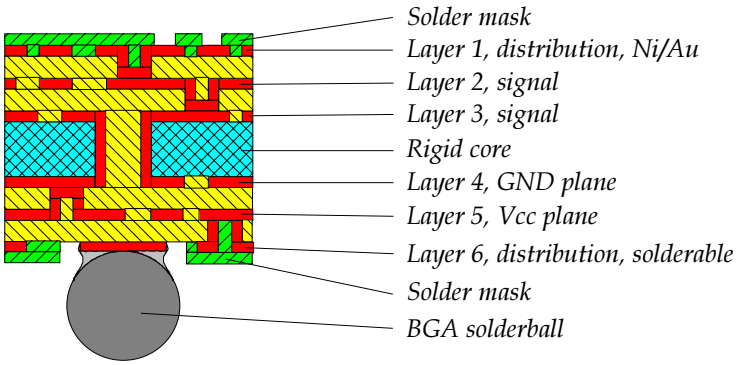

Figure 17 Schematic drawing of the SBU-board with BGA-termination in the Kongsberg Ericsson module.

2.1.5 Future Directions of MCM-L

MCM-Ls benefit from single-chip module (SCM) advancements such as ultra fine pitch wire bonding on BT resin substrates as well as evolving low-cost, low-melt flip-chip processes. As BGA pitch shrinks, the technology is directly extendable to MCM-Ls as well.

Manufacturing of MCM-Ls has begun to proliferate from module shops into card assembly shops. Vertically integrated companies that provide silicon, silicon packaging, and board-level assembly have found the elements required to process MCM-Ls are already available. Clearly, card assemblers have an in-depth knowledge of processing laminate assemblies. And for some, these processes have stretched to encompass chip-scale and micro-BGA packages, and the most advanced assemblers have developed processes for flip-chip, albeit for prototype purposes. Surface mount equipment has the proven capability of placing area array bare die, primarily due to their sophisticated vision systems. Design tools used for schematic and layout of cards can be adapted for use in MCM-L designs as well. Those shops having engineers experienced with complex test development will be able to take advantage of built-in selftest (BIST) and boundary scan test techniques to provide a full turn key MCM-L offering.

As the MCM trend continues toward flip-chip integration, the net result will be an increasing number of sources to manufacture these packages, assuring competitive costs. For MCMs, the drive has come from customers, such as telecom, where cell phones must be light and portable and where base stations must fit into closet-size spaces. MCM-L will continue to prevail in new applications, such as automotive, as advancements in materials and processes continue to be realised. As the growing infrastructure drives costs lower, the consumer market will enjoy the benefits of MCM-Ls as well.

2.1.6 MCM Flex

General Electric and Lockheed Martin have together developed a technology based on flex print. Naked chips are glued face down onto the pre-fabricated flex print. Electrical connections to the chip are made by laser, with a following metallization step and patterning. In total, it ends up with flexible film with three conductor layers. By moulding the chips in a polymer material, a conventional MCM can be made. Connections to the PCB can be made either as a Ball Grid Array (BGA) or by adding a lead frame.

2.1.6.1 Production of MCM flex

The first part of the process is actually to make a fine line flex print with two conductor layers. This will often be done by specialised sub-contractors. The polyimide film is typically 25 µm thick and has copper tracks on both sides, with down to 50 µm conductors and 50 µm metallized via holes. The finished flex print is typically

delivered in roles or large format panels. There are several manufacturers hat can deliver these circuits today.

In the next part of the process, the prefabricated polyimide film is cut and mounted onto aluminium frames, with dimensions similarly to silicon wafers. This makes it possible to utilise standard silicon processing equipment. At this stage the flex-print is easily testable. The silicon components are glued onto the film with a thermosetting adhesive, by the use of a standard pick and place machine. Both ordinary passive and packaged components can be mounted in the same way. The adhesive bonding is a critical process, and parameters like displacement of components before curing, out-gassing, thermal stability, humidity absorption, glass transition temperature and curing must be controlled.

After the components are mounted, a laser is used to cut holes in the flex and the adhesive, down to the metallized contact areas of the components. The use of laser means that there is little risk of “under cutting” as the light is reflected once it hits the metallisation. The whole surface, including the edge of the via wholes, is then metallized with a thin barrier layer of titan, with following electroplating of 2 to 6 μm of copper. A photoprocess is done to create the third conductor layer. If needed, more layers can be added.

The component side of the module can now be moulded into plastic, or be left without any moulding, as a thin flexible circuit.

Advantages with the technique are:

- The prefabricated flex film is reasonable cheap
- The supporting substrate can be cheap
- The surface of the prefabricated flex film is level, making further processing simpler
- Standard components from different vendors can be used
- Very good electrical properties, as the connection leads are made very short
- Low dielectric constant, good edge definition and good conduction in the copper means that the technology can be used at least up to 10 GHz
- A change in component layout can be incorporated by a change in the laser cutting software
- The number of connections are reduced by a factor of two, compared to wire bonding
- Cross-talk can be minimised by shielding

Disadvantages are:

- The laser cutting of the via holes are an expensive bottleneck in the production
- Since the technology is new, there is a lack of reliability data. Thermal cycling can cause opens in the via hole metallisation due to a large miss-match in thermal expansion between the metal and the flex-print and the adhesive
- The module can not be tested before the last conduction layer is finished. At this point it is not posibel to repair. Unless Known Good Dies can be used, this is a big disadvantage
- Polyimide is hygroscopic, with water absorption of the order of 2 to 3 % weigh. This can cause both reliability problems as well as changes in high frequency properties

2.2 MCM C

2.2.1 Thick Film Substrates

Important properties of thickfilm substrate materials are:

- Good dimensional stability during high temperature processing
- Good adhesion between substrate and printed materials
- High thermal conductivity
- A thermal coefficient of expansion matching that of other materials in the circuit
- High electrical resistivity that gives isolation between components
- Low dielectric constant

- Low dielectric loss tangent (for microwave circuits)
- Good machinability
- Low price.

However, no single material will satisfy all these requirements. This means that various types of ceramic are used as thick film substrate materials, with 96 % Al_2O_3 (alumina) as the dominant one. Alumina has many good electrical and mechanical properties please refer to Table 10. It has very good dimensional stability.

Table 10 Properties of substrate materials for hybrid technology, and other important properties (In: inorganic, Semi: semiconductor, P: plastic)

Material	Relative permit-ivity ε_r	Dielectric Loss Factor (at 10 GHz, 25°C), tan δ_ε	Specific Thermal Conduct-ivity K_{th} [W/cm °K]	Linear Thermal Expansion Coefficient (at 25°C) $\Delta l/l/\Delta T$ [10^{-6}/°K]	Temper-ature Coefficient of ε_ρ $\Delta\varepsilon/\varepsilon\Delta T$ [10^{-6}/°K]	Type	Remarks
Al_2O_3 ceramic (99.5% pure)	9,8	0,0001	0,37	6,3	+136	In	
Al_2O_3 ceramic (96% pure)	9,4	0,001	0,35	6,4		In	
Sapphire	9,4; 1,6	0,0001	0,42	6	+110 - +140	In	Aniso-tropic
Quartz glass	3,78	0,0001	0,017	0,55	+13	In	
Corning glass	5,75	0,0036	0,012	4,6		In	
Beryllium oxide Ceramic (BeO) (98%)	6,3	0,006	2,1	6,1	+107	In	Dust is poison-ous
Semi-Insulating GaAs	12,9	0,002	0,46	5,7		Semi	
(High-resistive) Silicon (ρ=10^3 ohm cm)	11,9	0,015	1,45	4,2		Semi	
PTFE	2,1	0,0003	0,002	106	+350	P	
Polyolefin (Glass reinforced)	2,32	0,0007	0,005	108	+480	P	
PTFE	2,55	0,001	0,003	16-100		P	
Aluminium			2,2	23,8			For
Copper			3,93	17			comp-
Invar				1,5			arison

It is brittle, and this limits the maximum size to 10 - 15 cm. After the material has been sintered, it is not easy to shape it. However, it can easily be cut by breaking after a partial cut is made by a high power laser, or after tracing with a diamond. For small circuits, it is common to print and mount components on many substrates that are produced together and then broken apart in the end, to make a rational production process. Holes through the substrate may also be made by laser, but it is simpler to form the substrate contour and punch holes while the ceramic is pliable, before the sintering.

The thermal conductivity of 20 - 30 W/ ^oC is approximately 100 times better than for organic materials, and the low thermal coefficient of expansion, 6 ppm/^oC, is advantageous for the mounting of ceramic components and semiconductor chips.

For circuits with very high power dissipation AlN substrates are used today, with 5 times or higher thermal conductivity than Al_2O_3. Many properties are similar to those of Al_2O_3. The thermal coefficient of expansion is somewhat lower, 4.5 ppm/°C. This, and different surface properties, give a need for special printing pastes

on AlN, to avoid flaking off during the high temperature processing. BeO has even higher thermal conductivity than AlN. However, its use is limited by the fact that dust and vapour from BeO are very poisonous. High price is also connected to this fact.

For high volume products with lower electrical demands, enamel coated metal is used as substrate, to some extent. Big circuits can be made, and we achieve electrical grounding in the substrate.

2.2.1.1 Materials for conductors, resistors, dielectrics

Conductors, resistors and dielectric materials are applied in paste form by screen printing and they are transformed/sintered by heating to high temperature, "firing". The pastes have three main ingredients:

- Functional element (metal-, alloy- or oxide particles)
- Matrix or "binder" (glass particles)
- Organic solvents and "temporary binder".

The organic, temporary binders are polymers that give control over the printing properties. They decompose and evaporate early in the firing process, together with the solvents. The glass particles melt in the firing process, adhere to the substrate, bind the active particles together and give stability for the circuit. The high firing temperature, typically 800 - 900 °C, see Figure 16, implies very good long term stability and reliability.

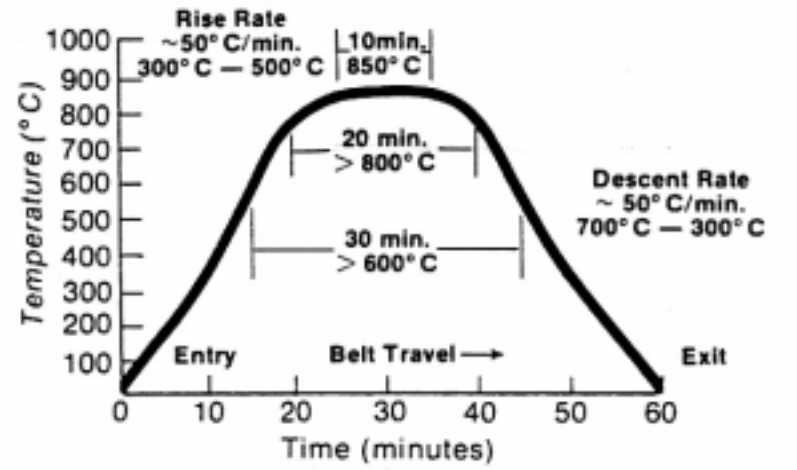

Figure 16 Typical temperature profile for thick film firing

2.2.1.1.1 Conductors

The conducting pastes should give:

- High electrical conductivity
- Strong adhesion to the substrate
- Excellent solderability for soldering of packaged components
- Reliable bondability for wire bonding of naked IC chips.
- Price is also an important parameter.

Normally one conductor paste can not satisfy all these criteria, and it is necessary to make several conductor prints.

The most used conductor systems are gold, copper, alloys of palladium/silver, palladium/gold and platinum/gold, with properties shown in Table 10. Noble metal systems are used because the heat treatment takes place at above 800 °C, where other metals are ruined by oxidation. However, gold and platinum are expensive materials, so the material cost is an important factor in the final price of the circuit. Gold is very well suited as basis for bonding, but it is not suitable for soldering. This is because gold is very quickly

dissolved in solder metal during the soldering process, and it gives a brittle intermetallic composition with poor reliability properties. Pure silver has a strong tendency for migration, which may cause reliability problems after some time. However, silver/palladium gives little migration, it is excellent for soldering, and is well suited for making contact areas for printed thick film resistors. Therefore, this alloy is the most used as conductor material, although it has lower conductivity than the pure elemental conductors. Silver is also used in alloys with platinum.

Copper has high conductivity and low price. However, strong oxidation in air at high temperature makes it necessary that copper must be fired in a neutral nitrogen atmosphere. This process is more complicated and costly and has impeded the use of copper conductors.

Nickel is also used to some extent, but it has lower electrical conductivity than the other materials.

Typical thickness for the conductors is 5 -10 µm after firing. The sheet resistivity is typically between 2 and 25 mohm/sq, please refer to Table 11.

Table 11 Properties of thickfilm conductor systems

Comparison of Parameters for Thick-film Conductors			
	AgPd (>13% Pd)	*Cu*	*Au*
Sheet Resistivity (mohm/❒)	25	1,8	2,5 - 3
Breakdown Current (mA/mm width)	3000	10000	10000
Thickness	10-20	15-30	5-15
Minimum With (µm)	150	150	50
Through-hole Diameter	0,4-1,5	0,4-1,5	-
Number of conductor layers	1-3	1-5	1-5
Substrate Area (cm^2)	0,2-100	0,2-200	0,2-50
Substrate Thickness (mm)	0,6-1	0,6-1	0,25-1
Tin-Lead Soldering Properties on Thick Film Conductors			
Parameter	*AgPd*	*Cu*	*Au*
Solderability	Good	Good	Unsolderable
Wetting	Good	Good-excellent	-
Leach Resistance	Fair-good	Excellent	-
Adhesion	Excellent	Excellent	-
Visual Quality	Good	Excellent	-

Silver with 1 % platinum (AgPt) has similar leach resistance and migration properties as AgPd, but the electrical conductivity is much higher. Gold – platinum is sometimes used, since has excellent soldering properties.

2.2.1.1.2 Resistors

Important properties of thick film resistors are:

- Large range of available resistor values
- High stability
- Low thermal coefficient of resistivity, with little spread over the substrate
- Low voltage dependence of the resistance
- Good noise properties.

The resistor pastes consist of the same three main ingredients as the conductor pastes, but the active elements have lower electrical conductivity. They are most often based on various types of oxides of ruthenium: RuO_2, $BaRuO_3$, $Bi_2Ru_2O_7$. In addition, oxides of iridium, rhodium and osmium are used. They may be produced with sheet resistance down to approximately 1 ohm/sq, and up to 10^9 ohm/sq, for a 25 µm thick print. The sheet resistivity is determined by the active material in the paste, the amount of glass matrix mixed in, and the details in the processing. The tolerance in achieved resistance is lowest for the intermediate values of sheet resistivity.

We obtain termination of the resistors by printing a conductor underneath or on top of the ends of the resistor, see Figure 17.

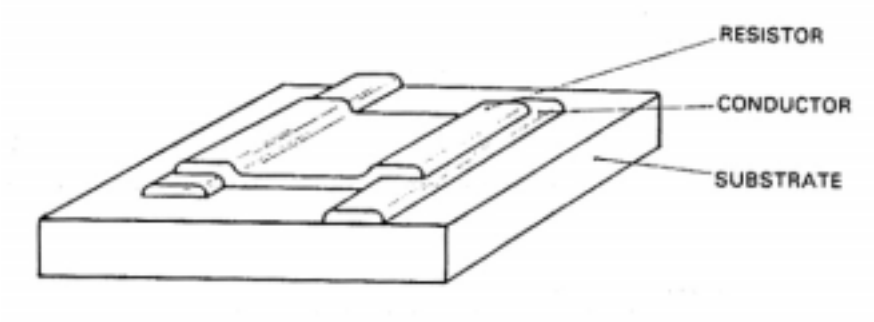

Figure 17 Thick film resistor with termination

Some typical resistor properties are shown in table 12. Resistance drift lower than 0.5 % under harsh climatic conditions over long periods of time makes thick film hybrid technology attractive for demanding applications. The difference in drift between several resistors on the same substrate is typically 0.1 %. The temperature coefficient of resistance depends on the material, and it is typically in the range +/- 100 - 700 ppm/°C, with variation over a circuit, for resistors printed with the same paste, below +/- 15 ppm/°C.

The tolerance in absolute resistance after printing and firing is typically +/- 10 - 20 %, and the relative tolerance between resistors on the same substrate one order of magnitude lower. However, by laser trimming one can achieve tolerances down to approximately 0.5 % absolute, and 0.1 % relative value.

Table 12 Typical properties of thick film resistors

Tolerances as fired	± 10 – 20 %
Tolerances, laser trimmed	± 0.5 - 1%
TCRs: 5 to 100K ohm/sq (-55° to 125°C)	± 100 - 150 ppm/°C
TCRs: 100K to 10M ohm/sq (-55° to 125°C)	± 150 - 750 ppm/°C
Resistance drift after 1,000 hr at 150°C no load	+0.3 to -0.3%
Resistance drift after 1,000 hr at 85°C with 25 watts/in2	0.25 to 0.3%
Resistance drift, short term overload (2.5 times rated voltage)	< 0.5%
Voltage coefficient	20 ppm/(V) (in)
At 100 ohm/sq	-30 to -20 dB
At 100 Kohm/sq	0 to +20
Power ratings	40-50 watts/in2

2.2.1.1.3 Dielectrics

Dielectric materials are printed to obtain insulation between various layers of conductors, to produce capacitors, and as passivating cover on top of the whole circuit. For insulation, low capacitance between conductors is desirable and we use materials with low dielectric constant. For capacitors, materials with high dielectric constant are used, to achieve high capacitance with little area consumption.

Important properties of dielectric materials:

- High insulation resistance
- High breakdown field
- Low loss tangent
- Low porosity

For insulators:

- Low dielectric constant

For capacitors:
- Suitable dielectric constant
- Low temperature coefficient
- Low voltage coefficient of dielectric properties

For insulation layers, aluminium oxide is the common functional element, together with glass. The glass melts and crystallises during firing at 850 - 950 °C, but it does not melt if heated again. The relative dielectric constant is typically ε_r = 9-10, and breakdown field strength 20 V/µm.

The dielectrics for high value capacitors consist of ferroelectric materials with ε_r up to above 1000, similarly to ceramic multilayer capacitors, please refer to Chapter 4. However, the properties of these materials change drastically near the Curie temperature. Barium titanate is used, with additives of strontium, calcium, tin or oxides of zirconium to change the Curie temperature and to reduce the temperature coefficient in the temperature range of use. That gives ε_r = 1000 - 3000 and temperature coefficient up to approximately +/- 5000 ppm/°C. For small capacitors the pastes of magnesium titanate, zinc titanate, titanium oxide, and calcium titanate are used, with ε_r = 12 - 160, and temperature coefficient +/- 200 ppm/°C.

Table 13 Typical properties of printed and discrete capacitors

Capacitor	Capacitance Range	Absolute Tolerance [%]	ε	Isolation Resistance [Mohm]	Tan δ [%]	TCC [ppm/°C]	Voltage Range
Thick-film I	2 pF/mm^2	5 - 20	12	>10^6	<0.25	45	50-200
Thick-film II	8 pF/mm^2	10 - 30	50	>10^4	<1.5	500	50-200
Thick-film III	50 pF/mm^2	10 - 30	500	>10^4	<2.0	2000	50-200
Thick-film IV	150 pF/mm^2	10 - 30	2000	>10^3	<4.0	-400	50-200
Ceramic-chip NPO	1 p F - 4 nF	1 - 10	10	>10^5	<0.1	±30	50-200
Ceramic-chip X7R	0.1 - 1.5 nF	3 - 20	1200	>10^5	<2.5	800	50-200
Tantalum-chip	0.1 - 100 µF	5 - 20	25	Maximum leakage current 0.5 - 3 µA	<6.0	500	4 - 50

Capacitors are not suitable for laser trimming. That, in addition to the above mentioned disadvantages, is the reason why printed capacitors are used only in small values and for uncritical purposes (de-coupling capacitors, etc.). Some properties of printed and discrete capacitors are compared in **Table 13**.

Pastes for the protection layer on top of thick film circuits are composed such that they may be fired at lower temperature, approximately 500 °C, and affect the previously printed layers as little as possible.

2.2.1.2 Production process

The layout of the circuit is made by CAD tools, photo plotting or laser plotting, analogous to the ones used for layout of multilayer PCBs. Photographic films are produced for the pattern of each layer. From these films, screens for screen printing are produced, using a photolithographic process.

When a print has been made, the circuit is dried in an in-line furnace at typically 100 - 150 °C. Then the firing is done in a different furnace at 700 - 1000 °C. The process is repeated for each layer, but all resistor layers are fired in the same process step, after the conductor-layers are finished. To achieve good reproducibility for resistors the temperature profile, the top temperature and the time have to be very precisely controlled, maximum deviation in temperature is below 1 °C.

The smallest conductor width that can be achieved with ordinary printing technique is approximately 100 µm. (Using an extra photolithography and etch step this may be reduced to 50 µm.)

It is possible to make conducting contact between the topside and the bottom side of the substrate by printing through holes in the substrate. This is done by sucking the paste through the hole by use of vacuum on the bottom side of the substrate while the printing on the topside is done. To achieve reliable contact the substrate is then turned around and the paste is printed again from the other side in combination with the vacuum. It is common to have all the conductors and discrete, surface mounted components on one side and the resistors on the other for easy laser trimming.

Figure 18 shows the typical process flow for a simple circuit with two conductor layers and one resistor layer. Dielectrics are normally printed twice to avoid pinholes that may cause short circuit faults through the insulating dielectric.

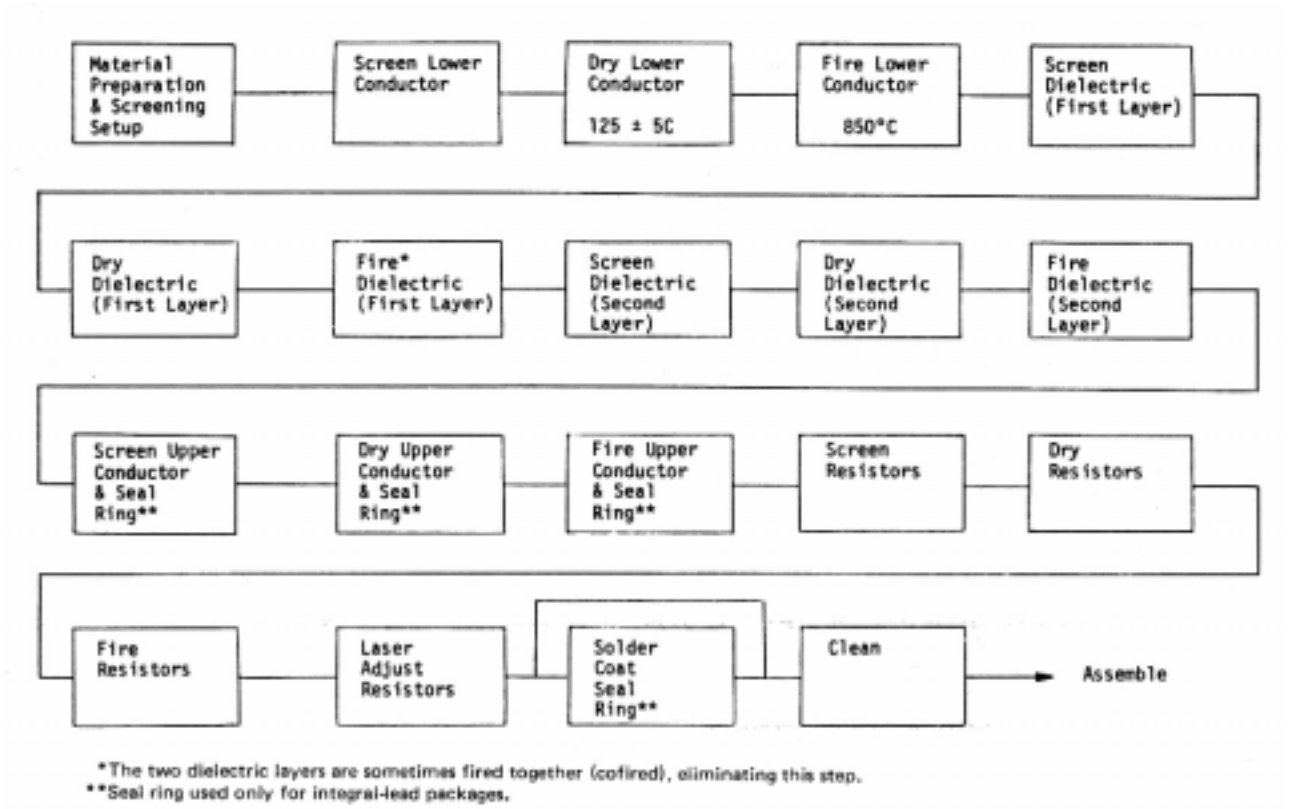

Figure 18 Process flow for production of thick film circuits

Testing is normally done on the substrates before component mounting, as well as on the completed circuits with the components mounted. Test probe-cards, as shown in Figure 19, are used for the contacting. During the testing the resistors are adjusted by laser trimming (previously sandblasting). It is done by a powerful pulsed YAG-laser automatically focused on one spot of the resistor, evaporating the resistor material, while the resistance value is measured. The laser focus is moved and it removes material along a track, until the resistance value is inside the desired tolerance. The resistance will always increase by the trimming; therefore, the resistance after printing is made 20 - 30 % lower than the desired end value. Three normal trim geometries are shown in Figure 20. With an L- cut the coarse trimming is done with a track perpendicular to the resistor length, and the fine trimming to accurate value is done by the track along the direction of the current. Digital trimming gives the best stability and noise properties but occupies more substrate area.

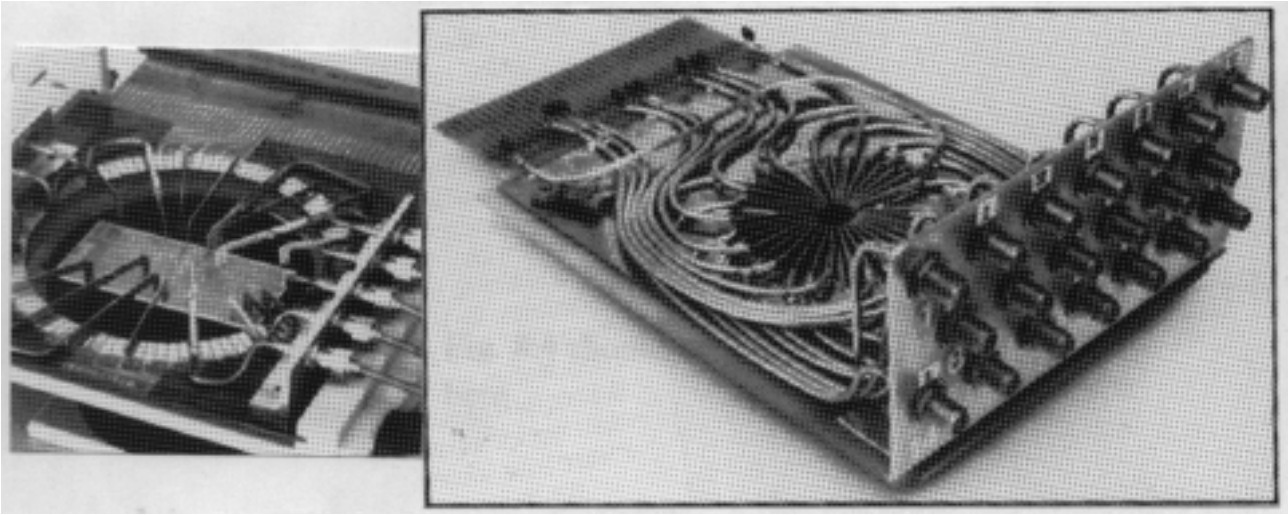

Figure 19 Probe card for testing of thin and thick film MCMs

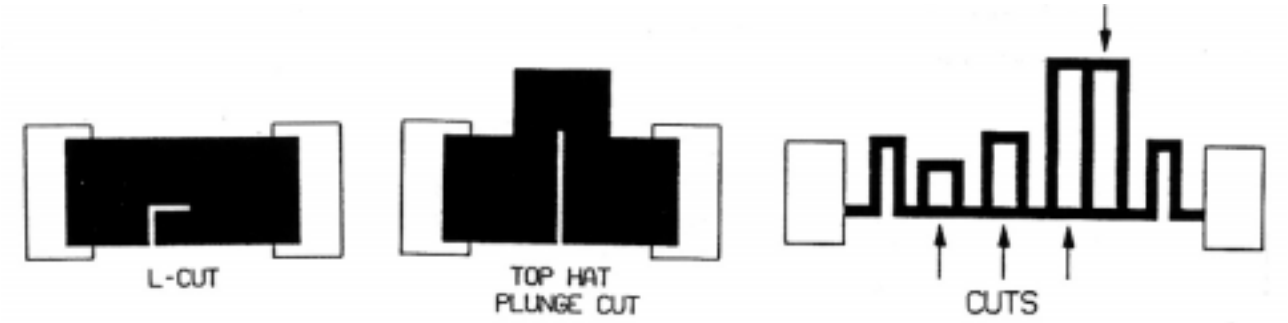

Figure 20 Laser trim cut forms. a): L-cut, the most common, b): Top hat plunge cut, c): Digital trimming, which is most used for high precision resistors.

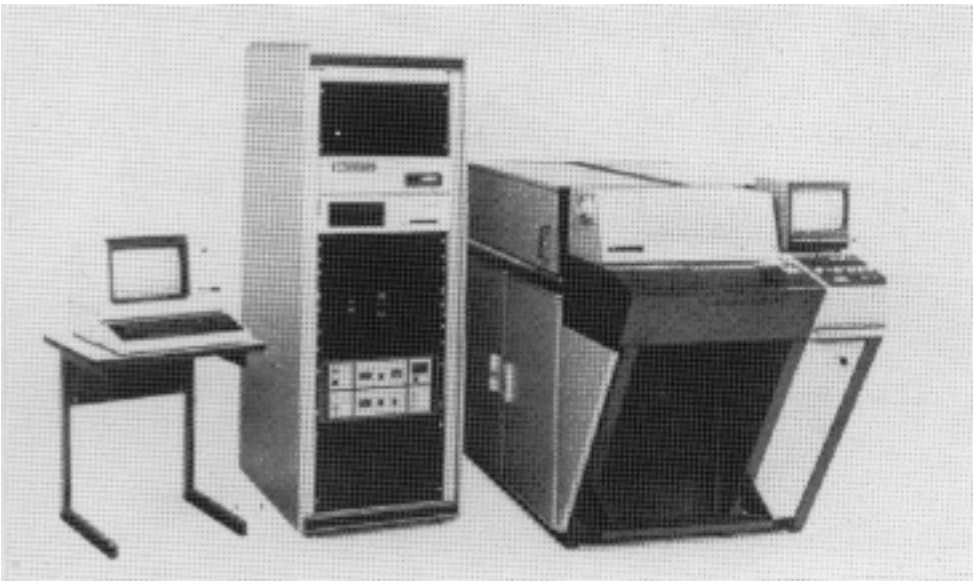

Figure 21 Laser trimmer for thickfilm hybrid circuits, ESI Model 44

Alternatively active functional trimming may be performed. Then one measures a circuit function (the frequency of an oscillator, the amplification of an amplifier, etc.), and the value for the critical resistor is trimmed until the correct value of the measured parameter is achieved.

After completing the trimming of a resistor, the X - Y table on which the circuit is placed is automatically moved and the next resistor is trimmed. A laser trimmer is shown in Figure 21.

2.2.1.3 Component mounting, encapsulation

Soldered, encapsulated ICs, as well as wire bonded naked chips, are used on thick film hybrids. SMD passive components are soldered by using solder paste and reflow soldering, or they are glued with electrically conductive adhesive. Reflow soldering is done either with a hot gas convection belt furnace, an IR. (infrared) furnace or vapour phase furnace. The process for "chip-and-wire" mounting and for soldered hybrid circuits is shown in Figure 22. Normally, soldered SMDs are not used on circuits together with wire bonded chip-on board, because of the danger of contamination from the solder process. This may make the surface unsuitable for wire bonding and/or give poor long-term reliability. Conformal coating is an extra protection by an organic material over the components and substrate, for example by using Parylene. Conformal means a coating covering all surfaces. It gives mechanical and environmental protection and binds loose particles.
The hybrid circuits may be used non-encapsulated or they may be mounted in metal- or ceramic flat-pack packages. Circuits with naked ICs are encapsulated hermetically or the naked chips may be protected by drops of epoxy ("glob top" encapsulation).

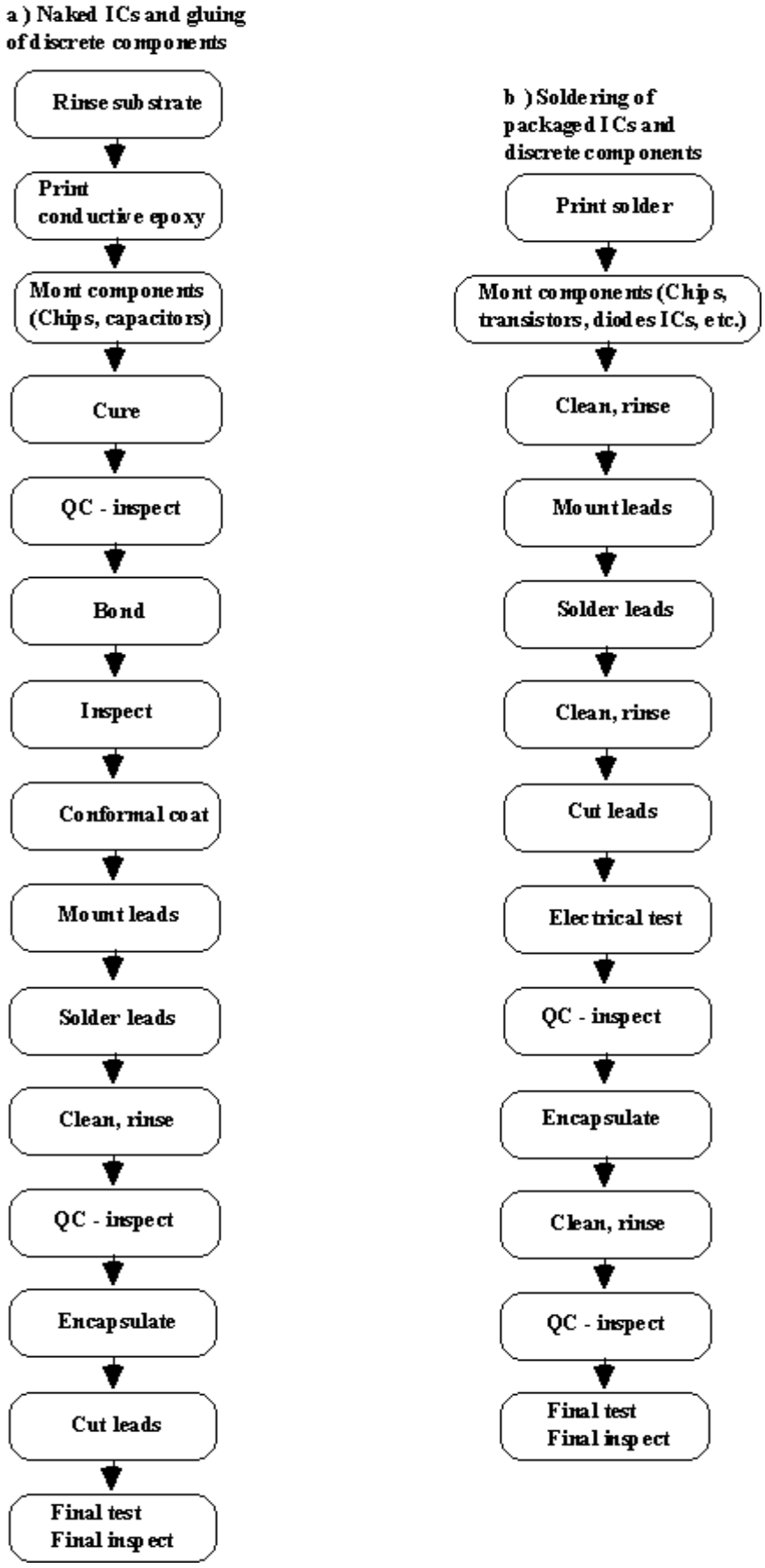

Figure 22 Process flow for mounting thick film hybrid circuits based on a) Bare-die, b)Soldering of packaged components.

2.2.1.4 Alterations

Pacific Microelectronics Corporation has developed a “Transfer Tape Dielectric”. This circumvents the problem with pin-holes in the dielectrics which are common for ordinary printed dielectrics. With this technique, there is only need for one layer of dielectric between each conductor layer, whereas ordinary thick film techniques requires at least two layers. Since the first conductor layer only can be fired a certain number of times, this increases the possible number of conductor layers on a thick film substrate. Since the number of process steps is reduced, the potential cost of the circuit is reduced.

2.2.1.5 Design rules

Some of the general design guidelines for PCBs, given in Chapter 6, also apply for hybrid circuits. The smallest conductor widths and distances are normally 0.2 mm. The demands for low voltage drop in high current circuits may cause the need for wider conductors.

The smallest length and width for resistors are 0.5 - 1 mm. The ratio between length and width should be between 0.1 and 10. For resistors that dissipates much power the resistor area should be increased such that the dissipation is maximum 100 mW/mm^2.

An efficient ground plane is achieved by metallizing the complete underside of the substrate.

2.2.2 High Temperature Cofired Ceramics LTCC

High-temperature multilayer ceramic technology has been used for many years for ceramic capacitors and for IC packages. For packages and multichip modules, Al_2O_3 and AlN (BeO and SiC to a smaller extent) are used. For multichip modules, alumina is the most used material, with 92 - 96 % Al_2O_3 content. The structure consists of many layers of ceramic, with metallisation between the layers, and via holes through the layers for electrical contact. The best known application of large modules with many layers of ceramic is IBM´s pioneering product "Thermal Conduction Module" (TCM) for mainframe computers, already in 1983. The module had 33 layers, and 133 silicon chips were mounted by flip chip soldering. Since then, mainframe computer manufacturers have used analogous technology, based on materials with even better thermal performance.

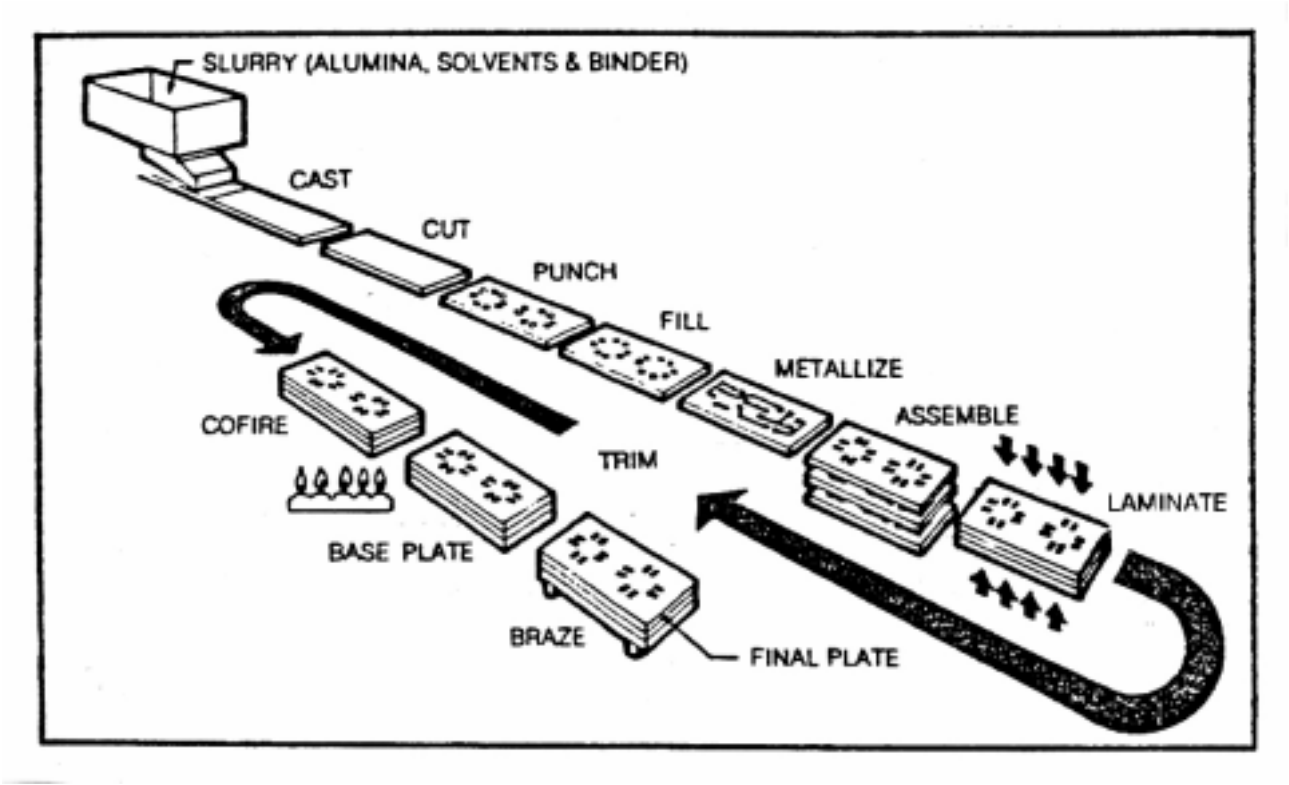

Figure 23 Production process for multilayer ceramic, schematically

2.2.2.1 Fabrication

The fabrication of multilayer ceramic modules by "tape casting" is shown schematically in Figure 23. The non-sintered, pliable ceramic consists of alumina powder, organic binders and solvents. The material is spread from a container down on a transport carrier underneath. The ceramic "tape" ("green sheet"), is given the appropriate thickness on the transport carrier by passing underneath a "doctor blade" in a precisely controlled distance. The tape is cut to correct size, and holes and component cavities are punched out with a numerically controlled punching tool or with a permanent, product specific punching tool for high production volume of a given product. Metallisation of the via holes and fabrication of conductors is done by screen printing of tungsten (or molybdenum). These are the only metals that can withstand the high process temperature during the subsequent sintering process. All layers are laminated together under hydrostatic (or uni-axial) pressure at elevated temperature (500 – 600 °C), to evaporate the binder and solvent. Then the whole structure is sintered at 1370 - 1650 °C, 30 - 50 hours, in hydrogen atmosphere. For small circuits, many modules are made on one substrate, and the individual circuits can be parted by breaking the substrate at the end of the process. Then the external contacts are brazed to the substrate and finally gold may be plated on the surface with nickel as diffusion barrier on top of the tungsten. The plating is preferably done electrolytically to achieve sufficient thickness and good conductivity, if one can make electrical contact to all parts of the conductor pattern. Otherwise, chemical plating is used.

During the process, the ceramic shrinks approximately 18 % linearly. This has to be taken into consideration during the design of the circuit, both sideways and in thickness (which affects the characteristic impedance). Normally the designer will operate in correct dimensions and the producer will scale the CAD information up by the necessary amount for production of printing screens and punching tools. The shrinkage is material- and process dependent, so the finished circuits typically have linear dimensional tolerances 0.5 - 1 %.

2.2.2.2 Properties

Some electrical, physical and mechanical properties are shown in **Table 14**. Black ceramic is used the most, the white material has somewhat higher purity and better properties at high frequencies, but it is transparent in a range of light wavelengths and is more expensive.

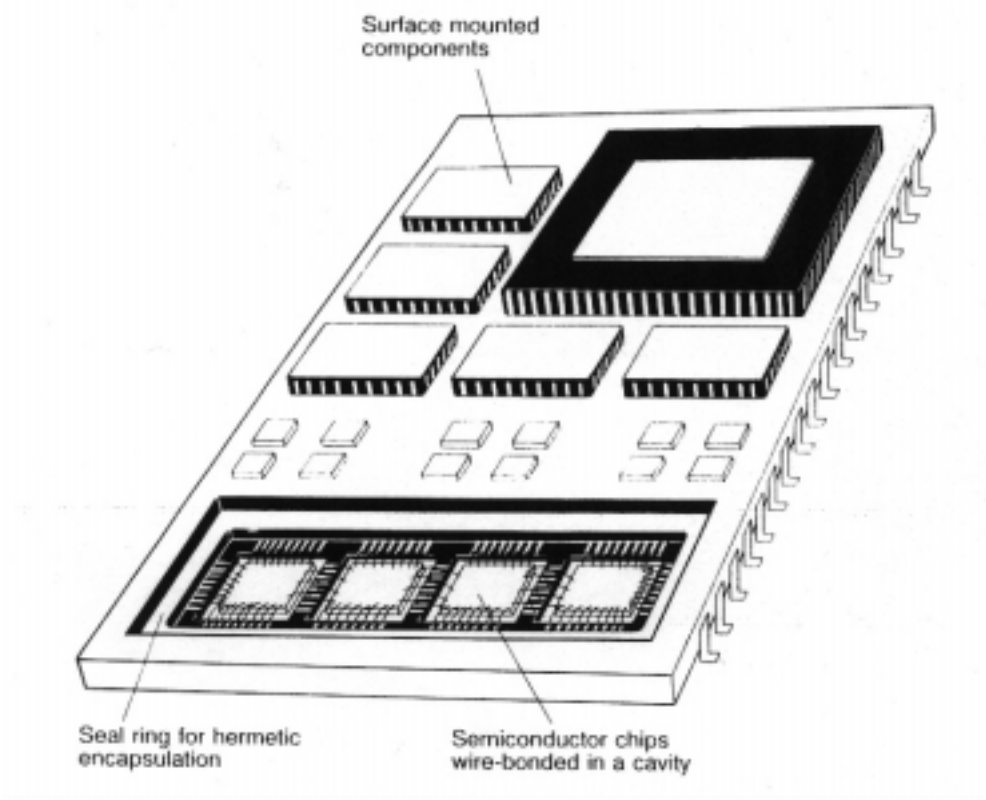

Figure 24 Combination of naked chips in cavities and soldered, packaged SMD components on multilayer ceramic module

The minimum conductor widths and conductor distances are typically 0.15 - 0.2 mm. Minimum diameter of via holes is typically 0.1 - 0.2 mm. Extended ground planes are made as grids of printed lines rather than continuous, due to the dissimilar thermal expansion of metal and ceramic. The typical thickness of the printed W conductor layer is 15 µm. The electrolytically plated Au on the surface is 2 µm or more, with a 2 µm Ni barrier/adhesion layer between the Au and W.

Among the advantages of high temperature multilayer ceramic are the following:

- Reasonable thermal conductivity
- Low TCE, good thermal match to Si and GaAs as well as to leadless SMD components
- Good control over characteristic impedance, good high frequency properties
- Both soldering of encapsulated components, TAB bonding of naked chips and flip chip mounting of smaller Si chips can be used (although there is not a perfect thermal match to flip chip soldered Si chips)
- Complete hermetic encapsulation is possible, or hermetic encapsulation of local areas, by using a lid over individual ICs in cavities. High reliability.
- Many layers are possible, with high production yield. This is because each layer can be inspected before the lamination, and faulty layers be discarded (contrary to thick film where one fault in one layer will ruin the whole circuit)
- Easy to mount edge contacts, coaxial contacts, etc.

Among the disadvantages are the following:

- Low electrical conductivity in the inner layers (sheet resistivity 15 mohm/sq)
- High dielectric constant gives delay, inferior pulse rise time and increased power loss and cross talk at very high frequencies
- The producers generally make standard packages in large volumes, and have high start-up cost for custom circuits

Table 14 Properties of alumina-based high-temperature multilayer ceramic

Ceramic		Colour	
Property	Unit	Black	White
$Al_2 0_3$ content	%	90	92
Density	g/cm^3	3,60	3,60
Relative dielectric constant (1 MHz)		9,5	9,0
Loss tangent (1 MHz)	%	1,3	0,3
Breakdown field	kV/mm	10	10
Resistivity	ohm cm	10^{14}	10^{14}
Thermal coeff. of expansion (0-100°C)	ppm/°C	5,0	5,0
Thermal coeff. of expansion (0-300°C)	ppm/°C	6,5	6,5
Thermal conductivity	W/m x °C	15	17
Specific heat	W s/g x °C	80	84
Module of elasticity	N/mm^2	$3x10^5$	$3x10^5$
Conductors Property	Unit	Value	
Tungsten Sheet resistivity (0.1 mm con. width) (0.2 mm - " -) (0.3 mm - " -)	mohm/□	 20 14 12	
Thermal coefficient of resistance	ppm/°C	4300	
Plated (W + Ni + Au) Sheet resistivity	mohm/□	 3-4	

2.2.3 Low Temperature Cofired Ceramics LTCC

DuPont, IBM and others have introduced multilayer ceramic based on glass compositions similar to those used in thick film dielectrics, instead of alumina. The fabrication is made in a process similar to that used for high temperature ceramic. The advantage of the low temperature technology is primarily that the sintering takes place at around 850 °C, 15 min., normally in air atmosphere (after a burnout at 350 °C to remove the organic binders and solvents). The effect of this is that the metal systems used in ordinary thickfilm technology are suitable for inner layers, with much better electrical conductivity than tungsten. Thick film firing furnaces may be used for the process. Resistors may also be printed in the inner layers. Materials in the substrate are mullite, corderite, lead borosilicate glass and others.

DuPont, one of those making the base materials, is promoting the technology among the thick film producers. The tape casting of the tape materials is done by DuPont and the user buys the tape mounted on a Mylar foil that is removed before the punching and printing. In Europe some three producers make custom designed low temperature ceramic circuits (1992), and many companies are testing out the technology. Several producers in the USA and Japan are making low temperature multilayer ceramic circuits, primarily for internal use.

Table 15 Properties of low-temperature multilayer ceramic

	Resistance [mohm/sq]	Fired Thickness [µm]
Inner Layer (Co-fired)		
Gold	5	7
Silver	5	8
Silver/Platinum	20	8
Top Layer (Post fired)		
Gold	4	8
Platinum/Gold	80	15
Silver/Palladium	20	15
Silver	4	15

Table 16 Resistor Performance - Resistance and TCR

	Over Tape		Over Thick Film Dielectric	
	R [ohm/sq]	HCTR [ppm/°C]	R [ohm/sq]	HCTR [ppm/°C]
100 ohm/sq	122	+20	102	+65
10 Kohm/sq	10,0 k	+71	12,5 k	+41
100 Kohm/sq	92,4 k	+75	95,7 k	+73

Table 17 Physical Properties

Thermal expansion	
Fired dielectrics	7,9 ppm/°C
96% alumina	7,0 ppm/°C
Fired density	
Theoretical	3,02 g/cm^3
Actual	>2.89 g/cm^3 (>96%)
Camber	
Fired	±75 µm (±3 mil.)
68 x 68 mm^2 (2.7 x 2.7 in^2)	
Surface smoothness	
Fired dielectric	0,8 µm/50mm
50 x 50 mm^2 (2 x 2 in^2)	(Peak to peak)
Thermal conductivity	
Fired dielectric	15 - 25% of alumina
Flexure strength	
Fired dielectric	2,1x10^3 kg/cm^2 (3,0x10^4 psi)
96% Alumina	3,8x10^3 kg/cm^2 (5,6x10^4 psi)
Flexure modulus	
Fired dielectric	1,8x10^6 kg/cm^2 (2,5x10^7 psi)
96% Alumina	0,9x10^6 kg/cm^2 (1,3x10^7 psi)

Many properties are similar to those of the high temperature system, but the thermal conductivity is about 5 times lower for the low temperature materials. The shrinkage is only approximately 12 %. The materials are more brittle than alumina, and they must be handled with caution. Some parameters are given in Table 17.

Typical conductors minimum width and separation are 0.15 - 0.2 mm, diameter of the via hole 0.15 - 0.2 mm, and distance between via holes 0.25 - 0.4 mm. The DuPont tape is made in two standard thicknesses: 90 and 250 µm (after sintering). The surface roughness is approximately 1 µm, lot-to-lot variation of the shrinkage: 0.2 %. The relative dielectric constant ε_r = 7.5 - 8.0 (but materials with lower ε_r are available), tan δ = 0.2 - 1 %. Thermal conductivity K = 2 W/m °C. Buried, silver based conductors have quite good migration properties, and the resistors have properties similar to those of thick film resistors. Circuits with 20 layers of ceramic have been demonstrated, the potential is said to be over 40.

Some advantages compared to high temperature multilayer ceramic technology are:

- Low process temperature, normal process atmosphere, requires low investments for thick film producers to start their own production
- ($ 100k - 200 k).
- Flexibility in choice of conductor materials, low sheet resistivity
- Plating is not necessary, bondable gold can be screen printed
- Resistors may be screen printed internally and on the surface
- Dielectric materials with relative dielectric constant down to 4 - 5 are used.

Disadvantages:

- New, immature technology
- Low thermal conductivity
- Brittle material, mechanically less robust
- So far, low availability.

A "transfer tape" version is also available, which is fired for each layer.

2.3 MCM D

2.3.1 Thin Film Technology

Thin film hybrid technology that has been in use since the 1960´s, with one layer of conductor, one layer of resistor and an inorganic dielectric. Thin film circuits consist of conductor layers, resistor layers and dielectric layers, similarly to thick film circuits. However, the conductor thickness is normally 1 µm or less, an order of magnitude less than for thick film. Processes from the semiconductor industry are used for deposition of conductors and dielectrics and for the definition of patterns. That gives a much higher circuit density than in thick film.

The substrate materials that are used the most are 99.6 % alumina and glass. The fine conductor line dimensions require a smooth and uniform surface, so the alumina substrates are polished. The purer quality alumina, used in thin film circuits has lower tan δ than the substrates used in thick film technology. This is particularly important for high frequency use.

The metal that is used for most for thin film conductors are gold. Gold is chemically stable, it has high electrical conductivity and good bondability. However, as previously mentioned, gold diffuses very rapidly into many other metals. Together with gold special, elements are used as diffusion barriers, and in addition as adhesion layers, because gold has poor adhesion to non-metallic materials. Nickel is suitable for diffusion barrier, a nickel/chromium alloy improves the adhesion, and it is also suitable as resistor material, see below. The much used Au - NiCr system is deposited by vacuum evaporation or by sputtering. Gold may also be electrolytically plated. This is particularly important for microwave circuits, where a 5 - 10 µm thick layer gives low conductor resistance, reducing the high frequency loss.

Various materials are used for dielectric depending on whether one wants to make capacitors, multilayer insulation or passivation. For passivation, SiN_3 is well suited. SiO_2 is used much for insulation between conductor layers, because it has low dielectric constant ($\varepsilon_r = 4$), and high breakdown field strength (10^6 V/cm). Both are produced by chemical vapour-phase deposition. For capacitor dielectric SiO_2, Al_2O_3, Ta_2O_5 are used. They are produced by vacuum evaporation, chemical deposition, or anodic oxidation.

Resistors are made, as mentioned, from NiCr, as well as Ta_2N, by vacuum evaporation or by sputtering.

While we can achieve over 6 decades of variation in sheet resistivity in thickfilm hybrid technology, the range we achieve with practical thickness in thin film technology is only between approximately 10 and 1000 ohm/sq. Some properties are shown in Table 18.

Table 18 Properties of thin film resistors

Material	*Specific Surface Resistance ($t<<\delta$), $R_f = \rho / t$ (in ohm)*	*Temperature Coefficient of the resistance, $\Delta R/(R\,\Delta T)$ (in $10^{-6}/°K$)*	*Stability $\Delta R/(R\,\Delta T)$ (in %/1000h)*	*Production method*
NiCr (nickel-chrome)	40 - 250	-100 - +100	<0,2 good	Evap
Cr (chrome)	10 - 500	-300 - +300	medium	Evap
Ta (tantalum)	40 - 200	-200 - +200	<1 medium	Sp
Ta_2N (tantalum-nitride)	10 - 100	-60 - +30	<0,2 good	Reactive sp
Ti (Titanium)	5 - 2000	-500 - +500	medium	Evap
Cr-SiO Cement	500 - 2000	-250 - +250	<0,5 medium	Flash sp

2.3.1.1 Production process

Figure 25 shows the process steps for a thin film circuit, with one conductor layer and one resistor layer. In the first step, the resistor layer is deposited all over the substrate. If the circuits are small, many circuits are made on the same substrate, and they are separated at the end of the production process.

First a diffusion barrier (also improves the adhesion) is deposited and then the conductor metal. This is preferably done in the same vacuum chamber, in order to have a clean surface and good adhesion. These standard processes require special equipment and clean room facilities. Minor thin film circuit producer companies will normally buy the substrates, which are processed to this stage.

Conductor and resistor geometries are defined by photolithography and etching. A few drops of photoresist are deposited and spread by the centrifugal force when the substrate is rotated on a spinning disk. The conductor pattern for the circuit is defined by exposing the resist through a photo mask, development and curing. Then the gold is removed by etching where it is not wanted. A solution of potassium iodide solution may be used for etching the gold, without dissolving the NiCr layer. If the need exists for conductor widths less than 2-3 µm, the etching is done by reactive ion etching, which etches fast vertically, but more slowly horizontally, and thus reducing the under-etching.

A new step of photo-processing is done to define the pattern of the resistors, and the diffusion barrier and the resistor films are etched where they are to be removed, for example with nitric acid. (Where the circuit has conductor pattern, there is still the resistor layer underneath the conductor material, see Figure 25.)

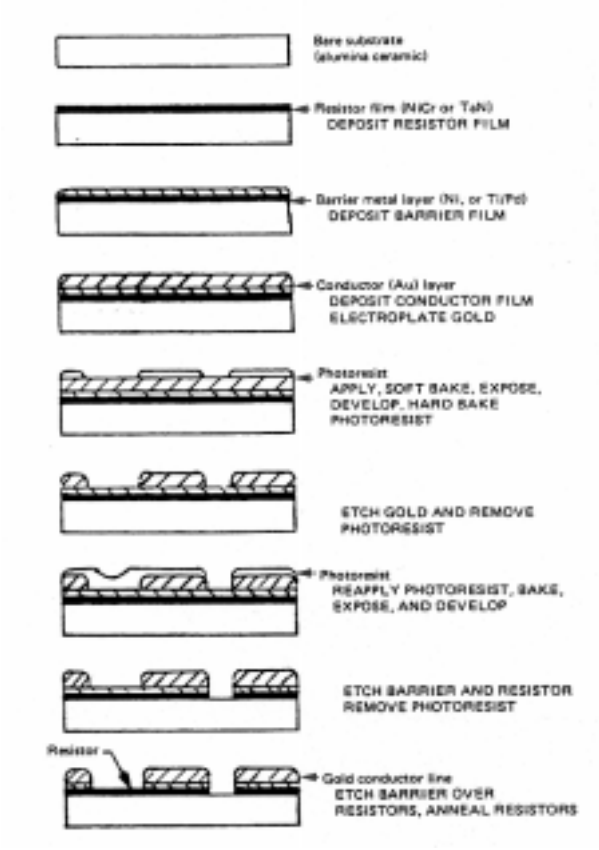

Figure 25 Process flow for production of thin film hybrid circuits

Finally, the circuit is cured in air at 250 - 350 °C for some hours, to make a passivating layer of chromium-oxide to protect and stabilise the resistors.

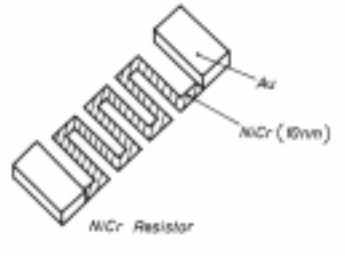

Figure 26 Structure of thin film resistor with gold termination.

2.3.1.2 Thin film components

A type of "components" that is very suitable for being made by thin film technology is precision R/C networks. They are also available as off-the-shelf components for mounting on other thin- or thick film substrates.

Diodes and transistors can also be fabricated. Large thin film diodes made from Cu_2S/CdS hetero-junctions give low price solar cells, and thin film transistors have been under development for 10 - 15 years. A matrix of thin film transistors is of great interest for the control of big LCD screens for flat televisions, etc. The structure is similar to Si -MOS transistors, see Figure 27. CdSe as well as Si/H are used as the semiconducting material.

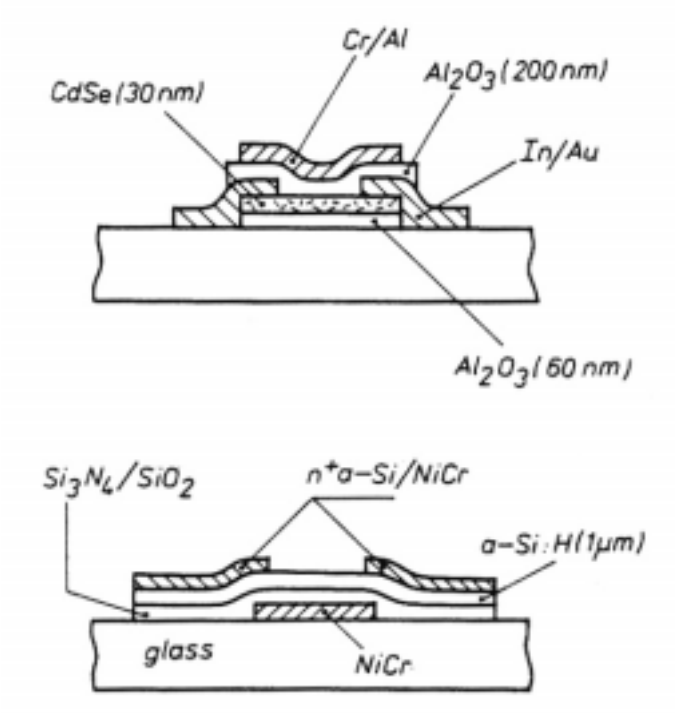

Figure 27 Thin film transistors, structure

2.3.1.3 The complete thin film circuit

When the thin film substrate has been completely processed, resistors may be laser trimmed like in the case of thick film circuits. After this, components will be mounted on the substrate. Integrated circuits are normally mounted in the form of naked chips that are glued on to the substrate and wire bonded. Discrete resistors and capacitors are normally mounted with conductive adhesives for electrical and mechanical contact and not soldered. In most cases, the complete circuit will be mounted in a hermetic package that is made of metal, or in some cases of ceramic. Terminal points on the substrate will be connected to the leads of the package by wire bonding. A welded or soldered metal lid on the package ensures hermeticity and good reliability.

2.3.1.4 Multilayer thin film, multichip modules

This is an extension of conventional thin film technology, but with many conductor layers, that makes it possible to achieve a very high circuit density. We may also achieve controlled characteristic impedance and good high frequency properties.

The normal substrates are either 99.6 % alumina or silicon wafers. Figure 28 shows a cross section. The dielectric most often used is polyimide or benzocyclobutene. The organic dielectrics are deposited in a similar way as the photoresist described earlier to a thickness of approximately 10 µm. Some of these materials are photo immagible, which means that they can be patterned without the use of an additional photoresist. The dielectric constant as well as the dielectric loss for these materials is low which means that good high frequency performance may be obtained.

Also non organic materials like silicon oxide and silicon nitride are used for dielectrics. These materials are deposited by chemical vapour deposition or sputtering. These materials will typically be deposited in a thickness of the order of 1 µm. The dielectric constant is significantly higher than for the organic materials. On the other hand, these dielectrics give a hermetically sealing of the metal tracks.

Aluminium (Al), copper (Cu), and gold (Au) are most commonly used as conductor metals. IC process technology makes it possible to achieve a minimum conductor width/distance of 25 µm or less, i.e. a higher conductor density than any other substrate technology (except full wafer scale integration). AT&T has been a pioneer in this technology. Over 100 companies and research labs had this technology under development /

production in 1992 and it will be a mainstream technology for high performance systems during the coming years. One high performance product employing the technology is the mainframe computer VAX 9000, of Digital Equipment Corporation. Silicon substrates are used and the IC chips are mounted as TAB-components.

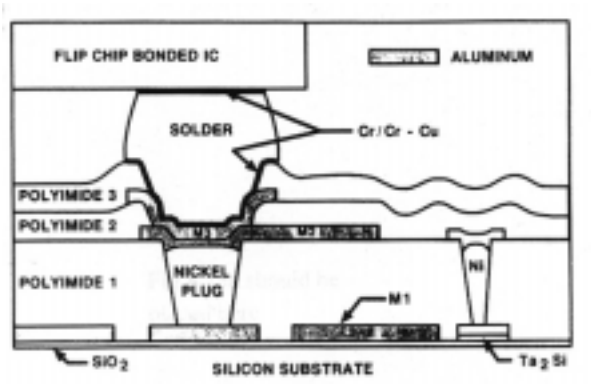

Figure 28 AT&T´s structure for multilayer thin film

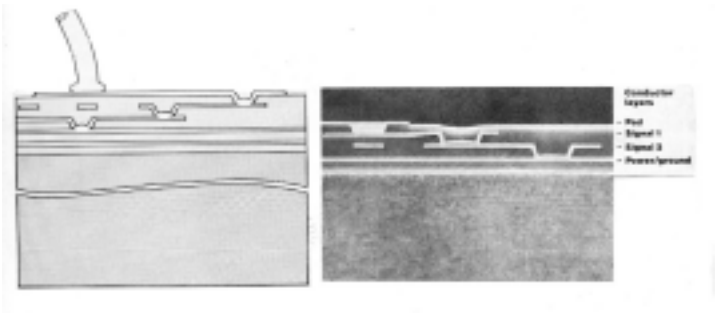

Figure 29 Cross-section of Raychem´s High Density Interconnect (HDI) schematically and observed through microscope

A typical process is as follows:

1. Spinning of polyimide insulation
2. Deposition of Al metallisation (sputtering, 5 µm, R=6 mohm/sq)
3. Photolithography and wet etch of conductor pattern
4. Spinning of polyimide
5. Etching of via holes. Several methods are used, this is a critical point.
6. Repetition of steps 1 - 5 for multilayer
7. Metallisation and etching of the surface metal (5 µm Al or 2 µm Au).

Some design rules for Raychem´s "High density interconnect" (HDI) technology are shown in Figure 30. All the way up to 10 GHz the losses in the conductor dominate, the dielectric loss is negligible. However both the dielectric constant as well as the dielectric loss depends on the moisture absorption in the polyimide: ε_r = 3.4 (dry) and 4.5 (maximum moisture content, 3.5 %). A lot of work is going on to develop new types of polyimide and alternative materials that are less hygroscopic.

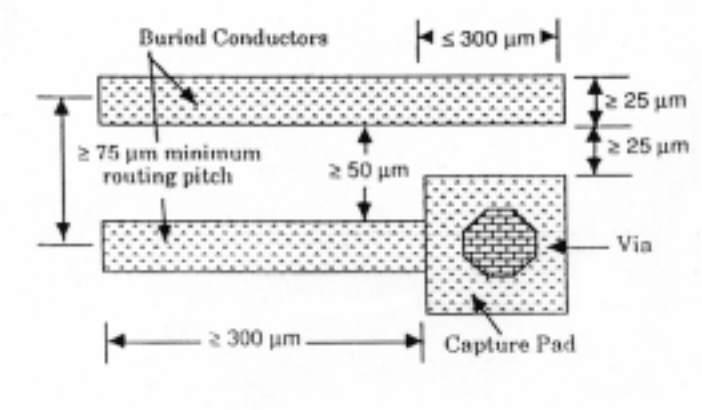

Figure 30 Elements of the design rules for Raychem´s HDI technology

For ICs with high power dissipation it is possible to make a "thermal well", by mounting the chip directly on the substrate, without the polyimide which acts as a large thermal resistance. This technique is used in the VAX 9000 computer, where ECL technology gives high power dissipation. However, the result is a reduced area for signal routing.

Some advantages of multilayer thin film with Si substrates:

- Optimal thermal match between Si substrate and Si chip components
- Very good thermal conductivity in Si substrate: 150 W/°C m
- Termination resistors and de-coupling capacitors may be integrated in the substrate
- Compatibility with wire bonding, TAB and flip chip. Also with gluing of discrete components
- Very high conductor density and package density
- Very good high frequency properties
- Short wire lengths
- Low ε_r (with organic dielectric materials, and a ground-plane on top of the silicon)
- Low dielectric losses (with organic dielectric materials, and a ground-plane on top of the silicon)
- Very good mechanical properties
- High reliability when it is hermetically encapsulated

Some disadvantages:

- Thus far; low availability and high cost
- Polyimide is hygroscopic
- Moisture uptake may give swelling and corrosion over long time
- Changed dielectric properties
- Hermetic encapsulation is necessary.
- Immature technology.

2.3.2 Alternative techniques (substrates)

Micro Module Systems has developed a thin film technique based on aluminium substrates. Polyimide is used as dielectric, and copper is used for metallisation in the inner layers, whereas gold is used at the outer layer to allow ordinary wire bonding. The minimum pitch is 50 µm, which gives 200 conductors per centimetre. The via-holes are formed by plasma etching, where all the holes are etched in one step, which gives potentially low cost. The components (passive, bare dies or packaged chips) are glued to the substrate with a special glue. The large miss-match in thermal expansion between the components and the aluminium means that large QFP components can not be used. Flip chip technique is not possible either due to the miss-match. The metal substrate can be used as a ground plane.

2.4 IBM's Thin-film on ceramic

IBM offers thin film MCMs on glass ceramic, which address the needs of the high-end, high-performance semiconductor applications, represent an advance over the standard alumina substrates. The MCM is based on a multilayer glass ceramic, known as corderite (borosilicate glass), onto which a polyimide based thin film structure is added. The two parts are described below.

2.4.1 Properties of IBM's glass ceramic multilayer[4]

IBM is using a corderite glass multilayer ceramic (MLC) with copper circuits capable of accommodating off-chip I/O up to 5000 and off-package I/O count of more than 1600. The material has a matched thermal coefficient of expansion with silicon, addressing the needs of those high-end applications requiring large die sizes to integrate complex function. The size of a typical high-performance MPU is 18 mm square or larger[5], making it important to find materials with a lower thermal coefficient of expansion (TCE) to match that of silicon. The glass ceramic package accommodates die sizes up to 30 mm on edge without chip-to-package reliability concerns. The copper conductors and low dielectric constant of the glass ceramic deliver improved electrical performance, a typical characteristic impedance of 50 ohms and high dimensional stability.

Higher processor speed requirements have led to a search for packages with lower resistance wiring and lower dielectric constant. The controlled collapse chip connection (C4) of flip-chip die in this size range needs improved fatigue life as MPU field conditions demand higher numbers of on/off cycles, higher operating temperatures and very high numbers of mini-cycles (rest-mode)[6]. Furthermore, the stress in the silicon itself grows proportionally to the TCE of the chip carrier as large die are attached and underfilled to the carrier[7].

Table 19 The key features of the multilayer ceramic substrate.

Dielectric Material	Corderite GC
Substrate Colour	Red
Bulk Density	2.6 gm/cc
Effective Dielectric Constant	5
Dielectric Loss	0.0004 @ 9Ghz
Dielectric Resistivity	10E 15 ohm-cm
Thermal Conductivity	50.0 W/m-K
Coefficient of Thermal Expansion	3.0 ppm/C
Conductor	Copper
Conductor Resistivity	2.8 µohm-cm
Pattern Dimension Tolerance	±0.15%
Camber/Flatness	< 8.5 µm/cm
Flexural Strength	210 MPa

Table 20 Dimensional features of the ceramic substrate

	Present	Year 2000 or later
Fired Layer Thickness	90 µm,115 µm	60 µm, 90 µm, 115 µm
Line Width	75 µm	50 µm
Line Height	22 µm	22 µm
Line Spacing	100 µm (Min.)	75 µm

[4] B. V. Fasano, R. Indyk, D. O'Conner, A. L. Plachy, S. N. S. Reddy, "Glass Ceramic Substrates for Flip Chip Packages", IBM Corporation, East Fishkill, New York

[5] Kuracina, R., "Flip Chip Packaging for the Year 2000", Presented at Semicon West '98, to be published

[6] DiGiacomo, G., "Reliability of Electronic Packages and Semiconductor Devices", McGraw-Hill, 1996

[7] Sylvester, Mark F., Banks, Donald R., Kern Richard L., and Pofahl, Ronald G., "Thermomechanical Reliability Assessment of Large Organic Flip-Chip Ball Grid Array Packages", 1998 Proceedings, 48th Annual Electronic Components and Technology Conference, pp. 851-860

Line Pitch	225 µm, 450 µm	200 µm, 400 µm
Via Diameter	90 µm	75 µm
Via Pitch	225 µm, 450 µm	200 µm, 400 µm
Via Cap Dia.	112 µm	92 µm
C4 Pitch	225 µm, 250 µm	200 µm
C4 Array	Full or Partial	Full or Partial

Table 21 Electrical performance of the multilayer glass ceramic compared to that of alumina ceramic.

Performance improvement	IBM Glass Ceramic	Alumina comparison
Resistance	9.25 ohm/cm	64% < Alumina
Capacitance	1.40 pF/cm	50% < Alumina
Propagation Delay	78 psec/cm	28% < Alumina
Impedance	50-60 ohms	30% < Alumina (nontriplate)
Coupled Noise	13 m V/V	48% < Alumina
Switching Noise	205 mV	20% < Alumina

2.4.2 Properties of IBM's multilayer thin film

In addition to supporting significantly higher speed for critical nets, the thin film-based G5 MCM enables higher chip I/O density and higher net density (lines/cm2). In addition, higher simultaneous switching activity (with lower delta-I noise despite higher speed switching and greater delta-I current), and a lower signal-signal coupled noise is obtained.

The fine pitch of the thin film wiring (18 µm lines on a 45 µm pitch) enables theG5 MCM to support chips such as the SC, which require 1250 signal I/Os. The fine pitch thin film wiring was also essential to positioning large (17+ mm) chips on a pitch of only 22 mm. This extremely tight placement of chips also contributed to minimising critical net path lengths, essential to meeting the 4-ns system cycle time objective. The high performance, along with good cost/performance of the G5 module and system, would not have been achievable without the use of the multilevel, fine-featured thin film structure.

The dielectric material is polyimide and via holes are made by laser ablation.

The first metallized thin film layer, M0, is used for capture pad and voltage mesh. This layer contains capture pads, which overlay the copper vias in the glass ceramic. The capture pad is the electrical interface between ceramic and thin films (Figure 3).

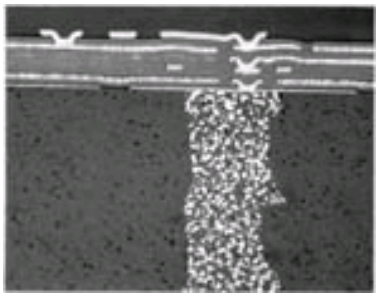

Figure 31 Cross-section of the S/390 G5 TSM thinfilm structure. The M0 thin film capture pad is shown overlaying the glass ceramic via. At the top of the film pattern is the M5. The M5 layer provides repair capability and chip connectivity. In between are the two mesh layers and X/Y plane pair.

The mesh in the M0 thin film structure provides uniform voltage distribution. The next metal level, M1, is another voltage mesh. The first wiring level, M2, follows. This is the X wiring level of the X/Y plane pair. It consists of 18-micron wide Cu lines that are 5 microns thick on a 45-micron pitch. The Y level, M3, has the

same design ground-rules as the X layer. The two wiring layers run perpendicular to one another to reduce coupling. Within this single plane pair are 212 meters of signal wiring. Following the X/Y plane pair is the M4 level, which is a ground mesh. The three voltage planes together provide a low inductance path between the chips and the high-performance de-coupling capacitors. This reduce the system level delta-I noise, even though there is a larger number of simultaneously switching drivers switching at higher speeds than in the earlier G4 system. The uppermost thin film layer, M5, provides the structures needed for chip-to-thin-film connectivity and reworkability as well as top surface line structures, which provide signal net repairability for both thin film and ceramic nets.

Net repairability is accomplished by laser line deletion and line reconnection to form alternate net paths. This technology enables the production of highly complex wiring in high yield. The metallization of the M5, unlike the copper only of the other layers, consists of chrome, copper, nickel, and gold. This particular structure is needed to create a good intermetallic connection between thin film pads and the lead/tin solder I/O of the chip, also known as the chip C4.

Between every thin film metal layer is a 6- to10-micron layer of low dielectric (3.2), low TCE polyimide, through which approximately 55,000 vias are created per layer by laser ablation of the polyimide through a patterned mask. When ultimately metallized, these small vias (on the order of 20 microns in diameter) provide reliable layer-to-layer thin film connectivity (Figure 3). Thin film metallization is accomplished by sputtering metal onto the surface, followed by photo definition of the pattern and then pattern creation through either sub-etch or plate-up techniques.

2.4.3 IBM's G5 MCM

In May of 1998, the S/390 G5 Parallel Enterprise Server was announced by IBM as the newest and most powerful member of IBM's mainframe family. Originally anticipated to offer more than 900 million instructions per second (MIPS) when configured as a "10+2" system, the S/390 G5 actually delivers a 15% increase in performance, making it the first commercially available mainframe in the 1000+ MIPS range. This performance is closely connected to the glass ceramic/thin film packaging. The result is the G5 multichip module (MCM), which, as the heart of the S/390 G5 system, offers both outstanding processing speed and very high reliability.

The G5 MCM is a 127,5 mm glass ceramic substrate consisting of 75 layers of ceramic, with six levels of thin films. This structure supports a system design with 12 CPUs and a total of 29 chips operating at a 4-ns system cycle time. There are a total of 12.000 nets in this MCM, with a total wiring length of approximately 600 meters.

A picture of the MCM is shown under, where the TSM side of the S/390 G5 MCM after thin film completion are seen. The 29 chip sites and the de-coupling capacitor sites between the chip sites are clearly visible. The one site in the centre of the top row is used for thin film process control.

Two additional thin film layers are built on the bottom surface of the MCM to support a high-density pin grid array. For both thin films and glass ceramic, this package represents the greatest number of layers and wiring length used in any MCM package announced to date by IBM. Table x shows a comparison of thin film packages used in various IBM systems

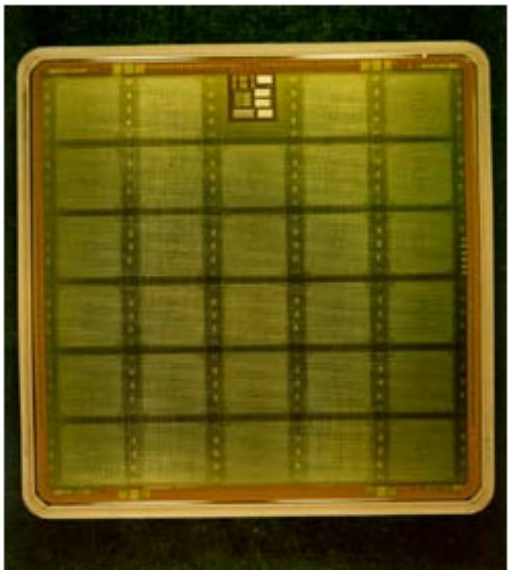

Figure 32 The TSM side of the S/390 G5 MCM after thin film completion are seen. The 29 chip sites and the de-coupling capacitor sites between the chip sites are clearly visible. The one site in the centre of the top row is used for thin film process control.

Table 22 Comparison of thin film packages used in various IBM systems.

	ES/9000	AS/400	Enterprise S/390 G3	Enterprise S/390 G4	Enterprise S/390 G5
CERAMIC					
Size (x/y in mm)	127.5	64.3	127.5	127.5	127.5
No. of Layers	70	31	69	68	75
No. of Plane Pairs	28	8	20	19	17
Meters of Wiring	275-420	18.3v	515	486	445
THIN FILMS					
No. of TSM layers	2	5	4	4	6
No. of Plane Pairs	0	1	0	0	1
Meters of Wiring	40*	75.3	65.1*	65.1*	212
I/O	2,772-3,526	882	3,526	3,526	4,224
Chips / MCM	110-121	7	34	30	29
Chip Technology		Bi-CMOS	CMOS 5X	CMOS 5X/66	CMOS 6S/6X

*Redistribution wiring only

A large portion of the glass ceramic layers that comprise the G5 MCM are represented by 17 X/Y signal wiring plane pairs. The thin film structure supports an additional high density X/Y plane pair. This one thin film plane pair—as a consequence of its fine pitch wiring—is the equivalent of 10 ceramic plane pairs. By leveraging the thin film wiring density to reduce ceramic layers, performance is enhanced and package thickness and cost are reduced. The thin film structure not only provides signal wiring capability, but also provides structures for several other critical functions:

- ceramic and thin film net repairability
- engineering change support
- chip connectivity to the MCM
- a low-noise environment
- and pin braze capability for high-density I/O.

On the BSM 4224 thin film I/Os are symmetrically arranged into four quadrants, each with an equal number of pins (Figure 5). Gold pins are then gold/tin brazed to the I/O pad. These pins then provide the connection to the S/390 G5 system board.

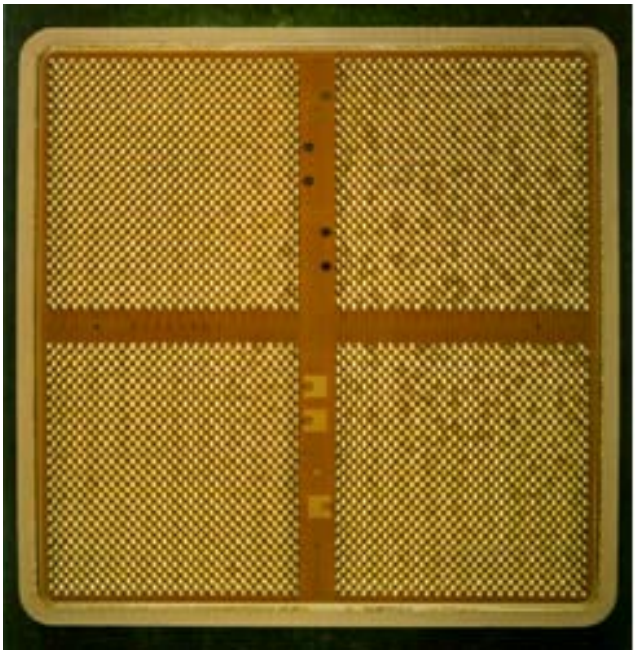

Figure 33. The BSM side of the S/390 G5 MCM after gold pins have been brazed to the thin film I/O. In the center channel are thin film VPT pads used to test voltage planes and to distribute current to the TSM during the thin film plating process.

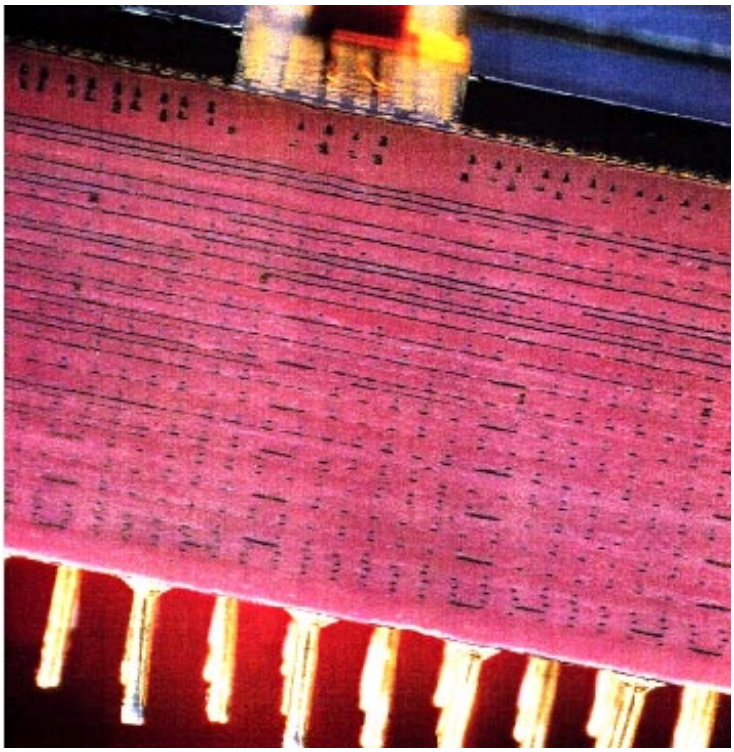

Figure 34. A cross-section of a IBM multilayer ceramic – thin film module

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4 REFERENCES

4.1 Table index

4.2 Figure index