ECE380 Digital Logic

Flip-Flops, Registers and Counters:

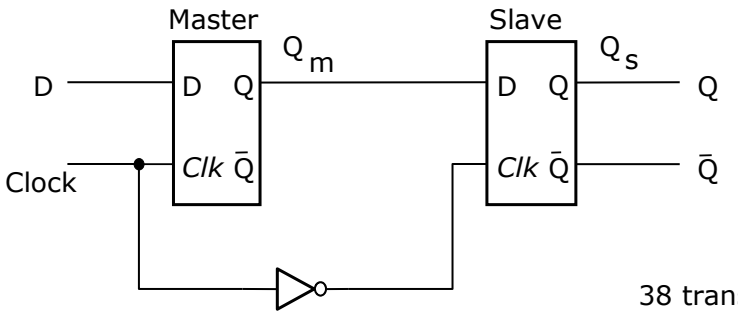
Flip-Flops

Flip-flops

- The gated latch circuits presented are level sensitive and can change states more than once during the 'active' period of the clock signal
- Circuits (storage elements) that can change their state no more than once during a clock period are also useful
- Two types of circuits with such behavior
  - Master-slave flip-flip
  - Edge-triggered flip-flop

Master-slave D flip-flop

- Consists of 2 gated D latches
  - The first, ***master***, changes its state while clock=1
  - The second, ***slave***, changes its state while clock=0

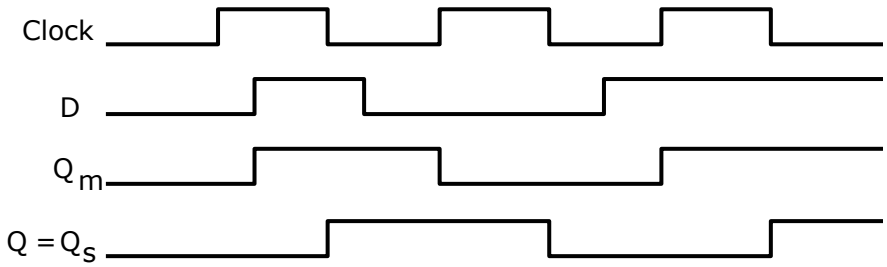


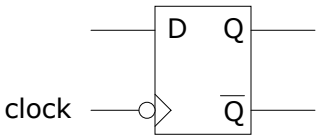
38 transistors

Master-slave D flip-flop

- When clock=1, the master tracks the values of the D input signal and the slave does not change
  - Thus Q_m follows any changes in D and Q_s remains constant
- When the clock signal changes to 0, the master stage stops following the changes in the D input signal
- At the same time, the slave stage responds to the value of Q_m and changes states accordingly
- Since Q_m does not change when clock=0, the slave stage undergoes at most one change of state during a clock cycle
- From an output point of view, the circuit changes Q_s (its output) at the ***negative edge*** of the clock signal

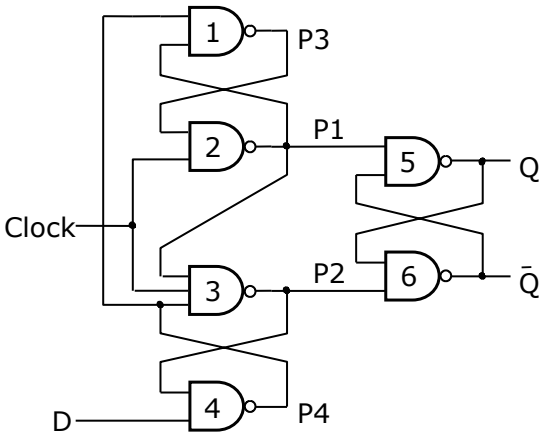
Master-slave D flip-flop

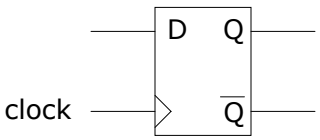




Edge-triggered flip-flop

- A circuit, similar in functionality to the master-slave D flip-flop, can be constructed with 6 NAND gates



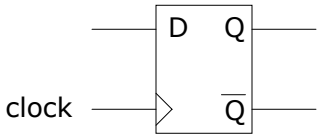


Positive-edge-triggered D type flip-flop

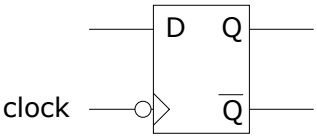
24 transistors

Edge-triggered flip-flop

- The previous circuit responds on the positive edge of the clock signal
- A negative-edge triggered D flip-flop can be constructed by replacing the NAND with NOR gates

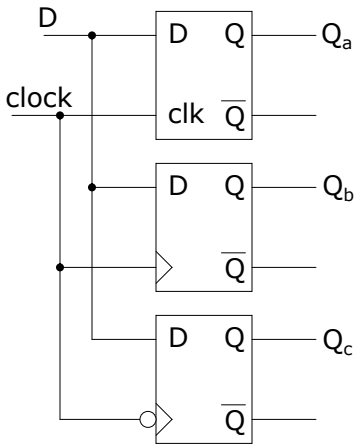


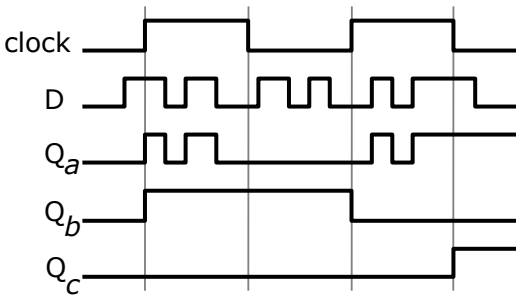
Positive-edge-triggered
D type flip-flop



Negative-edge-triggered
D type flip-flop

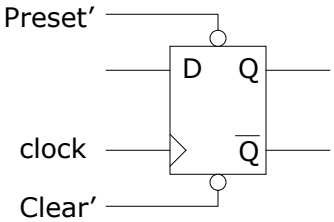
Comparing D storage elements





Clear and preset inputs

- It may be desirable to specifically set (Q=1) or clear (Q=0) a flip-flop
- Practical flip-flops often have ***preset*** and ***clear*** inputs
  - Generally, these inputs are ***asynchronous*** (they do not depend on the clock signal)

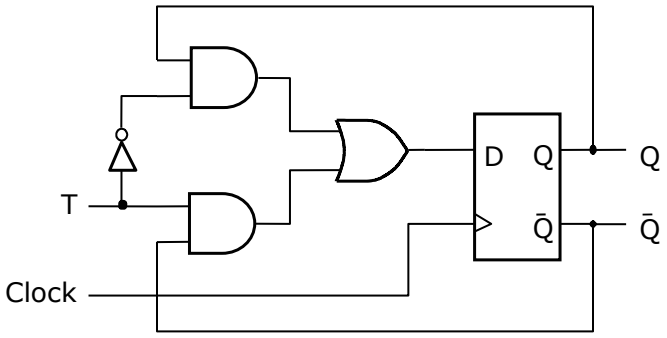


As long as Preset'=0, Q=1

As long as Clear'=0, Q=0

T flip-flop

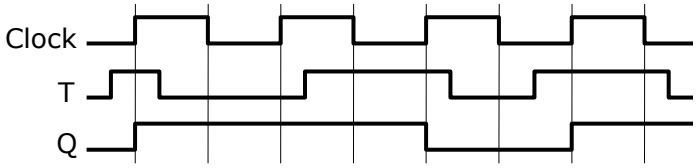
- Another flip-flop type, the ***T flip-flop***, can be derived from the basic D flip-flop presented
- Feedback connections make the input signal D equal to the value of Q or Q' under control of a signal labeled T

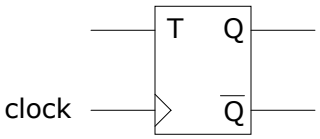


T flip-flop

- The name T derives from the behavior of the circuit, which 'toggles' its state when T=1
  - This feature makes the T flip-flop a useful element when constructing counter circuits

T	Q(t+1)
0	Q(t)
1	Q'(t)





Positive edge triggered

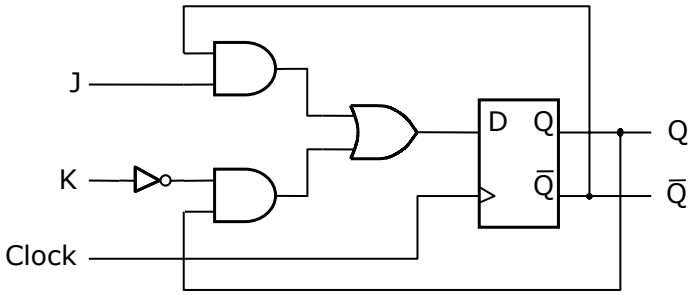
JK flip-flop

- The ***JK flip-flop*** can also be derived from the basic D flip-flop such that

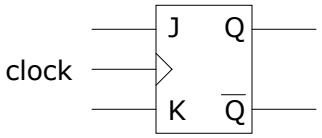
  $D=JQ'+K'Q$

- The JK flip-flop combines aspects of the SR and the T flip-flop
  - It behaves as the SR flip-flop (where J=S and K=R) for all values except J=K=1
  - For J=K=1, it toggles like the T flip-flop

JK flip-flop



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)



Positive edge triggered

JK flip-flop timing diagram

Complete the following timing diagram