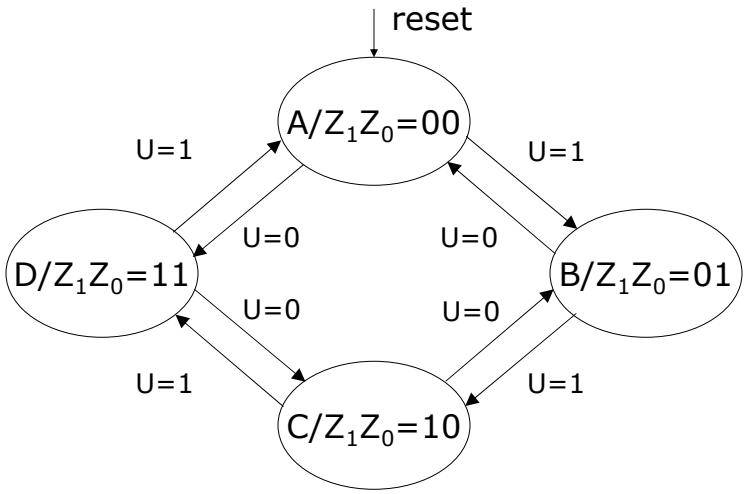
ECE380 Digital Logic

Synchronous Sequential Circuits:
Implementations using D-type,
T-type and JK-type Flip-Flops

Counter design example

- Design a 2-bit counter that counts
  - in the sequence 0,1,2,3,0,… if a given control signal U=1, or
  - in the sequence 0,3,2,1,0,… if a given control signal U=0
- This represents a 2-bit binary up/down counter
  - An input U to control to count direction
  - A RESET input to reset the counter to the value zero
  - Two outputs (Z_1Z_0) representing the output (0-3)
  - Counter counts on positive edge transitions of a common clock signal
- Design this counter as a synchronous sequential machine using
  - D-type, T-type, JK-type flip-flops

Counter state diagram



Counter state table

Present state	Next state		Output Z_1Z_0
	U=0	U=1	
A	D	B	00
B	A	C	01
C	B	D	10
D	C	A	11

State-assigned state table

- Choosing a state assignment of A=00, B=01, C=10 and D=11 makes sense here because the outputs Z_1Z_0 become the outputs from the flip-flops directly

	Present state y_2y_1	Next state		Output Z_1Z_0
		U=0	U=1	
		Y_2Y_1	Y_2Y_1	
A	00	11	01	00
B	01	00	10	01
C	10	01	11	10
D	11	10	00	11

D-type flip-flop implementation

- When D flip-flops are used to implement an FSM, the next-state entries in the state-assigned state table correspond directly to the signals that must be applied to the D inputs
- Thus, K-maps for the D inputs can be derived directly from the state-assigned state table
- This will not be the case for the other types of flip-flops (T, JK)

State table and next-state maps

	Present state y_2y_1	Next state U=0 Y_2Y_1	Next state U=1 Y_2Y_1	Output Z_1Z_0
A	00	11	01	00
B	01	00	10	01
C	10	01	11	10
D	11	10	00	11

$Z_1=y_2$ $Z_0=y_1$

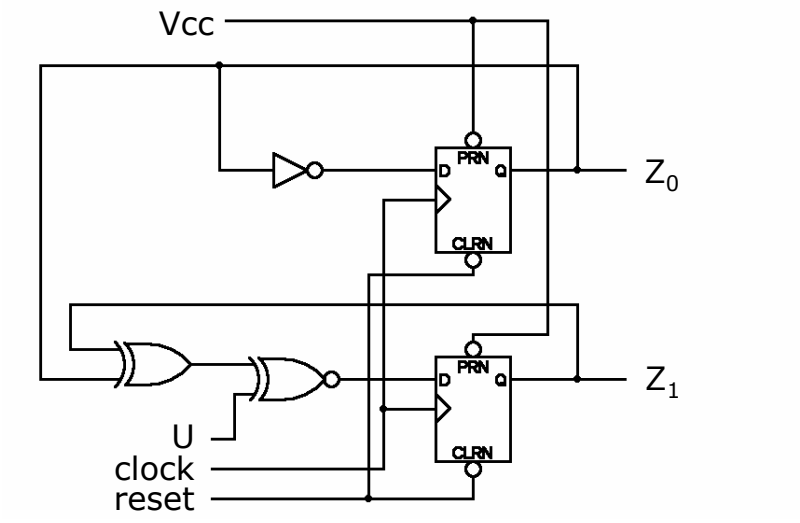
u \ y_2y_1	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$Y_1=y_1'$

u \ y_2y_1	00	01	11	10
0	1	0	1	0
1	0	1	0	1

$Y_2=(y_2 \oplus y_1 \oplus u)'$

Circuit diagram (D flip-flop)



Design using other flip-flop types

- For the T- or JK-type flip-flops, we must derive the desired inputs to the flip-flops
- Begin by constructing a **transition table** for the flip-flop type you wish to use
  - This table simply lists required inputs for a given change of state
- The transition table is used with the state-assigned state table to construct an **excitation table**
  - The excitation table lists the required flip-flop inputs that must be 'excited' to cause a transition to the next state

Transition tables

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Q	Q^+	J	K
0	0	0	D
0	1	1	D
1	0	D	1
1	1	D	0

JK transition table

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

T transition table

The transition table lists required flip-flop inputs to affect a specific change

T-type flip-flop implementation

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Use entries from the transition table to derive the flip-flop inputs based on the state-assigned state table.

excitation table

Present state y_2y_1	Flip-flop inputs				Output Z_1Z_0
	U=0		U=1		
	Y_2Y_1	T_2T_1	Y_2Y_1	T_2T_1	
00	11	11	01	01	00
01	00	01	10	11	01
10	01	11	11	01	10
11	10	01	00	11	11

Excitation table and K-maps

Present state y_2y_1	Flip-flop inputs		Output Z_1Z_0
	U=0	U=1	
	T_2T_1	T_2T_1	
00	11	01	00
01	01	11	01
10	11	01	10
11	01	11	11

$Z_1=y_2 \quad Z_0=y_1$

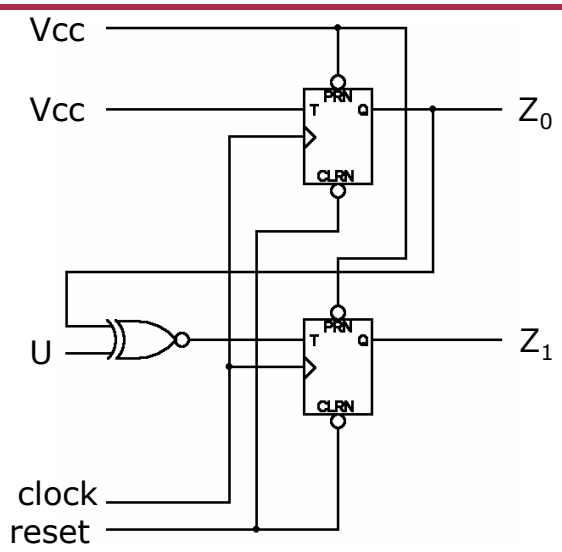
u \ y_2y_1	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$T_1=1$

u \ y_2y_1	00	01	11	10
0	1	0	0	1
1	0	1	1	0

$T_2=y_1u+y_1'u'=(y_1 \oplus u)'$

Circuit diagram (T flip-flop)



JK-type flip-flop implementation

- Use entries from the transition table to derive the flip-flop inputs based on the state-assigned state table
  - This must be done for each input (J and K) on each flip-flop

Present state y_2y_1	Next state		Output Z_1Z_0
	U=0	U=1	
	Y_2Y_1	Y_2Y_1	
00	11	01	00
01	00	10	01
10	01	11	10
11	10	00	11

Q	Q^+	J	K
0	0	0	D
0	1	1	D
1	0	D	1
1	1	D	0

JK transition table

JK-type flip-flop implementation

Q	Q^+	J	K
0	0	0	D
0	1	1	D
1	0	D	1
1	1	D	0

JK transition table

Present state y_2y_1	Flip-flop inputs						Output Z_1Z_0
	U=0			U=1			
	Y_2Y_1	J_2K_2	J_1K_1	Y_2Y_1	J_2K_2	J_1K_1	
00	11	1D	1D	01	0D	1D	00
01	00	0D	D1	10	1D	D1	01
10	01	D1	1D	11	D0	1D	10
11	10	D0	D1	00	D1	D1	11

Excitation table and K-maps

Present state y_2y_1	Flip-flop inputs						Output Z_1Z_0
	U=0			U=1			
	Y_2Y_1	J_2K_2	J_1K_1	Y_2Y_1	J_2K_2	J_1K_1	
00	11	1D	1D	01	0D	1D	00
01	00	0D	D1	10	1D	D1	01
10	01	D1	1D	11	D0	1D	10
11	10	D0	D1	00	D1	D1	11

u \ y_2y_1	00	01	11	10
0	1	D	D	1
1	1	D	D	1

$J_1=1$

u \ y_2y_1	00	01	11	10
0	D	1	1	D
1	D	1	1	D

$K_1=1$

Excitation table and K-maps

Present state y_2y_1	Flip-flop inputs						Output Z_1Z_0
	U=0			U=1			
	Y_2Y_1	J_2K_2	J_1K_1	Y_2Y_1	J_2K_2	J_1K_1	
00	11	1D	1D	01	0D	1D	00
01	00	0D	D1	10	1D	D1	01
10	01	D1	1D	11	D0	1D	10
11	10	D0	D1	00	D1	D1	11

u \ y_2y_1	00	01	11	10
0	1	0	D	D
1	0	1	D	D

$J_2 = (y_1 \oplus u)'$

u \ y_2y_1	00	01	11	10
0	D	D	0	1
1	D	D	1	0

$K_2 = (y_1 \oplus u)'$

Circuit diagram (JK flip-flop)