# EC3462 - LINEAR INTEGRATED CIRCUITS LABORATORY MANUAL

COURSE OBJECTIVES:

- To gain hands on experience in designing electronic circuits
- To learn simulation software used in circuit design
- To learn the fundamental principles of amplifier circuits
- To differentiate feedback amplifiers and oscillators.
- To differentiate the operation of various multivibrators

LIST OF EXPERIMENTS:

DESIGN AND ANALYSIS OF THE FOLLOWING CIRCUITS

1. Series and Shunt feedback amplifiers-Frequency response, Input and

output impedance

2. RC Phase shift oscillator and Wien Bridge Oscillator

3. Hartley Oscillator and Colpitts Oscillator

4. RC Integrator and Differentiator circuits using Op-Amp

5. Clippers and Clampers

6. Instrumentation amplifier

7. Active low-pass, High pass & Band pass filters

8. PLL Characteristics and its use as frequency multiplier, clock synchronization

9. R-2R ladder type D-A converter using Op-Amp

SIMULATION USING SPICE (Using Transistor):

1. Tuned Collector Oscillator

2. Twin -T Oscillator / Wein Bridge Oscillator

3. Double and Stagger tuned Amplifiers

4. Bistable Multivibrator

# VOLTAGE SHUNT FEEDBACK AMPLIFIER

**Exp.No:**

**Date:**

**AIM:**

To design and construct and test the voltage shunt feedback amplifier for the given specification and plot the frequency response.

**APPARATUS REQUIRED:**

| S.NO. | APPARATUS | RANGE | QUANTITY |
|---|---|---|---|
| 1. | Function Generator | 3MHz | 1 |
| 2. | Power Supply | (0-30)V | 1 |
| 3. | CRO | 30MHz | 1 |
| 4. | Transistor | BC107 | 1 |
| 5. | Resistor | 56KΩ | 1 |
| | | 12.2 KΩ | 1 |
| | | 10 KΩ | 1 |
| | | 5.6 KΩ | 1 |
| | | 2.2 KΩ | 1 |
| | | 470Ω | 1 |
| 6. | Capacitor | 47µF | 1 |
| | | 4.7 µF | 1 |
| | | 2 µF | 1 |
| 7. | Bread board | --- | 1 |
| 8. | Connecting wires | --- | As required |

**DESIGN:**

**GIVEN SPECIFICATION:**

$A_V$=50, S=20, $f_1$=100Hz, $f_2$=750 KHz, $R_L$=10KΩ, β=0.1, VCC=10V

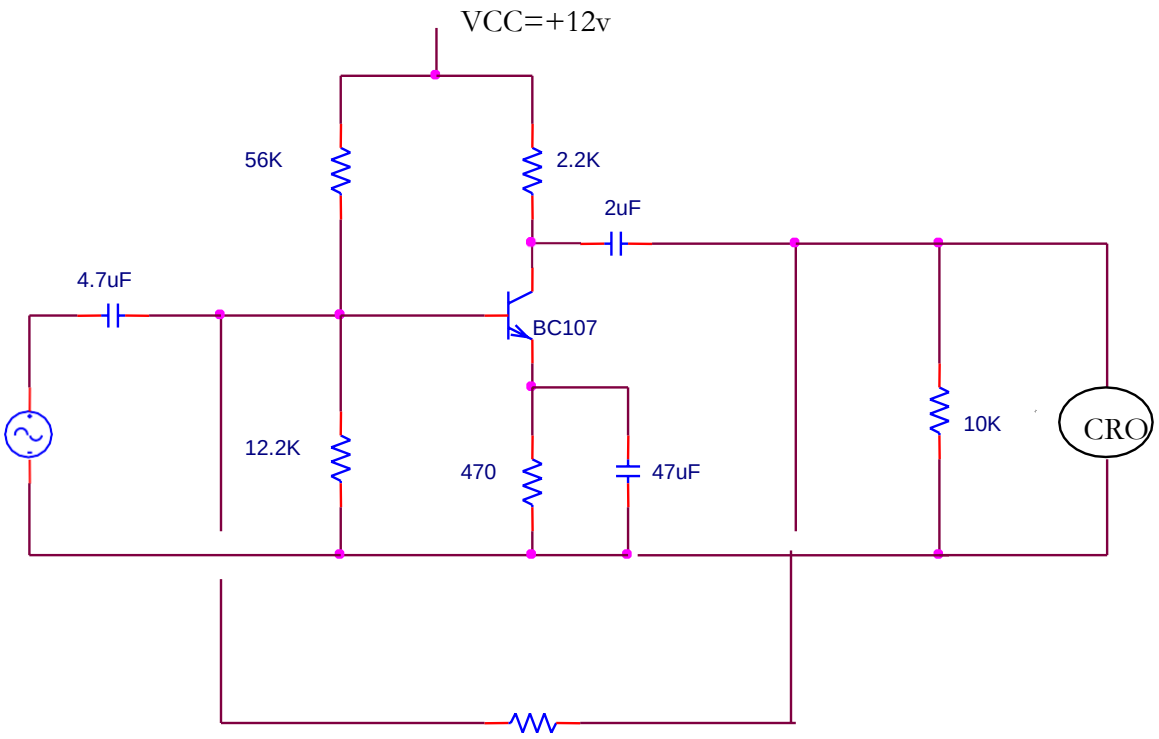
i.) Selection of Transistor:

$V_{cc} = 2V_{cc}$ and BC107 is selected.

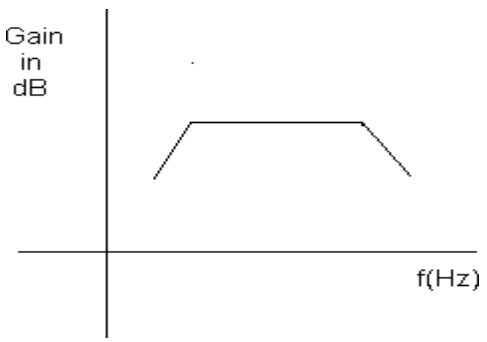
**CIRCUIT**

**DIAGRAM:**

VOLTAGE SHUNT FEEDBACK AMPLIFIER




**MODEL GRAPH:**



**THEORY:**

It is a transresistance amplifier with a Norton's equivalent in its circuit and a Thevenin's equivalent in its output circuit. In this output voltage is proportional to theinput signal current and the proportionality factor is independent on the source and load resistance and zero output resistance.

For practical transresistance amplifier $R_i << R_s$ and $R_o << R_L$. This feedback amplifier reduces the frequency distortion and noise and non-linear distortion. Also the gain withfeedback decreases.

Gain

$$R_{mf} = R_m / (1+ \beta Rm)$$

Input Resistance

$$R_{if} = R_i / (1+ \beta Rm)$$

Output Resistance

$$R_{of} = R_o / (1+ \beta Rm)$$

**PROCEDURE:**

- Circuit connections are given as per the circuit diagram.
- The input voltage is set to 2V.
- The output voltage is measured from the CRO for various frequencies.
- Gain is calculated.
- Frequency response curve is plotted and from the plot bandwidth is calculated.

**TABULATION:** $V_i$=

| S.No. | Frequency(Hz) | Output Voltage,$V_o$ | Gain= $V_o/V_i$ | Gain in dB $20\log(V_o/V_i)$ |
|---|---|---|---|---|
| | | | | |

**CALCULATION:**

$f_1$=

$f_2$=

Bandwidth= $f_2 - f_1$

= KHz

**VIVA VOCE QUESTIONS:**

1. What are the different types of feedback amplifier?
2. Why bandwidth is increased for feedback amplifier. Justify.
3. Mention the advantages of feedback amplifier.
4. Give the feedback factor and open loop gain for voltage shunt amplifier.
5. Tell the stability of feedback amplifier.
6. Define Gain and phase margin.
7. Why is negative feedback used in RC coupled amplifier?
8. What are the features of negative feedback?
9. What is Nyquist criterion?
10. A common collector amplifier circuit is an example of which negative feedback Circuit.

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the voltage shunt feedback amplifier was designed and the frequencyResponse was plotted. From the graph, $f_1$ & $f_2$ are noted.

Bandwidth= KHz

## CURRENT SERIES FEEDBACK AMPLIFIER

**Exp.No:**

**Date:**

**AIM:**

To design and construct and test the current series feedback amplifier for the givenspecification and plot the frequency response.

**APPARATUS REQUIRED:**

| S.NO. | APPARATUS | RANGE | QUANTITY |
|---|---|---|---|
| 1. | Function Generator | 3MHz | 1 |
| 2. | Power Supply | (0-30)V | 1 |
| 3. | CRO | 30MHz | 1 |
| 4. | Transistor | BC107 | 1 |
| 5. | Resistor | 56KΩ | 1 |
| | | 12.2 KΩ | 1 |
| | | 10 KΩ | 1 |
| | | 2.2 KΩ | 1 |
| | | 270Ω | 1 |
| | | 180Ω | 1 |
| 6. | Capacitor | 47µF | 1 |
| | | 4.7 µF | 1 |
| | | 2 µF | 1 |
| 7. | Bread board | --- | 1 |
| 8. | Connecting wires | --- | As required |

**DESIGN:**

**GIVEN SPECIFICATION:**

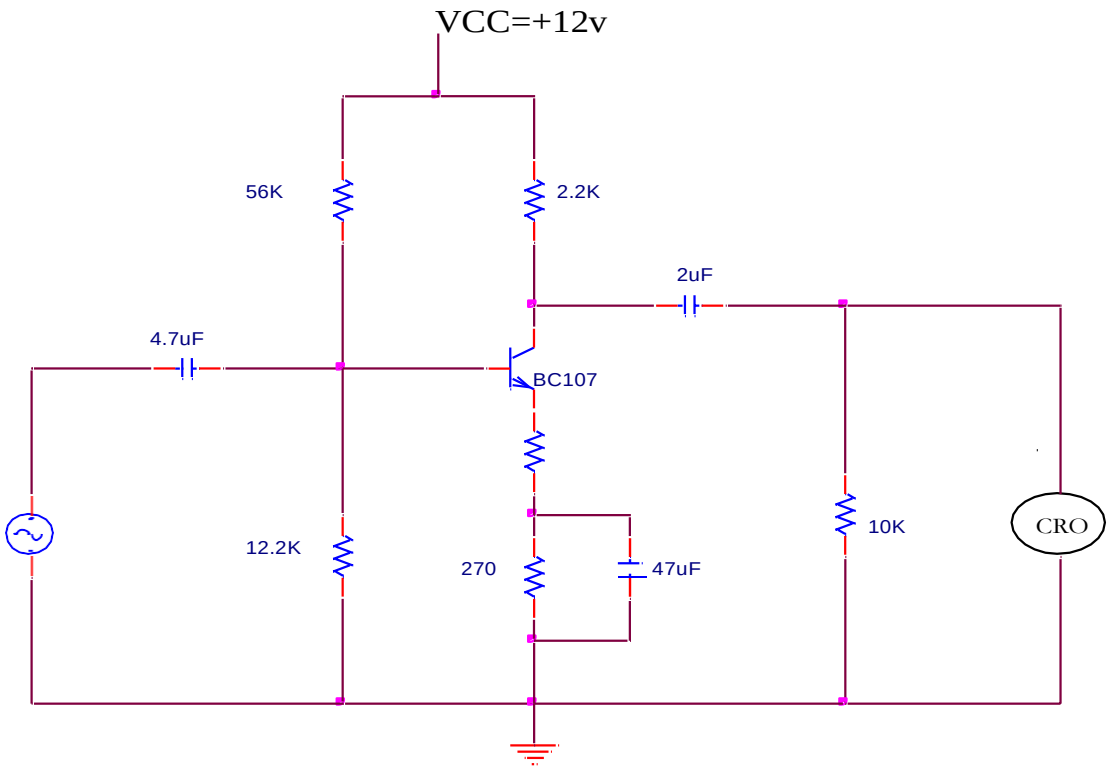
$A_V$=50, S=20, $f_1$=100Hz, $f_2$=750 KHz, $R_L$=10KΩ, β=0.1, VCC=10V

i. Selection of Transistor:

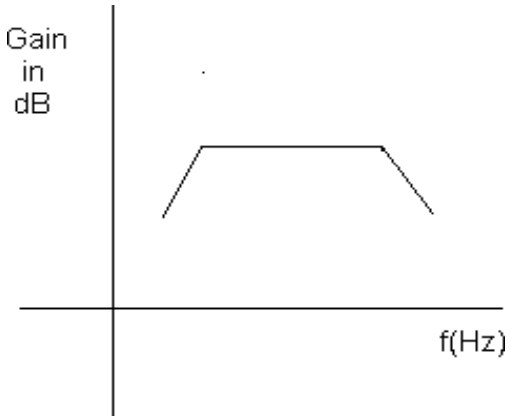
$V_{cc} = 2V_{cc}$ and BC107 is selected.

**CIRCUIT DIAGRAM:**

## CURRENT SERIES FEEDBACK AMPLIFIER




**MODEL GRAPH:**



**THEORY:**

The common emitter circuit with unbypassed $R_E$ is an example of current series feedback. In configuration, resistor $R_E$ is common to base and emitter input circuit so as well as collector to emitter output circuit and input current $I_b$ as well as output current $I_c$ both flow through The voltage drop across $R_E$, $V_E=(I_b+I_c)R_E=I_eR_E=I_cR_E=I_oR_E$.This voltage drop shows the output current.$I_o$ is being sampled and it is converted to voltage by feedback network at input side voltage $V_f$ is subtracted from Vo to perpendicular $V_i$.Therefore, feedback applied in series voltage feedback(current).

**PROCEDURE:**

- Circuit connections are given as per the circuit diagram.
- The input voltage is set to 2V.
- The output voltage is measured from the CRO for various frequencies.
- Gain is calculated.
- Frequency response curve is plotted and from the plot bandwidth is calculated.

TABULATION: $V_i$ =

| S.No. | Frequency(Hz) | Output Voltage,$V_o$ | Gain= $V_o/V_i$ | Gain in dB $20\log(V_o/V_i)$ |
|---|---|---|---|---|
| | | | | |

**CALCULATION:**

Bandwidth= $f_2 - f_1$

= KHz

**VIVA VOCE QUESTIONS:**

1. What is an amplifier?
2. Explain the basic concept of feedback.
3. Give the types of feedback.
4. Mention the terms feedback factor and open loop gain.
5. Compare the negative feedback and positive feedback.
6. Mention the applications of a feedback amplifier.
7. Differentiate positive feedback and negative feedback.
8. Give the features of negative feedback.
9. Why Current series amplifier is a Trans conductance amplifier?

   common – emitter circuit without By-pass capacitor is called a negative current feedback circuit. Justify?

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the current series feedback amplifier was designed and the frequency response was plotted. From the graph, $f_1$ & $f_2$ are noted.

Bandwidth= KHz

**Ex. No.:**

**Date:** ***PHASE SHIFT AND WEIN BRIDGE OSCILLATORS USING OP-AMP***

***Aim***

To construct and test RC Phase Shift and Wein bridge Oscillator using operational amplifier

***Apparatus Required***

1. IC 741
2. Power supply
3. Resistors
4. Capacitor
5. CRO
6. Breadboard
7. Connecting wires

**Theory**

An Oscillator is a type of feedback amplifier in which part of output is fed back to the input. The condition for sustained oscillation is $A_v\beta=1$.The types of waveform generated by an oscillator depend on thecomponents in the circuit and hence may be sinusoidal, or square or triangular.

***RC Phase Shift Oscillator***

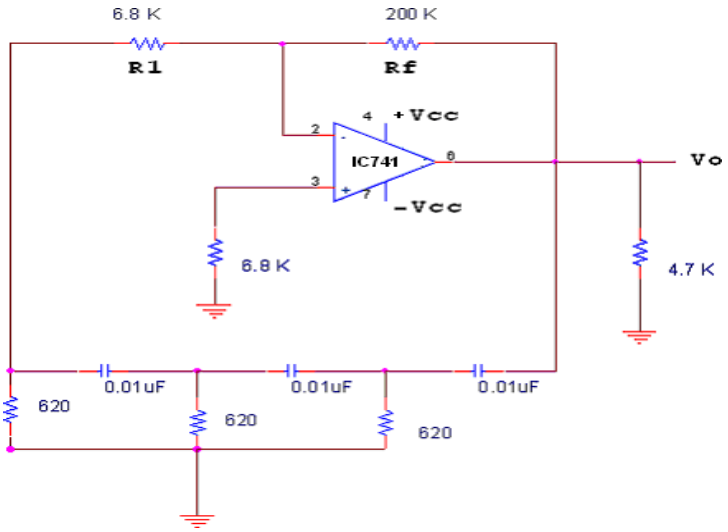
It consists of op-amp as amplifying stage and three RC cascaded networks as feedback circuit. The feedback circuit provides feedback voltage from the output to input of amplifier. The op-amp is used in the inverting mode and therefore provides a 180 degree phase shift to the signal at the inverting input terminal. The additional 180 degree phase shift is provided by cascaded RC networks. At some specific frequency when the phase shift of the cascaded RC networks is exactly 180 degree, the gain of the amplifier is sufficiently large and the circuit will oscillate at that frequency. This frequency of oscillation is given by $f_o$
$= 1/2\pi \sqrt{6}\, RC = 0.06/RC.$

***Procedure***

1. Connections are given as per circuit diagram
2. Connect the CRO probe to the output terminal of oscillator.
3. Check for polarity of supply voltage to op-amp.
4. Observe the output waveform on CRO and measure frequency and amplitude. Draw the outputwaveform.

***Circuit Diagram***

**RC Phase Shift oscillator**




Design

Frequency = 1 kHz ,Let C = 0.1

□F$f_o$ = 1 / ( 2 □ □6

RC)

= 0.06/ R C

Let R1 = 6.8 kΩ

$R_f$ = 29 $R_1$ = 6.8 * $10^3$ * 29

≈ 200 kΩ

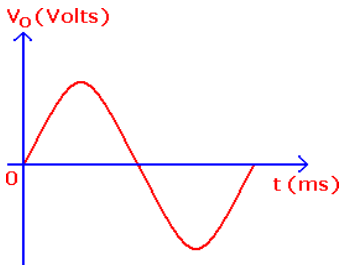
1000 = 0.06 / ( R * 0.1 * $10^{-6}$ )

R = 600 Ω (approx 620 Ω)

***Tabular Column:***

| Output voltage (volts) | Time period seconds | Observed Frequency(Hz) | obtained Frequency(Hz) |
|---|---|---|---|
| | | | |

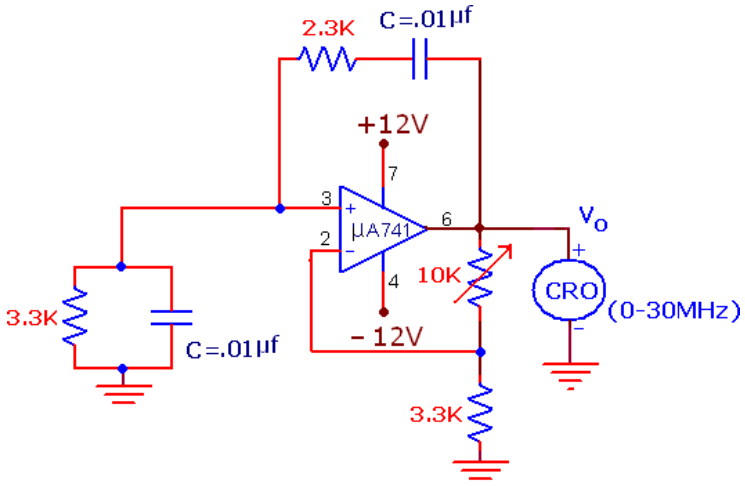
**MODEL GRAPH:**




***Wien Bridge Oscillator:***

A basic Wien bridge is used in this stage as amplifier. The output of amplifier is applied between terminal 1 and 3, which is input of feedback network. While amplifier input is applied from diagonal terminals 2 and 4, which is the output from the feedback network. Thus two arms of the bridge namely $R_1C_1$in series and $R_2C_2$ in parallel are called frequency sensitive arms. Because of components of these two arms decides the frequency of oscillation. Let us find out the gain of the feedback network. As seen earlier input $V_{in}$ to the feedback network is between 1 and 3 while output $V_f$ of the feedback network is between 2 and 4. Such a feedback network called lead-lag network. This is because at very low frequency it acts like a lead while at very high frequency it acts like a lag. Another important advantage of Wien bridge oscillator on varying the two capacitors simultaneously by mounting them on the common shaft, different frequency range can be provided. To satisfy Barkhausen criterion that $A\beta \geq 1$. It is necessary that the gain of the non inverting op-amp amplifier must be minimum 3.

***CIRCUIT DIAGRAM FOR WIEN BRIDGE OSCILLATOR:***




WIEN BRIDGE OSCILLATOR USING OP-AMP

**DESIGN:**

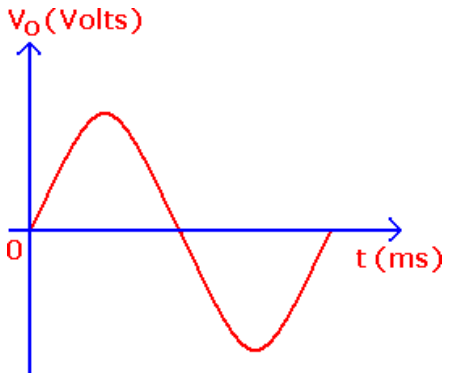
f = 5 KHz, $R_f$ = 10K, $R_1$=3.3K and C = 0.01μf (Std. Value)

$$f = \frac{1}{2\pi R C} \quad \square \quad R = \frac{1}{2\pi f C} = 3.2K \text{ (Use Std. Value 3.3K)}$$

***TABULAR COLUMN:***

| S.No | Output Voltage ($V_O$) in Volts | Time in ms | Designed Frequency | Observed Frequency |
|---|---|---|---|---|
| | | | | |

**MODEL GRAPH:**




***PROCEDURE:***

1. Make the connections as per the circuit diagram.
2. Supply Voltage is set as 12V using Dual power supply.
3. Calculate output voltage and time (ms) for both RC phase shift oscillator and Wien bridge oscillator.
4. Draw the graph between output voltage and time.

***VIVA QUESTIONS:***

1. State the two conditions for oscillator.
2. What is barkhausen criterion?
3. What is damped oscillation?
4. What are the applications of wein bridge oscillator.
5. What is the formula for RC-phase shift oscillator?
6. What is the formula for Wein Bridge oscillator oscillator?

***RESULT:***

Thus the RC phase shift oscillator and Wien bridge oscillator using operational were designed, constructed and performance was verified.

***Ex. No.:***

**Date:** **HARTLEY OSCILLATOR**

**AIM:**

To design and construct and test the Hartley oscillator for the given specification and plot the output waveform.

**APPARATUS REQUIRED:**

| S.NO. | APPARATUS | RANGE | QUANTITY |
|---|---|---|---|
| 1. | Power Supply | (0-30)V | 1 |
| 2. | CRO | 30MHz | 1 |
| 3. | Transistor | 2N3666<br>Or<br>BC107 | 1 |
| 4. | Resistor | 56KΩ | 1 |
| | | 12.2 KΩ | 1 |
| | | 2.2 KΩ | 1 |
| | | 470Ω | 1 |
| 5. | Capacitor | 100µF | 1 |
| | | 0.1 µF | 2 |
| | | 100pF | 1 |
| 6. | Decade Inductance Box | (0 mH – 1H) | 2 |
| 7. | Bread board | --- | 1 |
| 8. | Connecting wires | --- | As required |

**DESIGN:**

**GIVEN SPECIFICATION:**

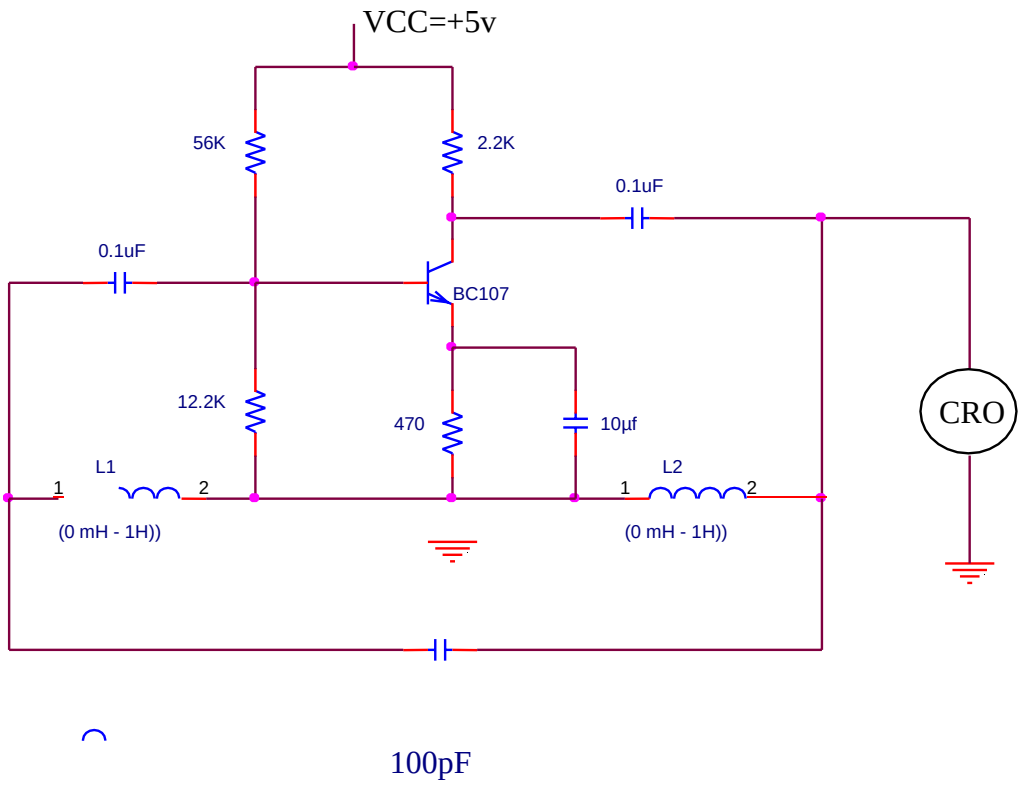
$A_V$=50, S=20, $f_o$=150 KHz, β=0.1, VCC=10V

i.) Selection of Transistor:

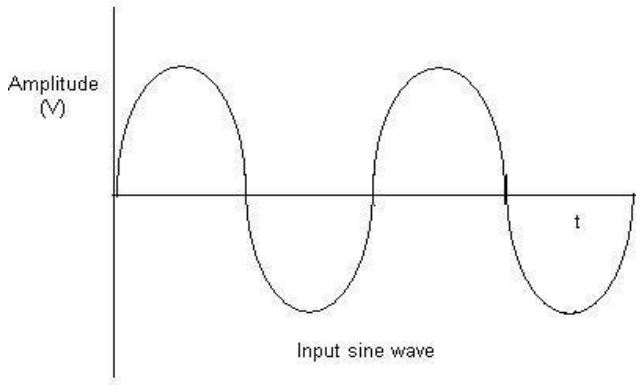
BC107 is selected.

**CIRCUIT DIAGRAM:**

HARTLEY OSCILLATOR




**MODEL GRAPH:**



**TABULATION:**

| Output waveform | Amplitude(V) | Time period(μs) |
|---|---|---|
| | | |

**CALCULATION:**

Obtained frequency of oscillation, $f_o = 1 / T$

= MHz

**THEORY:**

A LC oscillator which uses two inductive reactances and one capacitive reactance in its feedback network is Hartley oscillator. The amplifier stage uses transistor as an active device in common emitter configuration. The resistances R1&R2 are the biasing resistances. The RFC is the radio frequency choke. Its reactance value is very high frequencies, hence it can be treated as open circuit while for dc conditions, the reactanceis zero hence causes no problem for dc capacitors.

Frequency of oscillation for the Hartley oscillator is given by, $f_o = 1/$

$[2\pi\sqrt{(LeqC)}]$

=

**PROCEDURE:**

- Circuit connections are given as per the circuit diagram.
- Power supply is given to the circuit.
- Amplitude and Time period of the output waveform is noted from the CRO
- Frequency of oscillation is calculated.
- Output waveform is plotted in the graph.

**VIVA VOCE QUESTIONS:**

1. What is LC oscillator?
2. Give the difference between RC & LC oscillator.
3. How much amount of feedback obtained by the feedback loop?
4. Define damped Oscillations.
5. What are the feedback components present in LC oscillators?

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the Hartley oscillator is designed and tested and the time response was plotted.

Designed frequency of oscillation= 150 MHz

Obtained frequency of oscillation= MHz

# COLPITT'S OSCILLATOR

**AIM:**

To design and construct and test the Colpitt's oscillator for the given specification and plot the output waveform.

**APPARATUS REQUIRED:**

| S.NO. | APPARATUS | RANGE | QUANTITY |
|---|---|---|---|
| 1. | Power Supply | (0-30)V | 1 |
| 2. | CRO | 30MHz | 1 |
| 3. | Transistor | 2N3666<br>Or<br>BC107 | 1 |
| 4. | Resistor | 56KΩ | 1 |
| | | 12.2 KΩ | 1 |
| | | 2.2 KΩ | 1 |
| | | 470Ω | 1 |
| 5. | Capacitor | 10μF | 1 |
| | | 0.1 μF | 1 |
| | | 100pF | 2 |
| 6. | Decade Inductance Box | (0 mH – 1H) | 1 |
| 7. | Bread board | --- | 1 |
| 8. | Connecting wires | --- | As required |

**DESIGN:**

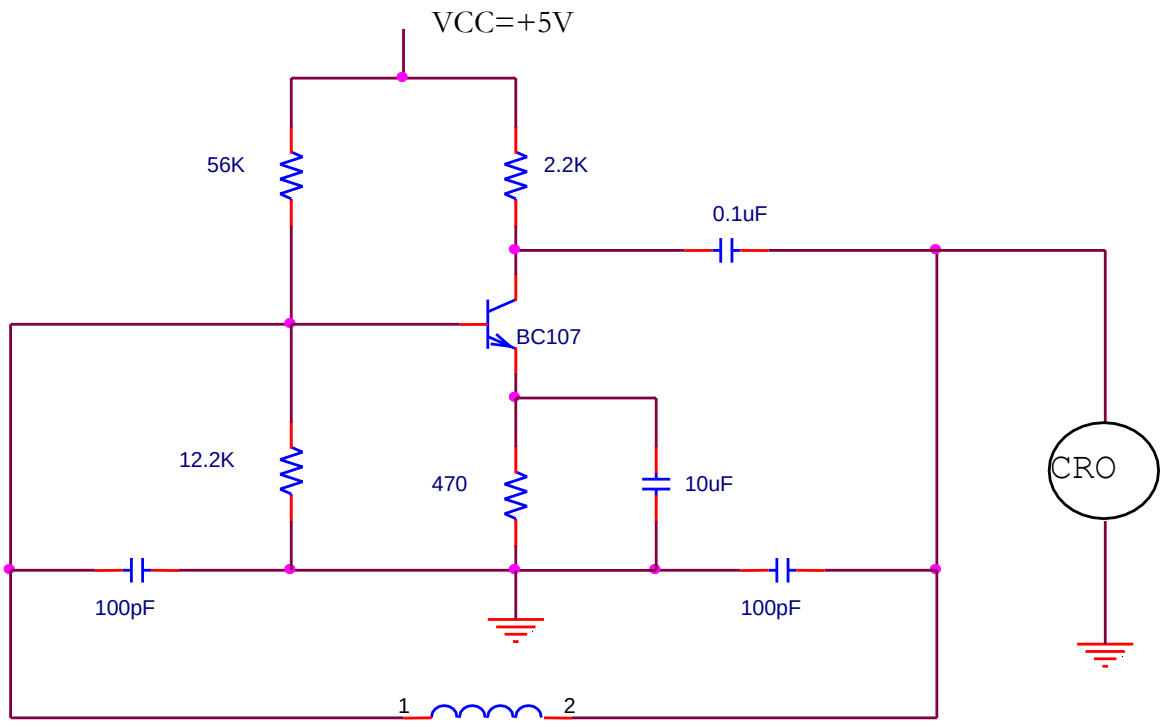
**GIVEN SPECIFICATION:**

$A_V$=50, S=20, $f_o$=150 KHz, β=0.1, VCC=10V

i.) Selection of Transistor:

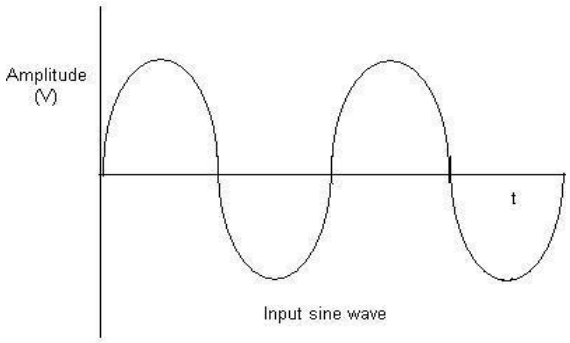
BC107 is selected.

**CIRCUIT DIAGRAM:**




(0 mH - 1 H)

**MODEL GRAPH**



**TABULATION:**

| Output waveform | Amplitude(V) | Time period(μs) |
|---|---|---|
| | | |

**CALCULATION:**

Obtained frequency of oscillation, $f_o = 1 / T$

= MHz

**THEORY:**

A LC oscillator which uses two inductive reactances and one capacitive reactance in its feedback network is Colpitt's oscillator. The amplifier stage uses transistor as an active device in common emitter configuration. The resistances R1&R2 are the biasing resistances. The RFC is the radio frequency choke. Its reactance value is very high frequencies, hence it can be treated as open circuit while for dc conditions, the reactance is zero hence causes no problem for dc capacitors.

Frequency of oscillation for the Colpitt's oscillator is given by, $f_o = 1/$

$[2\pi\sqrt{(CeqL)}]$

=

**PROCEDURE:**

- Circuit connections are given as per the circuit diagram.
- Power supply is given to the circuit.
- Amplitude and Time period of the output waveform is noted from the CRO
- Frequency of oscillation is calculated.
- Output waveform is plotted in the graph.

**VIVA VOCE QUESTIONS:**

1. Differentiate Colpitts & Hartley oscillator.
2. Mention the frequency range of LC oscillators.
3. Which type of oscillator is suitable for Radio frequency range applications?
4. Give the types of low frequency and high frequency oscillators.5 .

Which oscillator is suitable for RF range applications?

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the Colpitts oscillator is designed and tested and the time response wasplotted.

Designed frequency of oscillation= 100 MHz

Obtained frequency of oscillation= MHz

# INTEGRATOR AND DIFFERENTIATOR

***Aim***

To design, construct & test the performance of Integrator and Differentiator.

***Apparatus Required***

1. IC 741
2. Power supply
3. Resistors
4. Capacitor
5. Function generator
6. CRO
7. Bread board & Connecting wires

**Theory**

**Integrator**

The circuit performs the mathematical operation of Integration, that is, the output waveform is the integral of input waveform.

$$V_0(t) = -1/R_1C_f \int V_i(t)\,dt + V_0(0)$$

$V_0(0)$ = initial output voltage

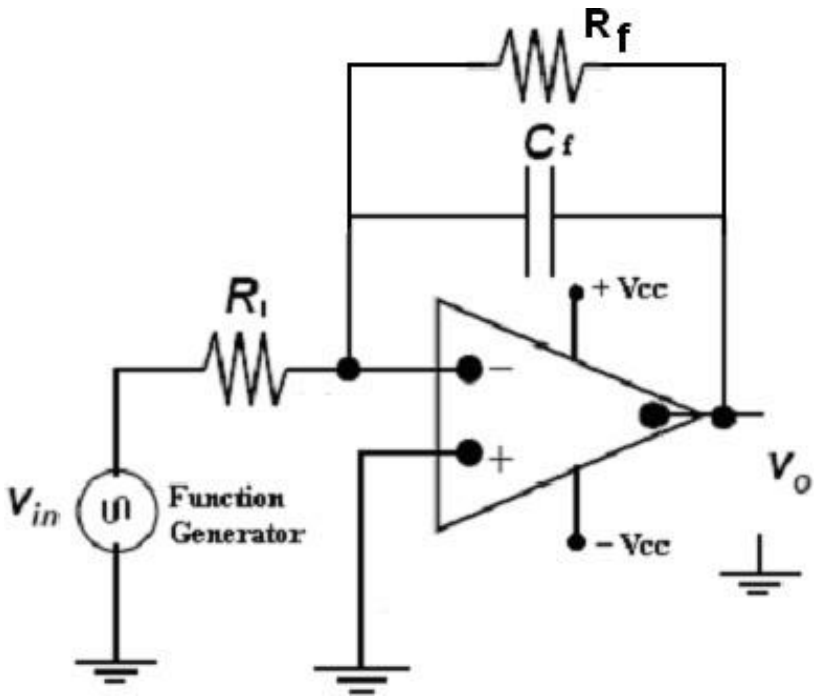
**Differentiator**

The circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform.

$$V_0 = -R_f C_1 \, dV_i / dt$$

**Integrator**

**Circuit diagram**




***Design Procedure***

$f_1 = 1/ (2\pi R_1 C_f)$

$C_f = 0.01\ \mu F$; $R_1 =$

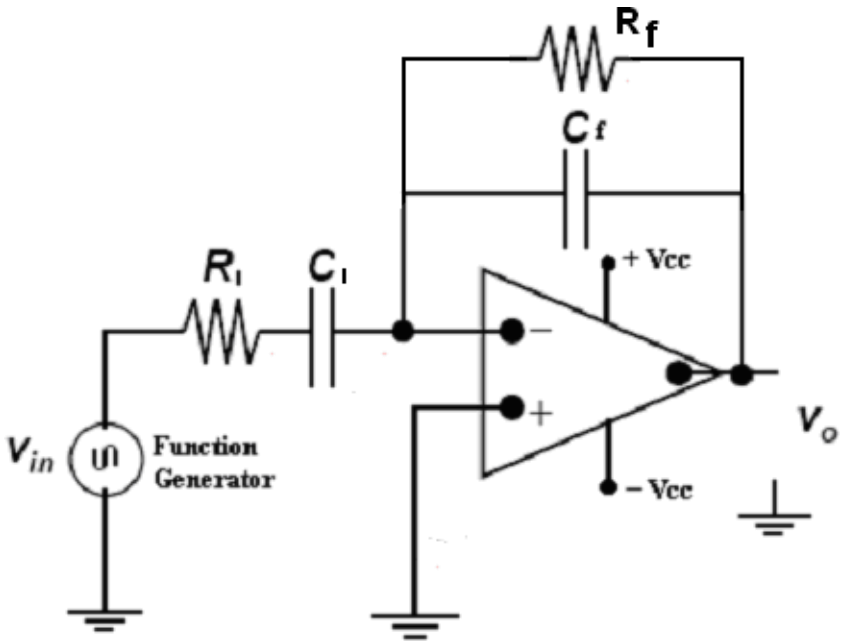
$R_f = 10\ R_1$; $R_f =$

**Tabulation**

| Input voltage $V_{in}$ (volt) | Input Frequency fi (Hz) | Output voltage Vo (volt) | Output Frequency fo (Hz) |
|---|---|---|---|
| Square Wave i/p | | | |
| Sine Wave i/p | | | |

**Differentiator**

**Circuit diagram**



***Design Procedure***

$V_0 = -R_f C_1 \, dVi/dt$

Max. input frequency, $f_a = 1/ (2\pi R_f C_1) = 1$ KHz

$C_1 = 0.01$ μF; $R_f$ =

$f_b = 10 f_a = 10$ kHz

$f_b = 1/ (2\pi R_1 C_1)$; $R_1$ =

$R_f C_f = R_1 C_1$; $C_f$ =

**Tabulation**

| Input voltage $V_{in}$ (volt) | Input Frequency $f_i$ (Hz) | Output voltageVo (volt) | Output frequency $f_o$ (Hz) | Phase Difference |
|---|---|---|---|---|
| | | | | |

Theoretical value of $f_1$ =

Practical value of $f_1$ =

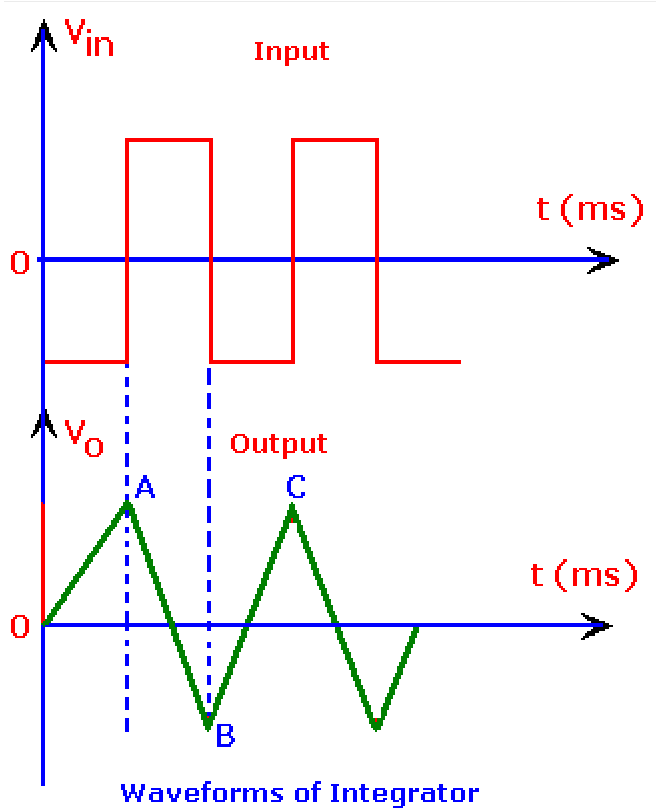
## Procedure

### Integrator

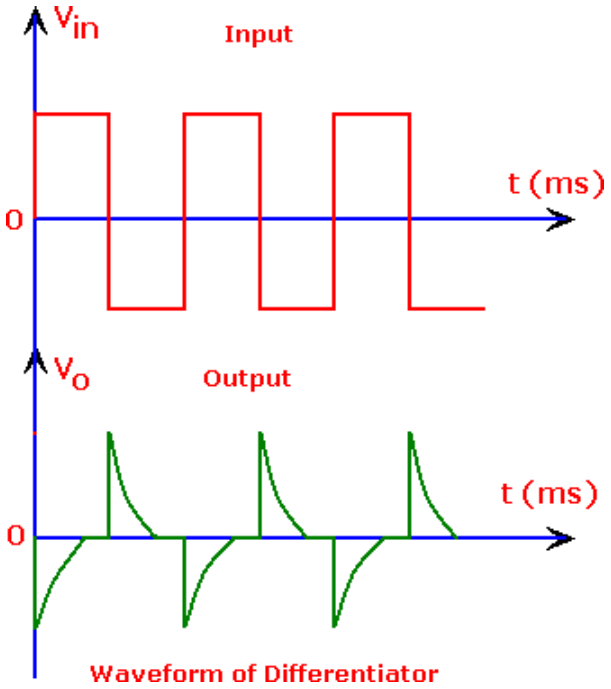
1. Connect the integrator circuit as shown in Fig. Set the function generator to produce a square wave of 1V peak – to – peak amplitude at 500 Hz. View simultaneously output Vo and input Vi.
2. Slowly adjust the input frequency until the output is a good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.
3. Now set the function generator to a sine wave of 1v peak – to – peak and frequency 500 Hz. Adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

### Differentiator

1. Connect the differentiator circuit shown in fig. Adjust the signal generator to produce a 5 volt peak sine wave at 100 Hz.
2. Observe input Vi and output Vo simultaneously on the oscilloscope. Measure and record the peak value of Vo and the phase angle of Vo with respect to Vi.
3. Repeat step 2 while increasing the frequency of the input signal. Find the maximum frequency at which the circuit performs differentiation. Compare it with the calculated value of $f_1$.


Vin
Input
t (ms)
0
Vo
Output
A
C
t (ms)
0
B
Waveforms of Integrator

**Model Graph:**


Vin
Input
t (ms)
0
Vo
Output
t (ms)
0
Waveform of Differentiator

**VIVA QUESTIONS.**

1. Define an integrator.
2. State the applications of an integrator.
3. What is a differentiator?
4. What are the steps to design a differentiator?
5. What are the steps to design an integrator?

**Result**

Thus the applications of operational amplifier such as integrator and differentiator are constructed and tested.

## CLIPPER AND CLAMPER

**Exp.No:**

**Date:**

**AIM:**

To construct clipper and clamper circuits and plot the output waveform.

**APPARATUS REQUIRED:**

| S.NO. | APPARATUS | RANGE | QUANTITY |
|---|---|---|---|
| 1. | Function Generator | 3MHz | 1 |
| 2. | CRO | 30MHz | 1 |
| 3. | Diode | IN4148 | 1 |
| 4. | Resistor | 6.8KΩ | 1 |
| | | 10 KΩ | 1 |
| 5. | Capacitor | 1μF | 1 |
| 6. | Bread board | --- | 1 |
| 7. | Connecting wires | --- | As required |

**THEORY:**

**CLIPPER:**

The circuits which are used to clip off unwanted portion of the waveform without distorting the remaining part of the waveform are called clippers. The half wave rectifier is the best and simplest type of clipper circuit.

There are two types of clippers:

- Positive clipper
- Negative clipper

**POSITIVE CLIPPER**

A clipper which clips off the positive part of the input is called positive clipper. For positive half cycle of input $V_1 > 0V$, and diode is reverse biased. Hence it acts as a open circuit and $V_o=0$.

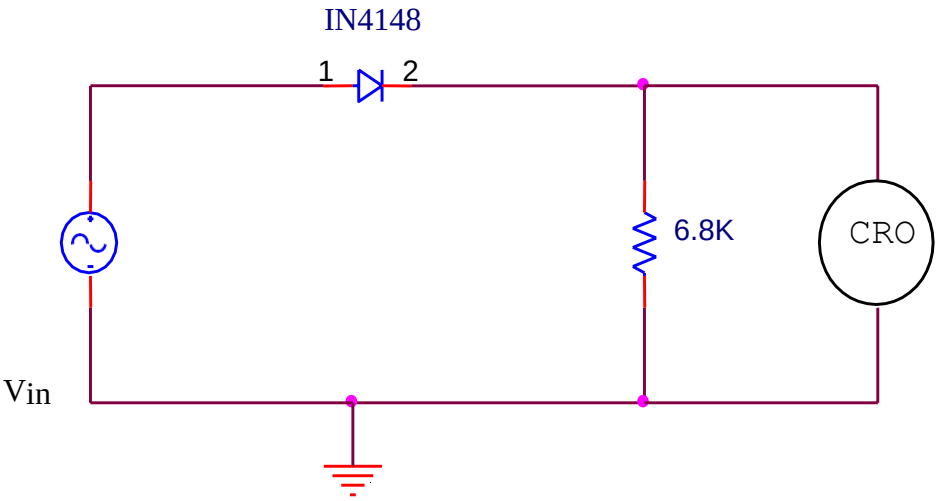
For negative half cycle of input, $V_1 < 0V$ and diode conducts. Assuming ideal diode and the output voltage is same as the input voltage. Thus entire negative half cycle is available at the output.

**NEGATIVE CLIPPER**

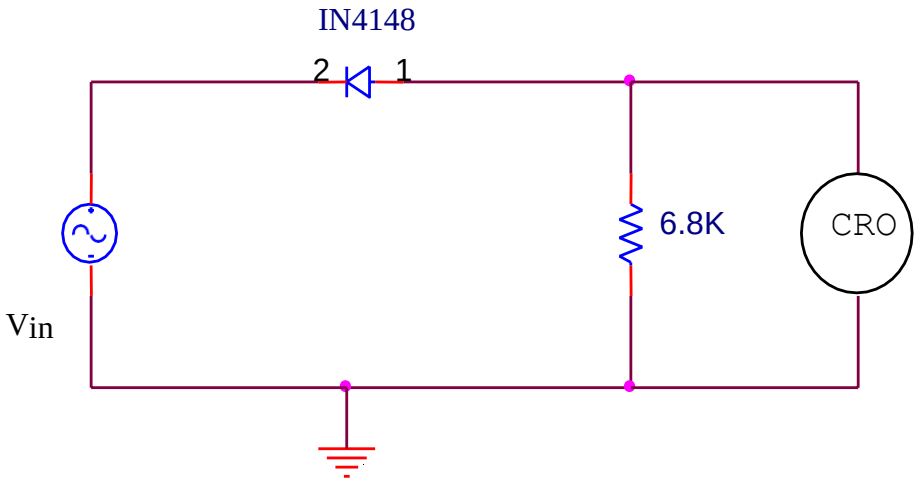
A clipper which clips off the negative part of input is called the negative clipper. For positive half cycle $V_1 > 0V$ and diode conduct. Assuming ideal diode the output is same as the input voltage. Thus entire positive half cycle is available at the output.

CIRCUIT DIAGRAM:

NEGATIVE CLIPPER

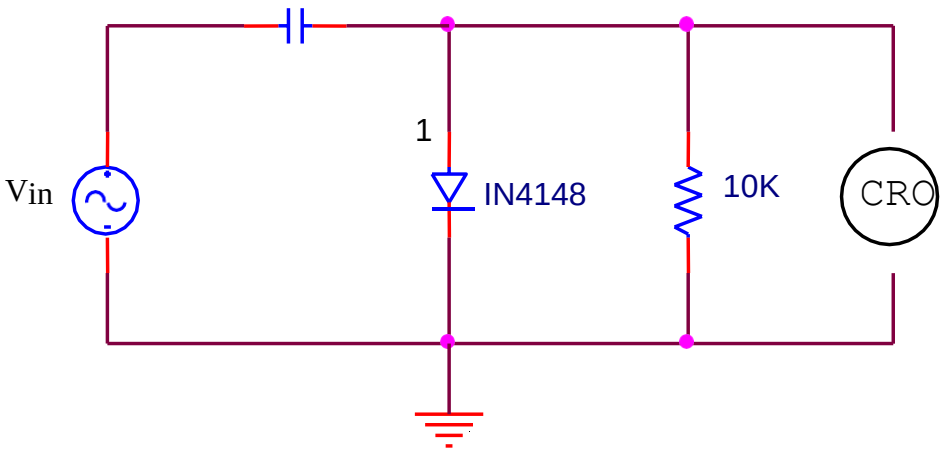



POSITIVE CLIPPER



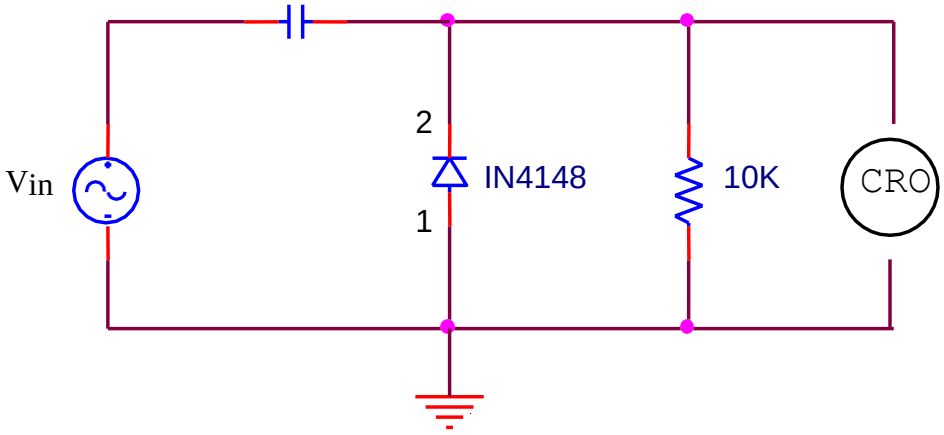
NEGATIVE CLAMPER

1uF

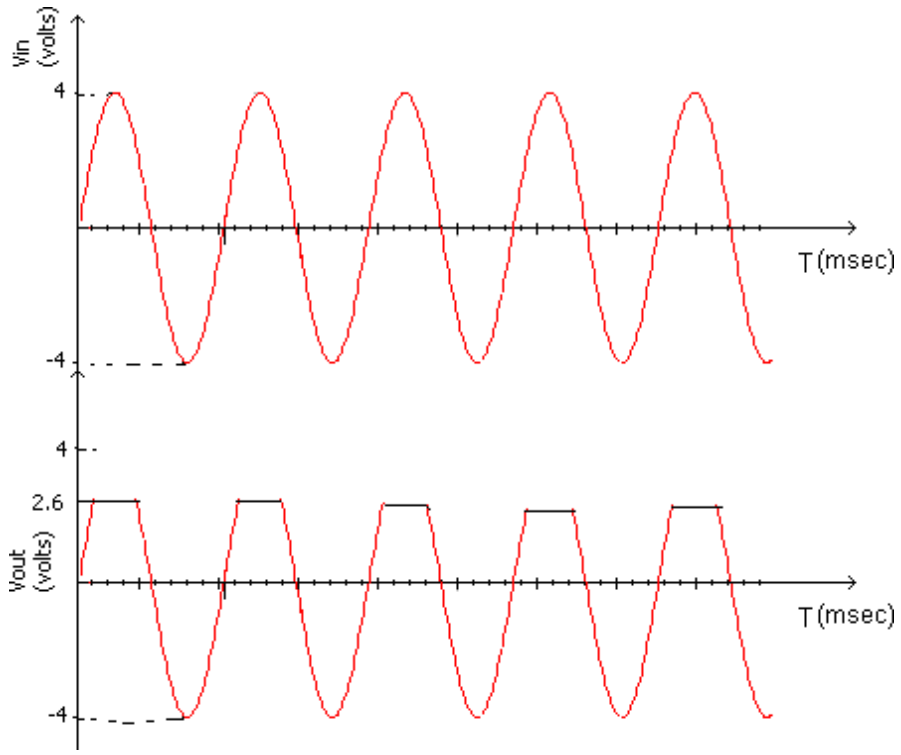



POSITIVE CLAMPER

1uF



**MODEL GRAPH:**



**CLAMPERS:**

The circuits which are used to add a dc level as per the requirements to the ac output signal is called the clamper circuits. The basic elements of the clamper circuits arediode, capacitor and resistor. This clamper circuit is also called as the dc restorer or dc inserter circuits

By changing the orientation of the diode in negative clamper, the positive clamper is achieved.

$V_o=V_m$ for $V_i=0$

$V_o=2V_m$ for $V_i=V_m$

$V_o=0$ for $V_i=0$

**PROCEDURE:**

- Circuit connections are given as per the circuit diagram.
- Input is given to the circuit and the output for the clipper and clamper is noted inthe CRO.
- Output waveform is plotted in the graph.

**TABULATION:**

**CLIPPER**

**NEGATIVE CLIPPER**

| waveform | Amplitude(V) | Time period(ms) |
|---|---|---|
| | | |
| | | |

**POSITIVE CLIPPER**

| waveform | Amplitude(V) | Time period(ms) |
|---|---|---|
| | | |
| | | |

**CLAMPER:**

**NEGATIVE CLAMPER**

| waveform | Amplitude(V) | Time period(ms) |
|---|---|---|
| | | |
| | | |

**POSITIVE CLAMPER**

| waveform | Amplitude(V) | Time period(ms) |
|---|---|---|
| | | |
| | | |

**VIVA VOCE QUESTIONS:**

1. What is a linear waveform-shaping circuit?
2. Define clipper.
3. Define clamper.
4. What are the other names of clipper circuit?
5. Define wave shaping circuit.
6. Differentiate clipper and clamper.
7. How does a clamper circuit adds a dc level to the output voltage?
8. Mention the types of clampers.
9. What is biased clipper?
10. What are the classifications of a clipper circuit?

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the clipper and clamper circuits have been constructed and the outputwas verified successfully

# *INSTRUMENTATION AMPLIFIER*

## Aim

To construct and verify the operation of an instrumentation amplifier using OP-AMP IC 741.

- To find out CMRR.
- To find out the output voltage under common mode and differential mode.

## *Apparatus Required*

- Operational amplifier
- Power Supply
- Signal Generator
- Decade Resistance
- Resistor
- CRO

## *Theory*

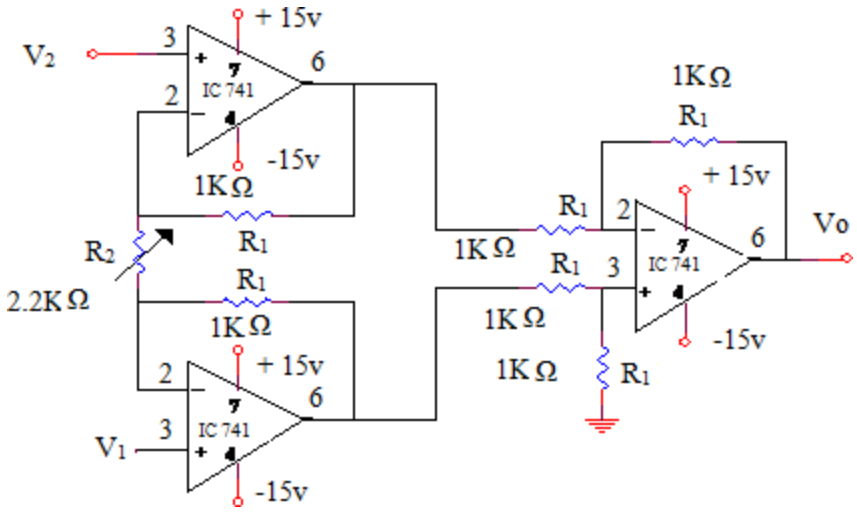
In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

## *Features of instrumentation amplifier*

- High gain accuracy
- High CMRR
- High gain stability with low temperature co-efficient

- Low DC offset
- Low output impedance
- **Formulae**

***CIRCUIT DIAGRAM OF INSTRUMENTATION AMPLIFIER***



| S.No | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_1$ (v) | $V_2$ (v) | $V_0$ (v) | | $V_1$ (v) | $V_2$ (v) | $V_0$ (v) | | |
| | | | | | | | | | | |

***Procedure***

1. Make connections as shown in figure.
2. Check the polarity of connection.
3. For different modes of operation the voltage $V_2$ is obtained by using a potential divider circuit.
4. The input voltage is set.
5. By varying the resistance value $R_1$ the output voltage is obtained for both common mode anddifferential mode of operation.
6. The CMRR is calculated using the formula.

**VIVA QUESTIONS:**

1. What are the features of instrumentation amplifier?
2. What are the applications of instrumentation amplifier?
3. What is an instrumentation amplifier?
4. Write the expression for output voltage.
5. What is the use of transducer in an instrumentation amplifier?

***Result***

Thus the instrumentation amplifier was constructed using OP-AMP IC741 and its operation was studied.

## ACTIVE LOW PASS, HIGH PASS BAND PASS FILTERS USING OP-AMP

### AIM

To design, construct and obtain the frequency response of active Low pass, High pass and Bandpass filter using operational amplifiers.

### COMPONENTS REQUIRED:

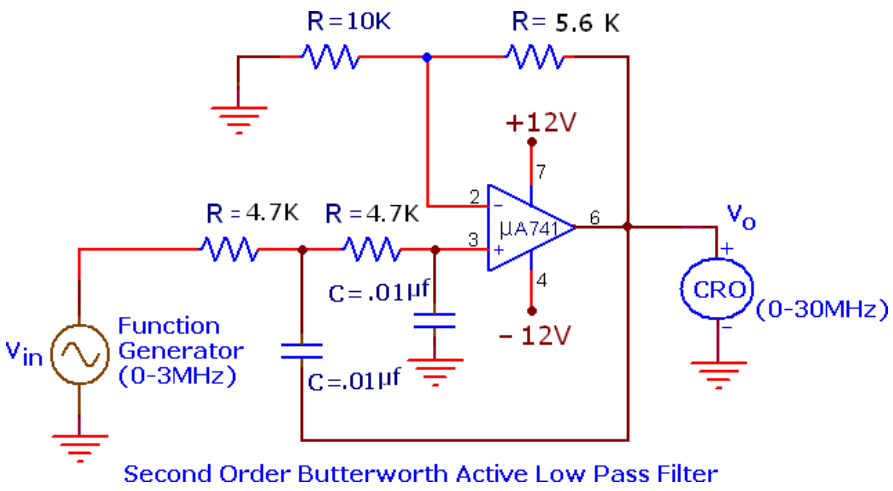
- Operational amplifier
- Power Supply
- Signal Generator
- Capacitor
- Resistor
- CRO
- Breadboard

### THEORY:

### Low Pass Filter:

The practical response of the filter must be very close to an ideal one. In case of low pass filter, it is always desirable that the gain rolls off very fast after the cut off frequency, in the stop band. In case of first order filter, it rolls off at a rate of 20 dB/ decade. In case of second order filter the gain rolls of at a rate of 40dB / decade. Thus the slope of the frequency response after $f=f_H$ is -40dB / decade, for a second order low pass filter. The first order filter can be converted to second order type by using an additional RC network. The gain of the second order filter is determined by $R_1$ and $R_f$. The $f_H$ is designed by$R_2$, $C_2$, $R_3$, and $C_3$ as follows.

## CIRCUIT DIAGRAM FOR BUTTERWORTH ACTIVE LOW PASS FILTER:




## DESIGN OF LOW PASS FILTER:

1. Select $f_H$ = 3 KHz
2. Set $R_2 = R_3 = R$ and $C_2 = C_3 = C = 0.01\mu f$ ($C$ is always $\leq 1\mu f$).
3. Calculate R from $f_H = 1 / 2\prod RC$

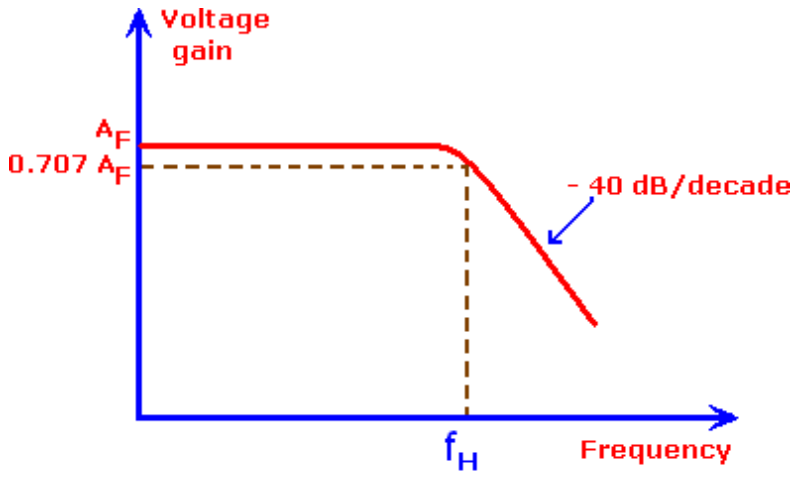
   $R = 1 / 2\prod f_H C = 5.3\ K\Omega = R_2 = R_3$ (* Choose standard resistor value 4.7 KΩ*)

4. For Butterworth response $A = 1 + \frac{R_f}{R_1} = 1.586$ ; $R_f = (1.586 - 1) R$

   F $\frac{f}{R}$ 1

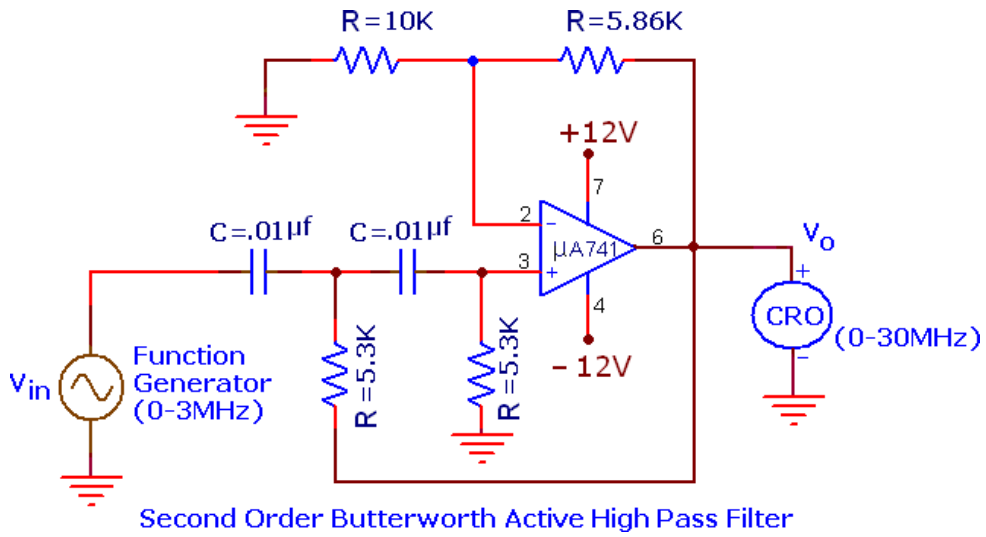
5. Choose $R_1$=10 KΩ then $R_f$ = 5.86 KΩ (* Choose standard resistor value 5.6 KΩ*)

**MODEL GRAPH:**




SECOND ORDER ACTIVE LOW PASS FILTER

***CIRCUIT DIAGRAM FOR 2[ND] ORDER BUTTERWORTH ACTIVE HIGH PASS FILTER:***




Second Order Butterworth Active High Pass Filter

**DESIGN OF HIGH PASS FILTER:**

1. Select $f_L$ = 3 KHz
2. Set $R_2 = R_3 = R$ and $C_2 = C_3 = C = 0.01\mu f$ ($C$ is always $\leq 1\mu f$).
3. Calculate R from $f_L = 1 / 2\prod RC$

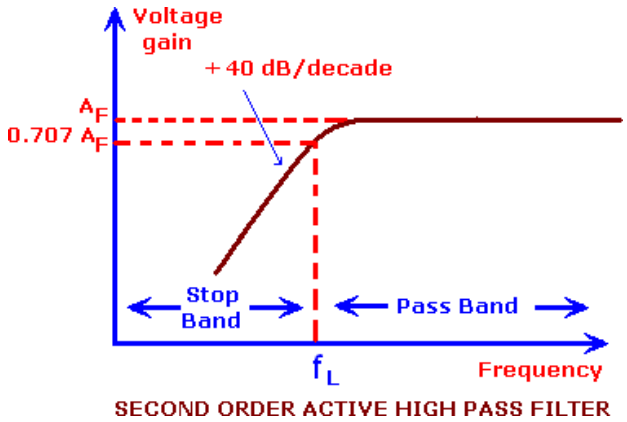
$$R = 1 / 2\prod f_L C = 5.3K\Omega = R_2 = R_3$$

4. For Butterworth response $A = 1 + \frac{R_f}{R_1} = 1.586$ ; $R_f = (1.586 - 1) R_1$

$$F = \frac{f}{f_H}$$

5. Choose $R_1$=10 KΩ then $R_f$ = 5.86 KΩ

***MODEL GRAPH:***




SECOND ORDER ACTIVE HIGH PASS FILTER

***High Pass Filter:***

A second order high pass filter can be obtained from a second order low pass filter simply by interchanging the frequency determining resistors and capacitors. The Voltage gain magnitude of the second order high pass filter is given by

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left[\frac{f_L}{f}\right]^4}}$$

Where $A_F = 1.586$ – Pass band gain; $f_L$ = Low cutoff frequency and f= frequency of the input signal

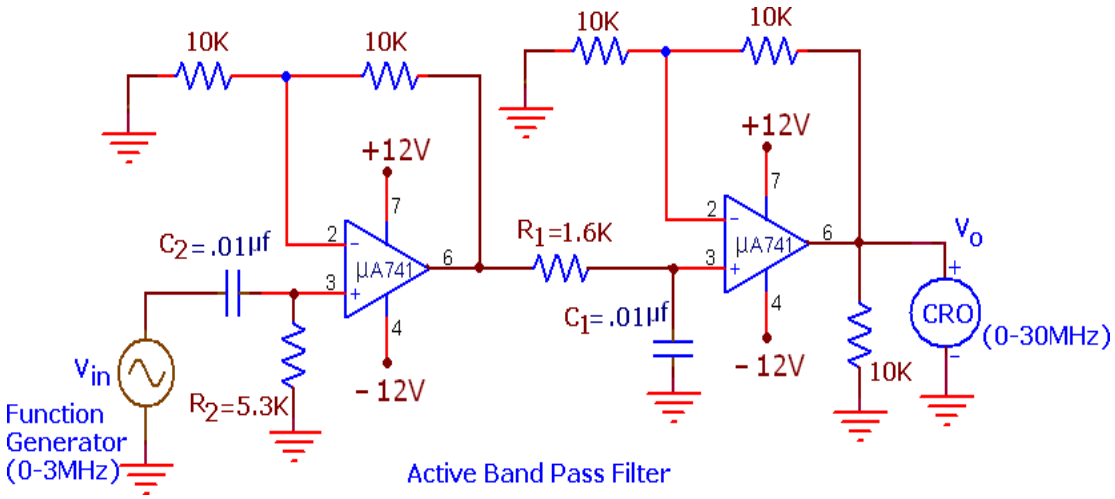
$$f_L = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

Since second order low pass and high pass filters are alike except that the positions of resistors and capacitors are being interchanged, the design and frequency scaling procedures are same for high pass filter as those for the low pass filter.

**Band Pass Filter:**

- A band pass filter is basically a frequency selector. It allows one particular band of frequencies topass.
- Thus the, the pass band is between the two cut-off frequencies fH and Fl
- Where $f_H > f_L$ any frequency outside this band gets attenuated. BW = fH-fL

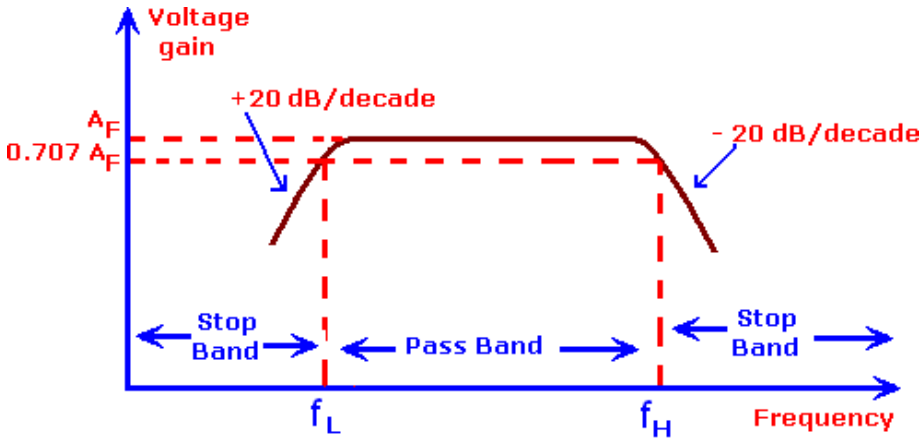
***CIRCUIT DIAGRAM FOR BUTTERWORTH WIDE BAND PASS FILTER:***




**DESIGN OF WIDE BAND PASS FILTER:**

1. Select $f_L$ = 3 KHz and $f_H$ = 10 KHz.
2. Choose $C_1 = C_2 = 0.01\mu f$.
3. $f_L = 1 / 2\prod R_2 C_2$ then $R_2 = 1 / 2\prod f_L C_2 = 5.3K\Omega$
4. $f_H = 1 / 2\prod R_1 C_1$ then $R_1 = 1 / 2\prod f_H C_1 = 1.6K\Omega$
5. Band Width= $f_H - f_L$

***MODEL GRAPH:***




SECOND ORDER ACTIVE BAND PASS FILTER

**PROCEDURE: LOW PASS FILTER**

1. Make the connections as per the circuit diagram.
2. Vary the frequency of input signal and note the corresponding output voltage.
3. Calculate the gain and draw the graph.
4. Find the Higher cut off frequency.

***PROCEDURE: HIGH PASS FILTER***

1. Make the connections as per the circuit diagram.
2. Vary the frequency of input signal and note the corresponding output voltage.
3. Calculate the gain and draw the graph.
4. Find the lower cut off frequency.

***PROCEDURE: BAND PASS FILTER***

1. Make the connections as per the circuit diagram.
2. The input voltage is set to the constant value say 2V.
3. Vary the frequency of input signal and note the corresponding output voltage.
4. Calculate the gain and draw the graph.
5. Find the Low and High cut off frequencies.

**TABULAR COLUMN: LOW PASS FILTER:**

**$V_{in}$ =**

| S.No | Frequency in Hz | Output Voltage ($V_O$)in Volts | Gain = 20 log($V_O/V_{in}$) dB. |
|---|---|---|---|
| | | | |

***TABULAR COLUMN: HIGH PASS FILTER:***

**$V_{in}$ =**

| S.No | Frequency in Hz | Output Voltage ($V_O$)in Volts | Gain = 20 log($V_O/V_{in}$) dB. |
|---|---|---|---|
| | | | |

***TABULAR COLUMN: BAND PASS FILTER***

**$V_{in}$ =**

| S.No | Frequency in Hz | Output Voltage ($V_O$)in Volts | Gain = 20 $\log(V_O/V_{in})$ dB. |
|---|---|---|---|
| | | | |

***VIVA QUESTIONS:***

1. What is the switched capacity filters?
2. What are the common applications of filters?
3. Define a state variable filter.
4. Why do we use higher order filters?
5. What is the roll-off a first order filter?
6. List out the other filters rather than these filters.

***RESULT:***

Thus the active low pass, High pass and band pass filter circuits were designed, constructed andtested the performance using op-amps and cut off frequencies were found.

## PLL CHARACTERISTICS AND FREQUENCY MULTIPLIER USING PLL

***Aim***

To design, construct and test the performance of PLL characteristics and to use PLL as a frequencymultiplier.

***Apparatus Required***

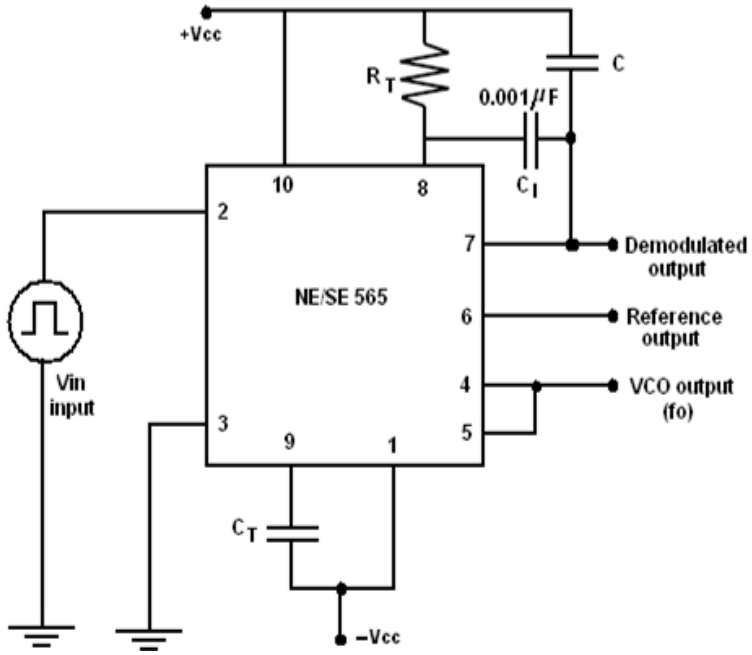
1. IC 565
2. Power supply
3. Resistor
4. Capacitor
5. Function generator
6. CRO & Probes
7. Bread board & Connecting wires

***THEORY:***

The basic block schematic of the PLL is shown in figure. This feedback system consists of phase detector/comparator, a low pass filter, an error amplifier and voltage controlled oscillator (VCO). The VCO is a free running multivibrator and operates at a set frequency $f_O$ called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a DC control voltage $V_C$ to an appropriate terminal of the IC. The frequency deviation is directly proportional to the DC control voltage and hence it is called a "Voltage Controlled Oscillator (VCO)". If an input signal $V_S$ of frequency $f_S$ is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output $V_O$ of the VCO. If the two signals differ in frequency and/or phase an error voltage $V_e$ is generated. The phase detector is basically a multiplier and produces sum ($f_S + f_O$) and difference ($f_S - f_O$) components at its output. The high frequency component ($f_S + f_O$) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage $V_C$ to VCO. The signal $V_C$ shifts the VCO frequency in a direction to reduce the frequency difference between $f_S$ and $f_O$. Once this action starts, we can say that the signal is in the capture range.

The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency $f_O$ of VCO is identical to $f_S$ except for a finite phase difference Φ. This phase difference Φ generates a corrective control voltage $V_C$ to shift the VCO frequency from $f_O$ to $f_S$ and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Important definitions related to PLL are (i) Lock in range, (ii) capture range and (iii) Pull in time.

**CIRCUIT DIAGRAM FOR PLL CHARACTERISTICS:**




**Design Procedure:**

Free running frequency of VCO, $f_0 = 0.25/R_TC_T$

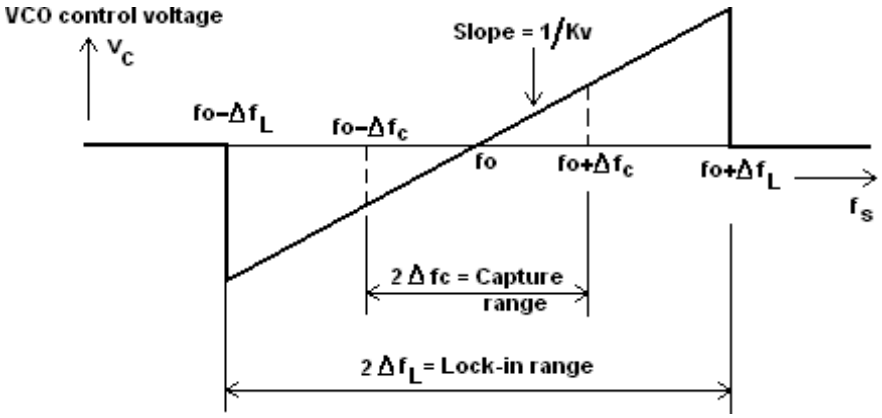
$f_0$ = 2.5 kHz; $C_T$ = 0.01□F; C = 10 µF

$R_T = 0.25/ f_0C_T$ = 10 K□

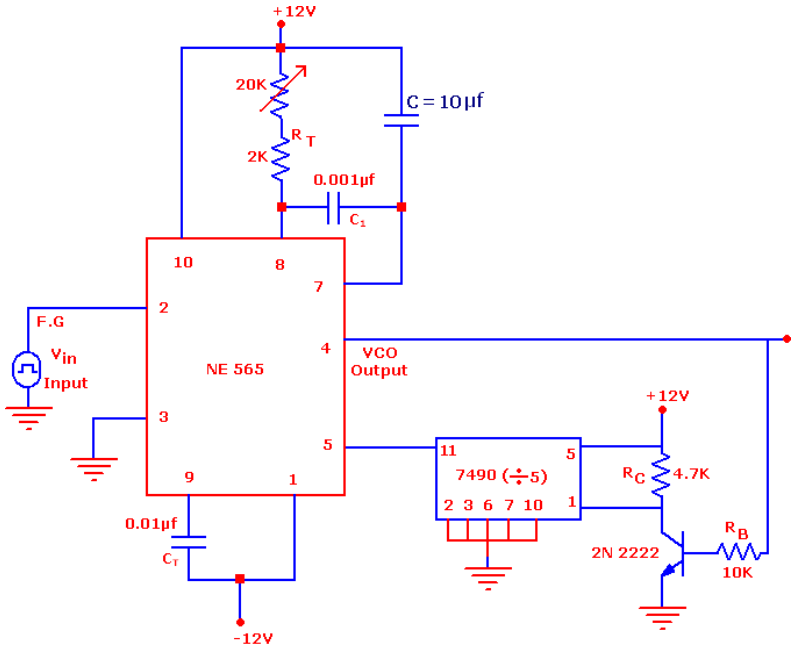
VCO output, **$f_0$** =

Lock range, **□$f_L = \pm 7.8f_0/V$ =**

Capture range, **□fc = ± [□$f_L$/ 2□ × 3.6 × $10^3$C]$^{1/2}$ =Model Graph:**




***PLL as a frequency multiplier:***




NE 565 PLL as a Frequency Multiplier

**TABULATION ( PLL CHARACTERISTICS):**

| S.NO | INPUT (Vin) | DEMODULATED OUTPUT (Vo) | VCO OUTPUT (fo) |
|---|---|---|---|
| | | | |

***TABULATION (FREQUENCY MULTIPLIER):***

| S.NO | INPUT FREQUENCY | OUTPUT FREQUENCY |
|---|---|---|
| | | |

**i) Lock In Range**

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock in range.

***ii) Capture Range***

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. The capture range is within the lock-in range.

***iii) Pull – In Time***

The total time taken by the PLL to establish the lock is called pull- in-time. This depends on the initial phase and frequency difference between the two signals as well as on the two signals as well as onthe overall loop gain and loop filter characteristics.

***Frequency Multiplication:***

The block diagram of a frequency multiplier using PLL is shown in the figure. A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency $f_O$ is given by, $\mathbf{f_O = N f_S}$

The multiplication factor can be obtained by selecting a proper scaling factor N of the counter. Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc. then VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. How ever, as the amplitude of the higher order harmonics becomes less, effective locking may not takes place for high values of n. Typically n is kept less than 10. The same circuit can also be used for frequency division. Since the VCO output (a square wave) rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal $f_S$. The output $f_O$ of VCO is now given by,

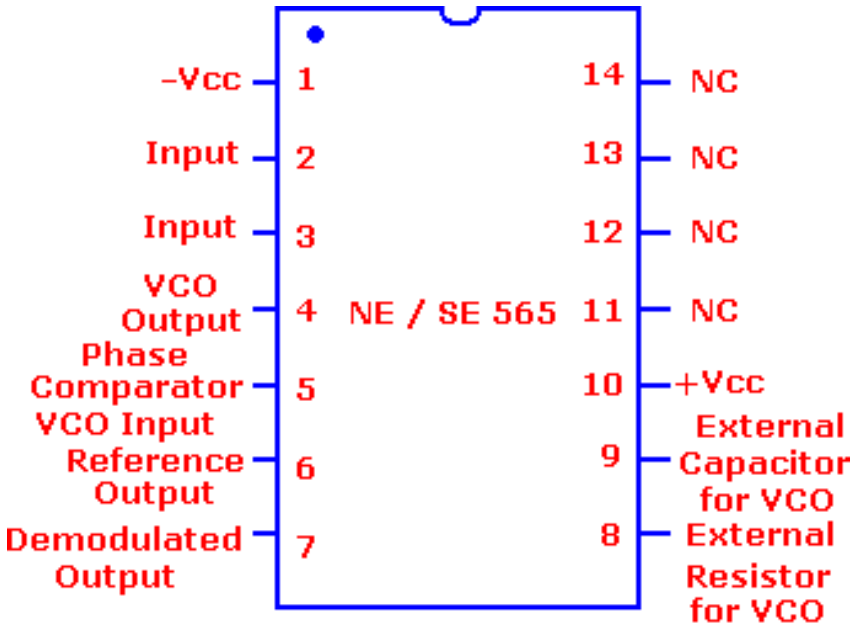
$$f_O = f_S / m$$

***Procedure: PLL Characteristics***

1. Make the connections as per the circuit diagram.
2. Measure the free running frequency of VCO at pin 4, with the input signal $V_{in}$ set equal to zero.Compare it with the calculated value = $0.25 / R_T C_T$.
3. Now apply the input signal of 1 $V_{PP}$ square wave at a 1 KHz to pin 2. Connect one channel of theCRO to pin 2 and display the signal on the CRO.
4. Gradually increase the input frequency till the PLL is locked to input frequency. This frequency $f_1$ gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency $f_2$. This frequency $f_2$ gives the upper end of the lock in range. If the input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency $f_3$, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency $f_4$ gives the lower end of the lock in range.
6. The lock in range $\Delta f_L = (f_2 - f_4)$. Compare it with the calculated value of $\Delta f_L = \pm 7.8 f_0 / 12$.

   Also the capture range is $\Delta f_C = (f_3 - f_1)$. Compare it with the calculated value of capture change.

**PIN DIAGRAM OF NE / SE 565 PLL IC:**




NE 565 PLL Pin Diagram

***Procedure: Frequency Multiplication***

1. Make the connections as per the circuit diagram.
2. Set the input signal at 1 $V_{PP}$ square wave at 500Hz.
3. Vary the VCO frequency by adjusting the 20kΩ potentiometer till the PLL is locked.
4. Measure the output frequency (It should be equal to 5 times the input frequency).
5. Repeat the steps 2, 3 and 4 for input frequency of 1 KHz and 1.5 KHz.

***VIVA QUESTIONS:***

1. State the various blocks included in PLL.
2. Define capture range.
3. What is a VCO?
4. Define Lock-in Range.
5. What is the function of a phase detector?

***RESULT:***

Thus the PLL characteristics and frequency multiplication using PLL NE / SE 565 PLL IC weredesigned, performed and their characteristics were obtained.

# R-2R DIGITAL TO ANALOG CONVERTER

**Aim:** To design 4bit R-2R ladder DAC using Op-Amp for an output voltage of 5V when the input is 10 (Binary 1010).

**Apparatus:**

| Sl. No. | Particulars | Specification | Quantity |
|---|---|---|---|
| 1. | IC | µA741 | 02 |
| 2. | Resistors | As per design | - |
| 3. | Multimeter | - | 01 |
| 4. | Baseboard+connectingwires | - | 01Set |

**Procedure:**

1. Connections are made as shown in the circuit diagram.
2. Digital input data is given at D3,D2,D1, D0 and corresponding analog output voltage V0 is measured.
3. Tabulate the readings & plot the graph between Vo on y-axis Vin on X-axis.

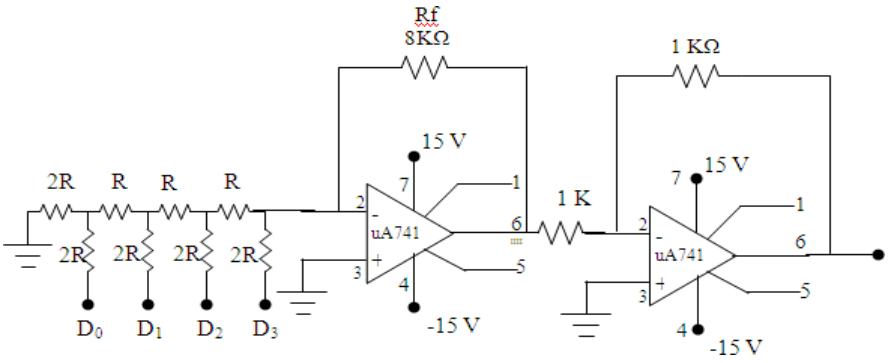
**Note:**

1. D0.D1.D2&D3 are binary input.
2. Vo is the analog output.
3. Binary inputs Do.D1.D2&D3 can take either the value„0“or „1“.
4. Binary input Di(i=0to3) can be made„0“by connecting the i/p to ground. It can be made „1“ by connecting to–5 V.

   Logic0 0V

   Logic1 5V

## Circuit Diagram



**Result :**

Thus the R-

| Decimal Value | BinaryInputs | | | | AnalogO/P Vo(volts) Theoreticalvalues | AnalogO/P Vo(volts) Practicalvalues |
|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0 | | |
| 1 | 0 | 0 | 0 | 1 | | |
| 2 | 0 | 0 | 1 | 0 | | |
| 3 | 0 | 0 | 1 | 1 | | |
| 4 | 0 | 1 | 0 | 0 | | |
| 5 | 0 | 1 | 0 | 1 | | |
| 6 | 0 | 1 | 1 | 0 | | |
| 7 | 0 | 1 | 1 | 1 | | |
| 8 | 1 | 0 | 0 | 0 | | |
| 9 | 1 | 0 | 0 | 1 | | |
| 10 | 1 | 0 | 1 | 0 | | |
| 11 | 1 | 0 | 1 | 1 | | |
| 12 | 1 | 1 | 0 | 0 | | |
| 13 | 1 | 1 | 0 | 1 | | |
| 14 | 1 | 1 | 1 | 0 | | |
| 15 | 1 | 1 | 1 | 1 | | |

## SIMULATION USING SPICE (Using Transistor)

## TUNED COLLECTOR OSCILLATOR

**AIM:**

To simulate a tuned collector oscillator using PSPICE**.**

**REQUIREMENTS:**

1. PC

2. PSPICE software

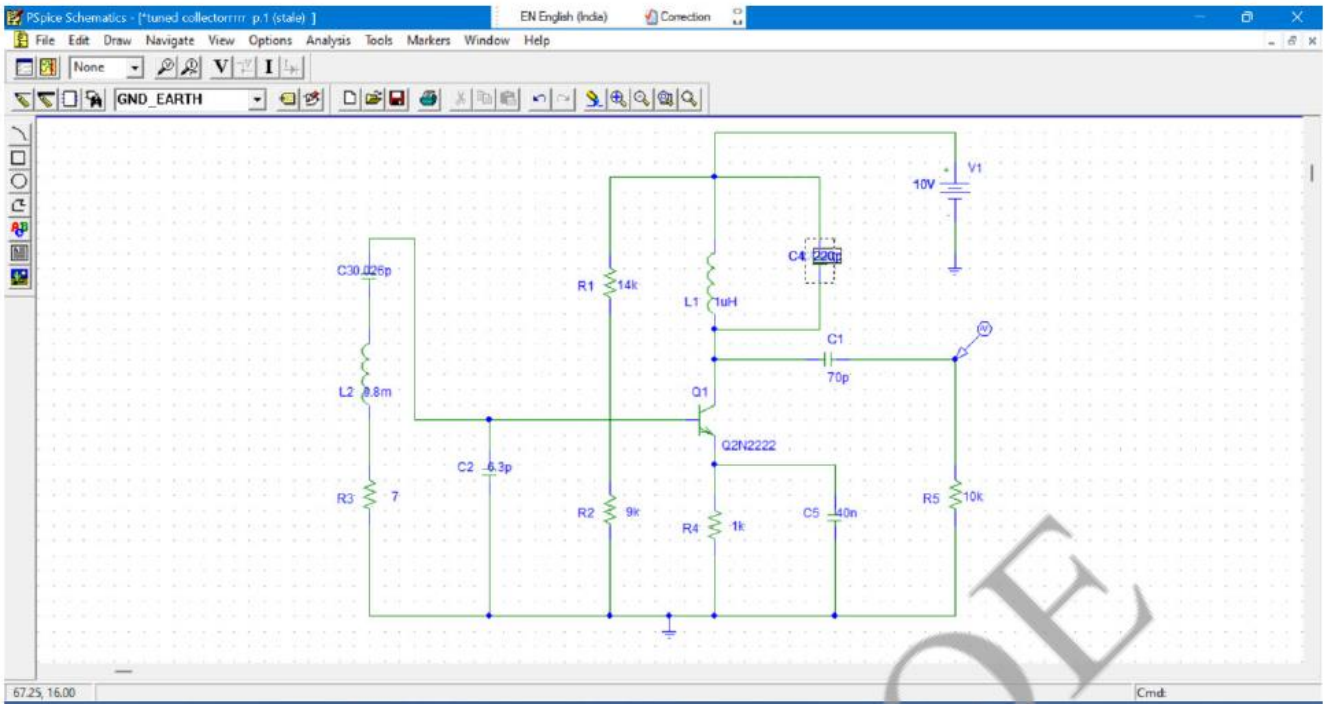
**THEORY:**

Tuned collector oscillation is a type of transistor LC oscillator where the tuned circuit (tank) consists of a transformer and a capacitor is connected in the collector circuit of the transistor. Tuned collector oscillator is of course the simplest and the basic type of LC oscillators. The tuned circuit connected at the collector circuit behaves like a purely resistive load at resonance and determines the oscillator frequency. The common applications of tuned collector oscillator are RF oscillator circuits, mixers, frequency demodulators, signal generators etc.,

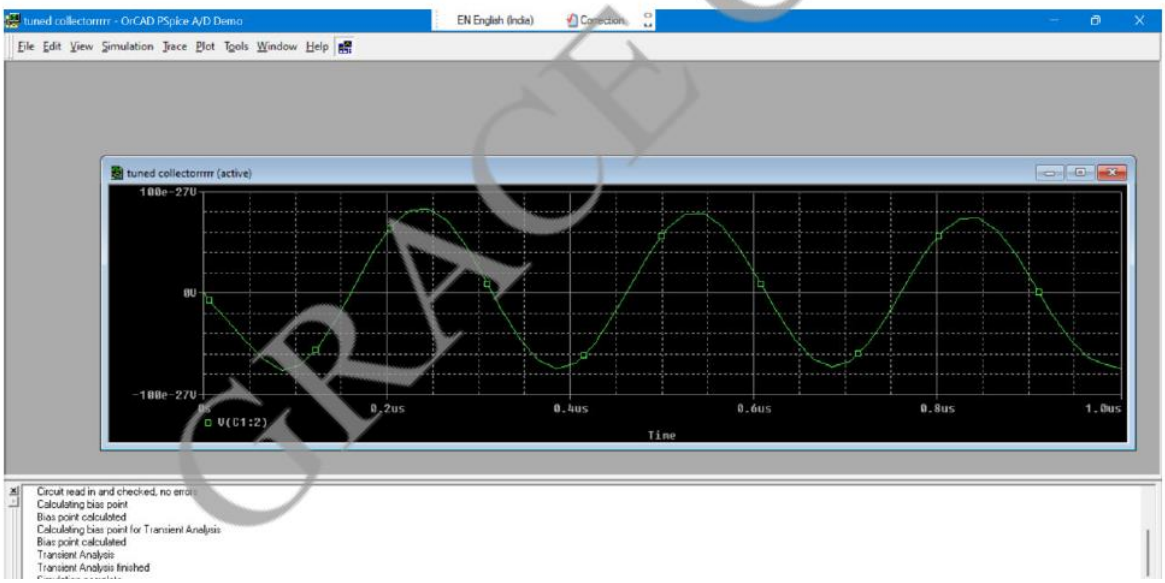
**PROCEDURE:**

1. Double click the PSPICE software icon the following screen will appear.
2. Schematic window will open and draw the given circuit by choosing the components from place part.
3. Finish the circuit and save it.
4. Create new simulation profile and give simulation file name as tuned oscillator.sch
5. In simulation settings window set transient time initial value as 1ms and final value as 10ms and the input voltage as AC=0.5V, DC=0V and offset voltage as 0V and appropriate amplitude and frequency value.
6. Set the probe at the output and click Run.

## CIRCUIT DIAGRAM:




## OUTPUT WAVEFORM:




## VIVA QUESTIONS:

1. What is PSpice?
2. What is the use of Pspice?
3. What are the different types of analysis done using Spice?
4. List the limitation of Pspice
5. What are the different output commands?

# TWIN-T OSCILLATOR

**AIM:**

To simulate Twin – T Oscillator circuit using PSPICE.

**COMPONENTS & EQUIPMENTS REQUIRED:**

| S.No | Components / Software |
|---|---|
| 1 | Personal Computer |
| 2 | PSPICE Software |

**THEORY:**

The "Twin-T" oscillator as it uses two "T" RC circuits operated in parallel. Onecircuit is an R-C-R "T" which acts as a low-pass filter. The second circuit is a C-R-C "T" which operates as a high-pass filter. Together, these circuits form a bridge which is tuned at the desired frequency of oscillation. The signal in the C-R-C branch of the Twin-T filter is advanced, in the R-C-R - delayed, so they may cancel one another for frequency 1

$$f = \frac{}{2\pi RC}, \quad x = 2$$

if it is connected as a negative feedback to an amplifier, and x>2, the amplifier becomes an oscillator.

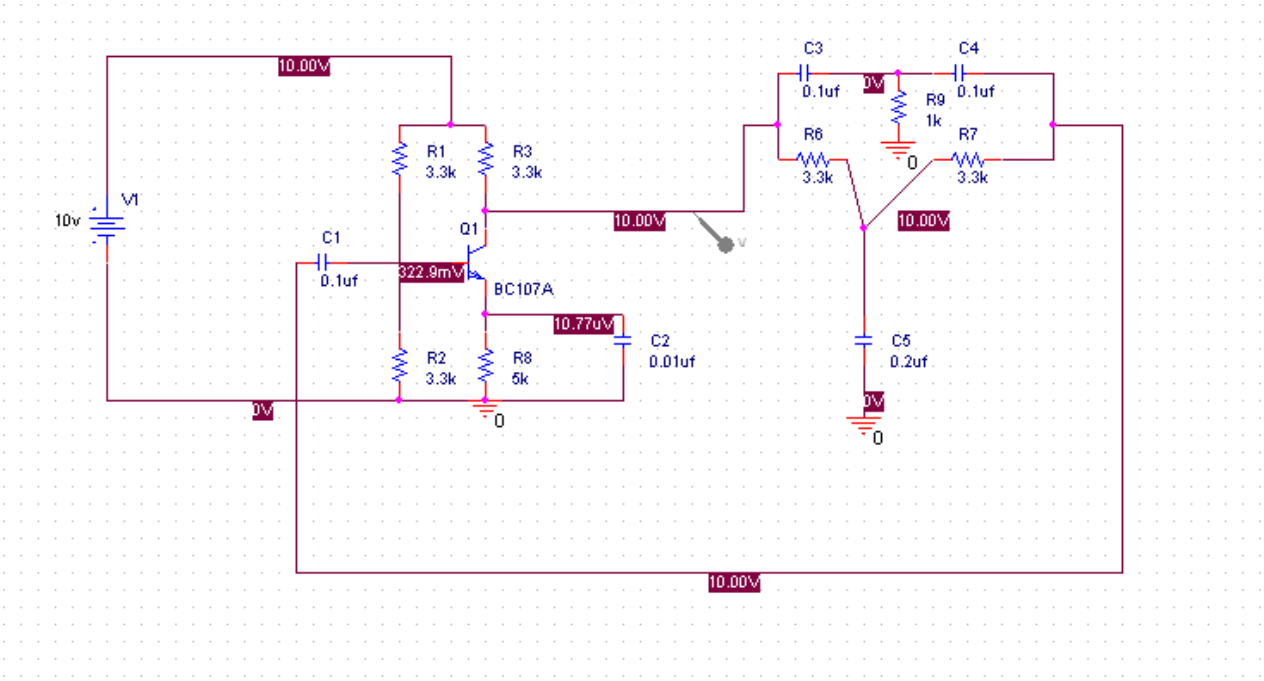
**PROCEDURE:**

1. Open Orcad-> Capture CIS ->File->New-> Project
2. Place->Part , select the required components for the circuit to be designed fromthe library.
3. Select R,C components from the Analog.olb and edit the values as per the circuit diagram.
4. Select Transistor Q2N2222 from bipolar.olb
5. For the DC supply select VDC from source.olb and edit the value as 12V for VCC
6. Connect the placed components by using the option Place->wire.
7. Pspice -> New Simulation profile -> name->create

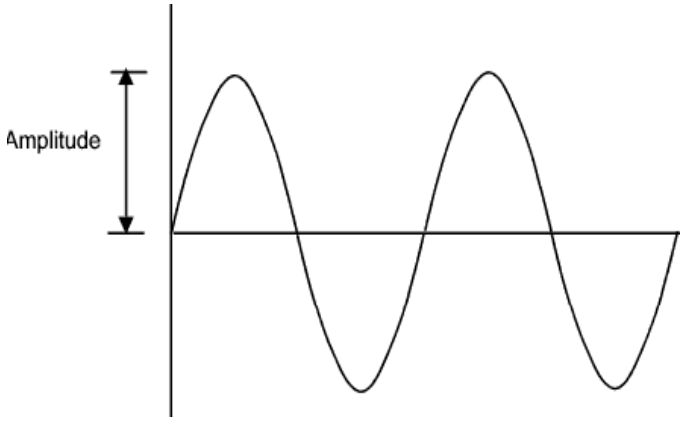
8. Analysis ->Time Domain
9. Enter Run to time and maximum step size value.
10. Pspice-> Run.
11. Plot->Add plot to window, two plot windows will be displayed.
12. Keep the cursor in the first plot window , Trace-> Add Trace ->V(Q1:b),V(Q2:b).
13. Keep the cursor in the second plot window ,Trace-> Add Trace ->(Q1:c),V(Q2:c

**CIRCUIT DIAGRAM:**

**TWIN-T OSCILLATOR**



MODEL GRAPH:




**VIVA VOCE QUESTIONS**

1. What is an oscillator?
2. Give the difference between an amplifier and an oscillator?
3. What are the constituent parts of an oscillator?
4. Why RC network is connected in feedback?
5. What is the frequency of oscillation of RC network?

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the given Twin T oscillator circuit was simulated using PSPICE tool and theoutput graphs were obtained.

# WEIN BRIDGE OSCILLATOR

**AIM:**

To simulate Wein Bridge Oscillator circuit using PSPICE.

**COMPONENTS & EQUIPMENTS REQUIRED:**

| S.No | Components / Software |
|---|---|
| 1 | Personal Computer |
| 2 | PSPICE Software |

**THEORY:**

A Wien bridge oscillator is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The oscillator is based on a bridge circuit originally developed by Max Wien in 1891 for the measurement of impedances.[1] The bridge comprises four resistors and two capacitors. The oscillator can also be viewed as a positive gain amplifier combined with a bandpass filter that provides positive feedback. Automatic gain control, intentional non-linearity and incidental non-linearity limit the output amplitude in various implementations of the oscillator.The condition that R1=R2=R and C1=C2=C, the frequency of oscillation is given by,

$$f = \frac{1}{2\pi RC}$$

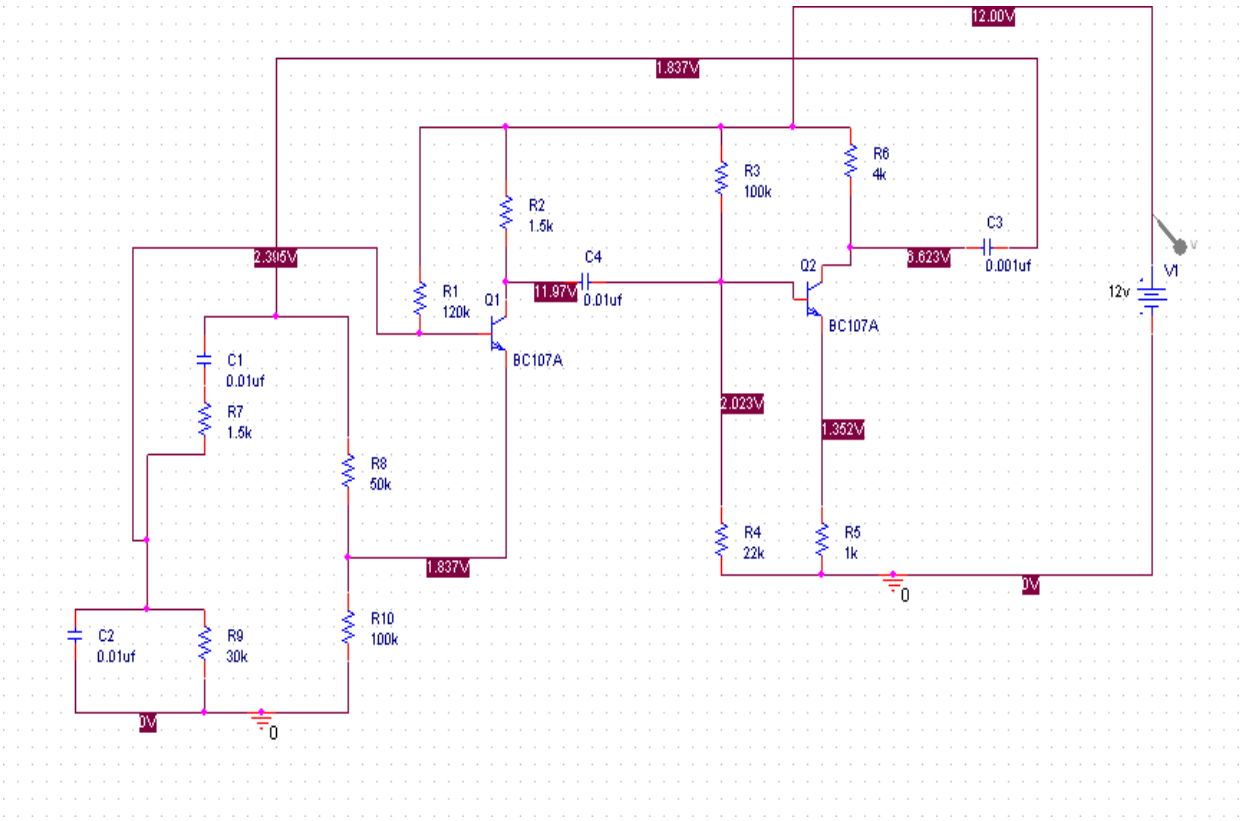
and the condition of stable oscillation is given by,

$$R_b = R_f / 2$$

**PROCEDURE:**

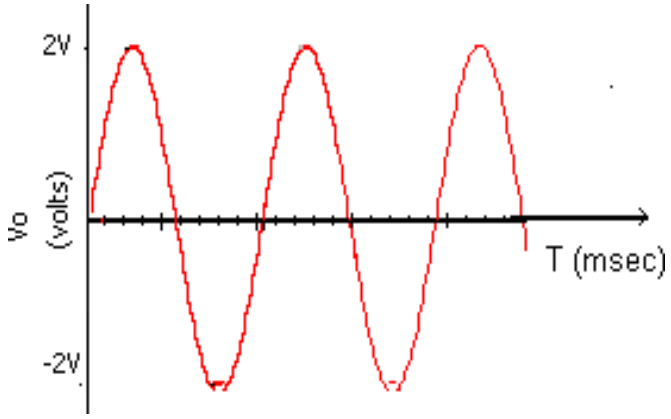
1. Open Orcad-> Capture CIS ->File->New-> Project
2. Place->Part , select the required components for the circuit to be designedfrom the library.
3. Connect the placed components by using the option Place->wire.
4. Pspice -> New Simulation profile -> name->create
5. Analysis ->Time Domain
6. Enter Run to time and maximum step size value.
7. Pspice-> Run.
8. Plot->Add plot to window.
9. Keep the cursor in the first plot window , Trace-> Add the required Trace

**CIRCUIT DIAGRAM:**




**WEIN BRIDGE OSCILLATOR**

**MODEL GRAPH:**




**VIVA VOCE QUESTIONS:**

1. Give the formula for frequency of oscillations.
2. What is the condition for Wien bridge oscillator to generate oscillations?
3. What is the total phase shift provided by the oscillator?
4. What is the function of lead-lag network in Wein bridge oscillator?
5. Find whether the Wein bridge oscillator is LC or RC oscillator.

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the given Wein Bridge oscillator circuit was simulated using PSPICE tool andoutput graphs were obtained.

# DOUBLE AND STAGGER TUNED AMPLIFIER

**AIM:**

To simulate the Double Tuned and Stagger tuned amplifier using PSPICE.

**COMPONENTS & EQUIPMENTS REQUIRED:**

| S.No | Components / Software |
|---|---|
| 1 | Personal Computer |
| 2 | PSPICE Software |

**THEORY:**

**DOUBLE-TUNED AMPLIFIER :**

A double-tuned amplifier is a tuned amplifier with transformer coupling between the amplifier stages in which the inductances of both the primary and secondary windings are tuned separately with a capacitor across each. The scheme results in a wider bandwidth and steeper skirts than a single tuned circuit would achieve.

There is a critical value of transformer coupling coefficient at which the frequency response of the amplifier is maximally flat in the pass band and the gain is maximum at the resonant frequency. Designs frequently use a coupling greater than this (over- coupling) in order to achieve an even wider bandwidth at the expense of a small loss of gain in the centre of the pass band.

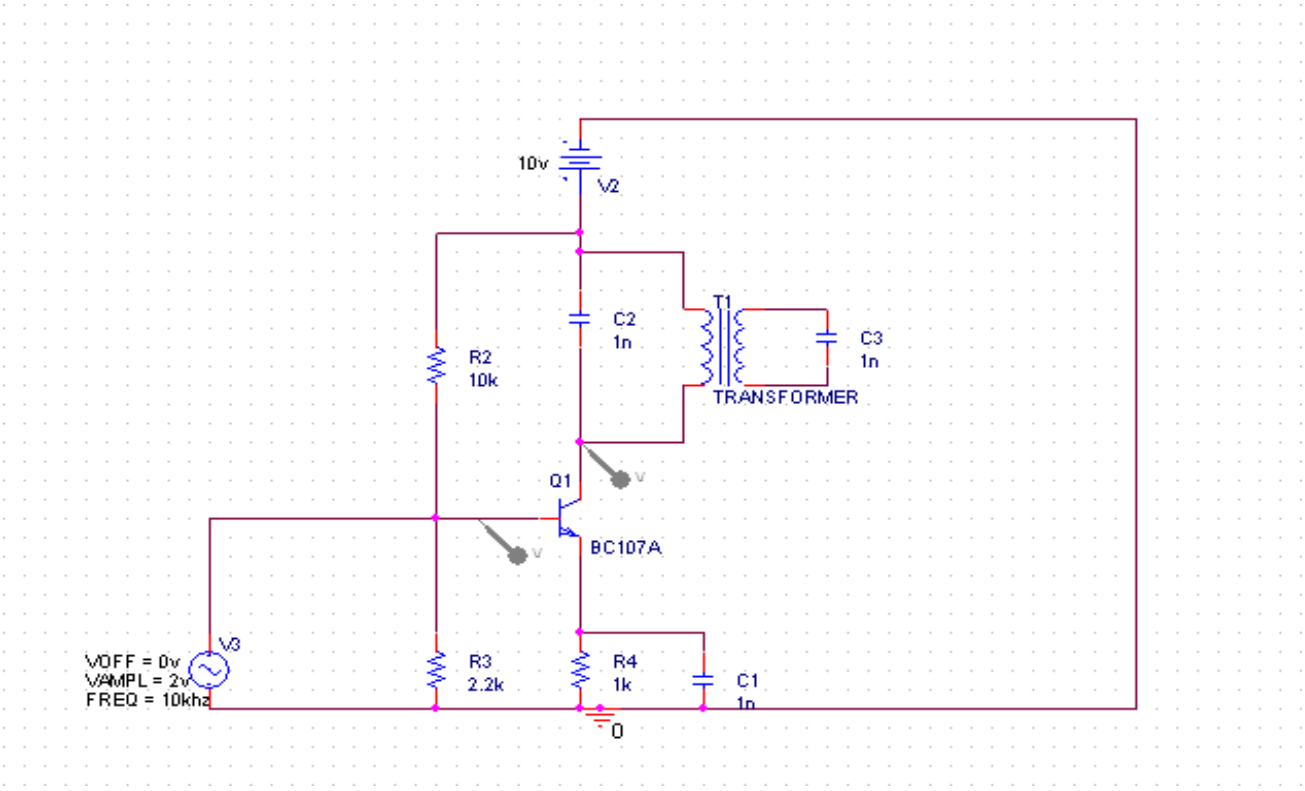
Cascading multiple stages of double-tuned amplifiers results in a reduction of the bandwidth of the overall amplifier. Two stages of double-tuned amplifier have 80% of the bandwidth of a single stage. An alternative to double tuning that avoids this loss of bandwidth is staggered tuning. Stagger-tuned amplifiers can be designed to a prescribed bandwidth that is greater than the bandwidth of any single stage. However, staggered tuning requires more stages and has lower gain than double tuning.

**STAGGER TUNED AMPLIFIER:**

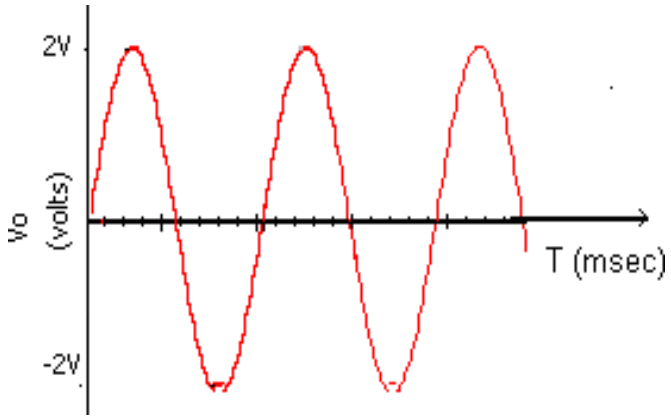
Staggered tuning is a technique used in the design of multi-stage tuned amplifiers whereby each stage is tuned to a slightly different frequency. In comparison to synchronous tuning (where each stage is tuned identically) it produces a wider bandwidth at the expense of reduced gain.

**CIRCUIT DIAGRAM:**

**DOUBLE AND STAGGER TUNED AMPLIFIER**




**MODEL GRAPH:**



**PROCEDURE:**

1. Open Orcad-> Capture CIS ->File->New-> Project

2. Place->Part , select the required components for the circuit to be designed fromthe library.

3. Connect the placed components by using the option Place->wire.

4. Pspice -> New Simulation profile -> name->create

5. Analysis ->Time Domain

6. Enter Run to time and maximum step size value.

7. Pspice-> Run.

8. Plot->Add plot to window.

9. Keep the cursor in the first plot window , Trace-> Add the required Trace

**VIVA VOCE QUESTIONS:**

1. How single tuned amplifiers are classified?
2. What are single tuned amplifiers?
3. What are double tuned amplifiers?
4. What are stagger tuned amplifiers?
5. What are the advantages of double tuned amplifier over single tunedamplifier?

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the given Double tuned and stagger tuned amplifier circuit was simulatedusing PSPICE tool and output were obtained.

## BISTABLE MULTIVIBRATOR

**AIM:**

To simulate the Bistable multivibrator using PSPICE.

**COMPONENTS & EQUIPMENTS REQUIRED:**

| S.No | Components / Software |
|---|---|
| 1 | Personal Computer |
| 2 | PSPICE Software |

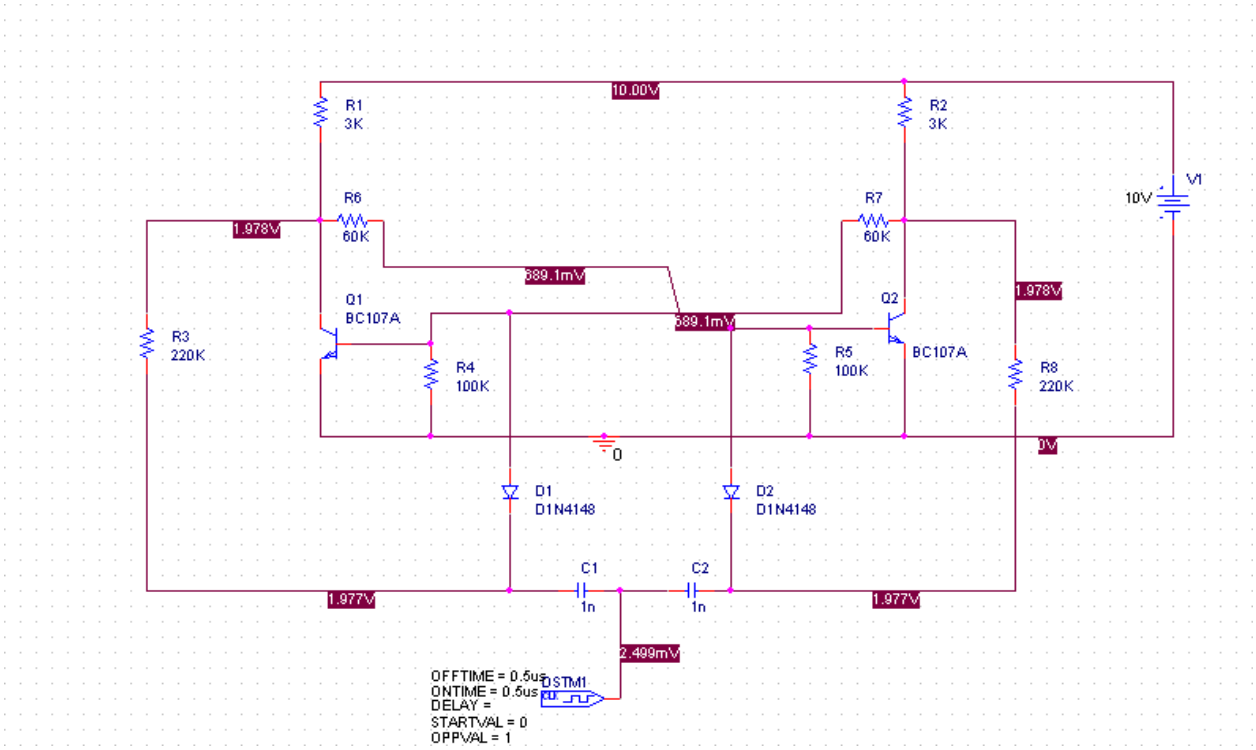
**THEORY:**

The Bistable Multivibrator is another type of two state device similar to the Monostable Multivibrator we looked at in the previous tutorial but the difference this time is that both states are stable.

**PROCEDURE:**

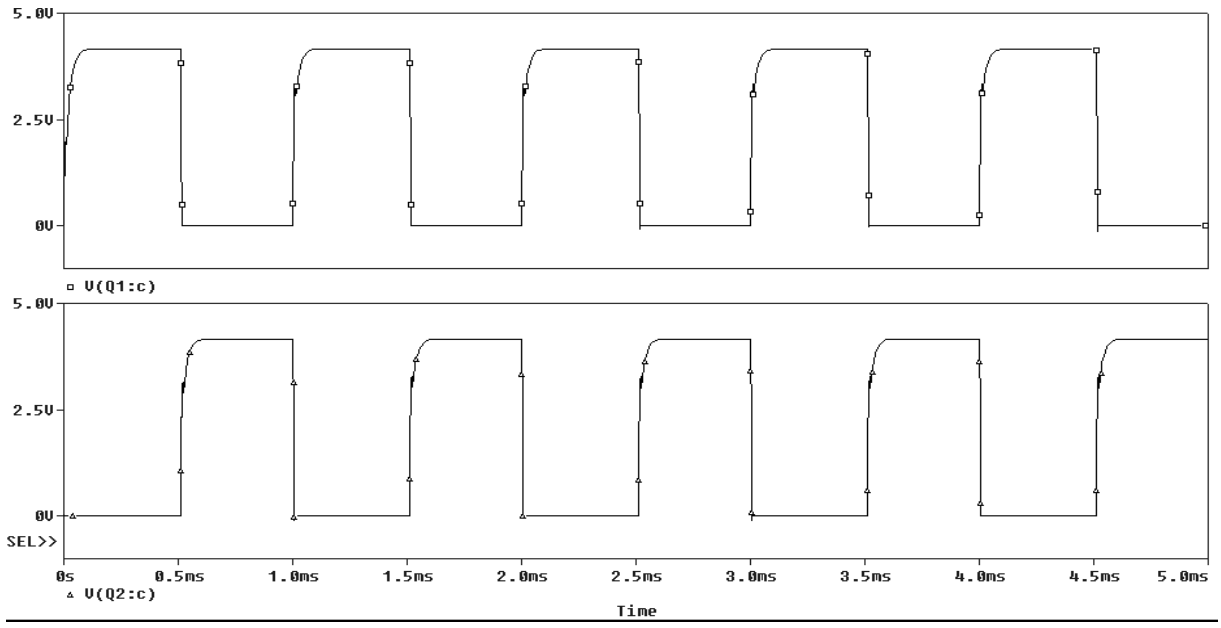
1. Open Orcad-> Capture CIS ->File->New-> Project
2. Place->Part , select the required components for the circuit to be designedfrom the library.
3. Select R,C components from the Analog.olb and edit the values as per thecircuit diagram.
4. Select Transistor Q2N2222 from bipolar.olb
5. For the DC supply select VDC from source.olb and edit the value as 12V for VCC
6. Connect the placed components by using the option Place->wire.
7. Pspice -> New Simulation profile -> name->create
8. Analysis ->Time Domain
9. Enter Run to time and maximum step size value.
10. Pspice-> Run.
11. Plot->Add plot to window, two plot windows will be displayed.
12. Keep the cursor in the first plot window , Trace-> Add Trace ->V(Q1:b),V(Q2:b).
13. Keep the cursor in the second plot window ,Trace-> Add Trace ->(Q1:c),V(Q2:c).

## CIRCUIT DIAGRAM:




**BISTABLE MULTIVIBRATOR**

## MODEL GRAPH:



**VIVA VOCE QUESTIONS:**

**1.** What are the different names of Bistable multivibrator?

**2.** Distinguish oscillator and multivibrator.

**3.** What are the states obtained in Bistable multivibrator?

**4.** What are the different types multivibrator .

**5.** What are the other names of a bistable multivibrator ?

| | | |
|---|---|---|
| **PREPARATION** | | **40** |
| **EXECUTION** | | **40** |
| **VIVA-VOCE** | | **20** |
| **TOTAL** | | **100** |

**RESULT:**

Thus the given Bistable multivibrator circuit was simulated using PSPICE tool andoutput were obtained