

# 1. Description

# 1.1. Project

Project Name	ModuCard_nav_module
Board Name	custom
Generated with:	STM32CubeMX 6.14.0
Date	03/26/2025

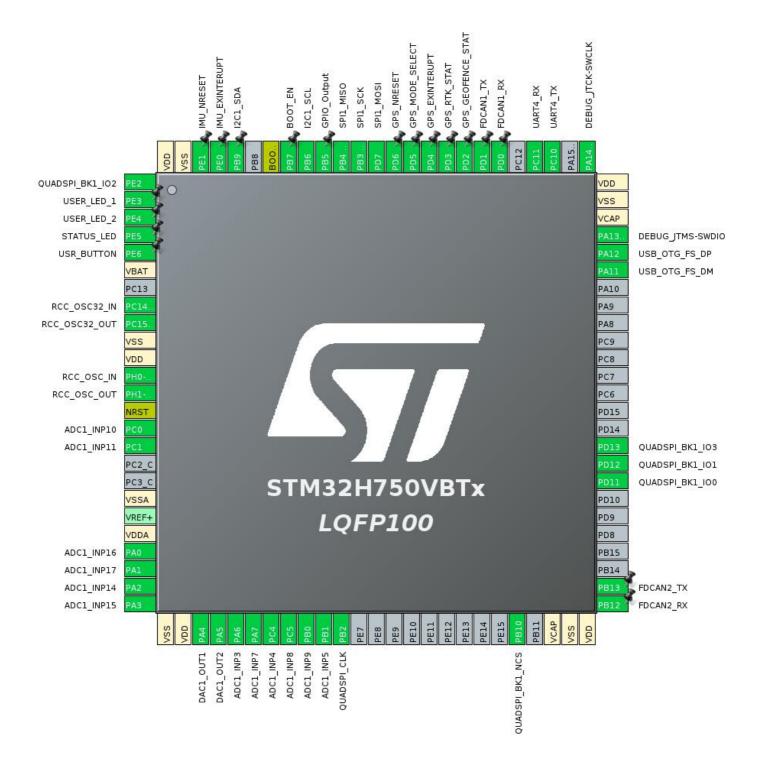
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750VBTx
MCU Package	LQFP100
MCU Pin number	100

# 1.3. Core(s) information

Core(s)	ARM Cortex-M7

# 2. Pinout Configuration



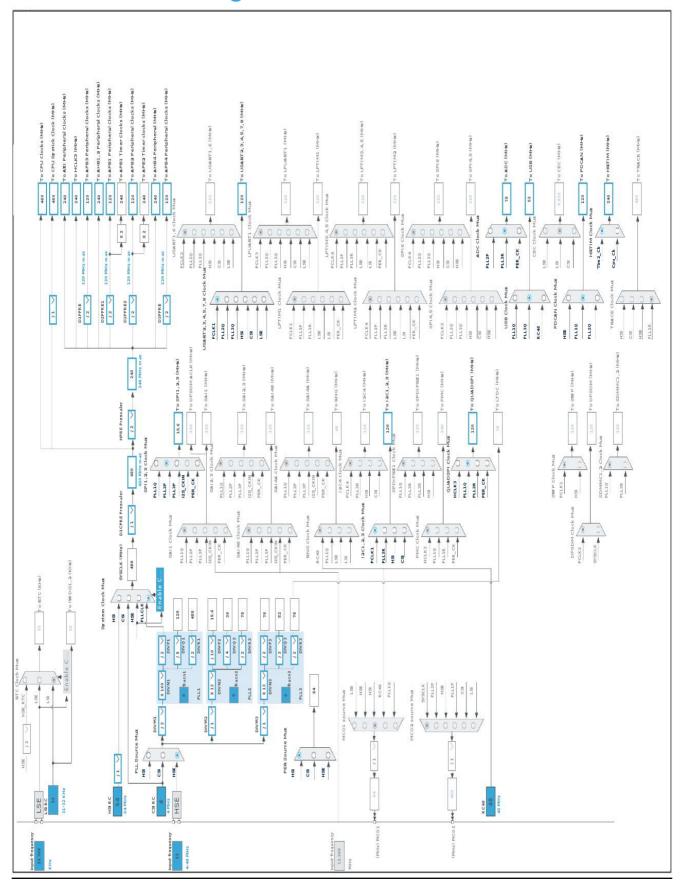
# 3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP100	(function after		Function(s)	
	reset)		· ,	
1	PE2	I/O	QUADSPI_BK1_IO2	
2	PE3 *	I/O	GPIO_Output	USER_LED_1
3	PE4 *	I/O	GPIO_Output	USER_LED_2
4	PE5 *	I/O	GPIO_Output	STATUS_LED
5	PE6 *	I/O	GPIO_Input	USR_BUTTON
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_INP10	
16	PC1	I/O	ADC1_INP11	
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	ADC1_INP16	
23	PA1	I/O	ADC1_INP17	
24	PA2	I/O	ADC1_INP14	
25	PA3	I/O	ADC1_INP15	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DAC1_OUT1	
29	PA5	I/O	DAC1_OUT2	
30	PA6	I/O	ADC1_INP3	
31	PA7	I/O	ADC1_INP7	
32	PC4	I/O	ADC1_INP4	
33	PC5	I/O	ADC1_INP8	
34	PB0	I/O	ADC1_INP9	
35	PB1	I/O	ADC1_INP5	
36	PB2	I/O	QUADSPI_CLK	
46	PB10	I/O	QUADSPI_BK1_NCS	
48	VCAP	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	FDCAN2_RX	
52	PB13	I/O	FDCAN2_TX	
58	PD11	I/O	QUADSPI_BK1_IO0	
59	PD12	I/O	QUADSPI_BK1_IO1	
60	PD13	I/O	QUADSPI_BK1_IO3	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
78	PC10	I/O	UART4_TX	
79	PC11	I/O	UART4_RX	
81	PD0	I/O	FDCAN1_RX	
82	PD1	I/O	FDCAN1_TX	
83	PD2 *	I/O	GPIO_Input	GPS_GEOFENCE_STAT
84	PD3 *	I/O	GPIO_Input	GPS_RTK_STAT
85	PD4	I/O	GPIO_EXTI4	GPS_EXINTERUPT
86	PD5 *	I/O	GPIO_Output	GPS_MODE_SELECT
87	PD6 *	I/O	GPIO_Output	GPS_NRESET
88	PD7	I/O	SPI1_MOSI	
89	PB3 (JTDO/TRACESWO)	I/O	SPI1_SCK	
90	PB4 (NJTRST)	I/O	SPI1_MISO	
91	PB5 *	I/O	GPIO_Output	
92	PB6	I/O	I2C1_SCL	
93	PB7 *	I/O	GPIO_Output	BOOT_EN
94	воото	Boot		
96	PB9	I/O	I2C1_SDA	
97	PE0	I/O	GPIO_EXTI0	IMU_EXINTERUPT
98	PE1 *	I/O	GPIO_Output	IMU_NRESET
99	VSS	Power		
100	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
мси	STM32H750VBTx
Datasheet	DS12556_Rev6

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

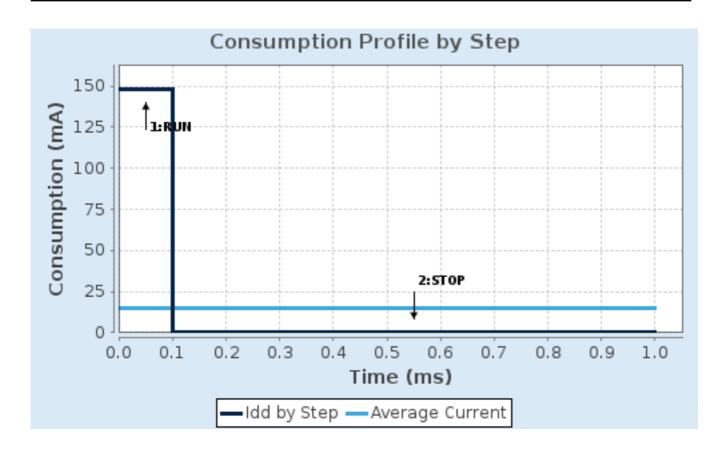
# 1.4. Sequence

	T	1
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.02	124.98
Category	In DS Table	In DS Table

### 1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001
			DMIPS

### 1.6. Chart



# 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	ModuCard_nav_module
Project Folder	/home/lemonx/it/ModuCard-nav-module-software
Toolchain / IDE	CMake
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0xF00
Minimum Stack Size	0x900

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_MDMA_Init	MDMA
4	MX_ADC1_Init	ADC1
5	MX_DAC1_Init	DAC1
6	MX_FDCAN1_Init	FDCAN1
7	MX_FDCAN2_Init	FDCAN2
8	MX_I2C1_Init	I2C1
9	MX_QUADSPI_Init	QUADSPI
10	MX_UART4_Init	UART4
11	MX_SPI1_Init	SPI1

Rank	Function Name	Peripheral Instance Name
12	MX_HRTIM_Init	HRTIM
13	MX_TIM2_Init	TIM2
14	MX_TIM12_Init	TIM12
15	MX_USB_DEVICE_Init	USB_DEVICE

# 3. Peripherals and Middlewares Configuration

3.1. ADC1

IN3: IN3 Single-ended IN4: IN4 Single-ended IN5: IN5 Single-ended

mode: IN7 mode: IN8 mode: IN9

IN10: IN10 Single-ended

mode: IN11 mode: IN14 mode: IN15

IN16: IN16 Single-ended

mode: IN17

3.1.1. Parameter Settings:

#### ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 16-bit resolution

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Left Bit Shift No bit shift

Conversion Data Management Mode Regular Conversion data stored in DR register only

Low Power Auto Wait Disabled

ADC\_Regular\_ConversionMode:

Enable Regular ConversionsEnableEnable Regular OversamplingDisableOversampling Ratio1Number Of Conversion1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 3
Sampling Time 1.5 Cycles

Offset Number No offset
Offset Signed Saturation Disable

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

#### 3.2. DAC1

OUT1 connected to: only external pin OUT2 connected to: only external pin

### 3.2.1. Parameter Settings:

#### **DAC Out1 Settings:**

Mode selected Normal Mode
Output Buffer Enable
Trigger None

User Trimming Factory trimming

**DAC Out2 Settings:** 

Mode selected Normal Mode
Output Buffer Enable
Trigger None

User Trimming Factory trimming

#### **3.3. DEBUG**

**Debug: Serial Wire** 

### 3.4. FDCAN1

mode: Activated

### 3.4.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format Classic mode

Mode Normal mode

Auto Retransmission Disable
Transmit Pause Disable
Protocol Exception Disable

 Nominal Sync Jump Width
 1

 Data Prescaler
 1

 Data Sync Jump Width
 1

 Data Time Seg1
 1

 Data Time Seg2
 1

 Message Ram Offset
 0

 Std Filters Nbr
 0

 Ext Filters Nbr
 0

Rx Fifo0 Elmt Size 8 bytes data field

0

Rx Fifo1 Elmts Nbr 0

Rx Fifo1 Elmt Size 8 bytes data field

Rx Buffers Nbr 0

Rx Buffer Size 8 bytes data field

 Tx Events Nbr
 0

 Tx Buffers Nbr
 0

 Tx Fifo Queue Elmts Nbr
 0

Tx Fifo Queue Mode FIFO mode
Tx Elmt Size 8 bytes data field

**Clock Calibration Unit:** 

Rx Fifo0 Elmts Nbr

Clock Calibration Disable

**Bit Timings Parameters:** 

Nominal Prescaler 8 \*

Nominal Time Quantum 66.666666666667 \*

Nominal Time Seg1 1
Nominal Time Seg2 1

Nominal Time for one Bit 200 \*

Nominal Baud Rate 5000000 \*

3.5. FDCAN2

mode: Activated

3.5.1. Parameter Settings:

**Basic Parameters:** 

Frame Format Classic mode

Mode Normal mode

Auto Retransmission Disable
Transmit Pause Disable
Protocol Exception Disable

 Nominal Sync Jump Width
 1

 Data Prescaler
 1

 Data Sync Jump Width
 1

 Data Time Seg1
 1

 Data Time Seg2
 1

 Message Ram Offset
 0

 Std Filters Nbr
 0

 Ext Filters Nbr
 0

 Rx Fif00 Elmts Nbr
 0

Rx Fifo0 Elmt Size 8 bytes data field

Rx Fifo1 Elmts Nbr 0

Rx Fifo1 Elmt Size 8 bytes data field

Rx Buffers Nbr 0

Rx Buffer Size 8 bytes data field

 Tx Events Nbr
 0

 Tx Buffers Nbr
 0

 Tx Fifo Queue Elmts Nbr
 0

Tx Fifo Queue Mode FIFO mode
Tx Elmt Size 8 bytes data field

**Clock Calibration Unit:** 

Clock Calibration Disable

**Bit Timings Parameters:** 

Nominal Prescaler 40 \*

Nominal Time Quantum 333.33333333333 \*

Nominal Time Seg1 1
Nominal Time Seg2 1
Nominal Time for one Bit 1000

Nominal Baud Rate 999999 \*

### **3.6. HRTIM**

### **Timer A: No external Output**

### 3.6.1. HRTIM Interrupt Configuration:

#### Sources:

1st Source of interrupt

2nd Source of interrupt

No interrupt enabled

No interrupt enabled

3rd Source of interrupt	No interrupt enabled
4th Source of interrupt	No interrupt enabled
5th Source of interrupt	No interrupt enabled
6th Source of interrupt	No interrupt enabled
7th Source of interrupt	No interrupt enabled
8th Source of interrupt	No interrupt enabled

### 3.6.2. Synchro Configuration:

Sync Options HRTIM instance doesn't handle external synchronization signals (SYNCIN,

SYNCOUT)

### 3.6.3. External Event Configuration:

**External Event 1:** 

Event Configuration Disable

**External Event 2:** 

Event Configuration Disable

**External Event 3:** 

Event Configuration Disable

**External Event 4:** 

Event Configuration Disable

**External Event 5:** 

Event Configuration Disable

**External Event 6:** 

Event Configuration Disable

**External Event 7:** 

Event Configuration Disable

**External Event 8:** 

Event Configuration Disable

**External Event 9:** 

Event Configuration Disable

**External Event 10:** 

Event Configuration Disable

### 3.6.4. Fault Lines Configuration:

#### Fault Line 1:

Line Configuration No Configuration of Fault Line

Fault Line 2:

Line Configuration No Configuration of Fault Line

Fault Line 3:

Line Configuration No Configuration of Fault Line

Fault Line 4:

Line Configuration No Configuration of Fault Line

Fault Line 5:

Line Configuration No Configuration of Fault Line

### 3.6.5. ADC Triggers Configuration:

**ADC Trigger 1:** 

ADC Trigger Configuration Disable

**ADC Trigger 2:** 

ADC Trigger Configuration Disable

**ADC Trigger 3:** 

ADC Trigger Configuration Disable

**ADC Trigger 4:** 

ADC Trigger Configuration Disable

#### 3.6.6. Burst Mode Configuration:

**Burst Mode Enabling:** 

Burst Mode Burst mode disabled

### 3.6.7. Timer A:

General:

Timer Idx Timer A

Basic/Advanced Configuration Advanced (using HAL\_Waveform methods)

**Time Base Setting:** 

Prescaler Ratio HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value =

400MHz)

fHRCK Equivalent Frequency 2.4E8

Period 0xFFFD \*

Resulting PWM Frequency 3662

Repetition Counter 0x00 \*

Mode The timer operates in continuous (free-running) mode

**Timing Unit:** 

Half Mode Enable - The Compare Value of CP Unit 1 is Half mode is disabled

set automatically to half the Timer Period -

Start On Sync Synchronization input event has no effect on the timer

Reset On Sync Synchronization input event has no effect on the timer

Dac Synchro No DAC synchronization event generated

Preload Enable Preload disabled: the write access is directly done into the active register

Update Gating Update done independently from the DMA burst transfer completion

Repetition Update Update on repetition disabled

Burst Mode Timer counter clock is maintained and the timer operates normally

Push Pull Push-Pull mode disabled

Number of Faults to enable 0

Fault Lock Timer fault enabling bits are read/write

Dead Time Insertion Output 1 and output 2 signals are independent

0

Delayed Protection Mode No action

Update Trigger Sources Selection : Please enter the

number of Triggers to select

Reset Update by Timer reset / roll-over disabled

Reset Trigger Sources Selection : Please enter the

number of Triggers to select

Interrupt Requests Sources Selection : Please enter

the number of Active Interrupt Requests

Number of Timer A Internal DMA Request Sources - you first have to enable the Timer A DMA Request in

the DMA Settings Tab

**Compare Unit 1:** 

Compare Unit 1 Configuration Disable

**Compare Unit 2:** 

Compare Unit 2 Configuration Disable

**Compare Unit 3:** 

Compare Unit 3 Configuration Disable

**Compare Unit 4:** 

Compare Unit 4 Configuration Disable

**Capture Unit 1:** 

Capture Unit 1 Configuration Disable

**Capture Unit 2:** 

Capture Unit 2 Configuration Disable

**External Event 1 Filtering:** 

Filtering Configuration Disable

**External Event 2 Filtering:** 

Filtering Configuration Disable

**External Event 3 Filtering:** 

Filtering Configuration Disable

**External Event 4 Filtering:** 

Filtering Configuration Disable

**External Event 5 Filtering:** 

Filtering Configuration Disable

**External Event 6 Filtering:** 

Filtering Configuration Disable

**External Event 7 Filtering:** 

Filtering Configuration Disable

**External Event 8 Filtering:** 

Filtering Configuration Disable

**External Event 9 Filtering:** 

Filtering Configuration Disable

**External Event 10 Filtering:** 

Filtering Configuration Disable

**Burst DMA Controller:** 

Burst DMA Configuration Disable

3.7. I2C1 I2C: I2C

#### 3.7.1. Parameter Settings:

#### Timing configuration:

Custom Timing Disabled

I2C Speed Mode Fast Mode \*

I2C Speed Frequency (KHz)400Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled

Timing 0x00B03FDB \*

**Slave Features:** 

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

#### 3.8. MEMORYMAP

mode: Activated

#### 3.9. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

### 3.9.1. Parameter Settings:

#### **General Parameters:**

Clock Prescaler 1 \*
Fifo Threshold 1

Sample Shifting No Sample Shifting

Flash \*

Flash Size 23 \*
Device Type Flas

Chip Select High Time 8 Cycles \*

 Clock Mode
 Low

 Flash ID
 Flash ID 1

 Dual Flash
 Disabled

### 3.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

### 3.10.1. Parameter Settings:

#### **Power Parameters:**

SupplySource PWR\_LDO\_SUPPLY

Power Regulator Voltage Scale Power Regulator Voltage Scale 0

**RCC Parameters:** 

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
CSI Calibration Value 32
HSI Calibration Value 64

**System Parameters:** 

VDD voltage (V) 3.3

Flash Latency(WS) 4 WS (5 CPU cycle)

Product revision rev.V

**PLL range Parameters:** 

PLL1 clock Input range

PLL2 input frequency range

Between 8 and 16 MHz

PLL3 input frequency range

Between 8 and 16 MHz

PLL1 clock Output range

Wide VCO range

PLL2 clock Output range

MEDIUM VCO range

PLL3 clock Output range

MEDIUM VCO range

#### 3.11. SPI1

# Mode: Full-Duplex Master 3.11.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format Motorola

Data Size 4 Bits

First Bit MSB First

**Clock Parameters:** 

Prescaler (for Baud Rate) 128 \*

Baud Rate 121.875 KBits/s \*

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

**Advanced Parameters:** 

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

Fifo Threshold 01 Data

Tx Crc Initialization Pattern

Rx Crc Initialization Pattern

All Zero Pattern

All Zero Pattern

Nss Polarity

Nss Polarity Low

Master Ss Idleness00 CycleMaster Inter Data Idleness00 CycleMaster Receiver Auto SuspDisable

Master Keep Io State Master Keep Io State Disable

IO Swap Disabled

#### 3.12. SYS

**Timebase Source: TIM7** 

3.13. TIM2

**Clock Source : Internal Clock** 

3.13.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 480 \*
Counter Mode Up

Counter Period (AutoReload Register - 32 bits value ) 4294967295
Internal Clock Division (CKD) No Division
auto-reload preload Enable \*

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Enable (Trigger delayed for master/slaves simultaneous start)

\*

Trigger Event Selection TRGO Update Event \*

3.14. TIM12

Slave Mode: External Clock Mode 1

**Trigger Source: ITR0** 

3.14.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD) No Division
auto-reload preload Disable

Slave Mode Controller ETR mode 1

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

3.15. UART4

**Mode: Asynchronous** 

### 3.15.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

#### **Advanced Features:**

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable **Data Inversion** Disable Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

### 3.16. USB\_OTG\_FS

Mode: Device\_Only

### 3.16.1. Parameter Settings:

Speed Full Speed 12MBit/s

Enable internal IP DMA Disabled
Low power Disabled
Battery charging Disabled
Link Power Management Disabled
Use dedicated end point 1 interrupt Disabled
VBUS sensing Disabled
Signal start of frame Disabled

#### 3.17. FREERTOS

Interface: CMSIS\_V2

#### 3.17.1. Config parameters:

API:

FreeRTOS API CMSIS v2

**Versions:** 

FreeRTOS version 10.3.1 CMSIS-RTOS version 2.00

MPU/FPU:

ENABLE\_MPU Disabled ENABLE\_FPU Enabled \*

Kernel settings:

USE\_PREEMPTION Enabled

CPU\_CLOCK\_HZ SystemCoreClock

TICK\_RATE\_HZ 1000 56 MAX\_PRIORITIES MINIMAL\_STACK\_SIZE 128 MAX\_TASK\_NAME\_LEN 32 \* USE\_16\_BIT\_TICKS Disabled IDLE\_SHOULD\_YIELD Enabled Enabled USE\_MUTEXES USE\_RECURSIVE\_MUTEXES Enabled USE\_COUNTING\_SEMAPHORES Enabled QUEUE\_REGISTRY\_SIZE 32 \* USE\_APPLICATION\_TASK\_TAG Disabled ENABLE\_BACKWARD\_COMPATIBILITY Enabled USE\_PORT\_OPTIMISED\_TASK\_SELECTION Disabled Disabled USE\_TICKLESS\_IDLE Enabled USE\_TASK\_NOTIFICATIONS

Memory management settings:

RECORD\_STACK\_HIGH\_ADDRESS

Memory Allocation Dynamic / Static

TOTAL\_HEAP\_SIZE 511000 \*

Memory Management scheme heap\_4

**Hook function related definitions:** 

USE\_IDLE\_HOOK Disabled
USE\_TICK\_HOOK Disabled
USE\_MALLOC\_FAILED\_HOOK Disabled

Disabled

USE\_DAEMON\_TASK\_STARTUP\_HOOK Disabled CHECK\_FOR\_STACK\_OVERFLOW Disabled

#### Run time and task stats gathering related definitions:

GENERATE\_RUN\_TIME\_STATS Disabled
USE\_TRACE\_FACILITY Enabled
USE\_STATS\_FORMATTING\_FUNCTIONS Disabled

#### Co-routine related definitions:

USE\_CO\_ROUTINES Disabled MAX\_CO\_ROUTINE\_PRIORITIES 2

#### Software timer definitions:

 USE\_TIMERS
 Enabled

 TIMER\_TASK\_PRIORITY
 2

 TIMER\_QUEUE\_LENGTH
 32 \*

 TIMER\_TASK\_STACK\_DEPTH
 256

#### Interrupt nesting behaviour configuration:

LIBRARY\_LOWEST\_INTERRUPT\_PRIORITY 15
LIBRARY\_MAX\_SYSCALL\_INTERRUPT\_PRIORITY 5

#### Added with 10.2.1 support:

MESSAGE\_BUFFER\_LENGTH\_TYPE size\_t
USE\_POSIX\_ERRNO Disabled

#### **CMSIS-RTOS V2 flags:**

USE\_OS2\_THREAD\_SUSPEND\_RESUME Enabled
USE\_OS2\_THREAD\_ENUMERATE Enabled
USE\_OS2\_EVENTFLAGS\_FROM\_ISR Enabled
USE\_OS2\_THREAD\_FLAGS Enabled
USE\_OS2\_TIMER Enabled
USE\_OS2\_MUTEX Enabled

#### 3.17.2. Include parameters:

#### Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled vTaskDelete Enabled vTaskCleanUpResources Disabled Enabled vTaskSuspend vTaskDelayUntil Enabled vTaskDelay Enabled Enabled xTaskGetSchedulerState xTaskResumeFromISR Enabled xQueueGetMutexHolder Enabled

xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

### 3.17.3. Advanced settings:

#### Newlib settings (see parameter description first):

USE\_NEWLIB\_REENTRANT Enabled \*

#### Project settings (see parameter description first):

Use FW pack heap file Enabled

### 3.18. USB\_DEVICE

### Class For FS IP: Communication Device Class (Virtual Port Com)

### 3.18.1. Parameter Settings:

#### **Basic Parameters:**

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled

USBD\_DEBUG\_LEVEL (USBD Debug Level) 0: No debug message

USBD\_LPM\_ENABLED (Link Power Management) 1: Link Power Management supported

**Class Parameters:** 

USB CDC Rx Buffer Size 2048
USB CDC Tx Buffer Size 2048

### 3.18.2. Device Descriptor:

#### **Device Descriptor:**

VID (Vendor IDentifier) 1155

LANGID\_STRING (Language Identifier) English(United States)

# ModuCard\_nav\_module Project Configuration Report

MANUFACTURER\_STRING (Manufacturer Identifier) STMicroelectronics

**Device Descriptor FS:** 

PID (Product IDentifier) 22336

PRODUCT\_STRING (Product Identifier) STM32 Virtual ComPort

CONFIGURATION\_STRING (Configuration Identifier)

INTERFACE\_STRING (Interface Identifier)

CDC Interface

<sup>\*</sup> User modified value

# 4. System Configuration

# 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_INP10	Analaa mada		n/a	
ADCI	PC0 PC1	_	Analog mode	No pull-up and no pull-down	n/a	
	PA0	ADC1_INP11	Analog mode	No pull-up and no pull-down		
		ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_INP17	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_INP14	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_INP7	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13 (JTMS/SWDI O)	DEBUG_JTMS- SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWC LK)	DEBUG_JTCK- SWCLK	n/a	n/a	n/a	
FDCAN1	PD0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN2	PB12	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_I O2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	QUADSPI_BK1_ NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	QUADSPI_BK1_I	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14- OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3 (JTDO/TRA CESWO)	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_ FS	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USER_LED_1
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USER_LED_2
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STATUS_LED
	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USR_BUTTON
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPS_GEOFENCE_STAT
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPS_RTK_STAT
	PD4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	GPS_EXINTERUPT
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPS_MODE_SELECT
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPS_NRESET
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BOOT_EN
	PE0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	IMU_EXINTERUPT
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_NRESET

# 4.2. DMA configuration

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nothing configured in DMA service

### 4.3. BDMA configuration

nothing configured in DMA service

### 4.4. MDMA configuration

MDMA Request	Channel	Trigger Mode	Priotity
QUADSPI_TC	MDMA_Channel0	Full transfer *	Very High *

### QUADSPI\_TC: MDMA\_Channel0 DMA request Settings:

Buffer Transfer Length: 1
Data Mask: 0

Source Burst Size: Single transfer

Destination Burst Size: Single transfer

Block Data Length: 0
Destination Address: 0
Destination Block Address 0

Offset:

Address Mask: 0

Data Alignement: N/A

Source Block Address 0

Offset:

Endianness: Little endianness preserved

Source Address: 0

Source Increment mode: Increment by a byte

Block Count: 0

**Destination Increment** 

Increment by a byte

mode:

Source Data Width: Byte
Destination Data Width: Byte

# 4.5. NVIC configuration

# 4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM7 global interrupt	true	15	0
USB On The Go FS global interrupt	true	5	0
MDMA global interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
EXTI line0 interrupt		unused	
EXTI line4 interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
FDCAN1 interrupt 0	unused		
FDCAN2 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
FDCAN2 interrupt 1		unused	
TIM2 global interrupt		unused	
I2C1 event interrupt		unused	
I2C1 error interrupt		unused	
SPI1 global interrupt		unused	
TIM8 break interrupt and TIM12 global interrupt		unused	
UART4 global interrupt		unused	
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts		unused	
FDCAN calibration unit interrupt		unused	
FPU global interrupt		unused	
QUADSPI global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
HRTIM master timer global interrupt		unused	
HRTIM timer A global interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
HRTIM fault global interrupt	unused		
HSEM1 global interrupt		unused	

# 4.5.2. NVIC Code generation

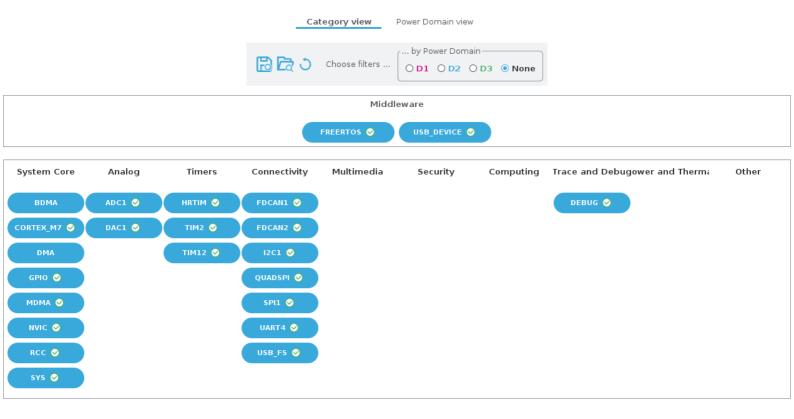
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM7 global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true
MDMA global interrupt	false	true	true

<sup>\*</sup> User modified value

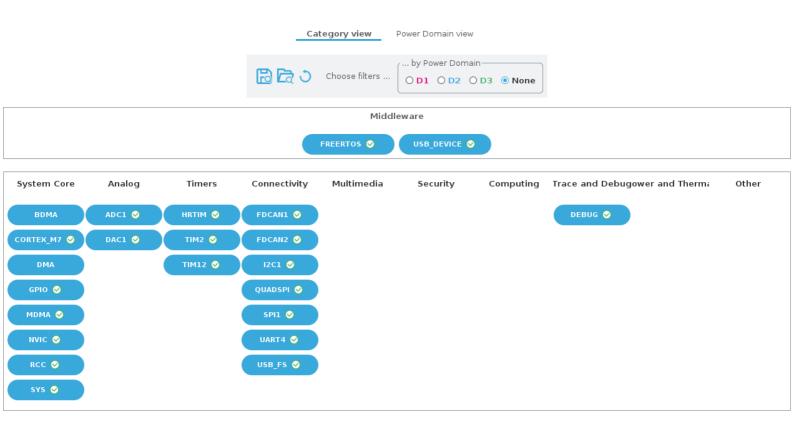
# 5. System Views

5.1. Category view

5.1.1. Current



### 5.1.2. Without filters



### 5.2. Power Domain view

Category view Power Domain view



# 6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32h7\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32h7\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32h7-svd.zip

Description

Presentations https://www.st.com/resource/en/product\_presentation/microcontrollers\_st

m32h7\_series\_product\_overview.pdf

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stm8\_embedded\_software\_solutions.pdf

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