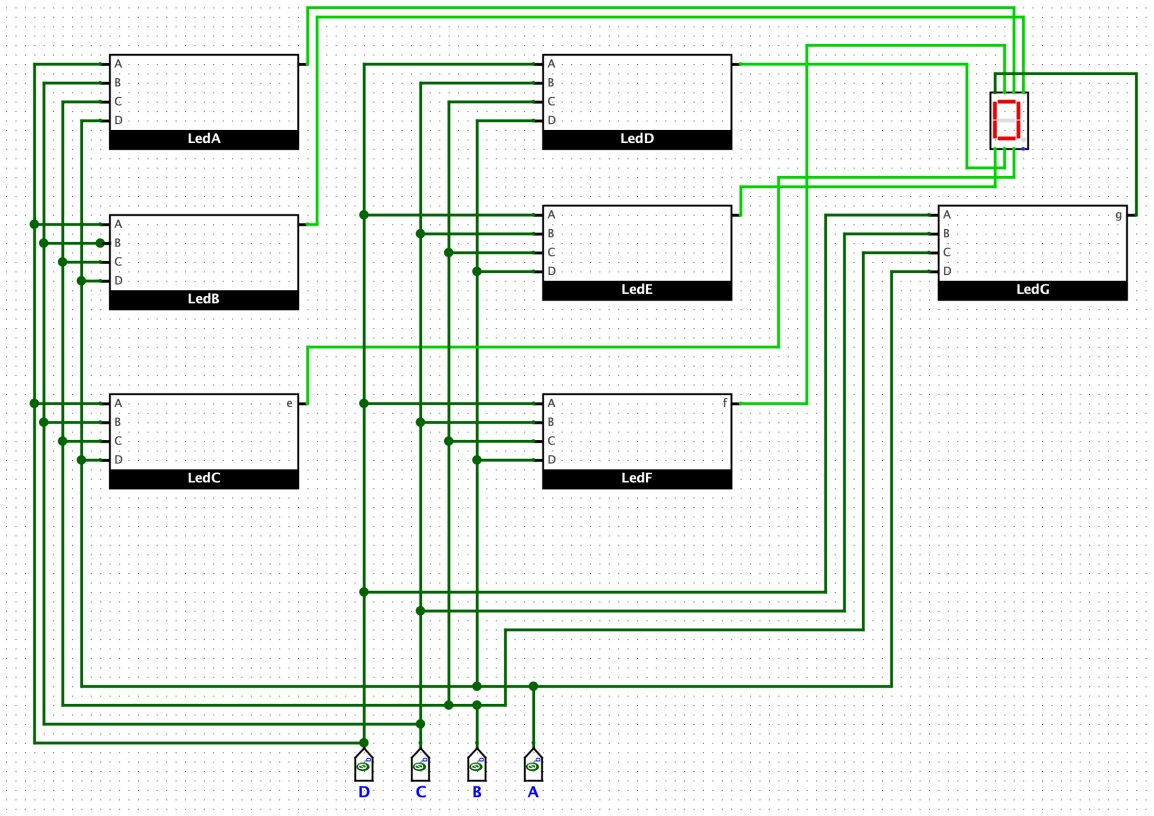
Lab 3

Problem 1.



This is the main structure using a common Cathode.

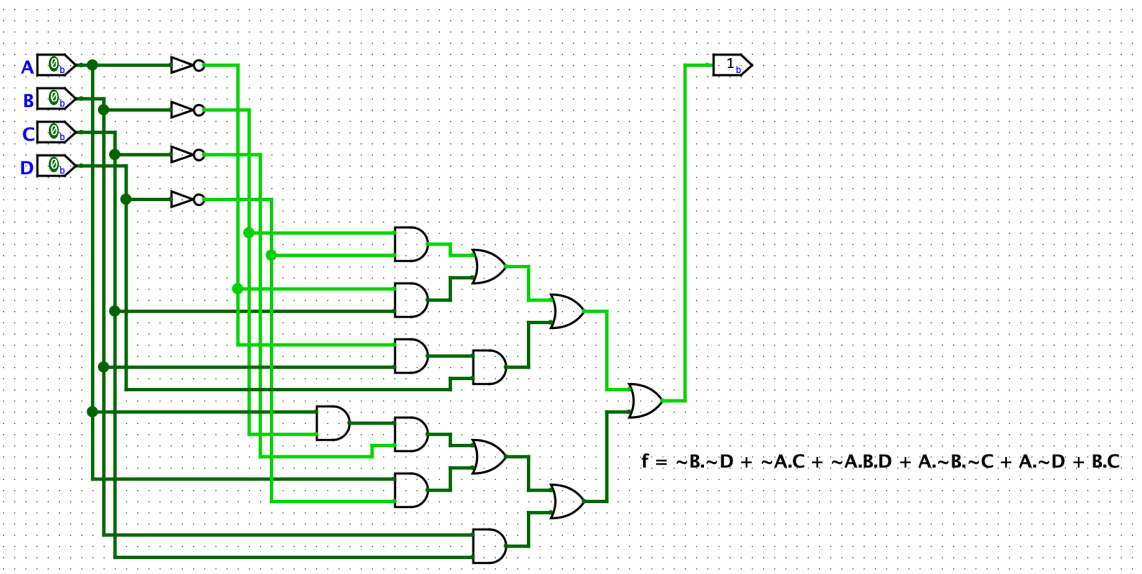


Figure 1: Led A

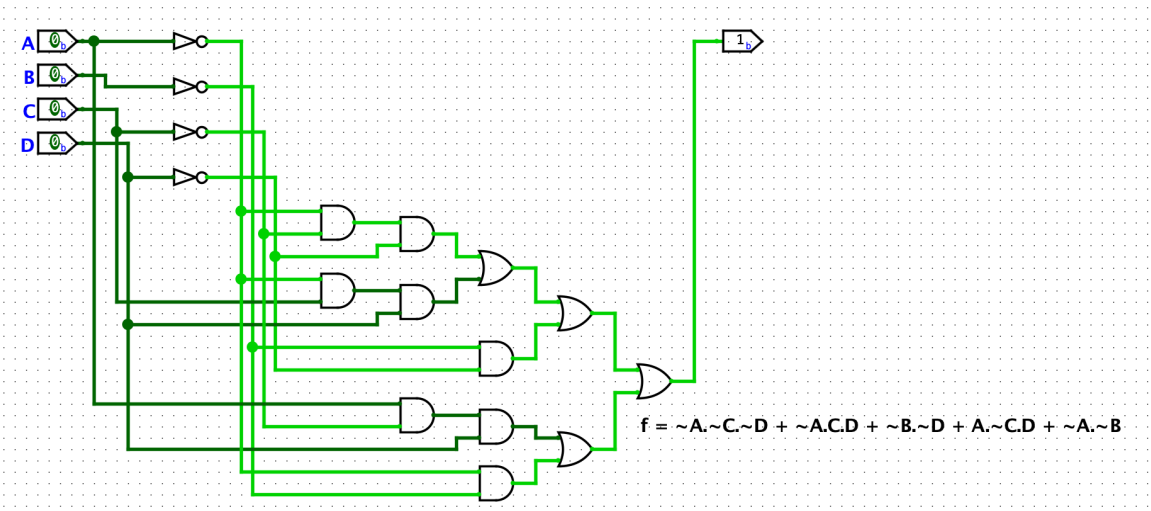


Figure 2: Led B

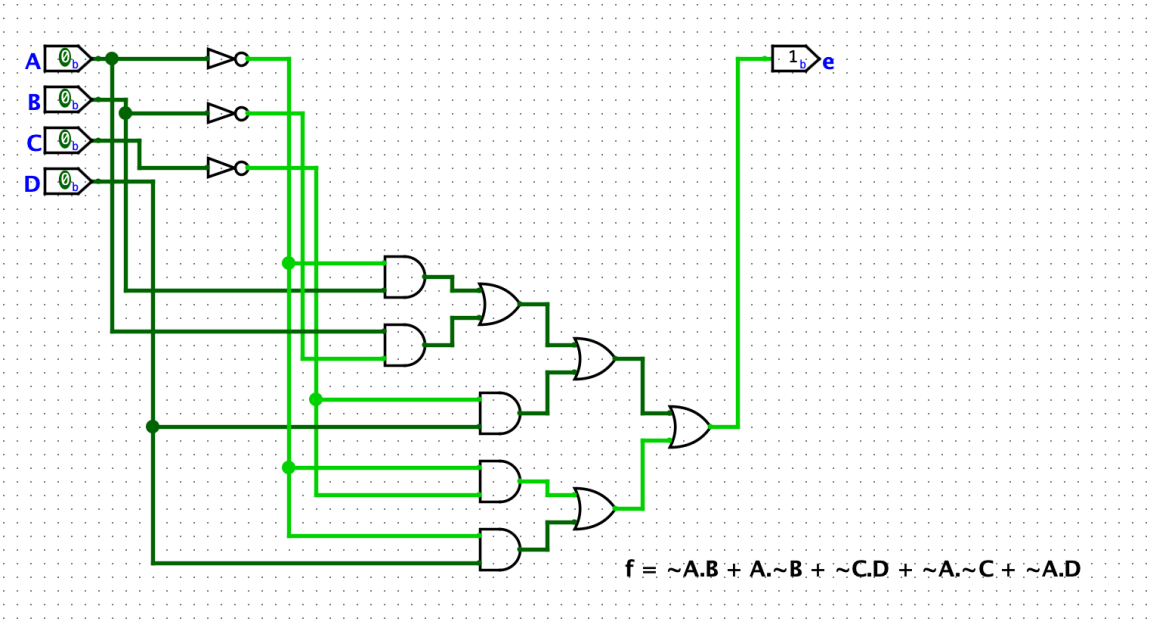


Figure 3: Led C

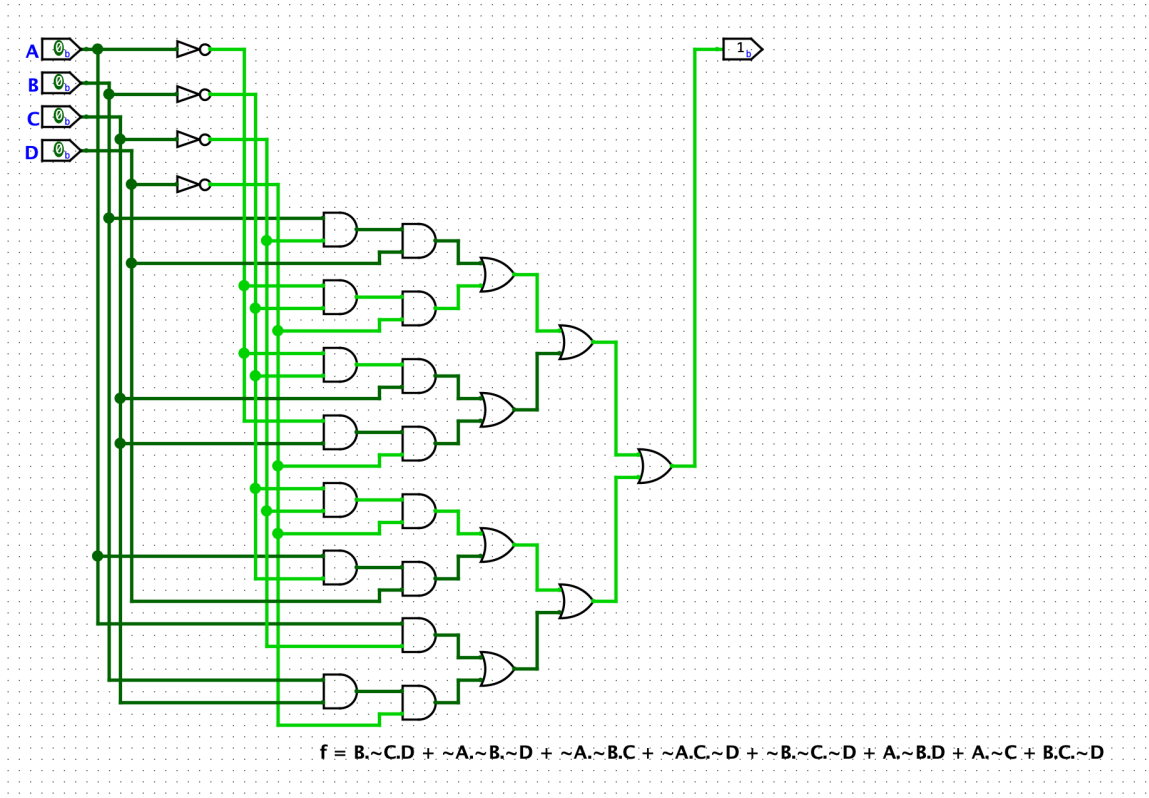


Figure 4: Led D

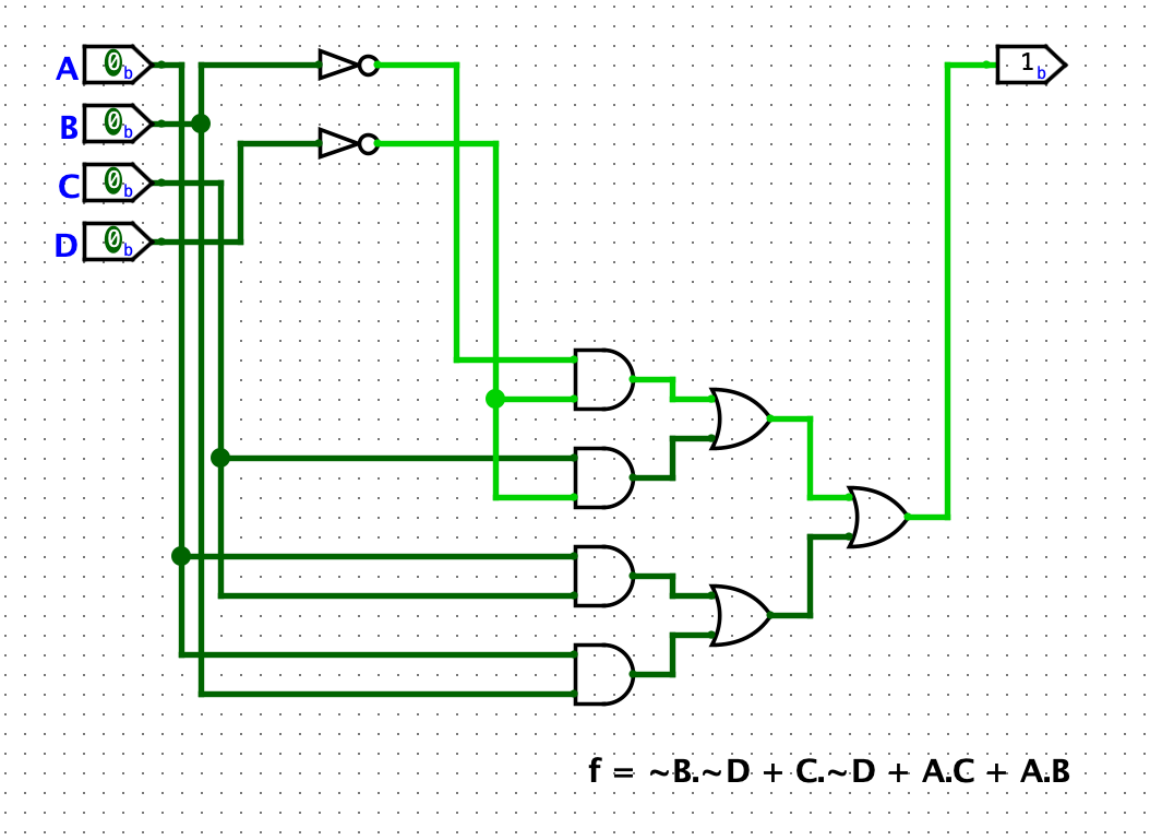


Figure 5: Led E

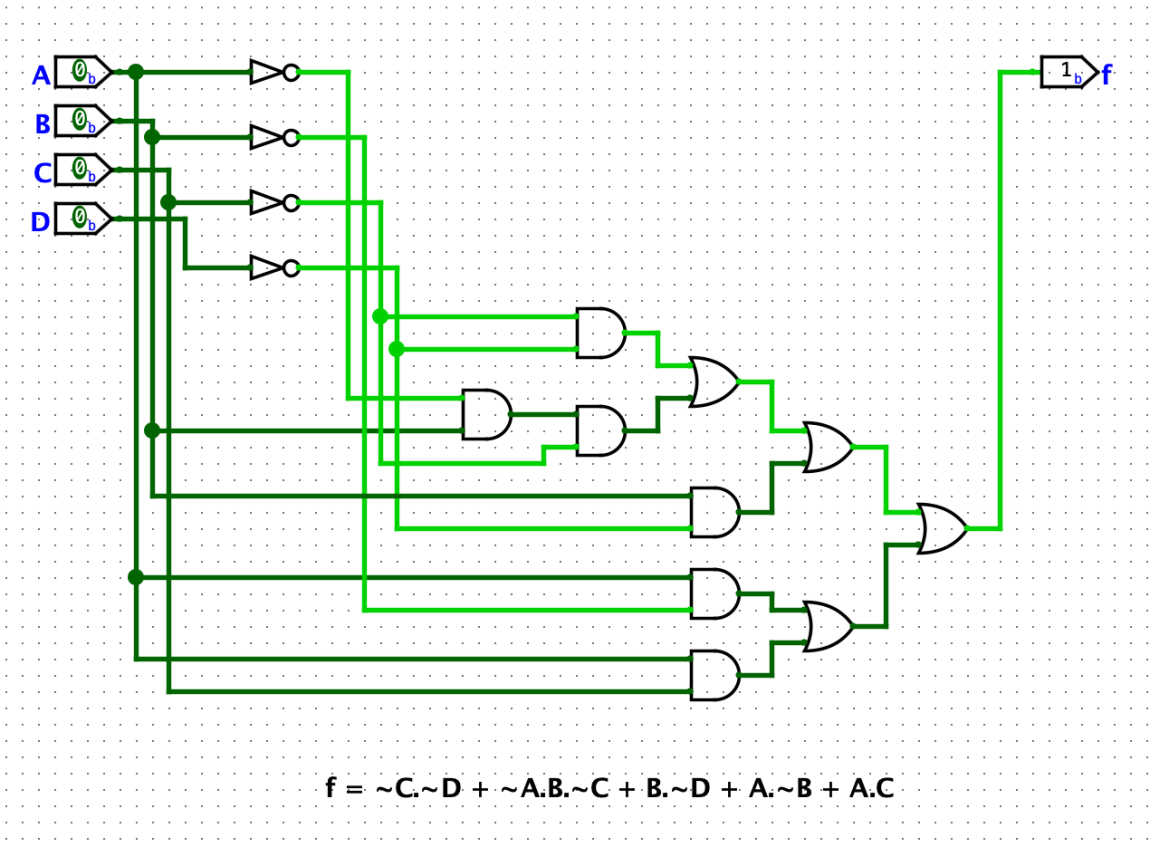


Figure 6: Led F

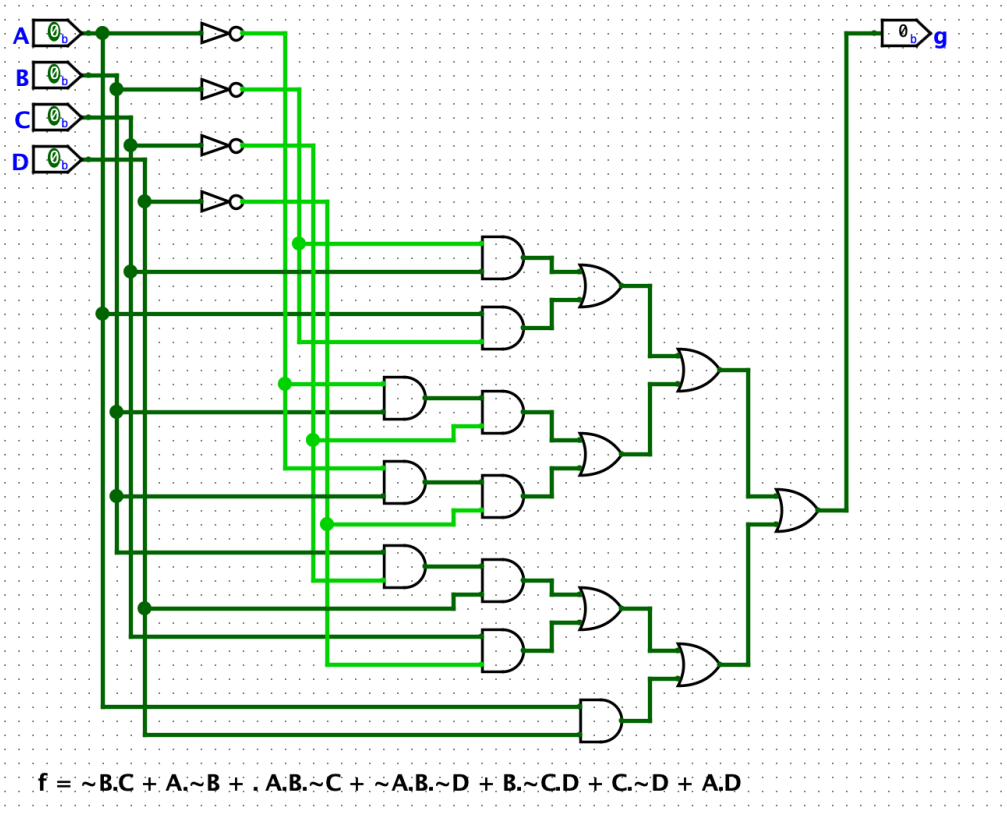


Figure 7: Led G

Problem 2.

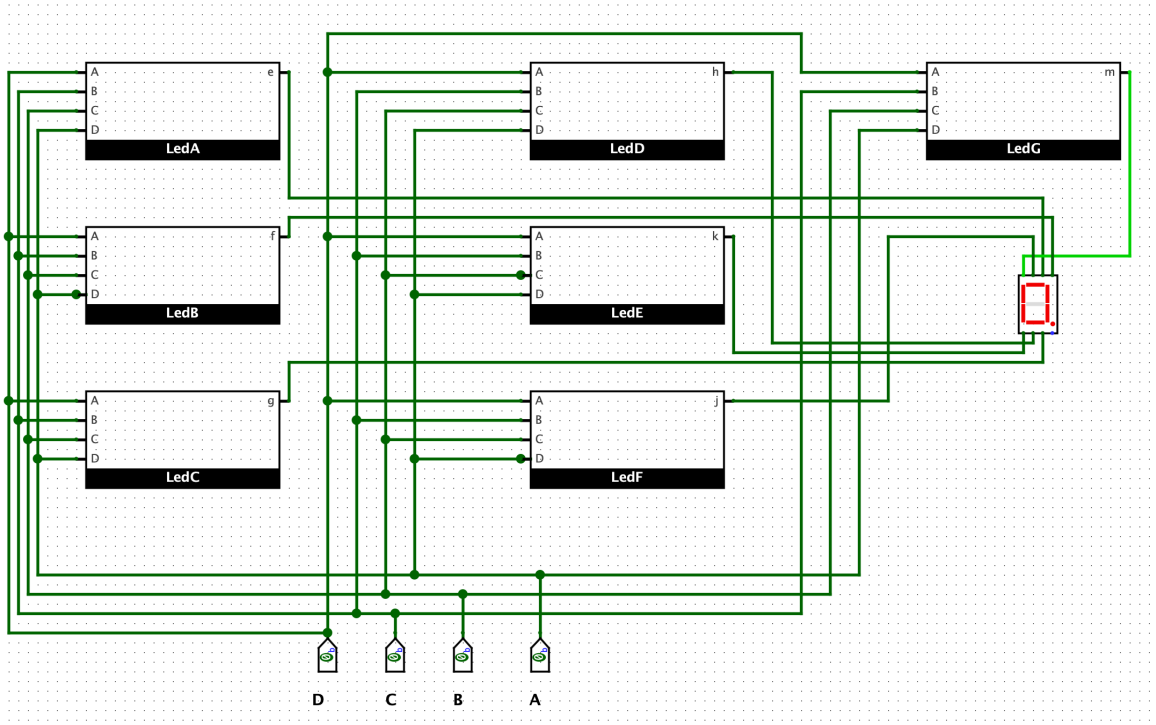


Figure 8: Main common Athode

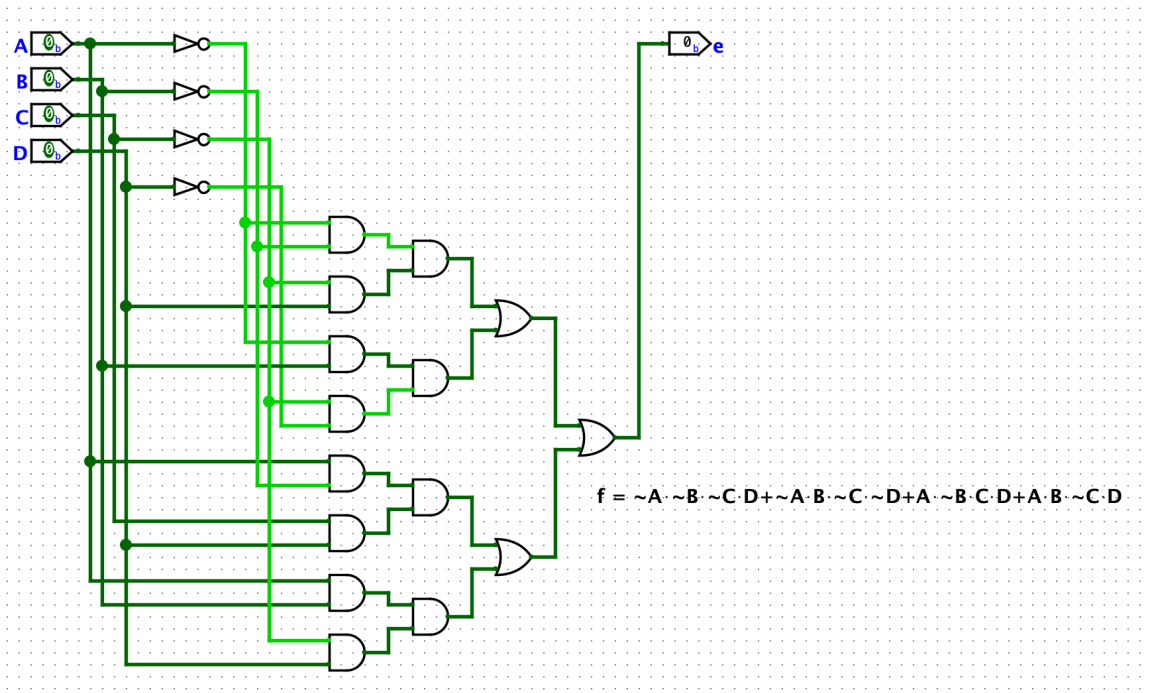


Figure 9: Led A

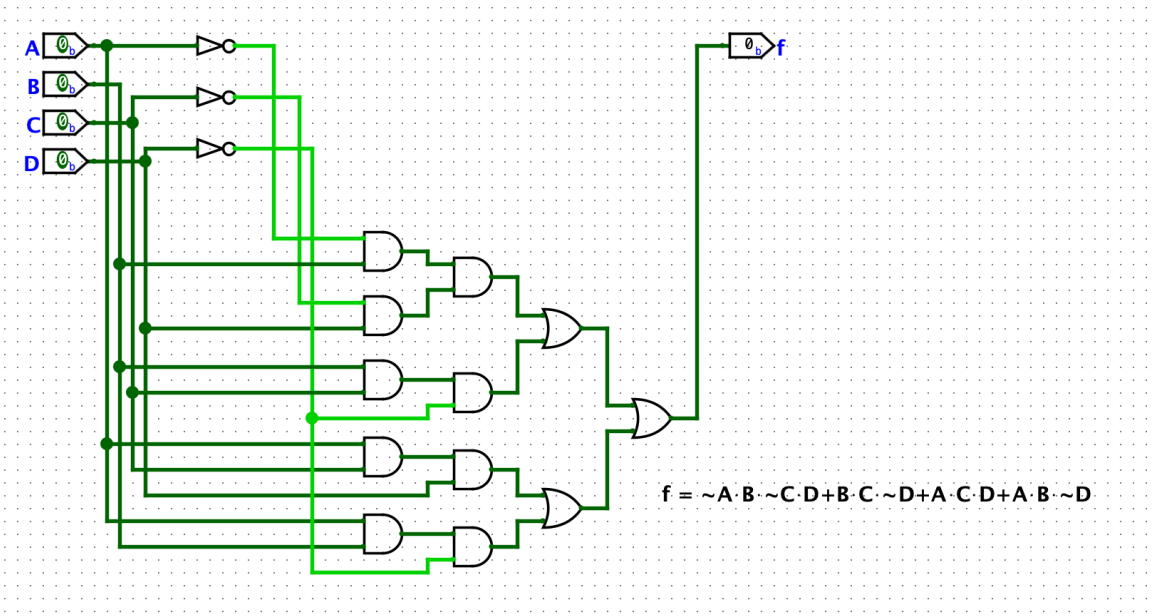


Figure 10: Led B

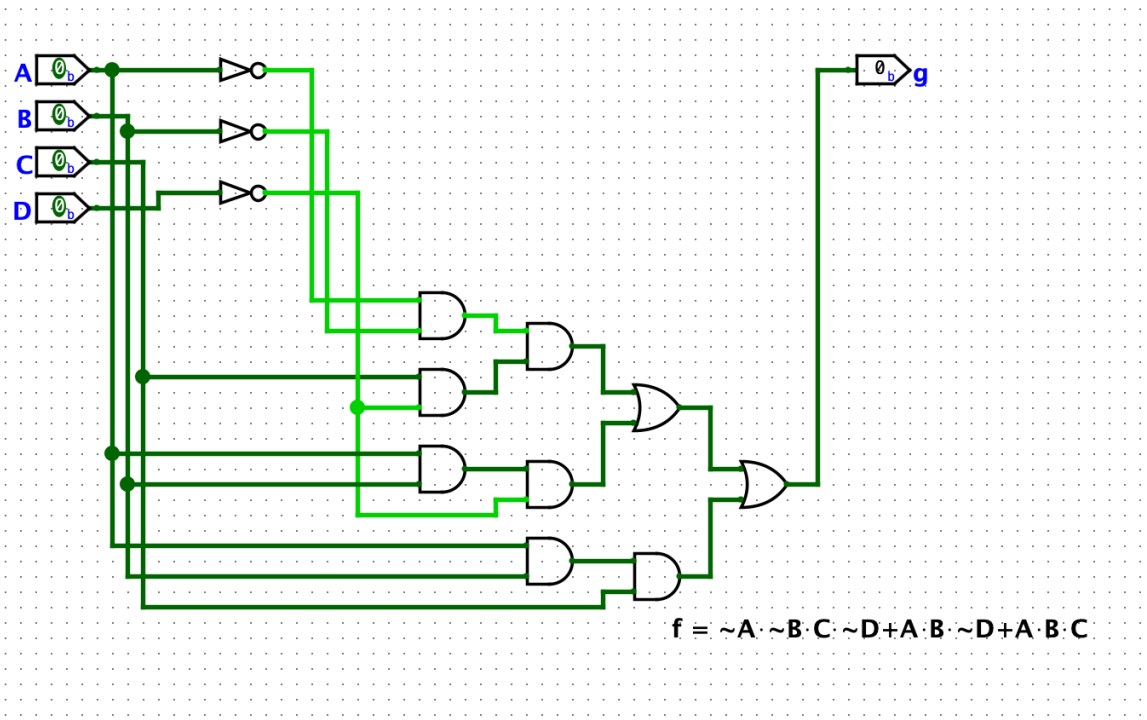


Figure 11: Led C

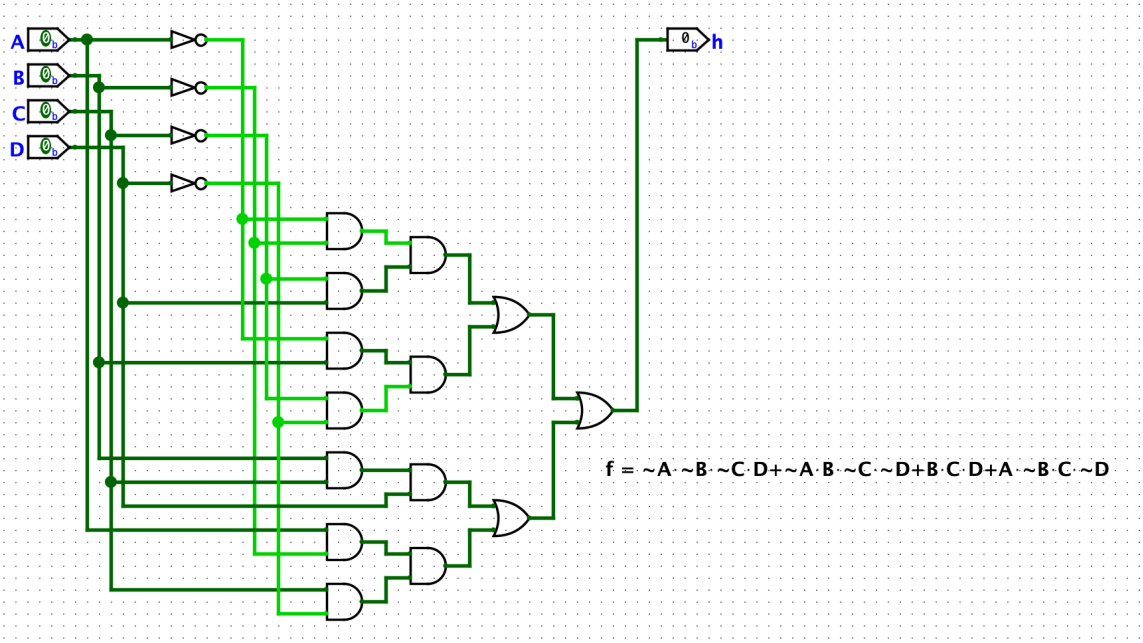


Figure 12: Led D

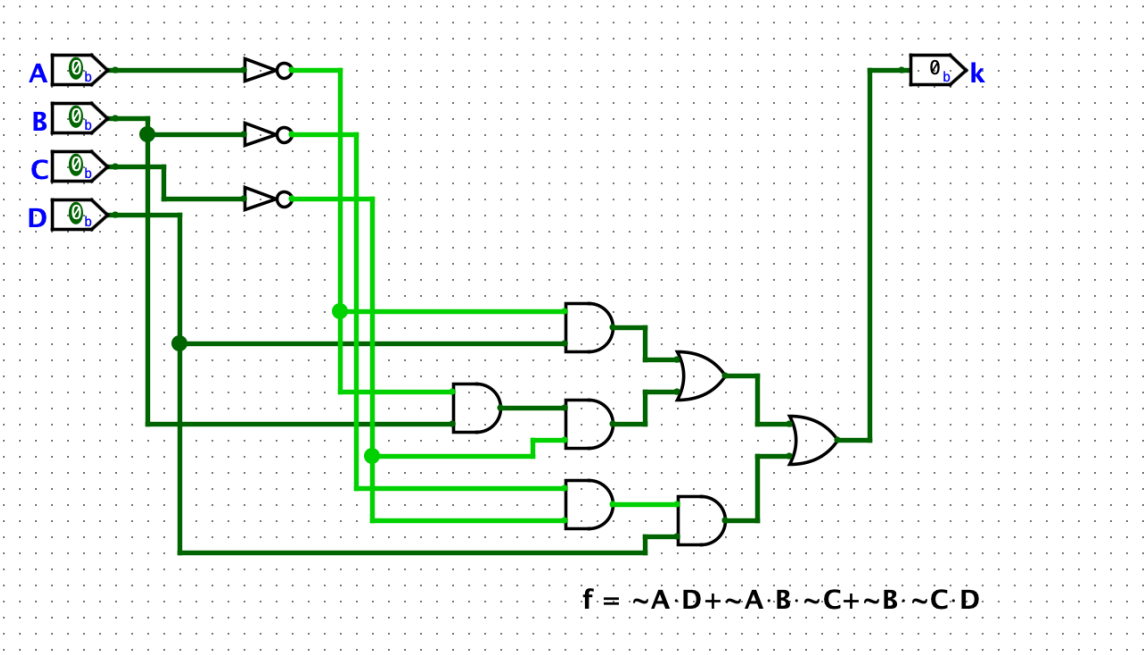


Figure 13: Led E

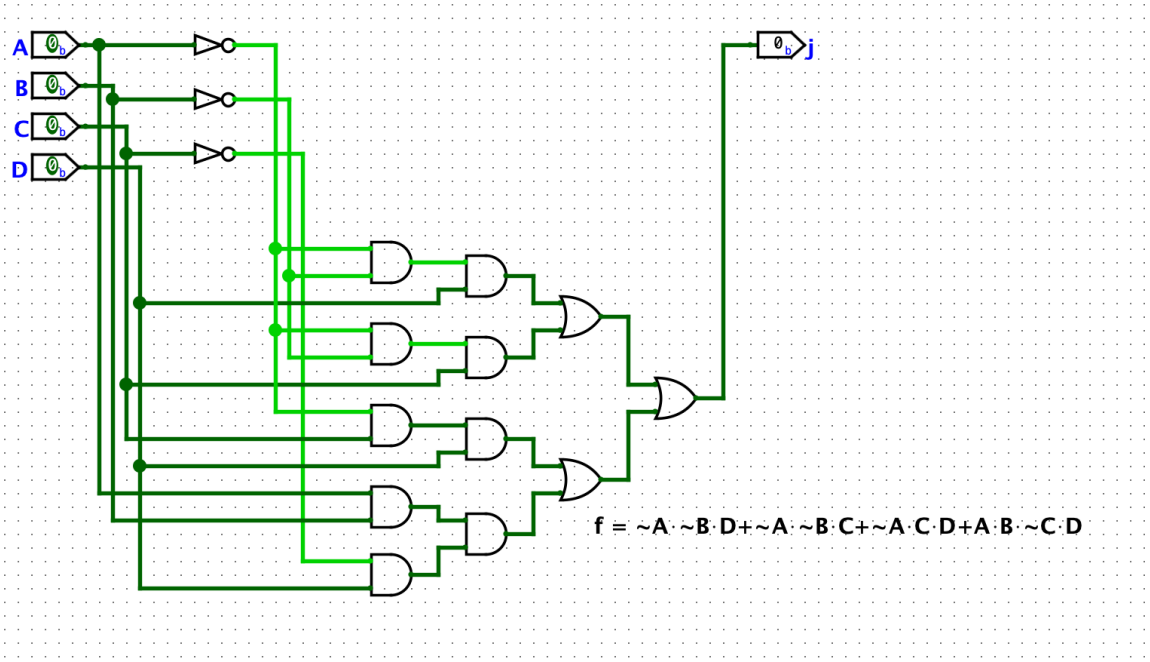


Figure 14: Led F

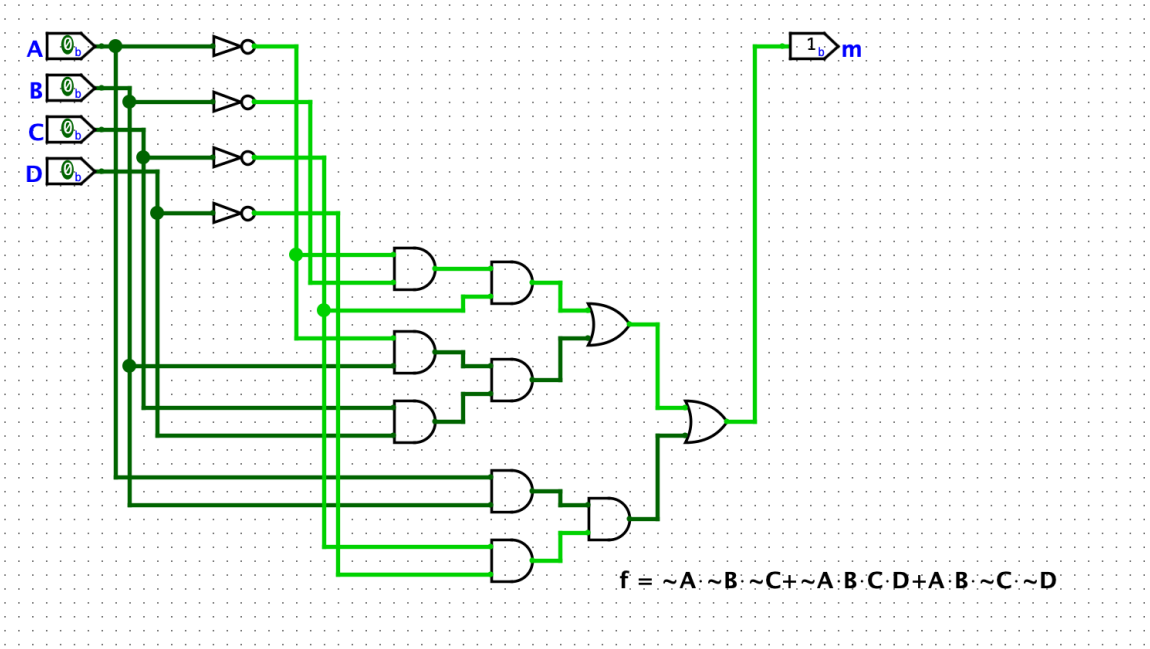
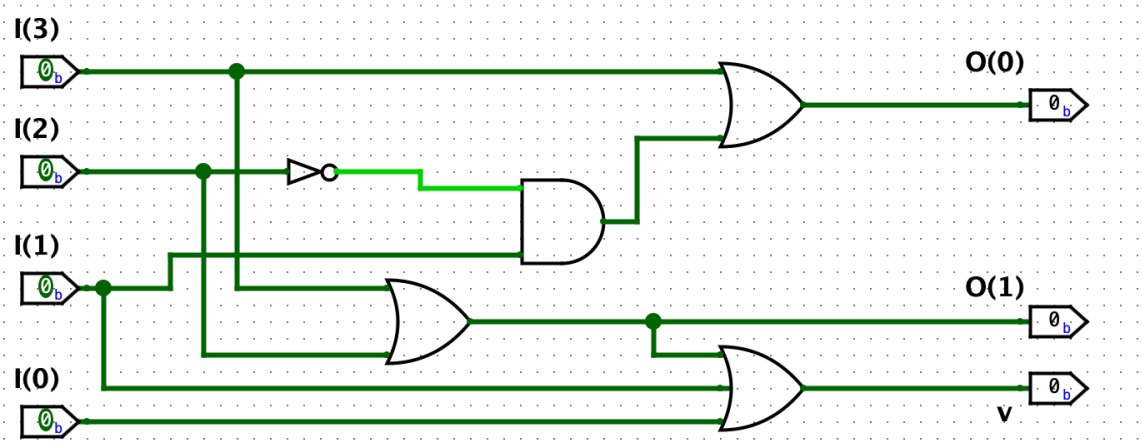


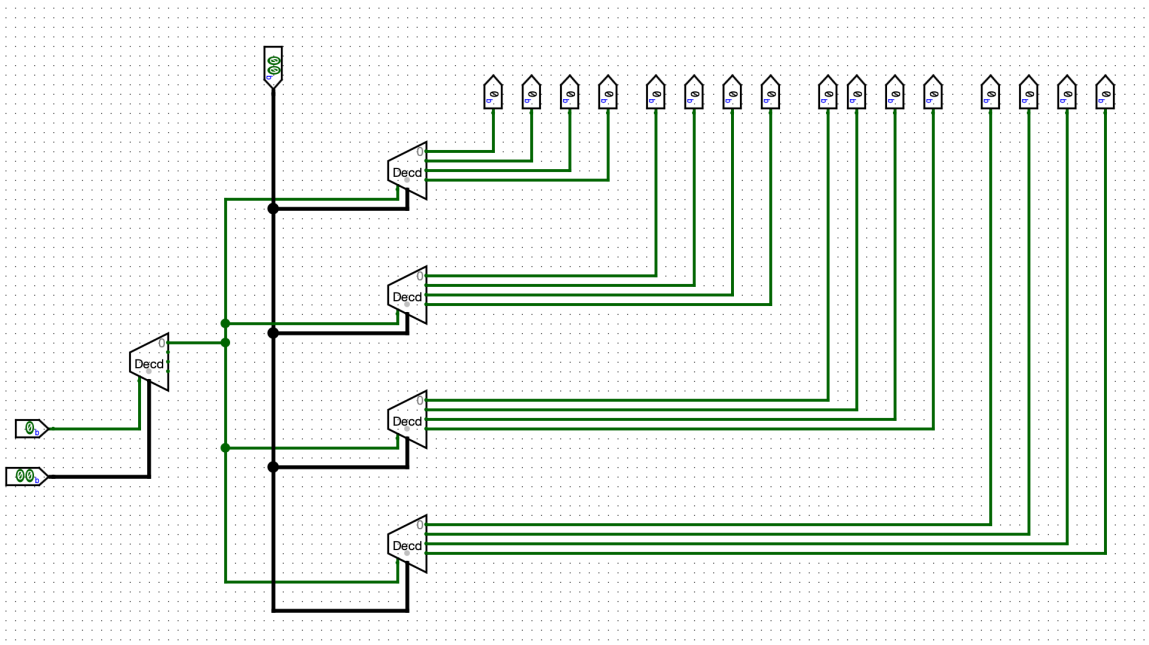
Figure 15: Led G

Problem 3.



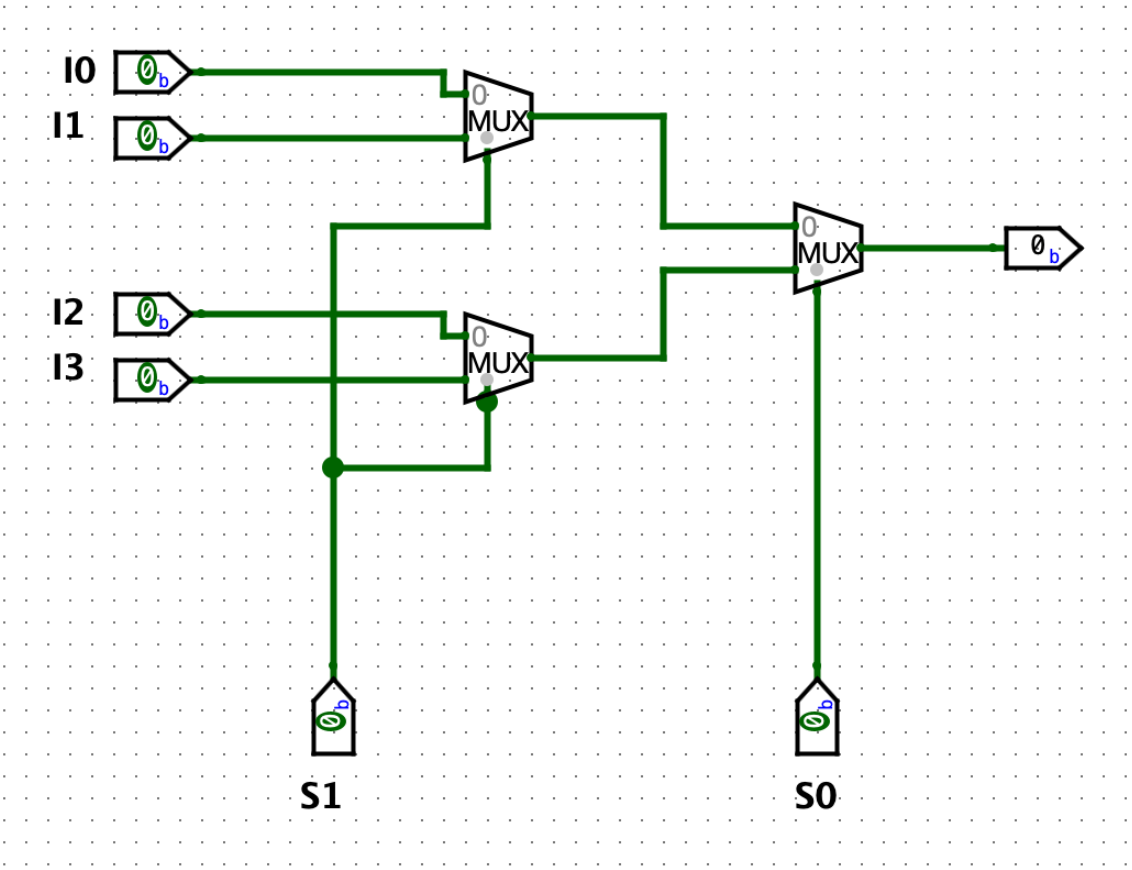
The Priority Encoder operates by indicating the position of the highest priority input. The "v" output will consistently reflect "1" if any inputs are "1," and vice versa. Outputs O(0) and O(1) indicate the position.

Problem 4.



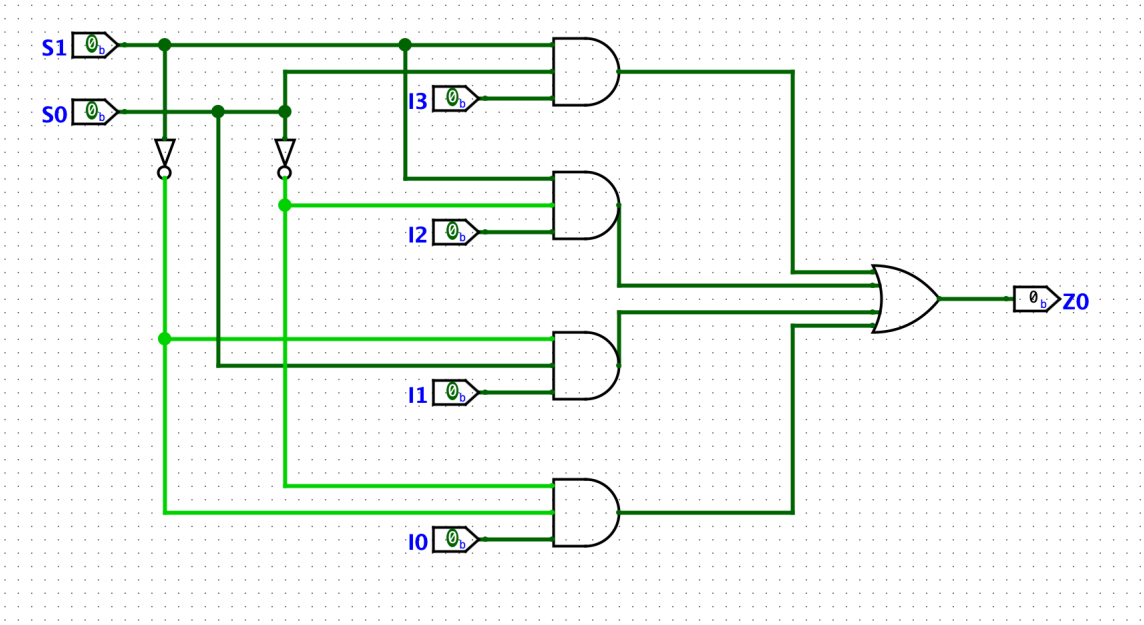
In this exercise, we will design a Decoder $4 \rightarrow 16$ from Decoder $2 \rightarrow 4$. We expand the input and output size and use multiple instances of the Decoder 2-to-4 and additional logic to connect and control the outputs.

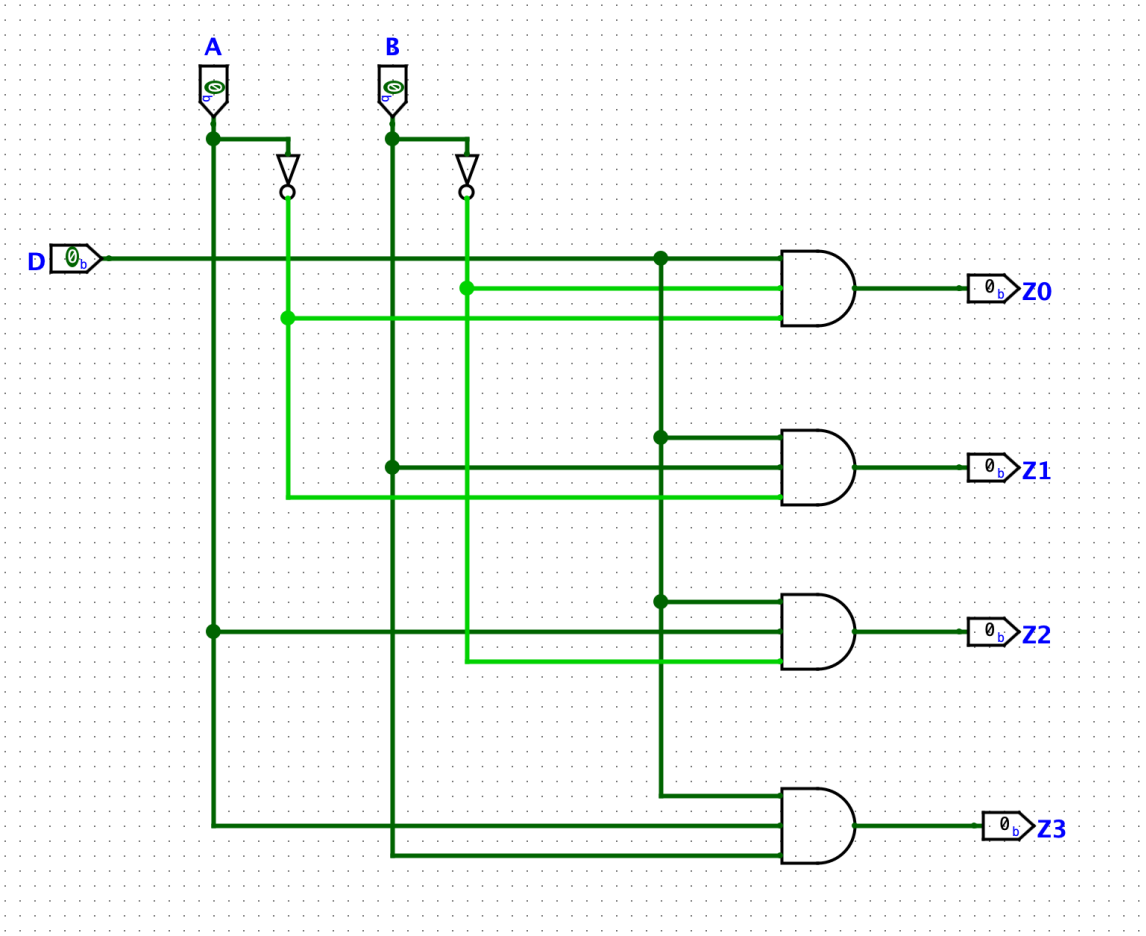
Problem 5.

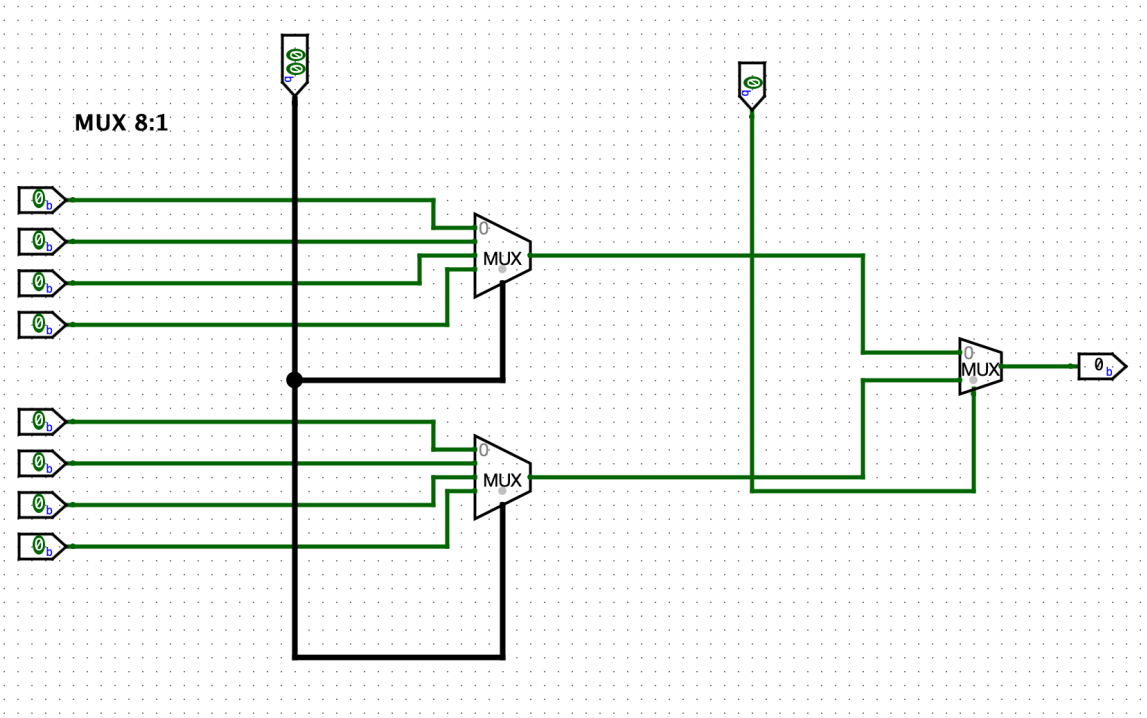


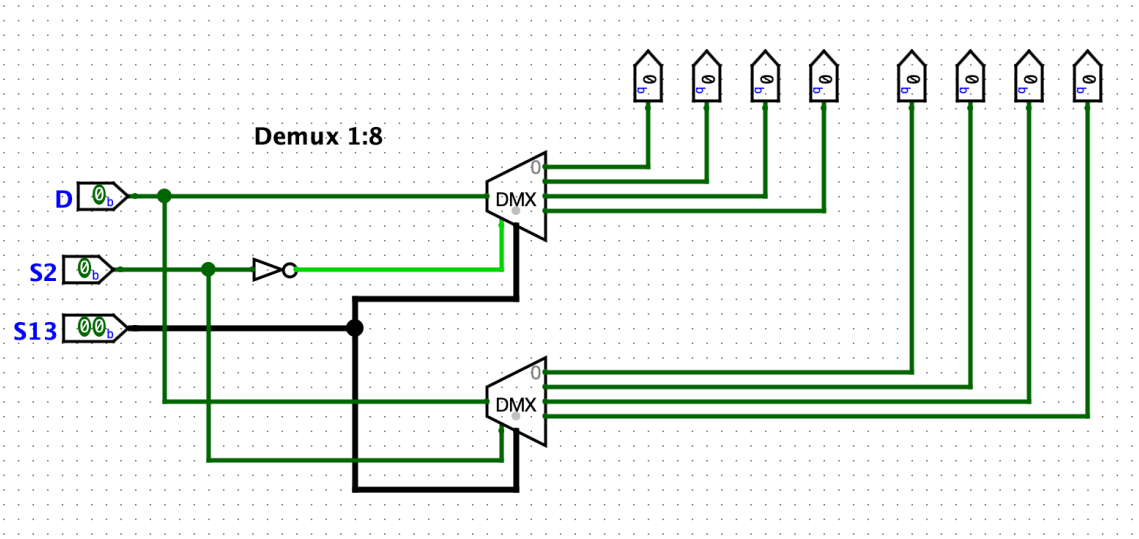
We will use a hierarchical approach, that the first select bit will connect to the 2 first MUX and the second select bit will connect to the second MUX.

Problem 6.




A
B
D
Z0
Z1
Z2
Z3


MUX 8:1
MUX
MUX
MUX


Demux 1:8
D
S2
S13
DMX
DMX