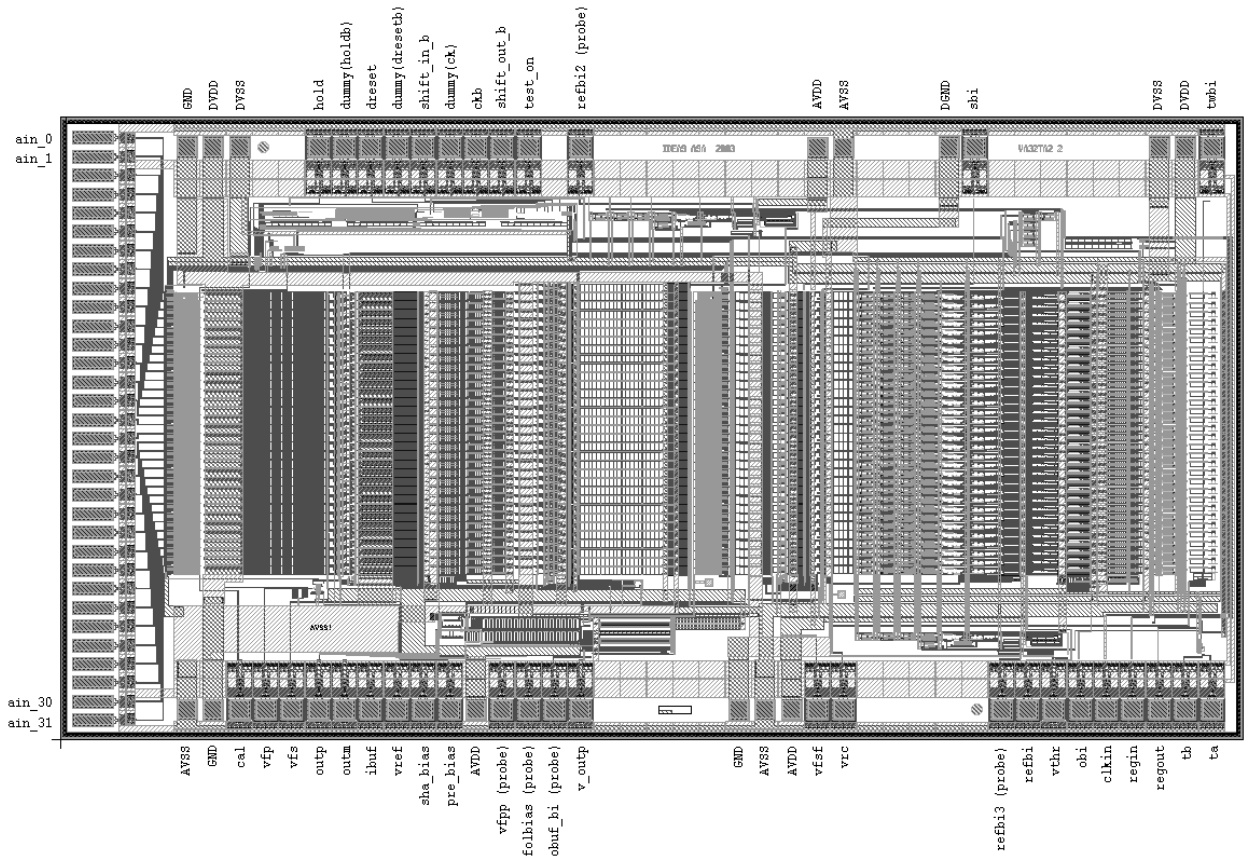
# Va32Ta2_2

## Ver. 0.1

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# 1 General

- Description:

  32 channel low-noise/low power high dynamic range charge sensitive fast triggering circuit of the VATA family, with simultaneous sample-and-hold and calibration facilities.

  For the rest of the this text, dummy shaper is referred to as reference shaper.

  The preamplifier-shaper subcircuit provides a multiplexed current and voltage readout with a global 5-bit DAC trimmed reference.

  The chip includes for each channel a fast CR-RC shaper followed by a level-sensitive discriminator. The trigger signals from each channel are wire-or'ed together onto one common trigger output. To reduce threshold-spread, this version has 4-bit trim-DACs on each discriminator and an additional global threshold
  5-bit trim DAC.

  All biases are internally generated with each being optionally adjustable externally from corresponding overriding pads.

  It's possible to test a channel while the rest of the channels are performing direct measurement.

# 2 Physical

- Process: 0.8 µm N-well CMOS, double-poly, double metal.

- Die size: 6300 µm x 3310 µm (including scribe)
  Thickness: ~ 600 µm

- Input/ Output bonding pads: Single row.
  Pad size: 50 µm x 200 µm
  Pad pitch: 100 µm

- Output, control and power pads: Single row.
  Pad size: 90 µm x 90 µm
  Pad pitch: 140 µm

# 3 Electrical

To be confirmed by measurements.

| | | | |
|---|---|---|---|
| Power rails: | Vdd = +2 V, Vss = -2 V<br>Each with separate connections for analog (avdd and avss) and digital sections (dvdd, dvss) of the chip. | | |
| Back contact: | metalized, connect to avss (-2V) | | |
| Current draw: (Quiescent, typical values) | dvdd | | 2.88 mA |
| | dvss | | -2.88 mA |
| | avdd | 500 µA pre_bias | 10.84 mA |
| | avss | 500 µA pre_bias | -28.38 mA |
| | gnd | 500 µA pre_bias | 17.54 mA |

Input bias currents: (all driven to devices (e.g. resistors) referred to avdd)

| Nominal values | |
|---|---|
| pre_bias: | 500 µA |
| sha_bias: | 22 µA |
| sbi: | 70 µA |
| ibuf: | 220 µA |
| obuf_bi: | 1 mA |

(Ibuf and obuf_bi active only during mux readout)

| | | |
|---|---|---|
| Peaking time: | Nominal: | Slow shaper: 2µs<br>Fast shaper: 75ns |
| Power dissipation: (Typical values) | Quiescent: | 96 mW (3 mW/channel) |

ESD Protection:
Inputs: diode
Control:
~ 600 Ω series resistor and protection diodes to Vdd and Vss, except for the following signals:
*cal, outp, outm, v_outp, vthr.*

Input stage:
Input device: PMOS referenced to gnd
Signal input potential: ~ -1.2 V to -1.3 V

Gain:
0.8 mV/fC and 0.8 µA/fC for multiplexed output

Linear range:
± 139 MIPs (can handle both signal polarities)
(1 MIP = 3.6 fC)

| | |
|---|---|
| Noise (ENC): | Typical values: ( *to be confirmed through measurement* )<br>710 + 3 /pF $e^-$ @ 2 µs |
| Readout: | The analog readout is controlled via 32-bit (output) shift register.<br>Analog outputs (outp, outm) of two or more chips can be connected in parallel to drive the inputs of an external, differential, transimpedance amplifier. An additional analog voltage output (vout_p) is available.<br><br>The triggering section's 32-channel wire-or'ed output circuitry generates a chip-global trigger signal on $t_a$ and $t_b$, and width-adjustable through the twbi analog control signal. |
| Calibration/test: | Voltage step applied via external 1.8 pF capacitor to the cal-input. 2 mV step represents 1 MIP (=22400 $e^-$ or 3.6 fC). Some additional noise has to be taken into account in test mode. Calibration signal can be given to one channel in a given chip at any time. The channel is selected via a 32-bit (input) shift register. |

# 4 Pad description

## 4.1 List of pads

The output, control and power pads are listed clockwise from upper left corner (see chip plot). Positive current direction into the chip.

| Pad name | Type | Description | Nominal value |
|---|---|---|---|
| Gnd | p | signal ground | 0 V |
| Dvdd | p | digital vdd | +2 V |
| Dvss | p | digital vss | -2 V |
| hold | di | used to hold analog data, see fig.1 | Logical |
| dummy (holdb) | di | *) | Logical |
| dreset | di | reset of digital part | Logical |
| dummy (dresetb) | di | *) | Logical |
| Shift_in_b | di | start pulse for read-out | Logical |
| dummy (ck) | di | *) | Logical |
| Ckb | di | clock for read-out register, see fig.1 | Logical |
| Shift_out_b | do | Signalling end of read-out. Can be used as shift_in_b for next chip. | Logical |
| test_on | di | Turns chip into test-mode | Logical |
| *Refbi2* | *ai* | *Bias for Vref-DAC* | *-365 mV 160µA* |
| Avdd | p | Anaolg vdd | +2 V |
| Avss | p | Analog vss (+ chip backplane) | -2 V |
| Dgnd | p | Ground | 0 V |
| Sbi | ai | Bias current for fast shaper-amplifiers. | -611 mV 70 µA |
| Dvss | p | digital vss | -2 V |
| Dvdd | p | digital vdd | +2 V |
| Twbi | ai | Bias adjust for trigger width Default: approx. 100 ns | 529 mV 32 µA |
| Ta | ao | Trigger out | current |
| Tb | ao | Trigger out inverted | current |
| regout | do | Output of the disable register | Logical |
| RegIn | di | Input to the disable register | Logical |
| ClkIn | di | Clock Input for disable register | Logical |
| Obi | ai | Bias current to Discriminator | -876 mV 144 µA |
| Vthr | ai | Discriminator threshold | ± 50mV (e.g) |
| Refbi | ai | Bias for trim-DACs | -816 mV 16 µA |
| *Refbi3* | *ai* | *Bias for global threshold DAC* | *-816 mV 32 µA* |

| | | | |
|---|---|---|---|
| Vrc | ai | Control voltage for High-pass filter resistor (NMOS) in front of Discrim. | 1.4 V |
| Vfsf | ai | Control voltage for feedback resistor (NMOS) in fast shaper | 850 mV |
| Avdd | p | Anaolg vdd | +2 V |
| Avss | p | Analog vss (+ chip backplane) | -2 V |
| Gnd | p | Ground | 0 V |
| V_outp | Ao | Output from analog output voltage buffer | Voltage |
| *Obuf_bi* | *ai* | *Bias current for voltage output buffer* | *-502 mV 1 mA* |
| *Folbias* | *ai* | *Bias current for preamplifier buffer* | *891 mV 90 µA* |
| *Vfpp* | *ai* | *Bias voltage for vfp, positive charges* | *-1.85 V* |
| Avdd | p | Anaolg vdd | +2 V |
| Pre_bias | ai | Bias current for pre-amplifiers. | -438 mV 500 µA |
| Sha_bias | ai | Bias current for shaper-amplifiers. | -620 mV 22 µA |
| Vref | ao | Internally generated reference voltage for the current output buffer. | -836 mV |
| Ibuf | ai | Bias-current for output-buffer. | 440 mV 220 µA |
| Outm | ao | Negative output signal (current) | |
| Outp | ao | Positive output signal (current) | |
| Vfs | ai | Control voltage to feedback resistance in shaper-amplifier | Pos. Q: -550mV Neg.Q: -450mV |
| Vfp | ai | Control voltage to feedback resistace in pre-amplifier, negative charges. For pos. Q see vfpp. | -220 mV |
| Cal | ai | Test input signal | 1 MIP |
| Gnd | p | signal ground | 0 V |
| Avss | p | Analog vss (+ chip backplane) | -2 V |

p = power, di = digital in, do = digital out, ai = analog in, ao = analog out

**Table 1:** Listing of input and output pads.

*) Unused pads which can be used to connect complementary signals to the effective ones in order to minimise clock-feedthrough. These ‘dummy’ signals are recommended for high performance.

## 4.2 Chip plot

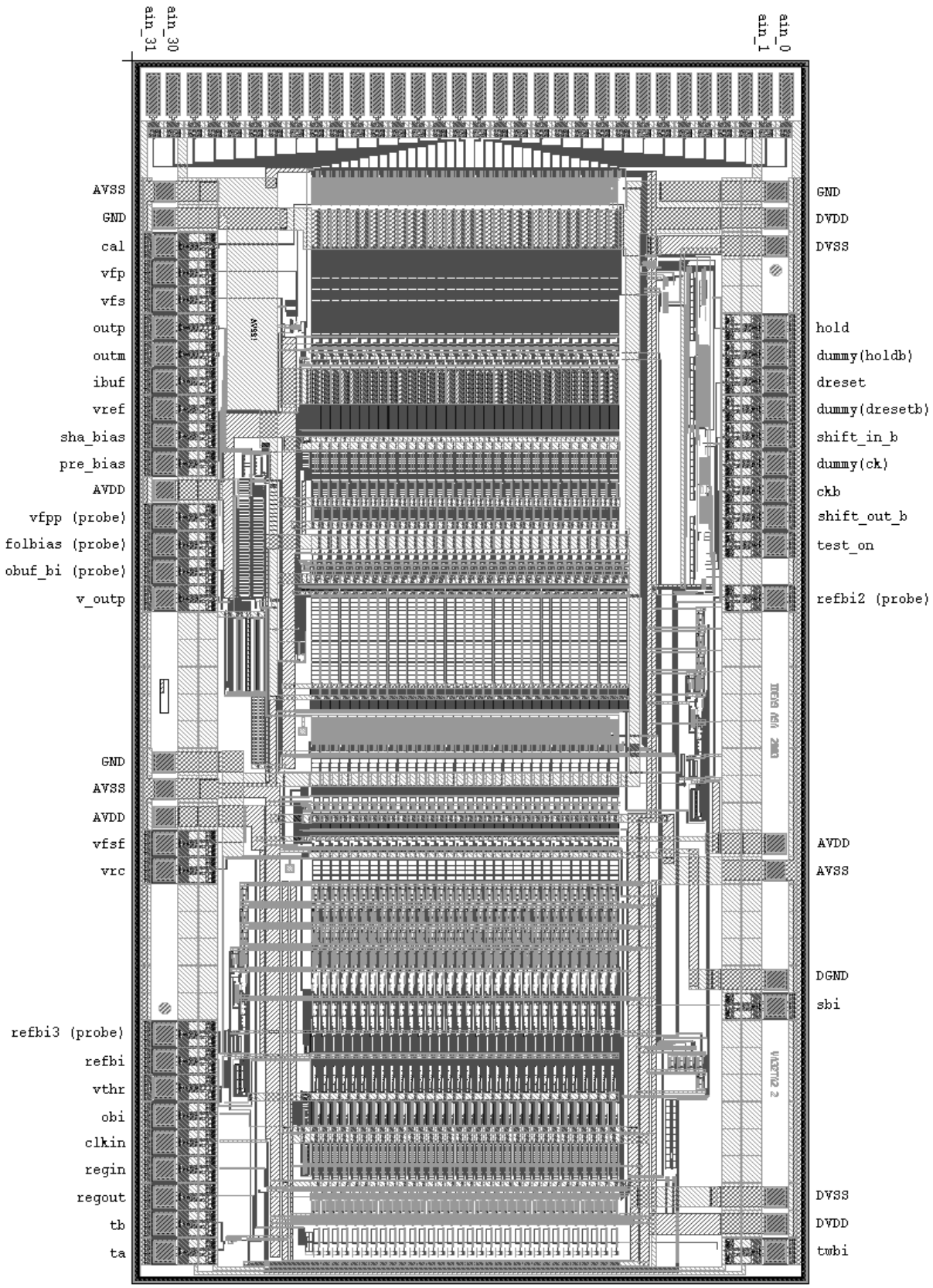


**Fig. 1 VA32TA2 chip plot (**Chip size: 6300µm * 3310 µm**)**

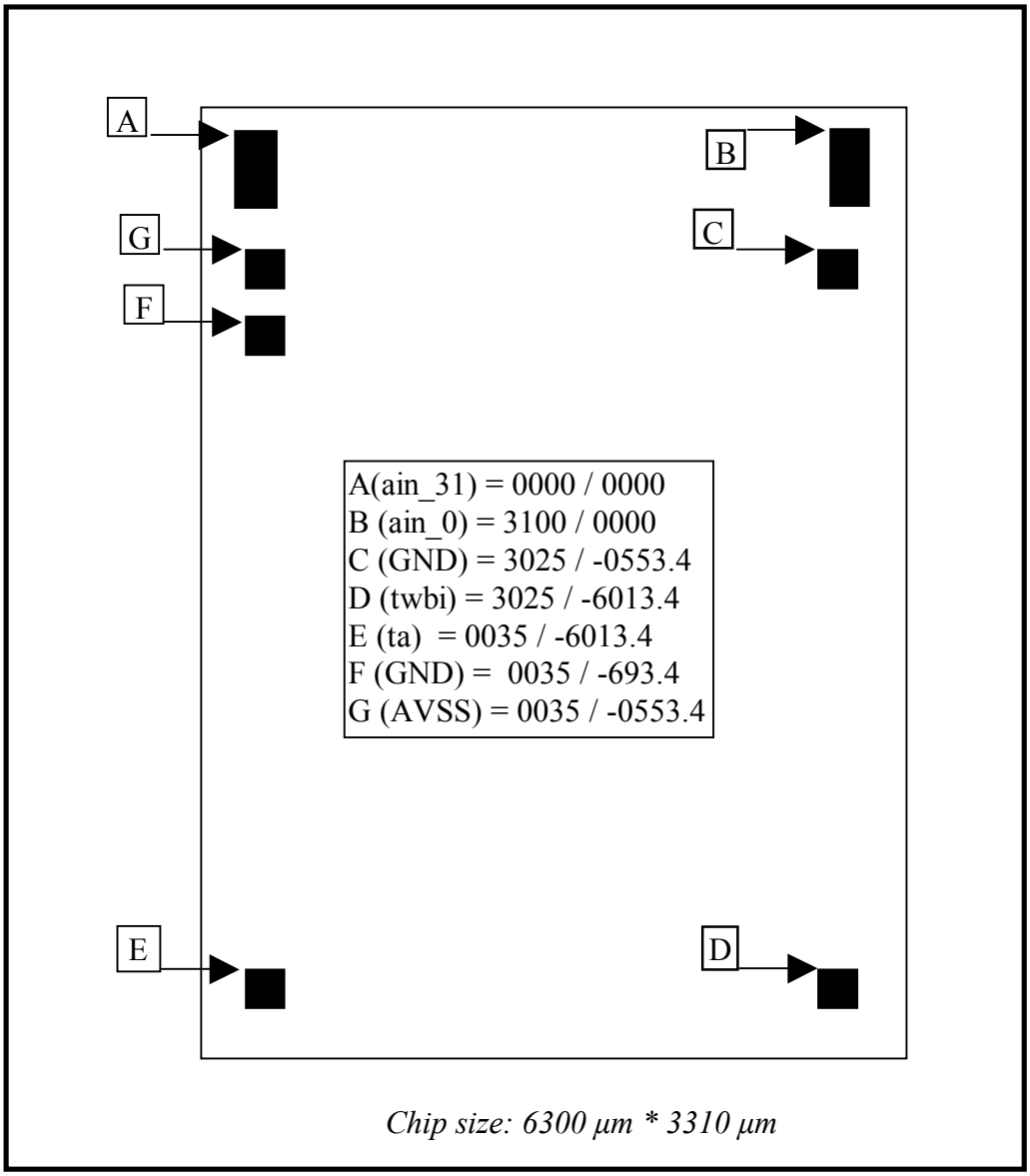


**Fig. 2** Chip geometry & pad placement (Not to scale - all dimensions in µm. Please note that the referred co-ordinates are layout co-ordinates. Add 50 µm -100 µm on each side for scribe/cutting tolerances).

# 5 Functional Description

As shown in Fig. 3 the chip consists of 32 identical parallel charge sensitive amplifiers.

The output of all amplifiers enters corresponding inputs of a 32 channel multiplexer. The switches in the multiplexer are controlled by a bit-register that runs in parallel. The output of the mux goes directly out of the chip via the output current buffer (signal = '**outp**' - '**outm**') and via an additional voltage buffer (signal = '**v_outp'**). Only one of the switches in the mux can be ¨on ¨ at a time. That is, one amplifier (channel) at a time can be seen on the output of the chip. The bit in the register ripples in sequence from the top- to the bottom- channel by clocking '**ckb**'. The clock can be stopped at any point, which will maintain the connection between the current channel and the output, which remains enabled.

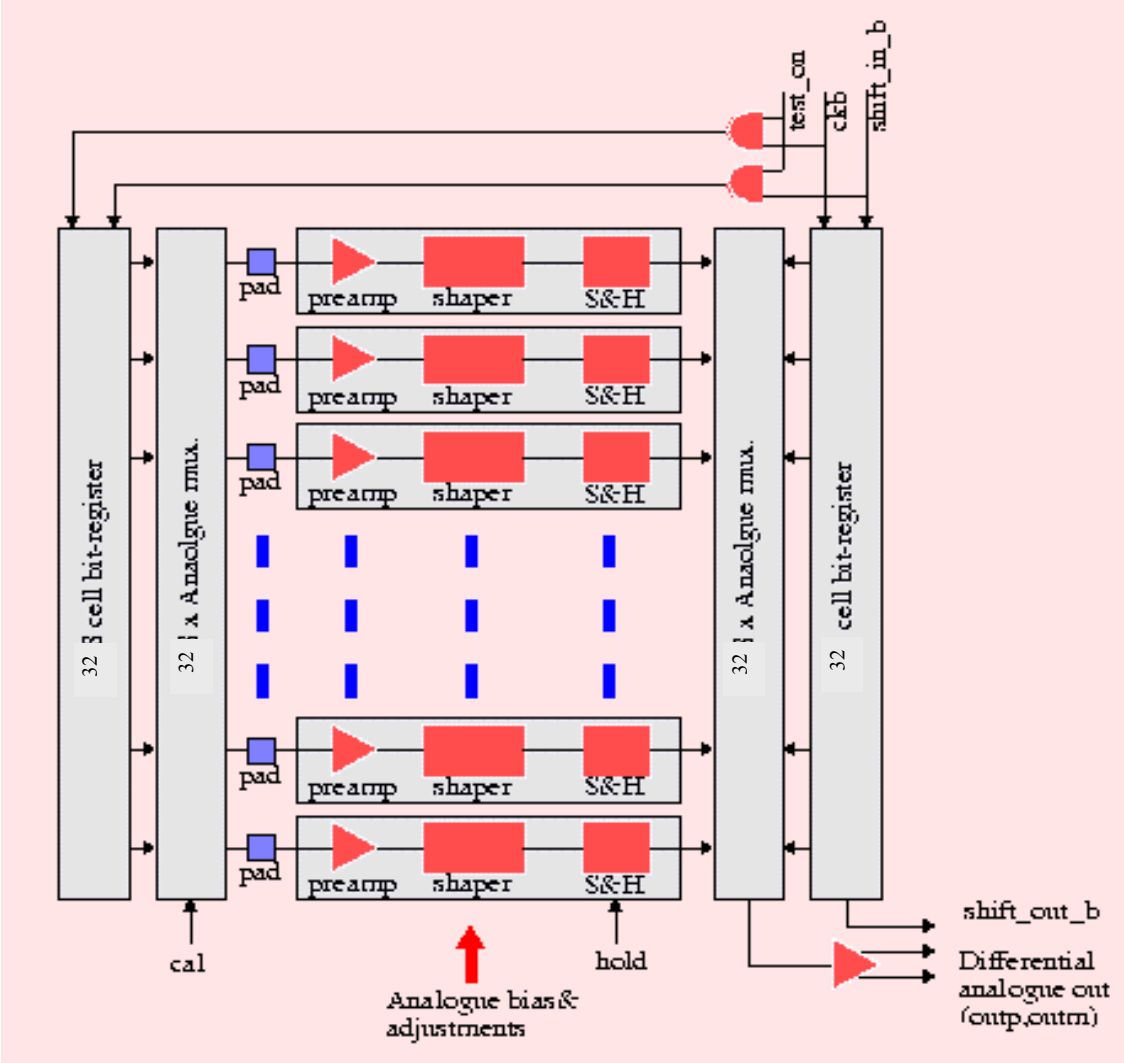


**Fig 3. VA32TA2 Architecture, VA-part**

The concept of the Ta-part is shown in Fig.4 and 5, The TA and VA parts share the same preamplifier, which is located in the VA-part. The inputs of TA are directly coupled to corresponding outputs of these preamplifiers.

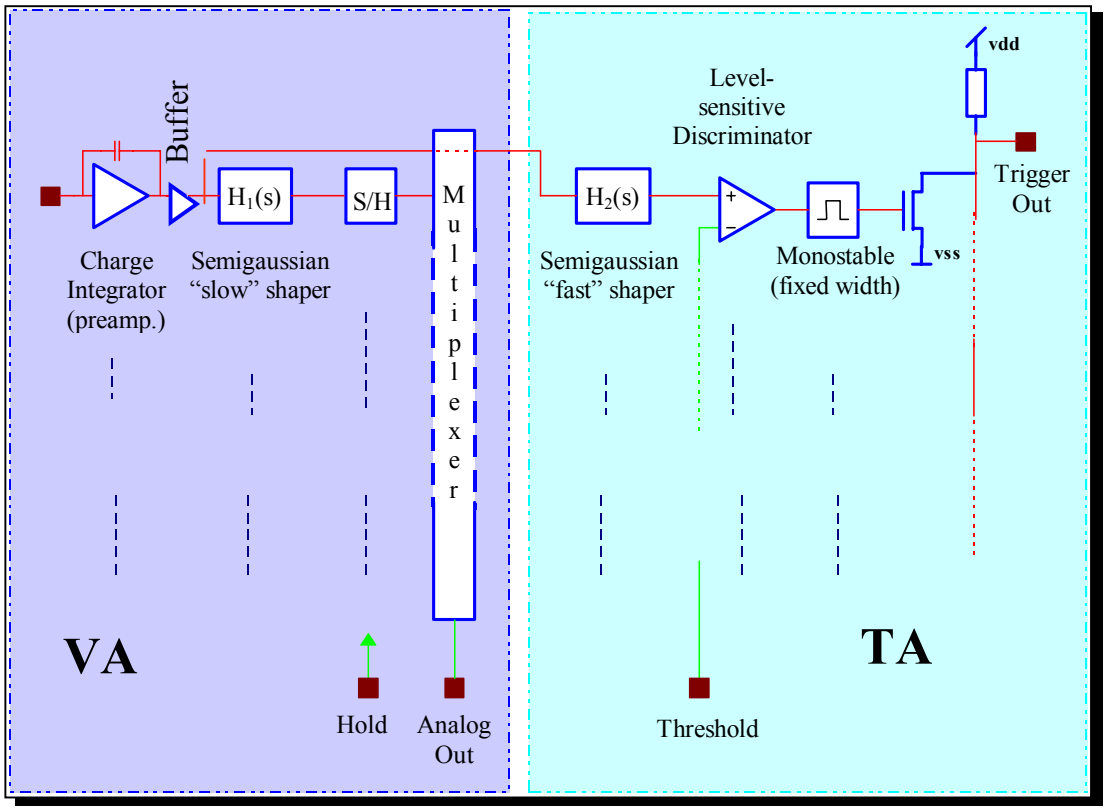


**Fig 4. The VA-TA principle**

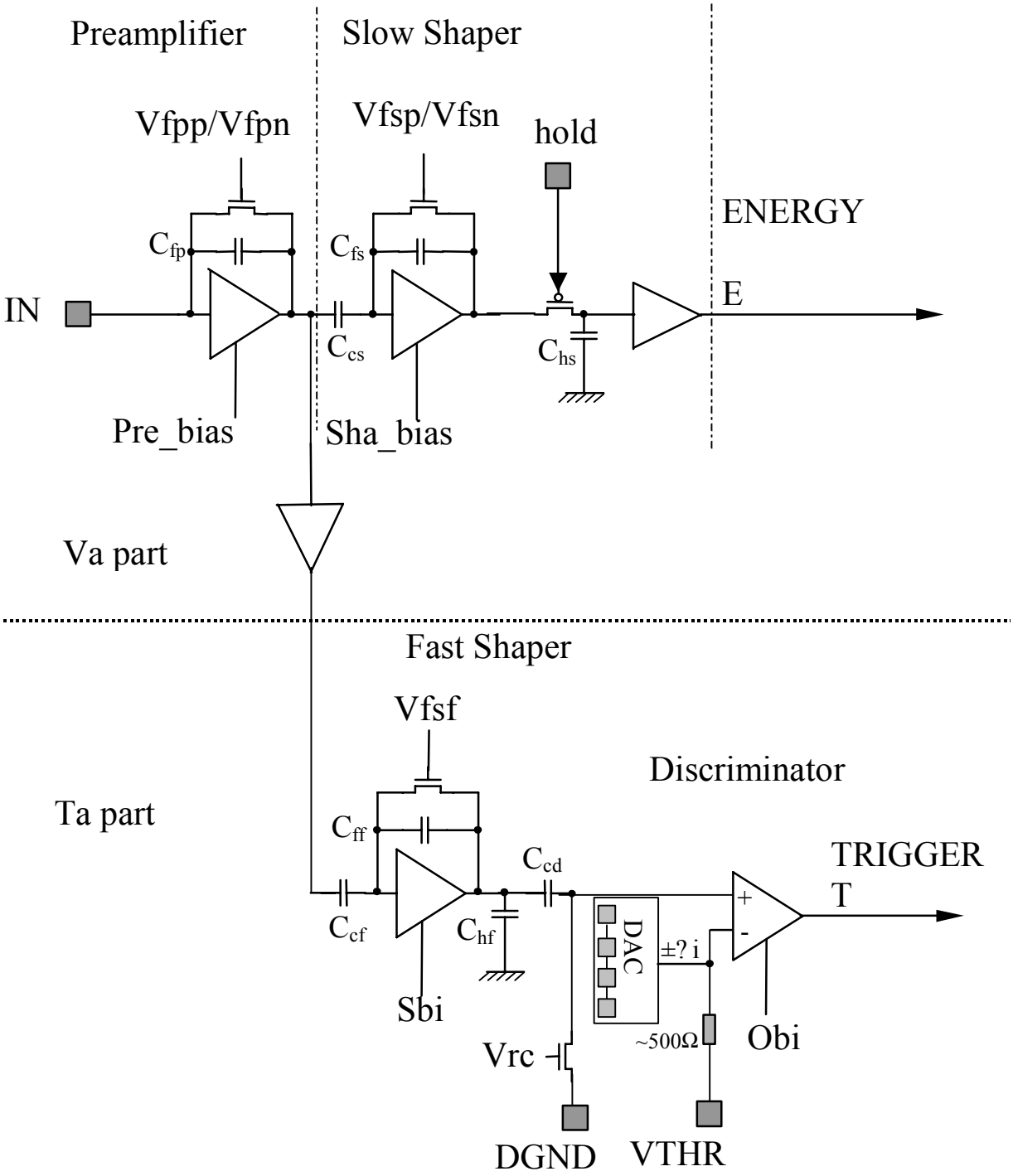


**Fig 5. VA32TA2 Architecture, VA and TA parts**

As shown in Fig.6 the TA part consists of 32 identical parallel channels. Each channel includes a fast CR-RC 75ns shaper which again is followed by a level-sensitive discriminator. The discriminator is preceded by a High-Pass filter (not shown) with a very low cut-off frequency in order to reduce offset-spread across chip. Each discriminator has individual offset adjustment that can be programmed through 4-bit DACs located on the negative input of each discriminator. An additional degree of freedom is added by a 5-bit trim DAC to adjust the global threshold voltage(vthr).

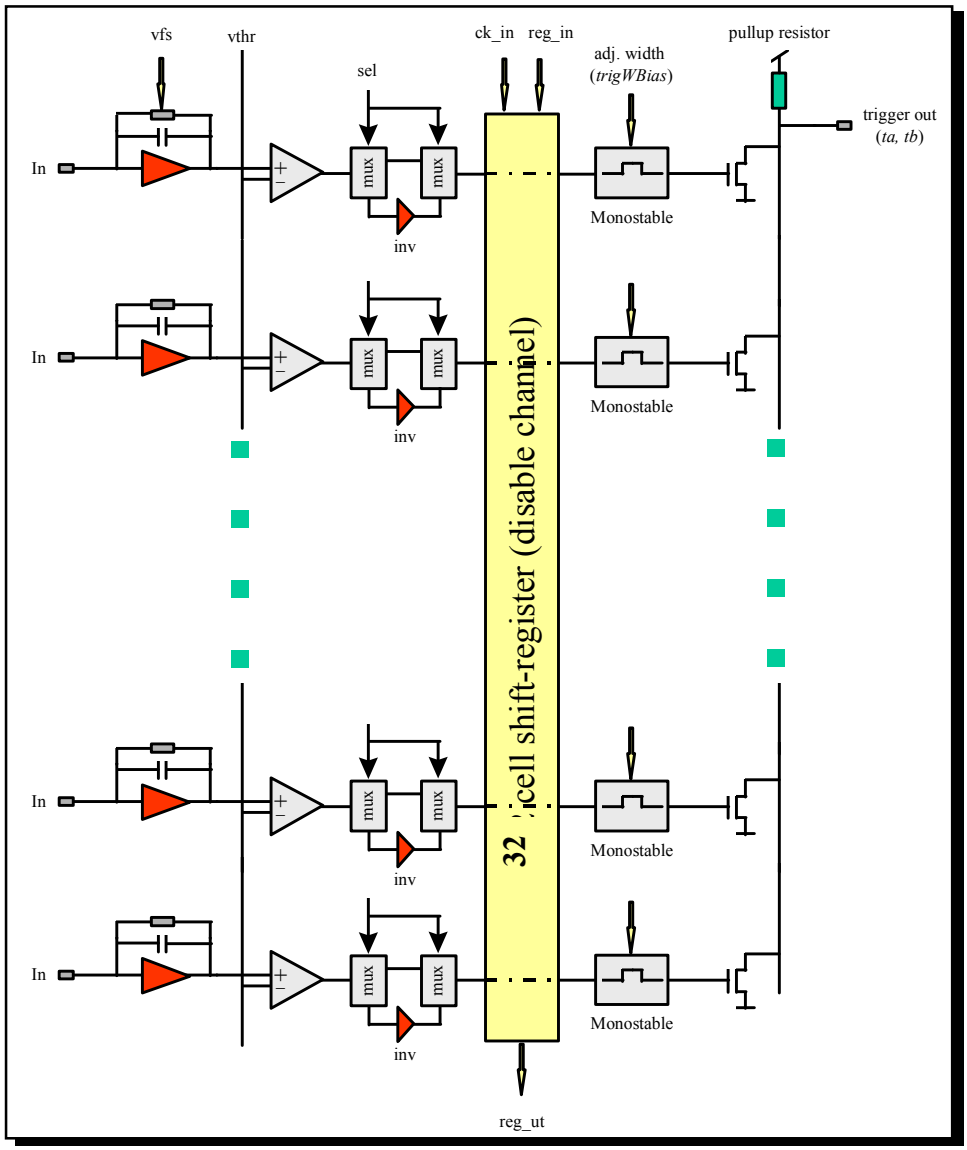


**Fig 6. TA Architecture**

Following the discriminator, which threshold is externally adjustable (***vthr***), is a circuitry which makes it possible to select between positive and negative input signals.

Following this circuitry is an edge-trigged monostable flip-flop that gives a fixed pulse-width which is externally adjustable (***trigWbias***). At the end of the channel is a pull-down transistor that serves as one input to all 32 channels wire-or circuitry.
Whenever a signal in any of the channels is rising above the discriminator threshold the wire-or'ed output will cause a chip-global trigger output on $\mathbf{t_a}$ end $\mathbf{t_b}$.

## 5.1 Control register

The VA32TA2 chip contains a 175 bits long shift register which can be loaded serially using *RegIn* (serial data) and *ClkIn* (clock). A more thorough description of the contents of the register is found below and in figure 7.

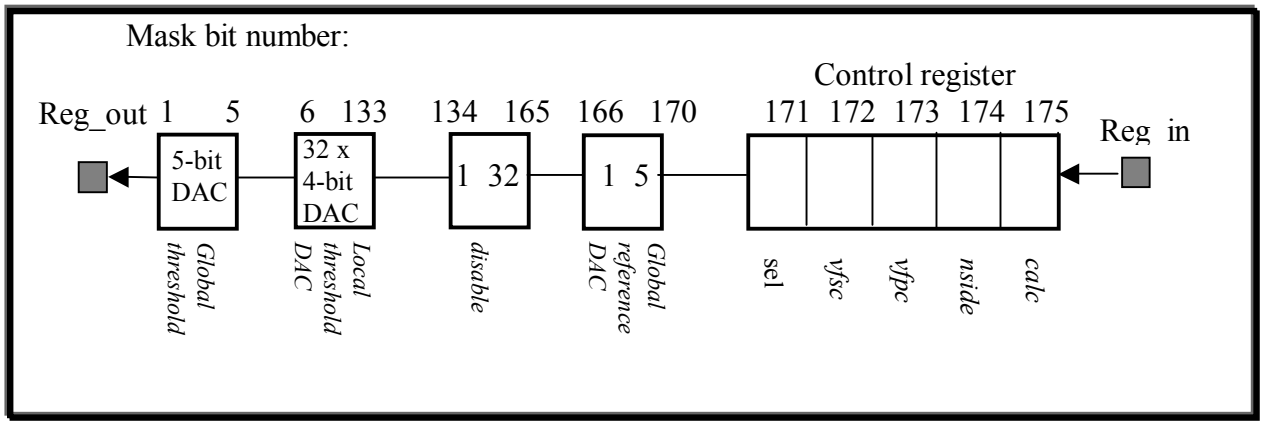


**Figure 7:** The sequence of the serial shift register mask. The sequence numbers are shown at the top of the boxes. Bit 0 is the first bit to be loaded. The channel numbers are indicated inside the boxes for the channel disable register and the channel threshold DAC register.

The following description starts with the last bit pushed into the register.

The serial shift register is shown in figure 7. The first 5 bits in the control register options or functions as shown in Table 2:

| *State (pos. logic)* | ***Calc*** | ***Nside*** | ***Vfpc*** | ***vfsc*** | ***sel*** |
|---|---|---|---|---|---|
| **High** | Floating cal. line | Positive input signal | Negative input signal | Positive input signal | Negative input signal |
| **Low** | Cal. line at AVDD | Negative input signal | Positive input signal | Negative input signal | Positive input signal |

Table 2: Control settings for polarity and calibration input line.

The next 5 bits are reserved for trimming the reference shaper output voltage.

The next 32 bits inhibit triggering when set to “1”, making possible selective trigger reading.

Next, a bit frame of 32 x 4-bits allows DAC trimming of the threshold voltage locally in each channel.

The last 5 bits in the register are applied to the 5-bit threshold DAC to tune the discriminator threshold globally. The correspondance between DAC-bits and nominal values, and the effect of the programming of the DACs are shown in table 3 to 5.
The first of the bits to be loaded into these DACs represents the MSB and will be referred to as *bit1*.

**Reference shaper DAC:**

This 5-bit DAC allows adjustment of the reference voltage of the reference shaper (dummy shaper).

| Bit1 | Bit2 | Bit3 | Bit4 | Bit5 | Reference offset(mV) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | None |
| 0 | 0 | 0 | 0 | 1 | - 10 |
| 0 | 0 | 0 | 1 | 0 | - 20 |
| 0 | 0 | 0 | 1 | 1 | - 30 |
| 0 | 0 | 1 | 0 | 0 | - 40 |
| 0 | 0 | 1 | 0 | 1 | - 50 |
| 0 | 0 | 1 | 1 | 0 | - 60 |
| 0 | 0 | 1 | 1 | 1 | - 70 |
| 0 | 1 | 0 | 0 | 0 | - 80 |
| 0 | 1 | 0 | 0 | 1 | - 90 |
| 0 | 1 | 0 | 1 | 0 | - 100 |
| 0 | 1 | 0 | 1 | 1 | - 110 |
| 0 | 1 | 1 | 0 | 0 | - 120 |
| 0 | 1 | 1 | 0 | 1 | - 130 |
| 0 | 1 | 1 | 1 | 0 | - 140 |
| 0 | 1 | 1 | 1 | 1 | - 150 |
| 1 | 0 | 0 | 0 | 0 | None |
| 1 | 0 | 0 | 0 | 1 | + 10 |
| 1 | 0 | 0 | 1 | 0 | + 20 |
| 1 | 0 | 0 | 1 | 1 | + 30 |
| 1 | 0 | 1 | 0 | 0 | + 40 |
| 1 | 0 | 1 | 0 | 1 | + 50 |
| 1 | 0 | 1 | 1 | 0 | + 60 |
| 1 | 0 | 1 | 1 | 1 | + 70 |
| 1 | 1 | 0 | 0 | 0 | + 80 |
| 1 | 1 | 0 | 0 | 1 | + 90 |
| 1 | 1 | 0 | 1 | 0 | + 100 |
| 1 | 1 | 0 | 1 | 1 | + 110 |
| 1 | 1 | 1 | 0 | 0 | + 120 |
| 1 | 1 | 1 | 0 | 1 | + 130 |
| 1 | 1 | 1 | 1 | 0 | + 140 |
| 1 | 1 | 1 | 1 | 1 | + 150 |

**Table 3:** The correspondance between the DAC bits and the resulting reference shaper voltage.

**Threshold DACs:**

Table 4 applies to the channel trim DACs, table 5 to the global threshold DAC. Be aware that if the netsum of the ± currents in the channel threshold trim DACs is non-zero, a common term offset will occur on the global threshold voltage.

| Bit1 | Bit2 | Bit3 | Bit4 | Offset change (mV), (R=500Ω) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | None |
| 0 | 0 | 0 | 1 | -1 |
| 0 | 0 | 1 | 0 | -2 |
| 0 | 0 | 1 | 1 | -3 |
| 0 | 1 | 0 | 0 | -4 |
| 0 | 1 | 0 | 1 | -5 |
| 0 | 1 | 1 | 0 | -6 |
| 0 | 1 | 1 | 1 | -7 |
| 1 | 0 | 0 | 0 | None |
| 1 | 0 | 0 | 1 | +1 |
| 1 | 0 | 1 | 0 | +2 |
| 1 | 0 | 1 | 1 | +3 |
| 1 | 1 | 0 | 0 | +4 |
| 1 | 1 | 0 | 1 | +5 |
| 1 | 1 | 1 | 0 | +6 |
| 1 | 1 | 1 | 1 | +7 |

**Table 4:** The correspondance between the DAC bits and the resulting threshold voltage offset in the channels.

| Bit1 | Bit2 | Bit3 | Bit4 | Bit5 | Threshold (mV) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | None |
| 0 | 0 | 0 | 0 | 1 | -1 |
| 0 | 0 | 0 | 1 | 0 | -2 |
| 0 | 0 | 0 | 1 | 1 | -3 |
| 0 | 0 | 1 | 0 | 0 | -4 |
| 0 | 0 | 1 | 0 | 1 | -5 |
| 0 | 0 | 1 | 1 | 0 | -6 |
| 0 | 0 | 1 | 1 | 1 | -7 |
| 0 | 1 | 0 | 0 | 0 | -8 |
| 0 | 1 | 0 | 0 | 1 | -9 |
| 0 | 1 | 0 | 1 | 0 | -10 |
| 0 | 1 | 0 | 1 | 1 | -11 |
| 0 | 1 | 1 | 0 | 0 | -12 |
| 0 | 1 | 1 | 0 | 1 | -13 |
| 0 | 1 | 1 | 1 | 0 | -14 |
| 0 | 1 | 1 | 1 | 1 | -15 |
| 1 | 0 | 0 | 0 | 0 | None |
| 1 | 0 | 0 | 0 | 1 | +1 |
| 1 | 0 | 0 | 1 | 0 | +2 |
| 1 | 0 | 0 | 1 | 1 | +3 |
| 1 | 0 | 1 | 0 | 0 | +4 |
| 1 | 0 | 1 | 0 | 1 | +5 |
| 1 | 0 | 1 | 1 | 0 | +6 |
| 1 | 0 | 1 | 1 | 1 | +7 |
| 1 | 1 | 0 | 0 | 0 | +8 |
| 1 | 1 | 0 | 0 | 1 | +9 |
| 1 | 1 | 0 | 1 | 0 | +10 |
| 1 | 1 | 0 | 1 | 1 | +11 |
| 1 | 1 | 1 | 0 | 0 | +12 |
| 1 | 1 | 1 | 0 | 1 | +13 |
| 1 | 1 | 1 | 1 | 0 | +14 |
| 1 | 1 | 1 | 1 | 1 | +15 |

**Table 5:** The correspondance between the DAC bits and the resulting on-chip global threshold.

## 5.2 Bias connections to the chip

All biases are internally generated. However, all of them are available through external pads for adjustment.

The bias currents and voltages are generated through an array of resistor voltage dividers to generate voltages, and by diode connected MOSFETs and transistors to produce the desired currents. These currents are then mirorred to the appropriate network.

Fig. 8 shows a resistor voltage divider and a diode connected MOSFET.

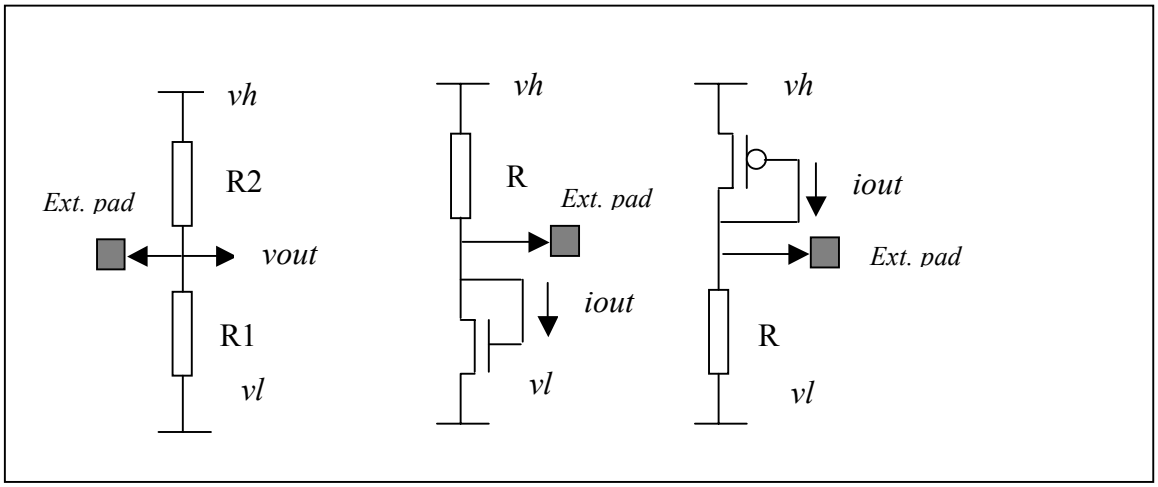


*Fig. 8 Voltage divider and MOSFET-resistor current generator*

The following tables provide a listing of all internally generated bias voltages for overriding purposes.

| | R1(kΩ) | R2(kΩ) | vh - vl |
|---|---|---|---|
| Vfpn | 1.1 | 8.9 | GND - AVDD |
| Vfpp | 9.25 | 0.75 | GND - AVDD |
| Vfsp | 2.75 | 7.25 | GND - AVDD |
| Vfsn | 2.25 | 7.75 | GND - AVDD |
| Vfsf | 5.75 | 4.25 | AVDD - GND |
| Vrc | 3 | 7 | AVDD - GND |

**Table 6:** Resistive biases and their power terminals

| | R(kΩ) | Terminal (vh / vl) |
|---|---|---|
| Pre_bias | 4.9 | AVDD |
| Sha_bias | 28.2 | GND |
| Sbi | 37.3 | AVDD |
| folbias | 9.8 | GND |
| Obi | 20 | DVDD |
| Twbi | 15 | GND |
| Ref_bi | 50.2 | GND |
| Ref_bi2 | 2.3 | GND |
| Ref_bi3 | 25.1 | GND |
| Ibuf | 7.2 | AVDD |
| Obuf | 2.5 | AVDD |

**Table 7:** Current bias generating resistors and their power terminals.

**Other signals**

*cal* is connected directly to the test register. When desired, set the chip in test-mode, select a channel (see earlier) and apply a proper voltage step on *cal* to emulate a charge input signal in one channel (only one at a time). When high, the calc in the control register leaves the cal line floating. Otherwise, cal is connected to AVDD. This allows testing of a channel together with real measurements.

*ClkIn* and *RegIn* are the clock and input for the shift register respectively. Logic values. Data at *RegIn* is sampled by the clock on the falling edge. The rise and fall time of the clock should not exceed 100ns. For daisy-chaining of chips, *RegIn* should only be connected to the first chip in the chain. For the others, *RegIn* should be fed from *RegOut* of the previous chip.

# 6 Normal mode of operation

The normal mode of operation is that the 32 inputs are connected to a detector from where the charge signal comes. After the physics event, each channel will integrate its eventual signal for up to 2µs. Usually, after the peak is reached (2µs), an external '**holdb**' signal should be applied to sample the value. Immediately after this a sequential read-out can be performed by activating the output bit-register using '**shift_in_b**' and '**ckb**'. See fig. 9 for an example of the timing in this mode. The logic part of the chip can be reset either by applying the '**dreset**' or, simply by running through a normal read-out once.

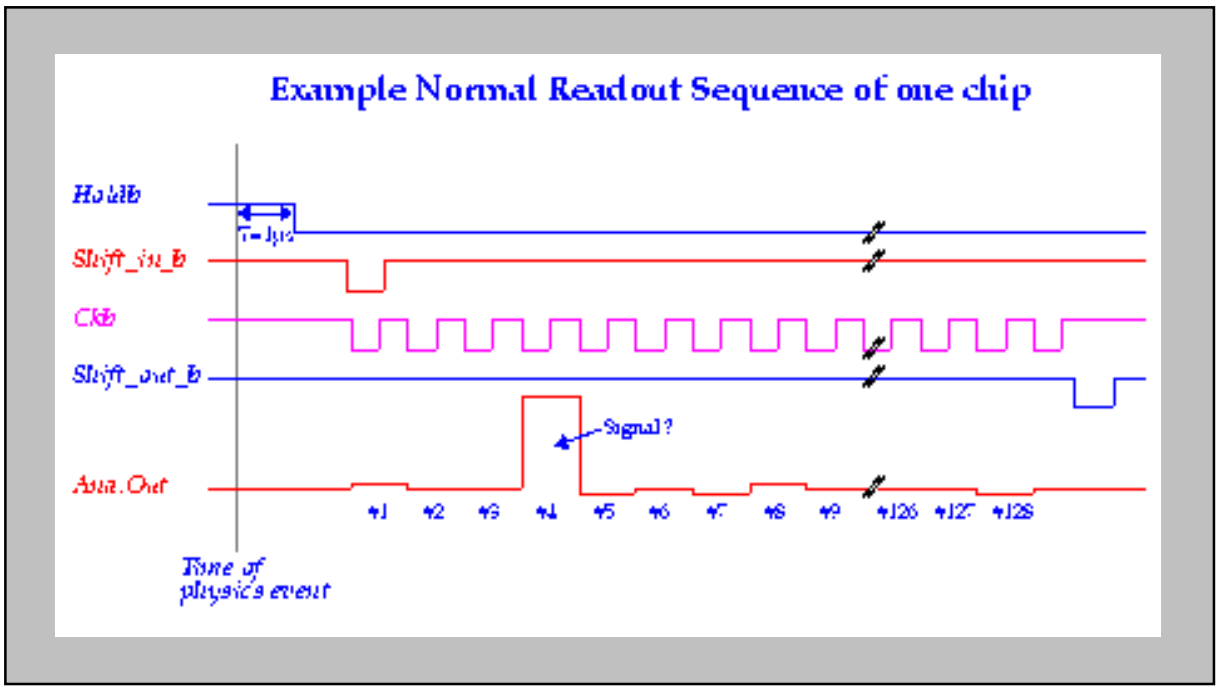


**Fig 9. Read-out timing of VA32TA2**

# 7 Operation in test mode

Each of the inputs of the amplifiers can be accessed via the input pads on the left side, see Fig. 3. In test mode, it is not necessary to connect any of these. Instead, the test facility of the chip can be turned on ('**test-on**'). This will enable another mux./bit-register on the input to run exactly in parallel with the output mux./bit-register. This input mux. connects all the inputs to the '**cal**' pad via a switch controlled by the bit-register. Also, in this case, only one connection at a time is possible and this connection will always correspond to the same channel as is connected in the output mux.

The register is reset by '**dreset**' and only when '**test-on**' is high. This keeps the test register intact while the chip is reset under normal measurement operation, giving access to a "test channel" under normal operation as well.