计算机组成原理 期中测验题

一、选择题（每小题 1 分，共10 分）

1. MIPS CPU 中存放待取出指令所在地址的是（   ）。
   A．指令寄存器 　　　　　　　　　　B．程序计数器 PC
   C．数据寄存器 　　　　　　　　　　D．地址寄存器

2. 下列选项中，不会引起指令流水线阻塞的是（   ）
   A．数据旁路（转发）　　　B．数据相关
   C．条件转移　　　　　　　D．资源冲突

3. Indicate the I-type instruction, according to the MIPS instruction format. (   )。
   A. lw $s1, 48($S3)　　　　B. add $s1, $S3, $s5
   C. and $s1, $S6, $s5　　　D. j label1

4. What is the range of addresses for conditional branches in MIPS (K =1024)?
   a) Addresses between 0 and 64K- 1
   b) Addresses between 0 and 256K -1
   c) Addresses up to about 32K before the branch to about 32K after
   d) Addresses up to about 128K before the branch to about 128K after

5. What is the range of addresses for jump and jump and link in MIPS (M = 1024K)?
   a) Addresses between 0 and 64M - 1
   b) Addresses between 0 and 256M- 1
   c) Addresses up to about 32M before the branch to about 32M after
   d) Addresses up to about 128M before the branch to about 128M after
   e) Anywhere within a block of 64M addresses where the PC supplies the upper 6 bits
   f) Anywhere within a block of 256M addresses where the PC supplies the upper 4 bits

6. 运算器执行两个补码表示的整数加法时，产生溢出的正确叙述为（   ）。
   a) 最高位有进位则产生溢出
   b) 相加结果的符号位与两同号加数的符号位相反则产生溢出
   c) 相加结果的符号位为 0 则产生溢出
   d) 相加结果的符号位为 1 则产生溢出

7. 下列选项中，能引起外部中断的事件是：（   ）
   A．键盘输入　　B．除数为 0　　　C．浮点运算下溢　　　D．访存缺页

8. Say we are designing a computer where all the instructions are 32 bits and all instructions are of the format as shown below:

Opcode	Destination register	Source register	Immediate

   If there are exactly 200 different instructions on this machine and there are 32 registers, how many bits would you expect the immediate field would hold?   (   )
   　　A.7　　B. 9　　C. 11　　D.12　　E. 14

9. Which of the following is correct for a load instruction? Refer to Figure 1. (   )。
   a. MemtoReg should be set to cause the data from memory to be sent to the register file.
   b. MemtoReg should be set to cause the correct register destination to be sent to the register file.

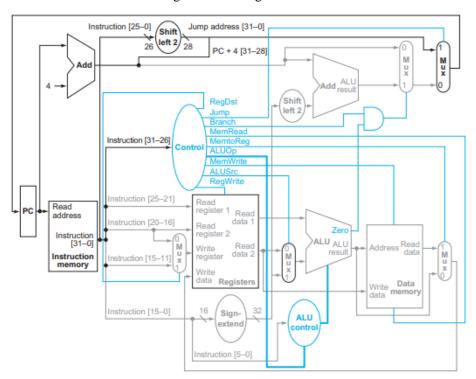c. We do not care about the setting of MemtoReg for loads.

Figure. 1 a single-cycle datapath for the MIPS architecture

10. The single-cycle datapath conceptually described in this section must have
separate instruction and data memories, because   (   )
a. the formats of data and instructions are different in MIPS, and hence
different memories are needed.
b. having separate memories is less expensive.
c. the processor operates in one cycle and cannot use a single-ported
memory for two different accesses within that cycle

二．（20 分）In this exercise we examine in detail how an instruction is executed in a single-cycle
datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the
following instruction word: 100011 00101 00100 10100 00000 010100 B. Assume that data
memory is all zeros and that the processor's registers have the following values at the beginning of
the cycle in which the above instruction word is fetched. (Note: This is a "LW" instruction)

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	−1	2	−3	−4	10	6	8	2	−16

1. What are the outputs of the sign-extend and the jump "Shift left 2" unit (near the top of Figure 1)
for this instruction word? (Fill in the following Table.)

sign-extend	jump "Shift left 2"

2. What is the new PC address after this instruction is executed? Highlight the path through which
this value is determined. (Fill in the following Table.)

New PC	Path

3. For each Mux, show the values of its data output during the execution of this instruction and
these register values. (Fill in the following Table.)

2

WrReg Mux	ALU Mux	Mem/ALU Mux	Branch Mux	Jump Mux

4.For the ALU and the two add units, what are their data input values? (Fill in the following Table.)

ALU	Add (PC+4)	Add (Branch)

5.What are the values of all inputs for the "Registers" unit and relative control lines? (Fill in the following Table.)

Read Register 1	Read Register 2	Write Register	Write Data	RegWrite	RegDst	MemtoReg

三．True or False （1 points for each question, 6 points total）

(1) Only one adder is required in a pipelined MIPS datapath.　(　)

(2) Because the register file is both read and written on the same clock cycle, any MIPS datapath using edge-triggered writes must have more than one copy of the register file.(　)

(3) Reordering code is a possible way to avoid pipeline stalls.　(　)

(4) Forwarding is primarily an attempt to fix Data Hazards in a pipeline. (　)

(5) In a pipelined system, forwarding will eliminate the need of any stalls.　(　)

(6) In the MIPS ISA each register holds 32 bits.　(　)

四. A group of students were debating the efficiency of the five-stage pipeline when one student pointed out that not all instructions are active in every stage of the pipeline. After deciding to ignore the effects of hazards, they made the following four statements. Which ones are correct?（1 points for each question, 4 points total）

1) Allowing jumps, branches, and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance under all circumstances.

2) Trying to allow some instructions to take fewer cycles does not help, since the throughput is determined by the clock cycle; the number of pipe stages per instruction affects latency, not throughput.

3) You cannot make ALU instructions take fewer cycles because of the writeback of the result, but branches and jumps can take fewer cycles, so there is some opportunity for improvement.

4) Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer, so that instructions take more cycles, but the cycles are shorter. This could improve performance.

五、分析题 (每小题6分，共30分)

1. 执行完下列 8086 指令后，AL 寄存器的内容为多少？标志位 CF、OF、SF、ZF 的值分别为多少？

    MOV　AL，0A8H

    ADD　AL，0CFH

2. Given the delay of the five pipeline stages as follows:

    IF: 300ns; ID: 400ns; EX: 350ns; MEM: 500ns; WB: 100ns

(1) What is the clock cycle time in a pipelined and nonpipelined processor?

(2) What is the total execution time of a lw instruction in a pipelined and nonpipelined processor?

3. For each code sequence below, state whether it must stall, can avoid stalls using only forwarding, or can execute without stalling or forwarding.

Sequence 1	Sequence 2	Sequence 3

lw $t0,0($t0)
add $t1,$t0,$t0
	add $t1,$t0,$t0
	addi $t2,$t0,#5
	addi $t4,$t1,#5
		addi $t1,$t0,#1
		addi $t2,$t0,#2
		addi $t3,$t0,#2
		addi $t3,$t0,#4
		addi $t5,$t0,#5

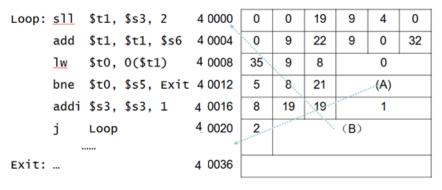4.、请计算图 2 中 (A)和（B）的值。

Loop: sll $t1, $s3, 2	4 0000	0	0	19	9	4	0
add $t1, $t1, $s6	4 0004	0	9	22	9	0	32
lw $t0, 0($t1)	4 0008	35	9	8	0		
bne $t0, $s5, Exit	4 0012	5	8	21	(A)		
addi $s3, $s3, 1	4 0016	8	19	19	1		
j Loop	4 0020	2		(B)			
......							
Exit: ...	4 0036						

图 2　分支及转移指令的寻址

5、假设有一条 MIPs 指令在内存中存放的信息如下：

Address	Instruction
00400004hex	Jal 400200hex

请问这条指令的功能是什么？执行这条指令后$ra 寄存器的内容是什么？JAL 指令的目标地址是多少？

六．（10 分） 给下面的 MIPS 代码添加注释，并用一句话描述它计算的是什么？假设$a0 和 $a1 用于输入，且在开始时分别包括整数 6 和 5，程序执行完后，$v0 寄存器的值是多少？

```
        add        $t0, $zero, $zero
loop:   beq        $a1, $zero, finish
        add        $t0, $t0, $a0
        sub        $a1, $a1, 1
        j          loop
finish: addi       $t0, $t0, 100
        add        $v0,      $t0, $zero
```

七、（10 分）将以下 C 代码段改成 MIPS 汇编语言程序：

```
Int A[100],B[100]
for(i = 0;i < 100;i++){
    A[i]=A[i-1]+B[i]
}
```

数组 A 和 B 的基地址在寄存器$a0 和$ a1 中。

八、（10 分） 请设计一个既可以用于两个 4 位补码表示的带符号数做加减法运算，又可以用于两个 4 位无符号数做加减法运算的电路，可以用全加器、与、或、非、异或门等基本数

字逻辑电路。要求设计的电路中包含检测溢出标志位 OF 和进位标志位 CF 的电路。解释其工作原理。