Features

- **Combination of a complete time-of-day clock, alarm**
- **Accessible by an 8-bit CPU bus**
- **Ultra low power consumption**
- **One hundred year calendar**
- **Programmable periodic interrupt**
- **Square wave generator**
- **Interface for connecting up to 114 bytes of RAM**
- **Gate Count: 2KGates**

Description

The CB_146818 combines a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt, and a square wave generator.

The time of day, alarm and calendar registers can all be accessed by an 8-bit CPU bus. A RAM enable signal and address lines are provided to enable the connection of a RAM block of up to 114 bytes. The time/calendar values can be stored in binary or binary coded decimal format. The time can be in 12 or 24 hour mode. A daylight saving time option is available. The CB_146818 has been designed for very low power consumption.

Operation

The CB_146818 has three time of day registers, three alarm registers and four calendar registers which are accessible by an 8-bit CPU bus. It also contains a clock divider which can be driven from a 32 768, 1 048 576 or 4 194 304 Hz clock. Once per second the time and calendar registers will be automatically updated. When the time of day registers match the alarm registers an alarm is flagged, this can be used to generate an interrupt. The clock divider can also be programmed to produce a periodic interrupt.

The CB_146818 decodes seven address lines (a block of 128 bytes). The first twelve locations are mapped to the twelve internal registers, the remaining 114 locations can be mapped to an external RAM block. Address lines and an enable line are provided for interfacing to this RAM block.

Standard Interface Macrocell

CB_146818 Real Time Clock

0888A/cb146818.fm5–8/97

Signal Description

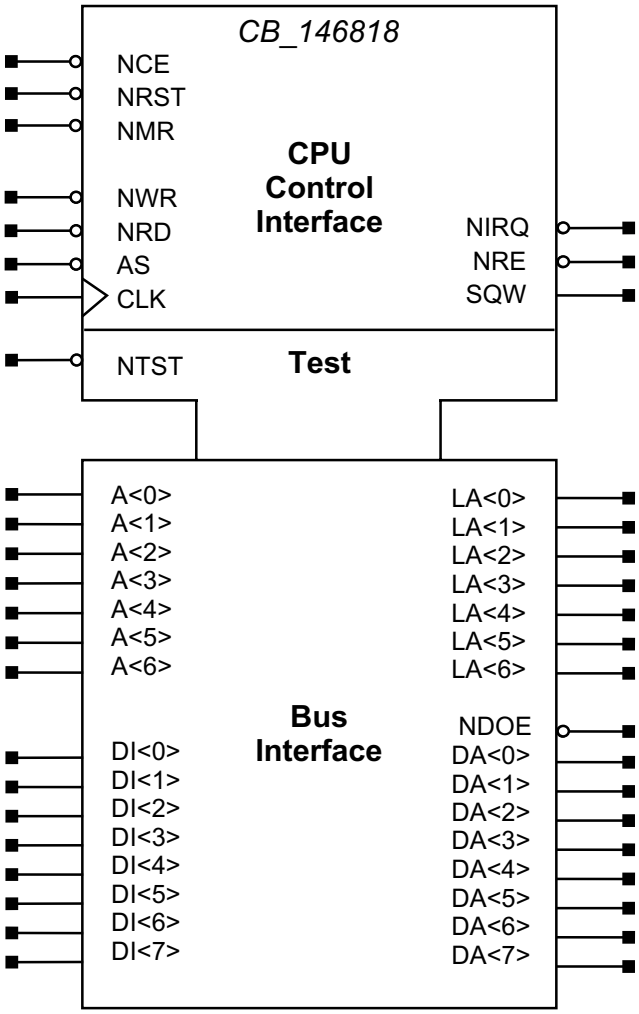

Table 1. CPU Control Interface

Signal Name	Type	Description
NCE	Input	Chip enable, active low
NRST	Input	Reset, active low. Clears interrupt enables: PIE, AIE, UIE, interrupt flags: PF, AF, UF, IRQF, and square wave enable SQWE
NMR	Input	Master reset, active low. This signal clears the VRT bit in register D to indicate that the time and calendar registers hold valid data. This signal should be asserted at power-up.
NWR	Input	Write strobe, active low
NRD	Input	Read strobe, active low
AS	Input	Address strobe, latches A 0-6 when low
CLK	Input	Clock, either 4.194304 MHz, 1.048576 MHz or 32768 Hz
NIRQ	Output	Interrupt request, active low
NRE	Output	External RAM enable, active low. This signal is low when NCE is low and none of the 14 internal registers are addressed.
SQW	Output	Square wave output

Table 2. Test

Signal Name	Type	Description
NTST	Input	Test mode enable, active low

Table 3. Bus Interface

Signal Name	Type	Description
A 0-6	Input	Address lines
DI 0-7	Input	Data bus
LA 0-6	Output	Latched address lines, can be used to address an external RAM block
NDOE	Output	Data bus output enable, active low. Can be used to control external bi-directional buffers.
DA 0-7	Output	Data bus