

LIST OF TABLES

Chapter 2		
Table 2-1.	Z80X30 Register Map (Shift Left Mode)	2-6
Table 2-2.	Z80X30 Register Map (Shift Right Mode)	2-7
Table 2-3.	Z80230 SDLC/HDLC Enhancement Options	2-8
Table 2-4.	Z80X30 Register Reset Values	2-9
Table 2-5.	Z85X30 Register Map	2-13
Table 2-6.	Z85C30/Z85230 Register Enhancement Options	2-14
Table 2-7.	Z85X30 Register Reset Value	2-15
Table 2-8.	Interrupt Source Priority	2-16
Table 2-9.	Interrupt Vector Modification	2-19
Chapter 3		
Table 3-1.	Baud Rates for 2.4576 MHz Clock and 16x Clock Factor	3-3
Chapter 4		
Table 4-1.	Write Register Bits Ignored in Asynchronous Mode	4-4
Table 4-2.	Transmit Bits per Character	4-5
Table 4-3.	Initialization Sequence Asynchronous Mode	4-7
Table 4-4.	Registers Used in Character-Oriented Modes	4-9
Table 4-5.	Transmitter Initialization in Character- Oriented Mode	4-10
Table 4-6.	Sync Character Length Selection	4-11
Table 4-7.	Enabling and Disabling CRC	4-16
Table 4-8.	Initializing the Receiver in Character-Oriented Mode	4-17
Table 4-9.	ESCC Action Taken on Tx Underrun	4-20
Table 4-10.	Residue Codes	4-24
Table 4-11.	Initializing in SDLC Mode	4-26
Table 4-12.	SDLC Loop Mode Initialization	4-32
Chapter 5		
Table 5-1.	SCC Write Registers	5
Table 5-2.	SCC Read Registers	5-1
Table 5-3.	Z85X30 Register Map	5-{
Table 5-4.	Receive Bits per Character	5-7
Table 5-5.	Transmit Bits per Character	5-10
Table 5-6.	Interrupt Vector Modification	5-14
Table 5-7.	Data Encoding	5-15



Table 5-8.	Receive Clock Source	5-18
Table 5-9.	Transmit Clock Source	5-18
Table 5-10.	Transmit External Control Selection	5-18
Table 5-11.	I-Field Bit Selection (8 Bits Only)	5-24
Table 5-12.	Bits per Character Residue Decoding	5-24
Table 5-13.	Read Register 7 FIFO Status Decoding	5-26